ESP32-S3

Technical Reference Manual

PRELIMINARY



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Espressif Systems
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About this Document

The **ESP32-S3 Technical Reference Manual** is targeted at developers working on low level software projects that use ESP32-S3 SoC. It provides information for the ESP32-S3 hardware modules listed below. The modules detailed in this document provide an overview, list of features, hardware architecture details, any necessary programming guidelines, as well as a register listing.

Release Status at a Glance

Note that this manual in still work in progress. See our release progress below:

No.	ESP32-S3 Chapters	Progress
1	I2C Controller (I2C)	Published
2	Reset and Clock	Published
3	I2S Controller (I2S)	53%
4	Camera-LCD Controller (CAM-LCD)	Published
5	Remote Control Peripheral (RMT)	Published
6	Random Number Generator (RNG)	Published
7	eFuse Controller (eFuse)	Published
8	Processor Instruction Extensions (PIE)	58%
9	System and Memory	Published
10	Permission Control (PMS)	Published
11	USB On-The-Go (USB)	Published
12	UART Controller (UART)	Published
13	Digital Signature (DS)	Published
14	Timer Group (TIMG)	Published
15	Watchdog Timers (WDT)	Published
16	GDMA Controller (GDMA)	Published
17	Motor Control PWM (MCPWM)	Published
18	SD/MMC Host Controller (SDHOST)	Published
19	LED PWM Controller (LEDC)	Published
20	Pulse Count Controller (PCNT)	Published
21	IO MUX and GPIO Matrix (GPIO, IO_MUX)	Published
22	Interrupt Matrix (INTERRUPT)	Published
23	System Registers (SYSREG)	Published
24	SPI Controller (SPI)	42%
25	On-Chip Sensors and Analog Signal Processing	89%
26	ULP Coprocessor (ULP-FSM, ULP-RISC-V)	Published
27	SHA Accelerator (SHA)	Published
28	Low-Power Management (RTC_CNTL)	84%
29	HMAC Accelerator (HMAC)	Published
30	AES Accelerator (AES)	Published
31	RSA Accelerator (RSA)	Published
32	Two-wire Automotive Interface (TWAI)	Published
33	External Memory Encryption and Decryption (XTS_AES)	Published
34	System Timer (SYSTIMER)	Published
35	Chip Boot Control (BOOTCTRL)	Published
36	Clock Glitch Detection	Published
37	XTAL32K Watchdog Timer (XTWDT)	Published
38	World Controller (WCL)	Published
39	USB Serial/JTAG Controller (USB_SERIAL_JTAG)	Published

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Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://www.espressif.com/sites/default/files/documentation/esp32-s3_technical_reference_manual_en.pdf

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1 ULP Coprocessor (ULP-FSM, ULP-RISC-V)

1.1 Overview

The ULP coprocessor is an ultra-low-power processor that remains powered on when the chip is in Deep-sleep (see Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*). Hence, users can store in RTC memory a program for the ULP coprocessor to access RTC peripherals, internal sensors, and RTC registers during Deep-sleep.

In power-sensitive scenarios, the main CPU goes to sleep mode to lower power consumption. Meanwhile, the coprocessor is woken up by ULP timer, and then monitors the external environment or interacts with the external circuit by controlling peripherals such as RTC GPIO, RTC I2C, SAR ADC, or temperature sensor (TSENS). The coprocessor wakes the main CPU up once a wakeup condition is reached.

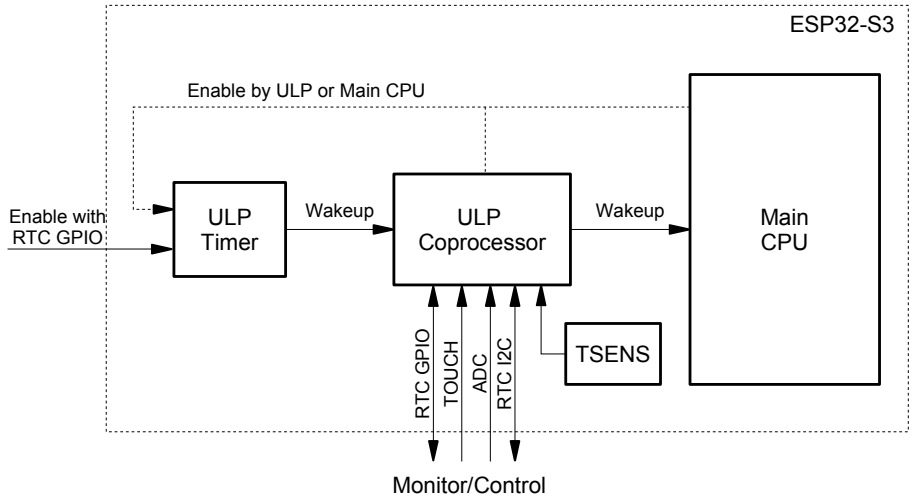


Figure 1-1. ULP Coprocessor Overview

ESP32-S3 has two ULP coprocessors, with one based on RISC-V instruction set architecture (ULP-RISC-V) and the other on finite state machine (ULP-FSM). Users can choose between the two coprocessors depending on their needs.

1.2 Features

- Access up to 8 KB of SRAM RTC slow memory for instructions and data
- Clocked with 17.5 MHz RTC_FAST_CLK
- Support working in normal mode and in monitor mode
- Wake up the CPU or send an interrupt to the CPU
- Access peripherals, internal sensors and RTC registers

ULP-FSM and ULP-RISC-V can not be used simultaneously. Users can only choose one of them as the ULP coprocessor of ESP32-S3. The differences between the two coprocessors are shown in the table below.

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Table 1-1. Comparison of the Two Coprocessors

Feature		ULP Coprocessors	
		ULP-FSM	ULP-RISC-V
Memory (RTC Slow Memory)		8 KB	
Work Clock Frequency		17.5 MHz	
Wakeup Source		ULP Timer	
Work Mode	Normal Mode	Assist the main CPU to complete some tasks after the chip is woken up.	
	Monitor Mode	Retrieve data from sensors to monitor environment, when the chip is in sleep.	
Control Low-Power Peripherals		ADC1/ADC2	
		RTC I2C	
		RTC GPIO	
		Touch Sensors	
		Temperature Sensor	
Architecture		Programmable FSM	RISC-V
Development		Special instruction set	Standard C compiler

ULP coprocessor can access the modules in RTC domain via RTC registers. In many cases the ULP coprocessor can be a good supplement to, or replacement of, the main CPU, especially for power-sensitive applications. Figure 1-2 shows the overall layout of ESP32-S3 coprocessor.

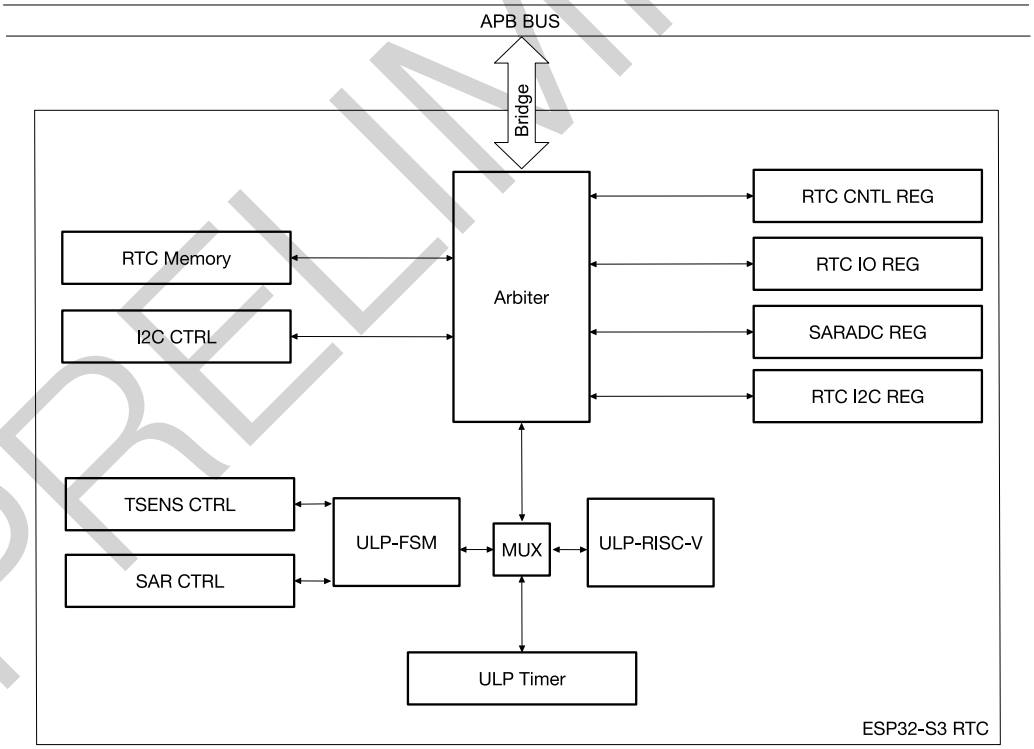


Figure 1-2. ULP Coprocessor Diagram

1.3 Programming Workflow

The ULP-RISC-V is intended for programming using C language. The program in C is then compiled to

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RV32IMC standard instruction code. The ULP-FSM is using custom instructions normally not supported by high-level programming language. Users develop their programs using ULP-FSM instructions (see Section 1.5.2).

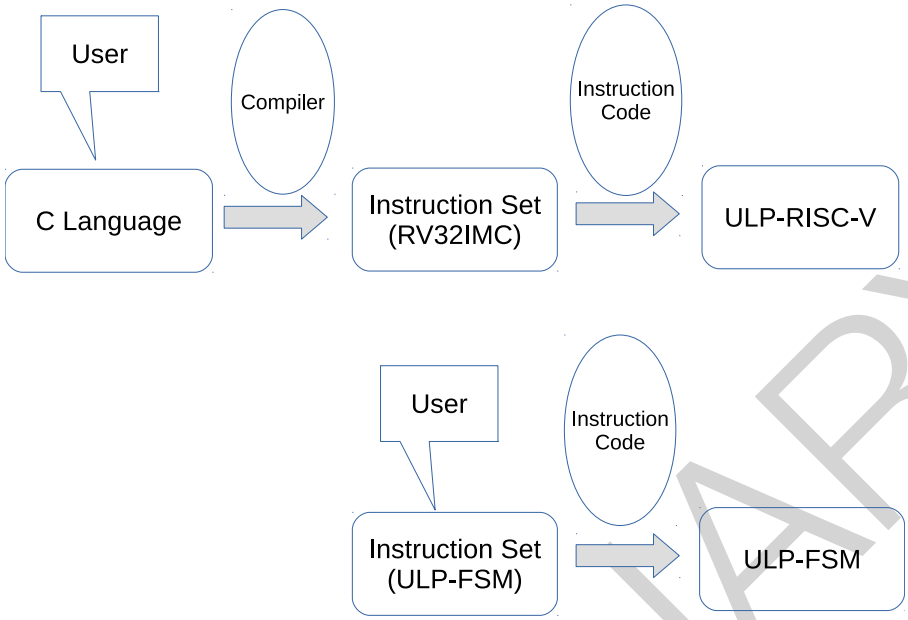


Figure 1-3. Programming Workflow

1.4 ULP Coprocessor Sleep and Weakup Workflow

ULP coprocessor is designed to operate independently of the CPU, while the CPU is either in sleep or running.

In a typical power-saving scenario, the chip goes to Deep-sleep mode to lower power consumption. Before setting the chip to sleep mode, users should complete the following operations.

1. Flash the program to be executed by ULP coprocessor into RTC slow memory.
2. Select the working ULP coprocessor by configuring RTC_CNTL_COCPU_SEL.
   - 0: select ULP-RISC-V
   - 1: select ULP-FSM
3. If ULP-RISC-V is selected as working ULP coprocessor, please
   - set and reset RTC_CNTL_COCPU_CLK_FO;
   - set RTC_CNTL_COCPU_CLKGATE_EN.
4. Set sleep cycles for the timer by configuring RTC_CNTL_ULP_CP_TIMER_1_REG.
5. Enable the timer by software or by RTC GPIO;
   - By software: set RTC_CNTL_ULP_CP_SLP_TIMER_EN.
   - By RTC GPIO: set RTC_CNTL_ULP_CP_GPIO_WAKEUP_ENA.
6. Set the system into sleep mode.

When the system is in Deep-sleep mode:

PRELIMINARY

1. The timer periodically sets the low-power controller (see Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*) to Monitor mode and then wakes up the coprocessor.
2. Coprocessor executes some necessary operations, such as monitoring external environment via low-power sensors.
3. After the operations are finished, the system goes back to Deep-sleep mode.
4. ULP coprocessor goes back to halt mode and waits for next wakeup.

In monitor mode, ULP coprocessor is woken up and goes to halt as shown in Figure 1-4.

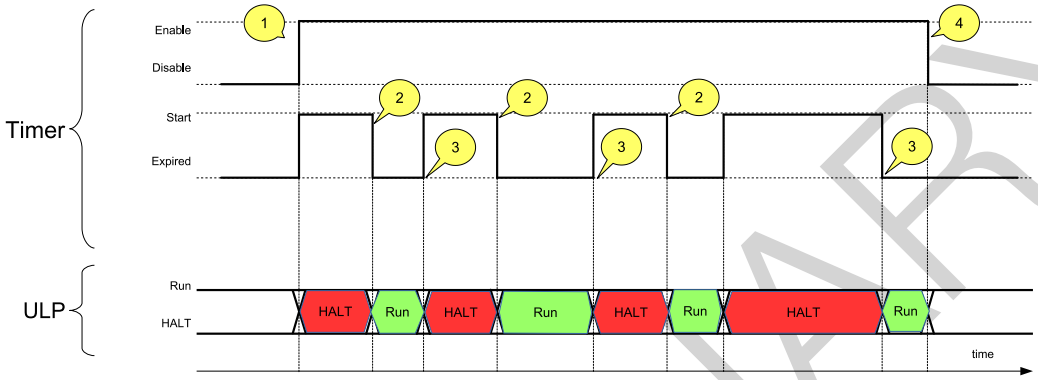


Figure 1-4. ULP Sleep and Wakeup Sequence

1. Enable the timer and the timer starts counting.
2. The timer expires and wakes up the ULP coprocessor. ULP coprocessor starts running and executes the program flashed in RTC slow memory.
3. ULP coprocessor goes to halt and the timer starts counting again.
   - Put ULP-RISC-V into HALT: set RTC_CNTL_COCPU_DONE.
   - Put ULP-FSM into HALT: execute HALT instruction.
4. Disable the timer by ULP program or by software. ULP coprocessor exits from monitor mode.
   - Disabled by software: clear RTC_CNTL_ULP_CP_SLP_TIMER_EN.
   - Disabled by RTC GPIO: clear RTC_CNTL_ULP_CP_GPIO_WAKEUP_ENA and set RTC_CNTL_ULP_CP_GPIO_WAKEUP_CLR.

Note:

- If the timer is enabled by software (RTC GPIO), it should be disabled by software (RTC GPIO).
- Before setting ULP-RISC-V to HALT, users should configure RTC_CNTL_COCPU_DONE first, therefore, it is recommended to end the flashed program with the following pattern:
  - Set RTC_CNTL_COCPU_DONE to end the operation of ULP-RISC-V and put it into halt;
  - Set RTC_CNTL_COCPU_SHUT_RESET_EN to reset ULP-RISC-V.

  Enough time is reserved for the ULP-RISC-V to complete the operations above before it goes to halt.

Figure 1-5 shows the relationship between the signals and register bits.

PRELIMINARY

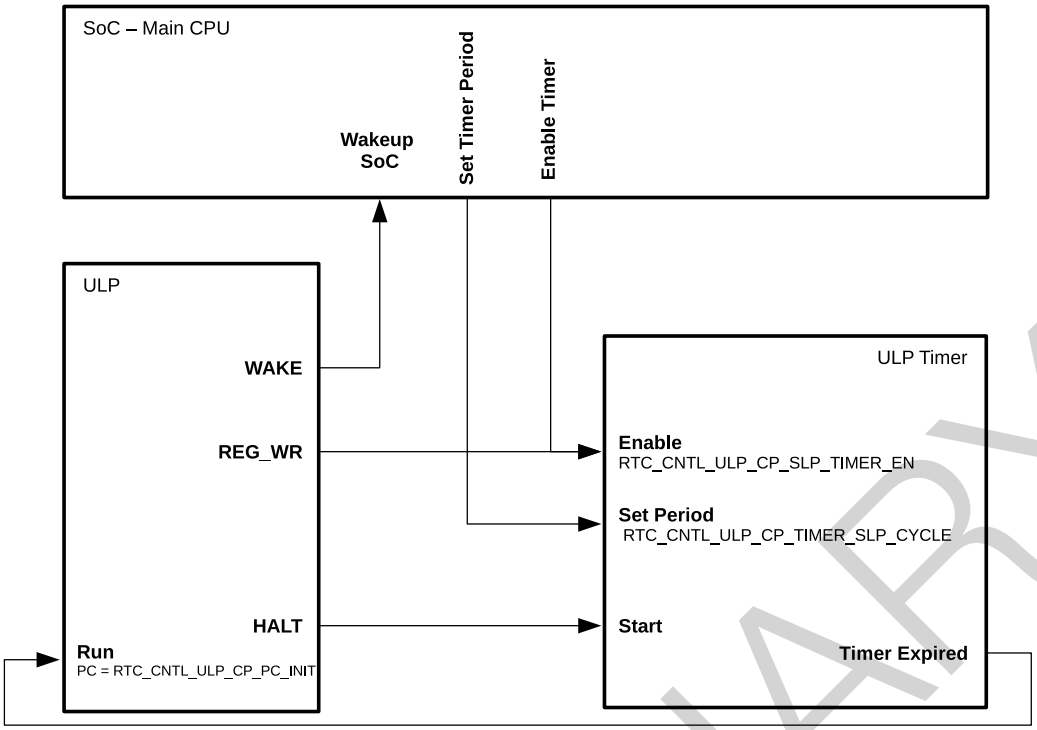


Figure 1-5. Control of ULP Program Execution

1.5 ULP-FSM

1.5.1 Features

ULP-FSM is a programmable finite state machine that can work while the main CPU is in Deep-sleep. ULP-FSM supports instructions for complex logic and arithmetic operations, and also provides dedicated instructions for RTC controllers or peripherals. ULP-FSM can access up to 8 KB of SRAM RTC slow memory (accessible by the CPU) for instructions and data. Hence, such memory is usually used to store instructions and share data between the ULP coprocessor and the CPU. ULP-FSM can be stopped by running HALT instruction.

ULP-FSM has the following features.

- Provides four 16-bit general-purpose registers (R0, R1, R2, and R3) for manipulating data and accessing memory.
- Provides one 8-bit stage count register (Stage_cnt) which can be manipulated by ALU and used in JUMP instructions.
- Supports built-in instructions specially for direct control of low-power peripherals, such as SAR ADC and temperature sensor.

1.5.2 Instruction Set

ULP-FSM supports the following instructions.

- ALU: perform arithmetic and logic operations
- LD, ST, REG_RD and REG_WR: load and store data
- JUMP: jump to a certain address

PRELIMINARY

- WAIT/HALT: manage program execution
- WAKE: wake up CPU or communicate with CPU
- TSENS and ADC: take measurements

Figure 1-6 shows the format of ULP-FSM instructions.

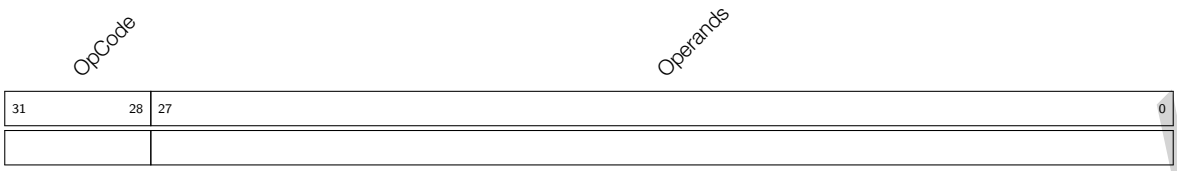


Figure 1-6. ULP-FSM Instruction Format

An instruction, which has one OpCode, can perform various operations, depending on the setting of Operands bits. A good example is the ALU instruction, which is able to perform 10 arithmetic and logic operations; or the JUMP instruction, which may be conditional or unconditional, absolute or relative.

Each instruction has a fixed width of 32 bits. A series of instructions can make a program be executed by the coprocessor. The execution flow inside the program uses 32-bit addressing. The program is stored in a dedicated region called Slow Memory, which is visible to the main CPU under an address range of 0x5000_0000 to 0x5000_1FFF (8 KB).

1.5.2.1 ALU - Perform Arithmetic and Logic Operations

ALU (Arithmetic and Logic Unit) performs arithmetic and logic operations on values stored in ULP coprocessor registers, and on immediate values stored in the instruction itself. The following operations are supported.

- Arithmetic: ADD and SUB
- Logic: bitwise logical AND and bitwise logical OR
- Bit shifting: LSH and RSH
- Moving data to register: MOVE
- PC register operations - STAGE_RST, STAGE_INC, and STAGE_DEC

The ALU instruction, which has one OpCode (7), can perform various arithmetic and logic operations, depending on the setting of the instruction bits [27:21].

Operations Among Registers

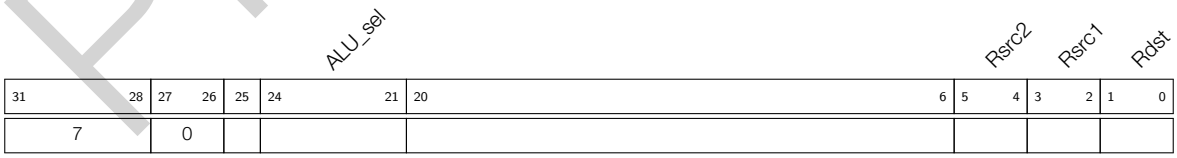


Figure 1-7. Instruction Type — ALU for Operations Among Registers

When bits [27:26] of the instruction in Figure 1-7 are set to 0, ALU performs operations on the data stored in ULP-FSM registers R[0-3]. The types of operations depend on the setting of the instruction bits ALU_sel[24:21] presented in Table 1-2.

PRELIMINARY

Operand	**Description** - see Figure 1-7
Rdst	Register R[0-3], destination
Rsrc1	Register R[0-3], source
Rsrc2	Register R[0-3], source
ALU_sel	ALU operation selection, see Table 1-2

ALU_sel	Instruction	Operation	Description
0	ADD	*Rdst = Rsrc1 + Rsrc2*	Add to register
1	SUB	*Rdst = Rsrc1 - Rsrc2*	Subtract from register
2	AND	*Rdst = Rsrc1 & Rsrc2*	Bitwise logical AND of two operands
3	OR	*Rdst = Rsrc1 | Rsrc2*	Bitwise logical OR of two operands
4	MOVE	*Rdst = Rsrc1*	Move to register
5	LSH	*Rdst = Rsrc1 << Rsrc2*	Bit shifting left
6	RSH	*Rdst = Rsrc1 >> Rsrc2*	Bit shifting right

Table 1-2. ALU Operations Among Registers

Note:

- ADD or SUB operations can be used to set or clear the overflow flag in ALU.
- All ALU operations can be used to set or clear the zero flag in ALU.

Operations with Immediate Value



Figure 1-8. Instruction Type — ALU for Operations with Immediate Value

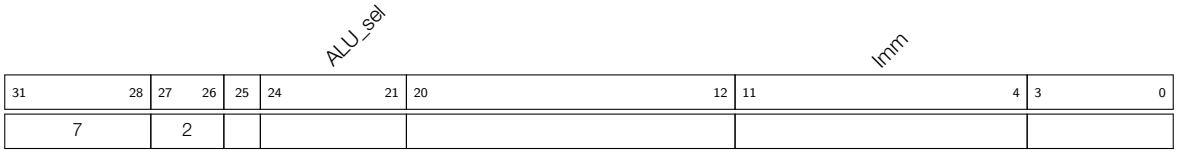
When bits [27:26] of the instruction in Figure 1-8 are set to 1, ALU performs operations using register R[0-3] and the immediate value stored in instruction bits [19:4]. The types of operations depend on the setting of the instruction bits ALU_sel[24:21] presented in Table 1-3.

Operand	**Description** - see Figure 1-8
Rdst	Register R[0-3], destination
Rsrc1	Register R[0-3], source
Imm	16-bit signed immediate value
ALU_sel	ALU operation selection, see Table 1-3

Note:

- ADD or SUB operations can be used to set or clear the overflow flag in ALU.
- All ALU operations can be used to set or clear the zero flag in ALU.

Operations with Stage Count Register



PRELIMINARY

ALU_sel	Instruction	Operation	Description
0	ADD	*Rdst* = *Rsrc1* + *Imm*	Add to register
1	SUB	*Rdst* = *Rsrc1* - *Imm*	Subtract from register
2	AND	*Rdst* = *Rsrc1* & *Imm*	Bitwise logical AND of two operands
3	OR	*Rdst* = *Rsrc1* | *Imm*	Bitwise logical OR of two operands
4	MOVE	*Rdst* = *Imm*	Move to register
5	LSH	*Rdst* = *Rsrc1* << *Imm*	Bit shifting left
6	RSH	*Rdst* = *Rsrc1* >> *Imm*	Bit shifting right

Table 1-3. ALU Operations with Immediate Value

Figure 1-9. Instruction Type — ALU for Operations with Stage Count Register

ALU is also able to increment or decrement by a given value, or reset the 8-bit register Stage_cnt. To do so, bits [27:26] of instruction in Figure 1-9 should be set to 2. The type of operation depends on the setting of the instruction bits ALU_sel[24:21] presented in Table 1-9. The Stage_cnt is a separate register and is not a part of the instruction in Figure 1-9.

Operand	**Description** - see Figure 1-9
Imm	8-bit signed immediate value
ALU_sel	ALU operation selection, see Table 1-4
Stage_cnt	Stage count register, a 8-bit separate register used to store variables, such as loop index

ALU_sel	Instruction	Operation	Description
0	STAGE_INC	*Stage_cnt* = *Stage_cnt* + *Imm*	Increment stage count register
1	STAGE_DEC	*Stage_cnt* = *Stage_cnt* - *Imm*	Decrement stage count register
2	STAGE_RST	*Stage_cnt* = 0	Reset stage count register

Table 1-4. ALU Operations with Stage Count Register

Note: This instruction is mainly used with JUMPS instruction based on the stage count register to form a stage count for-loop. For the usage, please refer to the following pseudocode:

STAGE_RST // clear stage count register
STAGE_INC // stage count register ++
{...} // loop body, containing n instructions
JUMPS (step = n, cond = 0, threshold = m) // If the value of stage count register is less than m, then jump to STAGE_INC, otherwise jump out of the loop. By such way, a cumulative for-loop with threshold m is implemented.

1.5.2.2 ST – Store Data in Memory

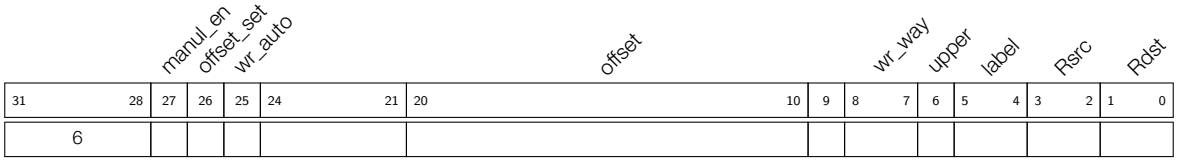


Figure 1-10. Instruction Type - ST

PRELIMINARY

Operand	**Description** - see Figure 1-10
Rdst	Register R[0-3], address of the destination, expressed in 32-bit words
Rsrc	Register R[0-3], 16-bit value to store
label	Data label, 2-bit user defined unsigned value
upper	0: write the low half-word; 1: write the high half-word
wr_way	0: write the full-word; 1: with the label; 3: without the label
offset	11-bit signed value, expressed in 32-bit words
wr_auto	Enable automatic storage mode
offset_set	Offset enable bit. 0: Do not configure the offset for automatic storage mode. 1: Configure the offset for automatic storage mode.
manul_en	Enable manual storage mode

Automatic Storage Mode

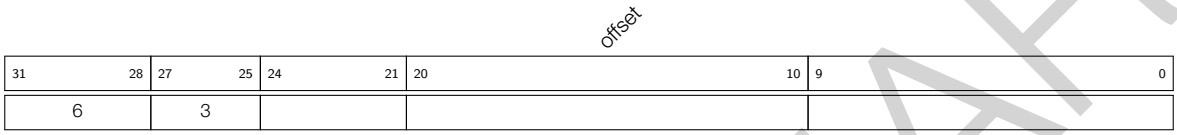


Figure 1-11. Instruction Type - Offset in Automatic Storage Mode (ST-OFFSET)

Operand	**Description** - see Figure 1-11
offset	Initial address offset, 11-bit signed value, expressed in 32-bit words



Figure 1-12. Instruction Type - Data Storage in Automatic Storage Mode (ST-AUTO-DATA)

Operand	**Description** - See Figure 1-12
Rdst	Register R[0-3], address of the destination, expressed in 32-bit words
Rsrc	Register R[0-3], 16-bit value to store
label	Data label, 2-bit user defined unsigned value
wr_way	0: write the full-word; 1: with the label; 3: without the label

Description

This mode is used to access continuous addresses. Before using this mode for the first time, please configure the initial address using ST-OFFSET instruction. Executing the instruction ST-AUTO-DATA will store the 16-bit data in *Rsrc* into the memory address *Rdst* + *Offset*, see Table 1-5. Write_cnt here indicates the times of the instruction ST-AUTO-DATA executed.

PRELIMINARY

wr_way	write_cnt	Store Data	Operation
0	*	Mem [Rdst + Offset]{31:0} = {PC[10:0],3'b0,Label[1:0],Rsrc[15:0]}	Write full-word, including the pointer and the data
1	odd	Mem [Rdst + Offset]{15:0} = {Label[1:0],Rsrc[13:0]}	Store the data with label in the low half-word
1	even	Mem [Rdst + Offset]{31:16} = {Label[1:0],Rscr[13:0]}	Store the data with label in the high half-word
3	odd	Mem [Rdst + Offset]{15:0} = Rsrc[15:0]}	Store the data without label in the low half-word
3	even	Mem [Rdst + Offset]{31:16} = Rsrc[15:0]	Store the data without label in the high half-word

Table 1-5. Data Storage Type - Automatic Storage Mode

The full-word written to RTC memory is built as follows:

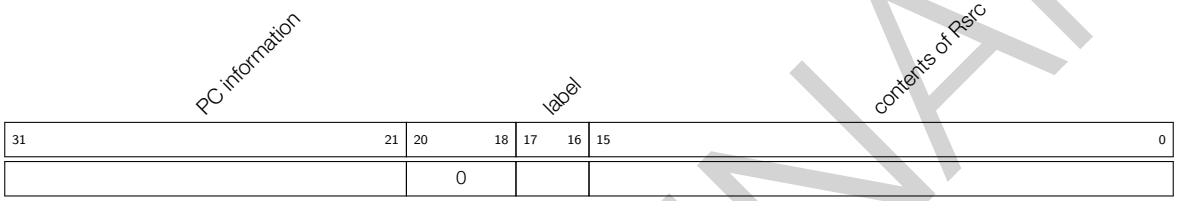


Figure 1-13. Data Structure of RTC_SLOW_MEM[Rdst + Offset]

Bits	**Description** - See Figure 1-13
bits [15:0]	store the content of Rsrc
bits [17:16]	data label, 2-bit user defined unsigned value
bits [20:18]	3'b0 by default
bits [31:21]	hold the PC of current instruction, expressed in 32-bit words

Note:

- When full-word is written, the offset will be automatically incremented by 1 after each ST-AUTO-DATA execution.
- When half-word is written (low half-word first), the offset will be automatically incremented by 1 after twice ST-AUTO-DATA execution.
- This instruction can only access 32-bit memory words.
- The "Mem" written is the RTC_SLOW_MEM memory. Address 0, as seen by the ULP coprocessor, corresponds to address 0x50000000, as seen by the main CPU.

Manual Storage Mode

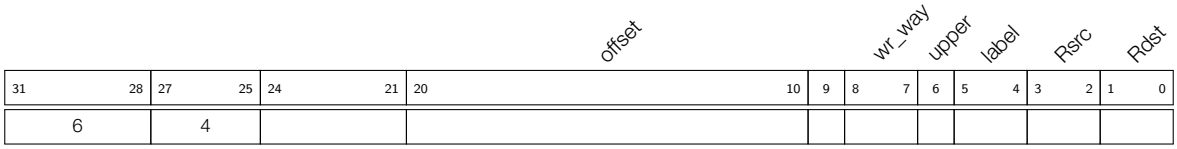


Figure 1-14. Instruction Type - Data Storage in Manual Storage Mode

PRELIMINARY

Operand	**Description** - See Figure 1-14
Rdst	Register R[0-3], address of the destination, expressed in 32-bit words
Rsrc	Register R[0-3], 16-bit value to store
label	Data label, 2-bit user defined unsigned value
upper	0: Write the low half-word; 1: write the high half-word
wr_way	0: Write the full-word; 1: with the label; 3: without the label
offset	11-bit signed value, expressed in 32-bit words

Description

Manual storage mode is mainly used for storing data into discontinuous addresses. Each instruction needs a storage address and offset. The detailed storage methods are shown in Table 1-6.

wr_way	upper	Data	Operation
0	*	Mem [Rdst + Offset]{31:0} = {PC[10:0],3'b0, Label[1:0],Rsrc[15:0]}	Write full-word, including the pointer and the data
1	0	Mem [Rdst + Offset]{15:0} = {Label[1:0],Rsrc[13:0]}	Store the data with label in the low half-word
1	1	Mem [Rdst + Offset]{31:16} = {Label[1:0],Rsrc[13:0]}	Store the data with label in the high half-word
3	0	Mem [Rdst + Offset]{15:0} = Rsrc[15:0]	Store the data without label in the low half-word
3	1	Mem [Rdst + Offset]{31:16} = Rsrc[15:0]	Store the data without label in the high half-word

Table 1-6. Data Storage - Manual Storage Mode

1.5.2.3 LD – Load Data from Memory



Figure 1-15. Instruction Type - LD

Operand	**Description** - see Figure 1-15
Rdst	Register R[0-3], destination
Rsrc	Register R[0-3], address of destination memory, expressed in 32-bit words
Offset	11-bit signed value, expressed in 32-bit words
rd_upper	Choose which half-word to read: 1 - read the high half-word 0 - read the low half-word

Description

This instruction loads the low or high 16-bit half-word, depending on *rd_upper*, from memory with address *Rsrc* + *offset* into the destination register *Rdst*:

Rdst[15:0] = Mem[Rsrc + Offset]

PRELIMINARY

Note:

- This instruction can only access 32-bit memory words.
- The "Mem" loaded is the RTC_SLOW_MEM memory. Address 0, as seen by the ULP coprocessor, corresponds to address 0x50000000, as seen by the main CPU.

1.5.2.4 JUMP – Jump to an Absolute Address

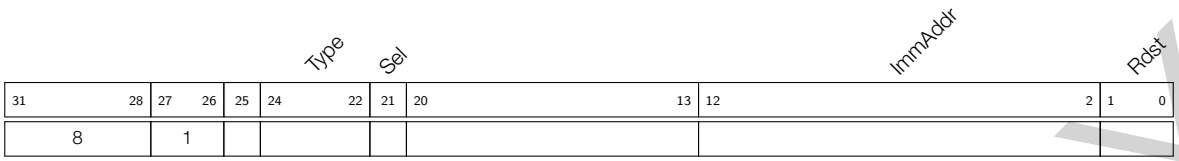


Figure 1-16. Instruction Type - JUMP

Operand	**Description** - see Figure 1-16
Rdst	Register R[0-3], containing address to jump to (expressed in 32-bit words)
ImmAddr	11-bit address, expressed in 32-bit words
Sel	Select the address to jump to: 0 - jump to the address stored in *ImmAddr* 1 - jump to the address stored in *Rdst*
Type	Jump type: 0 - make an unconditional jump 1 - jump only if the last ALU operation has set zero flag 2 - jump only if the last ALU operation has set overflow flag

Note:

All jump addresses are expressed in 32-bit words.

Description

The instruction executes a jump to a specified address. The jump can be either unconditional or based on the ALU flag.

1.5.2.5 JUMPR – Jump to a Relative Address (Conditional upon R0)

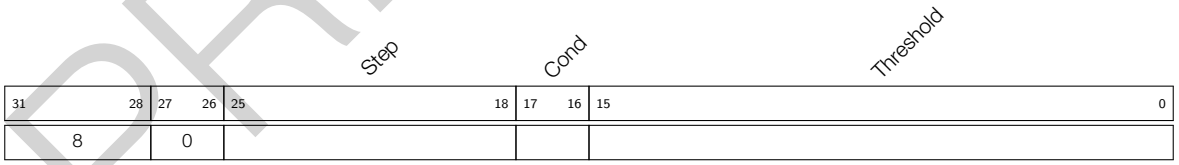


Figure 1-17. Instruction Type - JUMPR

PRELIMINARY

Operand	**Description** - see Figure 1-17
Threshold	Threshold value for condition (see *Cond* below) to jump
Cond	Condition to jump: 0 - jump if R0 < *Threshold* 1 - jump if R0 > *Threshold* 2 - jump if R0 = *Threshold*
Step	Relative shift from current position, expressed in 32-bit words: if Step[7] = 0, then PC = PC + Step[6:0] if Step[7] = 1, then PC = PC - Step[6:0]

Note:

All jump addresses are expressed in 32-bit words.

Description

The instruction executes a jump to a relative address, if the condition is true. The condition is the result of comparing the R0 register value and the *Threshold* value.

1.5.2.6 JUMPS – Jump to a Relative Address (Conditional upon Stage Count Register)

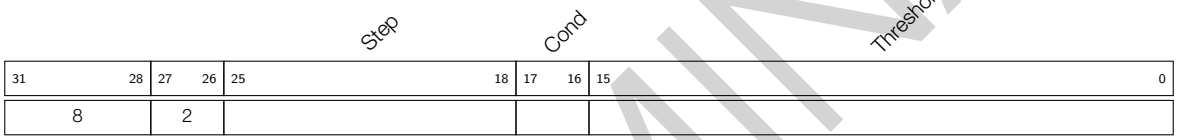


Figure 1-18. Instruction Type - JUMPS

Operand	**Description** - see Figure 1-18
Threshold	Threshold value for condition (see *Cond* below) to jump
Cond	Condition to jump: 1X - jump if *Stage_cnt* <= *Threshold* 00 - jump if *Stage_cnt* < *Threshold* 01 - jump if *Stage_cnt* >= *Threshold*
Step	Relative shift from current position, expressed in 32-bit words: if Step[7] = 0, then PC = PC + Step[6:0] if Step[7] = 1, then PC = PC - Step[6:0]

Note:

- For more information about the stage count register, please refer to Section 1.5.2.1.
- All jump addresses are expresses in 32-bit words.

Description

The instruction executes a jump to a relative address if the condition is true. The condition itself is the result of comparing the value of *Stage_cnt* (stage count register) and the *Threshold* value.

PRELIMINARY

1.5.2.7 HALT – End the Program

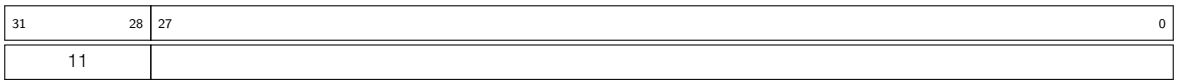


Figure 1-19. Instruction Type - HALT

Description

The instruction ends the operation of the ULP-FSM and puts it into power-down mode.

Note:

After executing this instruction, the ULP coprocessor wakeup timer gets started.

1.5.2.8 WAKE – Wake up the Chip

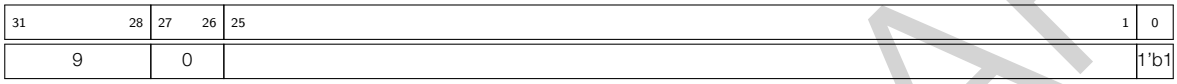


Figure 1-20. Instruction Type - WAKE

Description

This instruction sends an interrupt from the ULP-FSM to the RTC controller.

- If the chip is in Deep-sleep mode, and the ULP wakeup timer is enabled, the above-mentioned interrupt will wake up the chip.
- If the chip is not in Deep-sleep mode, and the ULP interrupt bit RTC_CNTL_ULP_CP_INT_ENA is set in register RTC_CNTL_INT_ENA_REG, an RTC interrupt will be triggered.

1.5.2.9 WAIT – Wait for a Number of Cycles

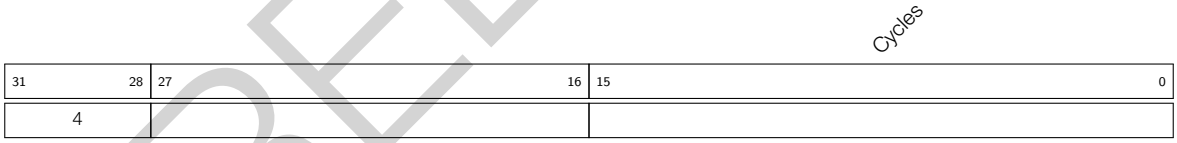


Figure 1-21. Instruction Type - WAIT

Operand	**Description** - see Figure 1-21
Cycles	The number of cycles to wait

Description

The instruction will delay the ULP-FSM for a given number of cycles.

PRELIMINARY

1.5.2.10 TSENS – Take Measurement with Temperature Sensor

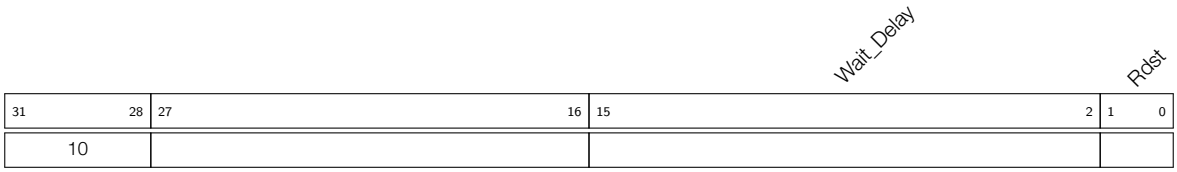


Figure 1-22. Instruction Type - TSENS

Operand	**Description** - see Figure 1-22
Rdst	Destination Register R[0-3], results will be stored in this register.
Wait_Delay	Number of cycles used to perform the measurement.

Description

Increasing the measurement cycles *Wait_Delay* helps improve the accuracy and optimize the result. The instruction performs measurement via temperature sensor and stores the result into a general purpose register.

1.5.2.11 ADC – Take Measurement with ADC



Figure 1-23. Instruction Type - ADC

Operand	**Description** - see Figure 1-23
Rdst	Destination Register R[0-3], results will be stored in this register.
Sar_Mux	Enable SAR ADC channel. Channel No. is [Sar_Mux - 1]. For more information, see Chapter 4 *On-Chip Sensors and Analog Signal Processing [to be added later]*.
Sel	Select ADC. 0: select SAR ADC1; 1: select SAR ADC2, see Table 1-7.

Table 1-7. Input Signals Measured Using the ADC Instruction

Pad/Signal/GPIO	*Sar_Mux*	ADC Selection (*Sel*)
GPIO1	1	*Sel* = 0, select SAR ADC1
GPIO2	2	
GPIO3	3	
GPIO4	4	
GPIO5	5	
GPIO6	6	
GPIO7	7	
GPIO8	8	
GPIO9	9	
GPIO10	10	

PRELIMINARY

Pad/Signal/GPIO	*Sar_Mux*	ADC Selection *Sel*
GPIO11	1	*Sel* = 1, select SAR ADC2
GPIO12	2	
GPIO13	3	
GPIO14	4	
XTAL_32k_P	5	
XTAL_32k_N	6	*Sel* = 1, select SAR ADC2
GPIO17	7	
GPIO18	8	
GPIO19	9	
GPIO20	10	

1.5.2.12 REG_RD – Read from Peripheral Register

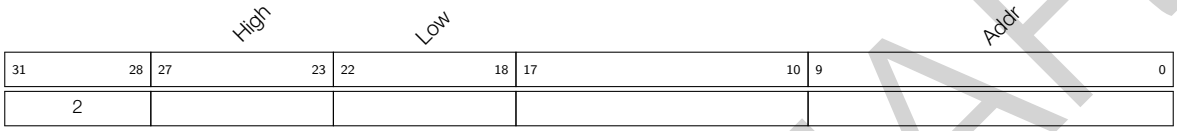


Figure 1-24. Instruction Type - REG_RD

Operand	**Description** - see Figure 1-24
Addr	Peripheral register address, in 32-bit words
Low	Register start bit number
High	Register end bit number

Description

The instruction reads up to 16 bits from a peripheral register into a general-purpose register:

R0 = REG[Addr][High:Low]

In case of more than 16 bits being requested, i.e. *High* - *Low* + 1 > 16, then the instruction will return [Low+15:Low].

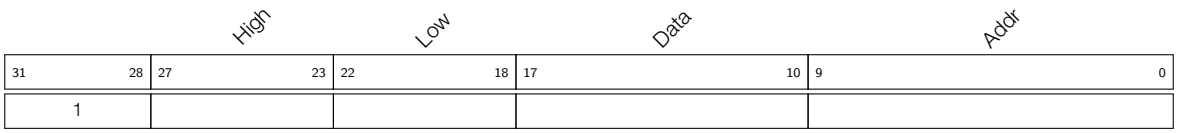
Note:

- This instruction can access registers in RTC_CNTL, RTC_IO, SENS, and RTC_I2C peripherals. Address of the register, as seen from the ULP coprocessor (addr_ulp), can be calculated from the address of the same register on the main bus (addr_bus), as follows:

  addr_ulp = (addr_bus - DR_REG_RTCCNTL_BASE)/4

- The *addr_ulp* is expressed in 32-bit words (not in bytes), and value 0 maps onto the DR_REG_RTCCNTL_BASE (as seen from the main CPU). Thus, 10 bits of address cover a 4096-byte range of peripheral register space, including regions DR_REG_RTCCNTL_BASE (0x6000800), DR_REG_RTCIO_BASE (0x60008400), DR_REG_SENS_BASE (0x60008800), and DR_REG_RTC_I2C_BASE (0x60008C00). For more information about address mapping, see Section 1.8.

1.5.2.13 REG_WR – Write to Peripheral Register



PRELIMINARY

Figure 1-25. Instruction Type - REG_WR

Operand	**Description** - see Figure 1-25
Addr	Register address, expressed in 32-bit words
Data	Value to write, 8 bits
Low	Register start bit number
High	Register end bit number

Description

This instruction writes up to 8 bits from an immediate data value into a peripheral register.

REG[Addr][High:Low] = Data

If more than 8 bits are requested, i.e. *High* - *Low* + 1 > 8, then the instruction will pad with zeros the bits above the eighth bit.

Note:

See notes regarding *addr_ulp* in Section 1.5.2.12.

1.6 ULP-RISC-V

1.6.1 Features

- Support RV32IMC instruction set
- Thirty-two 32-bit general-purpose registers
- 32-bit multiplier and divider
- Support for interrupts

1.6.2 Multiplier and Divider

ULP-RISC-V has an independent multiplication and division unit. The efficiency of multiplication and division instructions is shown in the following table.

Table 1-8. Instruction Efficiency

Operation	Instruction	Execution Cycle	Instruction Description
Multiply	MUL	34	Multiply two 32-bit integers and return the lower 32-bit of the result
	MULH	66	Multiply two 32-bit signed integers and return the higher 32-bit of the result
	MULHU	66	Multiply two 32-bit unsigned integers and return the higher 32-bit of the result
	MULHSU	66	Multiply a 32-bit signed integer with a unsigned integer and return the higher 32-bit of the result

PRELIMINARY

Operation	Instruction	Execution Cycle	Instruction Description
Divide	DIV	34	Divide a 32-bit integer by a 32-bit integer and return the quotient
	DIVU	34	Divide a 32-bit unsigned integer by a 32-bit unsigned integer and return the quotient
	REM	34	Divide a 32-bit signed integer by a 32-bit signed integer and return the remainder
	REMU	34	Divide a 32-bit unsigned integer by a 32-bit unsigned integer and return the remainder

1.6.3 ULP-RISC-V Interrupts

1.6.3.1 Introduction

The interrupt controller of ULP-RISC-V is implemented by using a customized instruction set, instead of RISC-V Privileged ISA specification, aiming to reduce the size of ULP-RISC-V.

1.6.3.2 Interrupt Controller

ULP-RISC-V has 32 interrupt sources, but only four of them are available in the real design, as shown in the table below, including:

- internal sources: INT 0 ~ INT 2, triggered by internal interrupt events.
- external source: INT 31, triggered by the peripheral interrupts of ESP32-S3.

Type	IRQ	Triggered by
Internal	0	Internal timer interrupt
Internal	1	EBREAK/ECALL or Illegal Instruction
Internal	2	BUS Error (Unaligned Memory Access)
External	31	RTC peripheral interrupts

Table 1-9. ULP-RISC-V Interrupt Sources

Note:

If illegal instruction interrupt or bus error interrupt is disabled, ULP-RISC-V goes to HALT when the two errors occur.

ULP-RISC-V provides four 32-bit interrupt registers, Q0 ~ Q3, to handle interrupt service routine (ISR). Table 1-10 shows the function of each register.

PRELIMINARY

Register	Function
Q0	Store the returned address. If the interrupt instruction is a compressed one, the lowest bit of this register will be set.
Q1	Bitmap. If the corresponding bit of an interrupt is set, this interrupt will trigger its ISR.
Q2	Reserved. An option for ISR to store data.
Q3	Reserved. An option for ISR to store data.

Table 1-10. ULP-RISC-V Interrupt Registers

Note:

- If more than one bits in Q1 are set, all the corresponding interrupts will call the same ISR. For such reason, users need to program ISR to check the interrupt number and execute corresponding program.
- After ULP-RISC-V is reset, all the interrupts are disabled.

1.6.3.3 Interrupt Instructions

All these interrupt instructions are standard R-type instructions, with the same OpCode of custom0 (0001011). Figure 1-26 shows the format of standard R-type instructions. Note the fields funct3 (f3) and rs2 are ignored in these instructions.

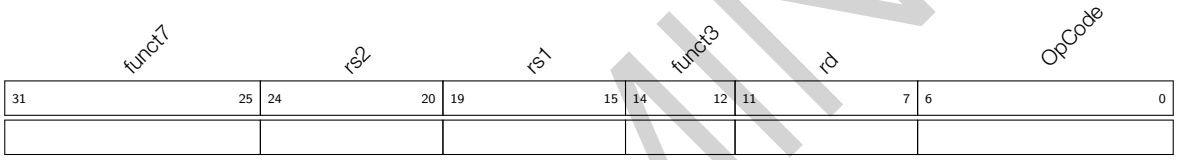


Figure 1-26. Standard R-type Instruction Format

Instruction: getq rd,qs

This instruction copies the value of Q*x* into a general purpose register rd.

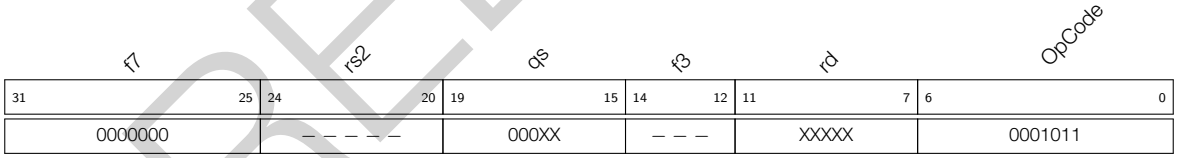
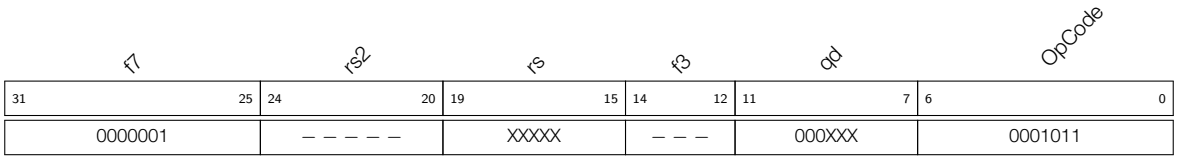


Figure 1-27. Interrupt Instruction - getq rd, qs

Operand	**Description** - See Figure 1-27
rd	Target general purpose register, holds the value of interrupt register specified by qs.
qs	Address of interrupt register Q*x*.
f7	Interrupt instruction number.

Instruction: setq qd,rs

This instruction copies the value of general purpose register rs to Q*x*.



PRELIMINARY

Figure 1-28. Interrupt Instruction - setq qd,rs

Operand	**Description** - See Figure 1-28
qd	Target interrupt register
rs	Source general purpose register, stores the value to be written to interrupt register.
f7	Interrupt instruction number.

Instruction: retirq

This instruction copies the value of Q*0* to CPU PC, and enables interrupt again.

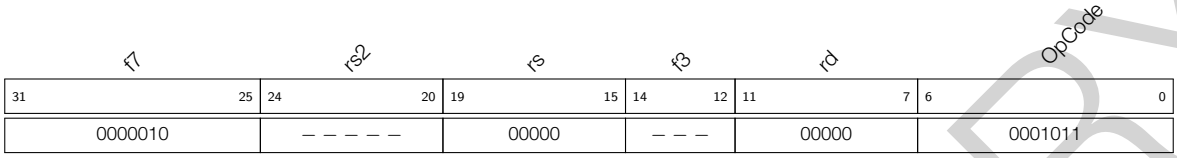


Figure 1-29. Interrupt Instruction - retirq

Operand	**Description** - See Figure 1-29
f7	Interrupt instruction number.

Instruction: maskirq rd,rs

This instruction copies the value of Q*1* to the register rd, and copies the value of register rs to Q*1*.

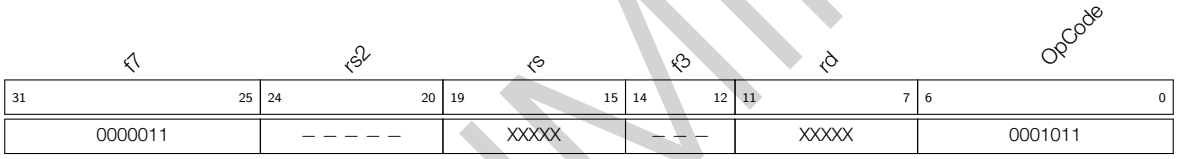


Figure 1-30. Interrupt Instruction — Maskirq rd rs

Operand	**Description** - See Figure 1-30
rd	Target general purpose register, stores current value of register Q1.
rs	Source general purpose register, stores the value to be written to Q1.
f7	Interrupt instruction number.

1.6.3.4 RTC Peripheral Interrupts

The interrupts from some sensors, software, and RTC I2C can be routed to ULP-RISC-V. To enable the interrupts, please set the register SENS_SAR_COCPU_INT_ENA_REG, see Table 1-11.

PRELIMINARY

Enable bit	Interrupt	Description
0	TOUCH_DONE_INT	Triggered when the touch sensor completes the scan of a channel
1	TOUCH_INACTIVE_INT	Triggered when the touch pad is released
2	TOUCH_ACTIVE_INT	Triggered when the touch pad is touched
3	SARADC1_DONE_INT	Triggered when SAR ADC1 completes the conversion one time
4	SARADC2_DONE_INT	Triggered when SAR ADC2 completes the conversion one time
5	TSENS_DONE_INT	Triggered when the temperature sensor completes the dump of its data
6	RISCV_START_INT	Triggered when ULP-RISC-V powers on and starts working
7	SW_INT	Triggered by software
8	SWD_INT	Triggered by timeout of Super Watchdog (SWD)
9	TOUCH_TIME_OUT_INT	Triggered by touch pad sampling timeout
10	TOUCH_APPROACH_LOOP_DONE_INT	Triggered when touch pad completes an APPROACH sampling
11	TOUCH_SCAN_DONE_INT	Triggered when touch pad completes the scan of the final channel

Table 1-11. ULP-RISC-V Interrupt List

Note:

- Besides the above-mentioned interrupts, ULP-RISC-V can also handle the interrupt from RTC_IO by simply configuring RTC_IO as input mode. Users can configure RTCIO_GPIO_PIN*n*_INT_TYPE to select the interrupt trigger modes, but only level trigger modes are available. For more details about RTC_IO configuration, see Chapter 5 *IO MUX and GPIO Matrix (GPIO, IO MUX)*.
- The interrupt from RTC_IO can be cleared by releasing RTC_IO and its source can be read from the register RTCIO_RTC_GPIO_STATUS_REG.
- The SW_INT interrupt is generated by configuring the register RTC_CNTL_COCPU_SW_INT_TRIGGER.
- For the information about RTC I2C interrupts, please refer to Section 1.7.4.

1.7 RTC I2C Controller

ULP coprocessor reads from or writes to external I2C slave devices via RTC I2C controller.

1.7.1 Connecting RTC I2C Signals

SDA and SCL signals can be mapped onto two out of the four GPIO pins, which are identified in Table RTC_MUX Pad List in Chapter 5 *IO MUX and GPIO Matrix (GPIO, IO MUX)*, using the register RTCIO_SAR_I2C_IO_REG.

PRELIMINARY

1.7.2 Configuring RTC I2C

Before ULP coprocessor can communicate using I2C instruction, RTC I2C need to be configured. Configuration is performed by writing certain timing parameters into the RTC I2C registers. This can be done by the program running on the main CPU, or by the ULP coprocessor itself.

Note:
The timing parameters are configured in cycles of RTC_FAST_CLK running at 17.5 MHz.

1. Set the low and high SCL half-periods by configuring RTC_I2C_SCL_LOW_PERIOD_REG and RTC_I2C_SCL_HIGH_PERIOD_REG in RTC_FAST_CLK cycles (e.g. RTC_I2C_SCL_LOW_PERIOD_REG = 40, RTC_I2C_SCL_HIGH_PERIOD_REG = 40 for 100 kHz frequency).
2. Set the number of cycles between the SDA switch and the falling edge of SCL by using RTC_I2C_SDA_DUTY_REG in RTC_FAST_CLK (e.g. RTC_I2C_SDA_DUTY_REG = 16).
3. Set the waiting time after the START signal by using RTC_I2C_SCL_START_PERIOD_REG (e.g. RTC_I2C_SCL_START_PERIOD = 30).
4. Set the waiting time before the END signal by using RTC_I2C_SCL_STOP_PERIOD_REG (e.g. RTC_I2C_SCL_STOP_PERIOD = 44).
5. Set the transaction timeout by using RTC_I2C_TIME_OUT_REG (e.g. RTC_I2C_TIME_OUT_REG = 200).
6. Configure the RTC I2C controller into master mode by setting the bit RTC_I2C_MS_MODE in RTC_I2C_CTRL_REG.
7. Write the address(es) of external slave(s) to SENS_I2C_SLAVE_ADDR*n* (*n*: 0-7). Up to eight slave addresses can be pre-programmed this way. One of these addresses can then be selected for each transaction as part of the RTC I2C instruction.

Once RTC I2C is configured, the main CPU or the ULP coprocessor can communicate with the external I2C devices.

1.7.3 Using RTC I2C

1.7.3.1 Instruction Format

The format of RTC I2C instruction is consistent with that of I2C0/I2C1, see Section I2C CMD Controller in Chapter 25 *I2C Controller (I2C)*. The only difference is that RTC I2C provides fixed instructions for different operations, as follows:

- Command 0 ~ Command 1: specifically for I2C write operation
- Command 2 ~ Command 6: specifically for I2C read operation

Note: All slave addresses are expressed in 7 bits.

PRELIMINARY

1.7.3.2 I2C_RD - I2C Read Workflow

Preparation for RTC I2C read:

- Configure the instruction list of RTC I2C (see Section CMD_Controller in Chapter 25 *I2C Controller (I2C)*), including instruction order, instruction code, read data number (byte_num), and other information.
- Configure the slave register address by setting the register SENS_SAR_I2C_CTRL[18:11].
- Start RTC I2C transmission by setting SENS_SAR_I2C_START_FORCE and SENS_SAR_I2C_START.
- When an RTC_I2C_RX_DATA_INT interrupt is received, transfer the read data stored in RTC_I2C_RDATA to SRAM RTC slow memory, or use the data directly.

The I2C_RD instruction performs the following operations (see Figure 1-31):

1. Master generates a START signal.
2. Master sends slave address, with r/w bit set to 0 ("write"). Slave address is obtained from SENS_I2C_SLAVE_ADDR*n*.
3. Slave generates ACK.
4. Master sends slave register address.
5. Slave generates ACK.
6. Master generates a repeated START (RSTART) signal.
7. Master sends slave address, with r/w bit set to 1 ("read").
8. Slave sends one byte of data.
9. Master checks whether the number of transmitted bytes reaches the number set by the current instruction (byte_num). If yes, master jumps out of the read instruction and sends an NACK signal. Otherwise master repeats Step 8 and waits for the slave to send the next byte.
10. Master generates a STOP signal and stops reading.

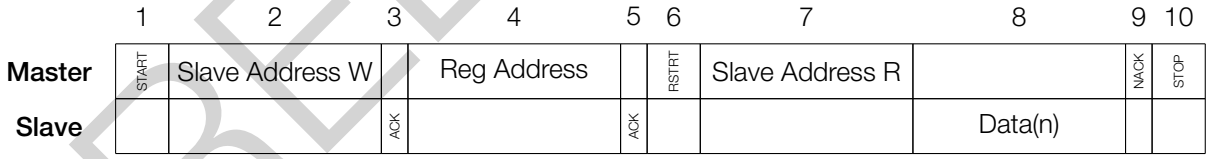


Figure 1-31. I2C Read Operation

Note:

The RTC I2C peripheral samples the SDA signals on the falling edge of SCL. If the slave changes SDA in less than 0.38 ms, the master may receive incorrect data.

1.7.3.3 I2C_WR - I2C Write Workflow

Preparation for RTC I2C write:

- Configure RTC I2C instruction list, including instruction order, instruction code, and the data to be written in byte (byte_num). See the configuration of I2C0/I2C1 in Section CMD_Controller in Chapter 25 *I2C Controller (I2C)*.

PRELIMINARY

- Configure the slave register address by setting the register SENS_SAR_I2C_CTRL[18:11], and the data to be transmitted in SENS_SAR_I2C_CTRL[26:19].
- Set SENS_SAR_I2C_START_FORCE and SENS_SAR_I2C_START to start the transmission.
- Update the next data to be transmitted in SENS_SAR_I2C_CTRL[26:19], each time when an RTC_I2C_TX_DATA_INT interrupt is received.

The I2C_WR instruction performs the following operations, see Figure 1-32.

1. Master generates a START signal.
2. Master sends slave address, with r/w bit set to 0 ("write"). Slave address is obtained from SENS_I2C_SLAVE_ADDR*n*.
3. Slave generates ACK.
4. Master sends slave register address.
5. Slave generates ACK.
6. Master generates a repeated START (RSTART) signal.
7. Master sends slave address, with r/w bit set to 0 ("write").
8. Master sends one byte of data.
9. Slave generates ACK. Master checks whether the number of transmitted bytes reaches the number set by the current instruction (byte_num). If yes, master jumps out of the write instruction and starts the next instruction. Otherwise the master repeats Step 8 and sends the next byte.
10. Master generates a STOP signal and stops the transmission.

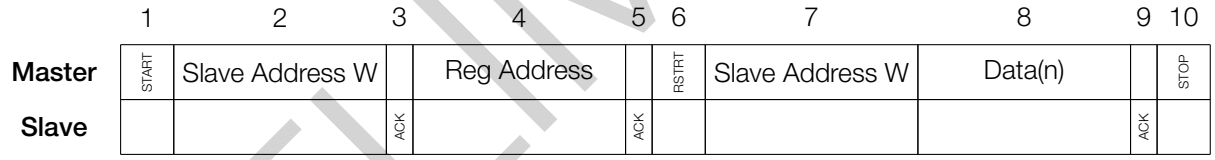


Figure 1-32. I2C Write Operation

1.7.3.4 Detecting Error Conditions

Applications can query specific bits in the RTC_I2C_INT_ST_REG register to check if the transaction is successful. To enable checking for specific communication events, their corresponding bits should be set in register RTC_I2C_INT_ENA_REG. Note that the bit map is shifted by 1. If a specific communication event is detected and its corresponding bit in register RTC_I2C_INT_ST_REG is set, the event can then be cleared using register RTC_I2C_INT_CLR_REG.

1.7.4 RTC I2C Interrupts

- RTC_I2C_SLAVE_TRAN_COMP_INT: Triggered when the slave finishes the transaction.
- RTC_I2C_ARBITRATION_LOST_INT: Triggered when the master loses control of the bus.
- RTC_I2C_MASTER_TRAN_COMP_INT: Triggered when the master completes the transaction.
- RTC_I2C_TRANS_COMPLETE_INT: Triggered when a STOP signal is detected.

PRELIMINARY

- RTC_I2C_TIME_OUT_INT: Triggered by time out event.
- RTC_I2C_ACK_ERR_INT: Triggered by ACK error.
- RTC_I2C_RX_DATA_INT: Triggered when data is received.
- RTC_I2C_TX_DATA_INT: Triggered when data is transmitted.
- RTC_I2C_DETECT_START_INT: Triggered when a START signal is detected.

1.8 Address Mapping

Table 1-12 shows the address mapping and available base registers for the peripherals accessible by ULP coprocessors.

Table 1-12. Address Mapping

Peripheral(s)	Base Register	Main Bus Address	ULP-FSM Base	ULP-RISC-V Base
RTC Control	DR_REG_RTCCNTL_BASE	0x60008000	0x8000	0x8000
RTC GPIO	DR_REG_RTC_IO_BASE	0x60008400	0x8400	0xA400
ADC, Touch, TSENS	DR_REG_SENS_BASE	0x60008800	0x8800	0xC800
RTC I2C	DR_REG_RTC_I2C_BASE	0x60008C00	0x8C00	0xEC00

To find more information about registers for these peripherals, please check the following chapters.

Table 1-13. Description of Registers for Peripherals Accessible by ULP Coprocessors

Registers Available for Peripherals	Described in Which Chapter
Registers for RTC Control	Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*
Registers for RTC GPIO	Chapter 5 *IO MUX and GPIO Matrix (GPIO, IO MUX)*
Registers for ARC, Touch, TSENS	Chapter 4 *On-Chip Sensors and Analog Signal Processing [to be added later]*
Registers for RTC I2C	Section 1.9 *Register Summary* in this chapter

1.9 Register Summary

The following registers are used in ULP coprocessor:

- ULP (ALWAYS_ON) registers: not reset due to power down of RTC_PERI domain. See Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*.
- ULP (RTC_PERI) registers: reset due to power down of RTC_PERI domain. See Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*.
- RTC I2C registers: I2C related registers, including RTC I2C (RTC_PERI) and RTC I2C (I2C) registers.

1.9.1 ULP (ALWAYS_ON) Register Summary

The addresses in this section are relative to low-power management base address provided in Table 3-3 in Chapter 3 *System and Memory*.

PRELIMINARY

Name	Description	Address	Access
ULP Timer Registers			
RTC_CNTL_ULP_CP_TIMER_REG	Configure the timer	0x00FC	varies
RTC_CNTL_ULP_CP_TIMER_1_REG	Configure sleep cycle of the timer	0x0134	R/W
ULP-FSM Register			
RTC_CNTL_ULP_CP_CTRL_REG	ULP-FSM configuration register	0x0100	R/W
ULP-RISC-V Register			
RTC_CNTL_COCPU_CTRL_REG	ULP-RISC-V configuration register	0x0104	varies

1.9.2 ULP (RTC_PERI) Register Summary

The addresses in this section are relative to low-power management base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
ULP-RISC-V Registers			
SENS_ SAR_COCPU_INT_RAW_REG	Interrupt raw bit of ULP-RISC-V	0x00E8	RO
SENS_SAR_COCPU_INT_ENA_REG	Interrupt enable bit of ULP-RISC-V	0x00EC	R/W
SENS_SAR_COCPU_INT_ST_REG	Interrupt status bit of ULP-RISC-V	0x00F0	RO
SENS_SAR_COCPU_INT_CLR_REG	Interrupt clear bit of ULP-RISC-V	0x00F4	WO

1.9.3 RTC I2C (RTC_PERI) Register Summary

The addresses in this section are relative to low-power management base address + 0x0800 provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
RTC I2C Controller Register			
SENS_SAR_I2C_CTRL_REG	Configure RTC I2C transmission	0x0058	R/W
RTC I2C Slave Address Registers			
SENS_SAR_SLAVE_ADDR1_REG	Configure slave addresses 0-1 of RTC I2C	0x0040	R/W
SENS_SAR_SLAVE_ADDR2_REG	Configure slave addresses 2-3 of RTC I2C	0x0044	R/W
SENS_SAR_SLAVE_ADDR3_REG	Configure slave addresses 4-5 of RTC I2C	0x0048	R/W
SENS_SAR_SLAVE_ADDR4_REG	Configure slave addresses 6-7 of RTC I2C	0x004C	R/W

1.9.4 RTC I2C (I2C) Register Summary

The addresses in this section are relative to low-power management base address + 0x0C00 provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
RTC I2C Signal Setting Registers			
RTC_I2C_SCL_LOW_REG	Configure the low level width of SCL	0x0000	R/W
RTC_I2C_SCL_HIGH_REG	Configure the high level width of SCL	0x0014	R/W
RTC_I2C_SDA_DUTY_REG	Configure the SDA hold time after a negative SCL edge	0x0018	R/W

PRELIMINARY

Name	Description	Address	Access
RTC_I2C_SCL_START_PERIOD_REG	Configure the delay between the SDA and SCL negative edge for a start condition	0x001C	R/W
RTC_I2C_SCL_STOP_PERIOD_REG	Configure the delay between SDA and SCL positive edge for a stop condition	0x0020	R/W
RTC I2C Control Registers			
RTC_I2C_CTRL_REG	Transmission setting	0x0004	R/W
RTC_I2C_STATUS_REG	RTC I2C status	0x0008	RO
RTC_I2C_TO_REG	Configure RTC I2C timeout	0x000C	R/W
RTC_I2C_SLAVE_ADDR_REG	Configure slave address	0x0010	R/W
RTC I2C Interrupt Registers			
RTC_I2C_INT_CLR_REG	Clear RTC I2C interrupt	0x0024	WO
RTC_I2C_INT_RAW_REG	RTC I2C raw interrupt	0x0028	RO
RTC_I2C_INT_ST_REG	RTC I2C interrupt status	0x002C	RO
RTC_I2C_INT_ENA_REG	Enable RTC I2C interrupt	0x0030	R/W
RTC I2C Status Register			
RTC_I2C_DATA_REG	RTC I2C read data	0x0034	varies
RTC I2C Command Registers			
RTC_I2C_CMD0_REG	RTC I2C Command 0	0x0038	varies
RTC_I2C_CMD1_REG	RTC I2C Command 1	0x003C	varies
RTC_I2C_CMD2_REG	RTC I2C Command 2	0x0040	varies
RTC_I2C_CMD3_REG	RTC I2C Command 3	0x0044	varies
RTC_I2C_CMD4_REG	RTC I2C Command 4	0x0048	varies
RTC_I2C_CMD5_REG	RTC I2C Command 5	0x004C	varies
RTC_I2C_CMD6_REG	RTC I2C Command 6	0x0050	varies
RTC_I2C_CMD7_REG	RTC I2C Command 7	0x0054	varies
RTC_I2C_CMD8_REG	RTC I2C Command 8	0x0058	varies
RTC_I2C_CMD9_REG	RTC I2C Command 9	0x005C	varies
RTC_I2C_CMD10_REG	RTC I2C Command 10	0x0060	varies
RTC_I2C_CMD11_REG	RTC I2C Command 11	0x0064	varies
RTC_I2C_CMD12_REG	RTC I2C Command 12	0x0068	varies
RTC_I2C_CMD13_REG	RTC I2C Command 13	0x006C	varies
RTC_I2C_CMD14_REG	RTC I2C Command 14	0x0070	varies
RTC_I2C_CMD15_REG	RTC I2C Command 15	0x0074	varies
Version register			
RTC_I2C_DATE_REG	Version control register	0x00FC	R/W

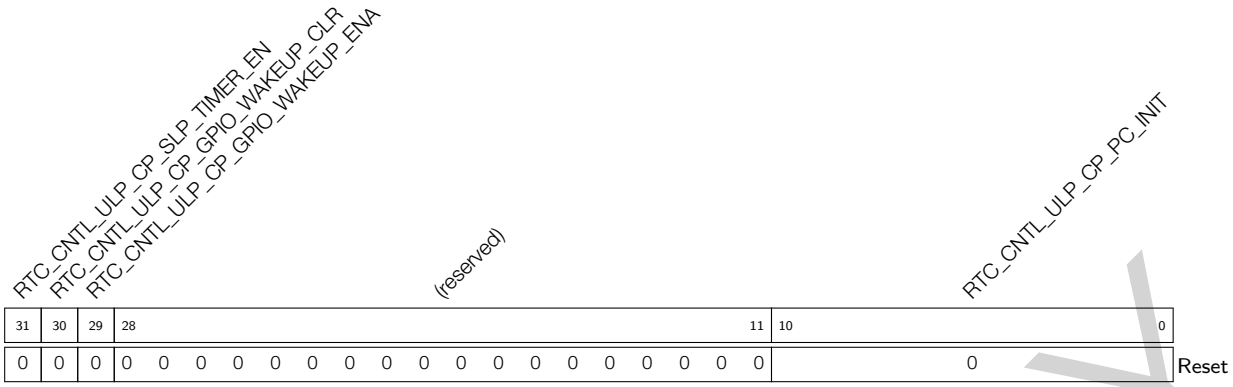
1.10 Registers

1.10.1 ULP (ALWAYS_ON) Registers

The addresses in this section are relative to low-power management base address provided in Table 3-3 in Chapter 3 *System and Memory*.

PRELIMINARY

Register 1.1. RTC_CNTL_ULP_CP_TIMER_REG (0x00FC)



RTC_CNTL_ULP_CP_PC_INIT ULP coprocessor PC initial address. (R/W)

RTC_CNTL_ULP_CP_GPIO_WAKEUP_ENA Enable the option of ULP timer woken up by RTC GPIO. (R/W)

RTC_CNTL_ULP_CP_GPIO_WAKEUP_CLR Disable the option of ULP timer woken up by RTC GPIO. (WO)

RTC_CNTL_ULP_CP_SLP_TIMER_EN ULP coprocessor timer enable bit. 0: Disable hardware timer; 1: Enable hardware timer. (R/W)

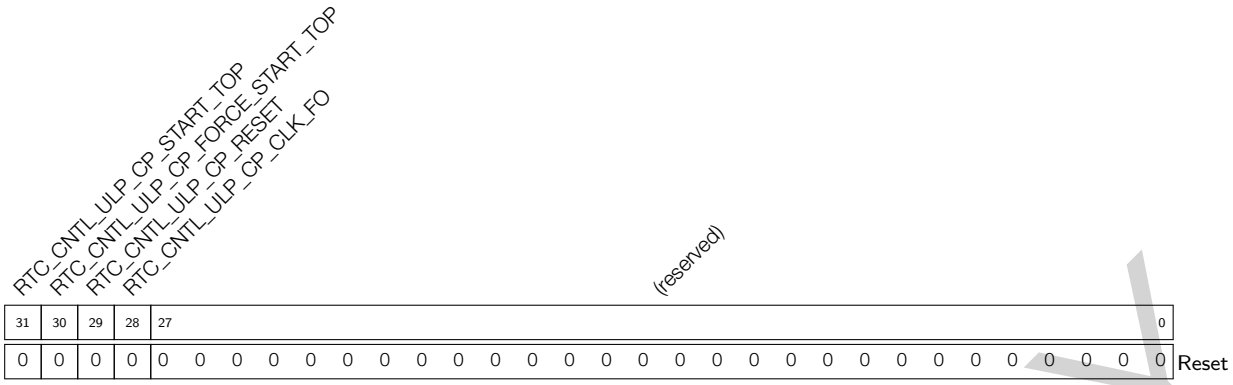
Register 1.2. RTC_CNTL_ULP_CP_TIMER_1_REG (0x0134)



RTC_CNTL_ULP_CP_TIMER_SLP_CYCLE Set sleep cycles for ULP coprocessor timer. (R/W)

PRELIMINARY

Register 1.3. RTC_CNTL_ULP_CP_CTRL_REG (0x0100)



RTC_CNTL_ULP_CP_CLK_FO ULP-FSM clock force on. (R/W)

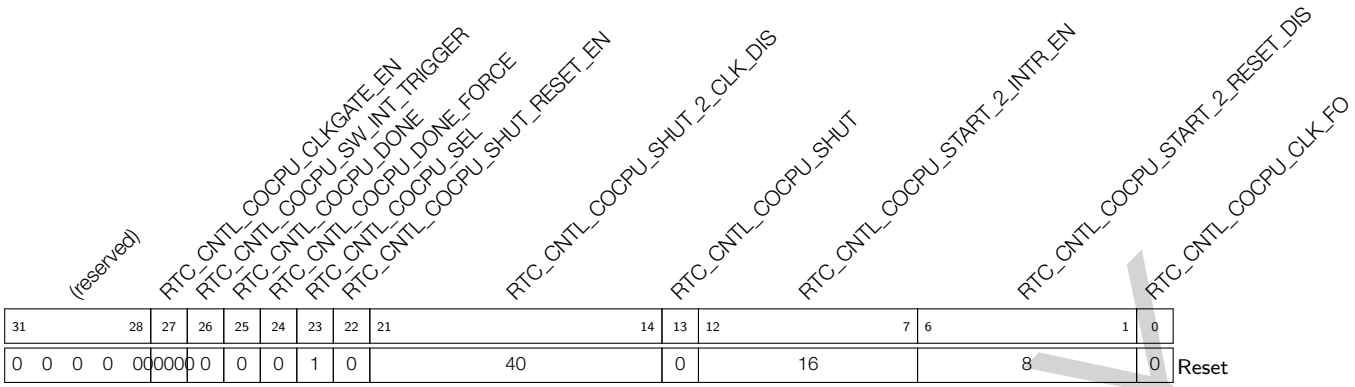
RTC_CNTL_ULP_CP_RESET ULP-FSM clock software reset. (R/W)

RTC_CNTL_ULP_CP_FORCE_START_TOP Write 1 to start ULP-FSM by software. (R/W)

RTC_CNTL_ULP_CP_START_TOP Write 1 to start ULP-FSM. (R/W)

PRELIMINARY

Register 1.4. RTC_CNTL_COCPU_CTRL_REG (0x0104)



RTC_CNTL_COCPU_CLK_FO ULP-RISC-V clock force on. (R/W)

RTC_CNTL_COCPU_START_2_RESET_DIS Time from ULP-RISC-V startup to pull down reset. (R/W)

RTC_CNTL_COCPU_START_2_INTR_EN Time from ULP-RISC-V startup to send out RISCV_START_INT interrupt. (R/W)

RTC_CNTL_COCPU_SHUT Shut down ULP-RISC-V. (R/W)

RTC_CNTL_COCPU_SHUT_2_CLK_DIS Time from shut down ULP-RISC-V to disable clock. (R/W)

RTC_CNTL_COCPU_SHUT_RESET_EN This bit is used to reset ULP-RISC-V. (R/W)

RTC_CNTL_COCPU_SEL 0: select ULP-RISC-V; 1: select ULP-FSM. (R/W)

RTC_CNTL_COCPU_DONE_FORCE 0: select ULP-FSM DONE signal; 1: select ULP-RISC-V DONE signal. (R/W)

RTC_CNTL_COCPU_DONE DONE signal. Write 1 to this bit, ULP-RISC-V will go to HALT and the timer starts counting. (R/W)

RTC_CNTL_COCPU_SW_INT_TRIGGER Trigger ULP-RISC-V register interrupt. (WO)

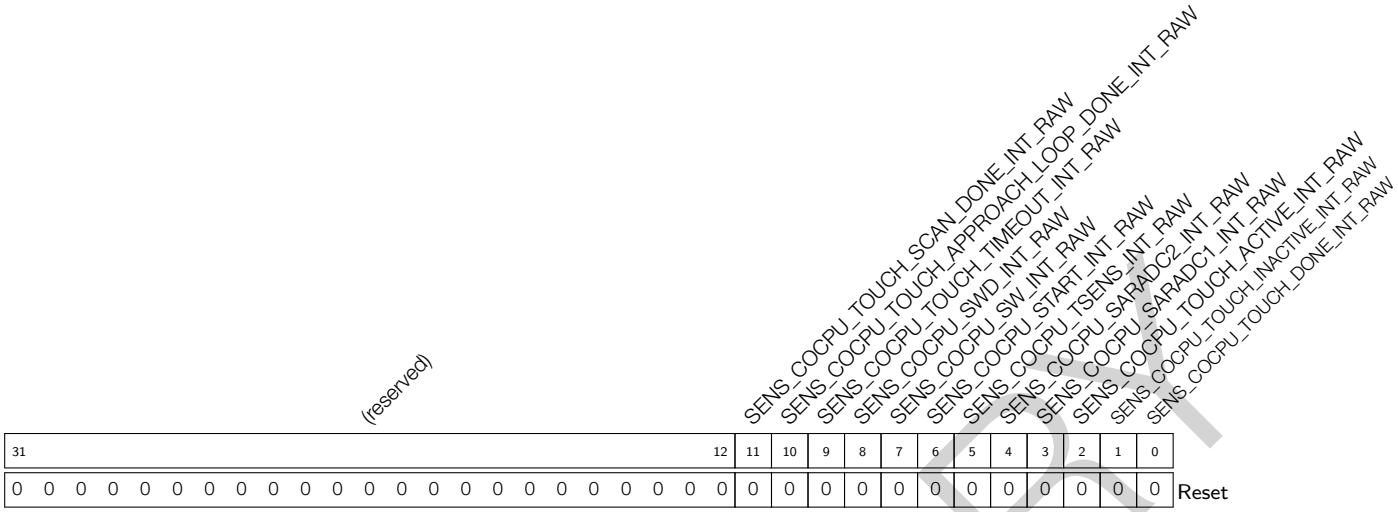
RTC_CNTL_COCPU_CLKGATE_EN Enable ULP-RICS-V clock gate. (WO)

1.10.2 ULP (RTC_PERI) Registers

The addresses in this section are relative to low-power management base address provided in Table 3-3 in Chapter 3 *System and Memory*.

PRELIMINARY

Register 1.5. SENS_ SAR_COCPU_INT_RAW_REG (0x00E8)



SENS_COCPU_TOUCH_DONE_INT_RAW TOUCH_DONE_INT interrupt raw bit. (RO)

SENS_COCPU_TOUCH_INACTIVE_INT_RAW TOUCH_INACTIVE_INT interrupt raw bit. (RO)

SENS_COCPU_TOUCH_ACTIVE_INT_RAW TOUCH_ACTIVE_INT interrupt raw bit. (RO)

SENS_COCPU_SARADC1_INT_RAW SARADC1_DONE_INT interrupt raw bit. (RO)

SENS_COCPU_SARADC2_INT_RAW SARADC2_DONE_INT interrupt raw bit. (RO)

SENS_COCPU_TSENS_INT_RAW TSENS_DONE_INT interrupt raw bit. (RO)

SENS_COCPU_START_INT_RAW RISCV_START_INT interrupt raw bit. (RO)

SENS_COCPU_SW_INT_RAW SW_INT interrupt raw bit. (RO)

SENS_COCPU_SWD_INT_RAW SWD_INT interrupt raw bit. (RO)

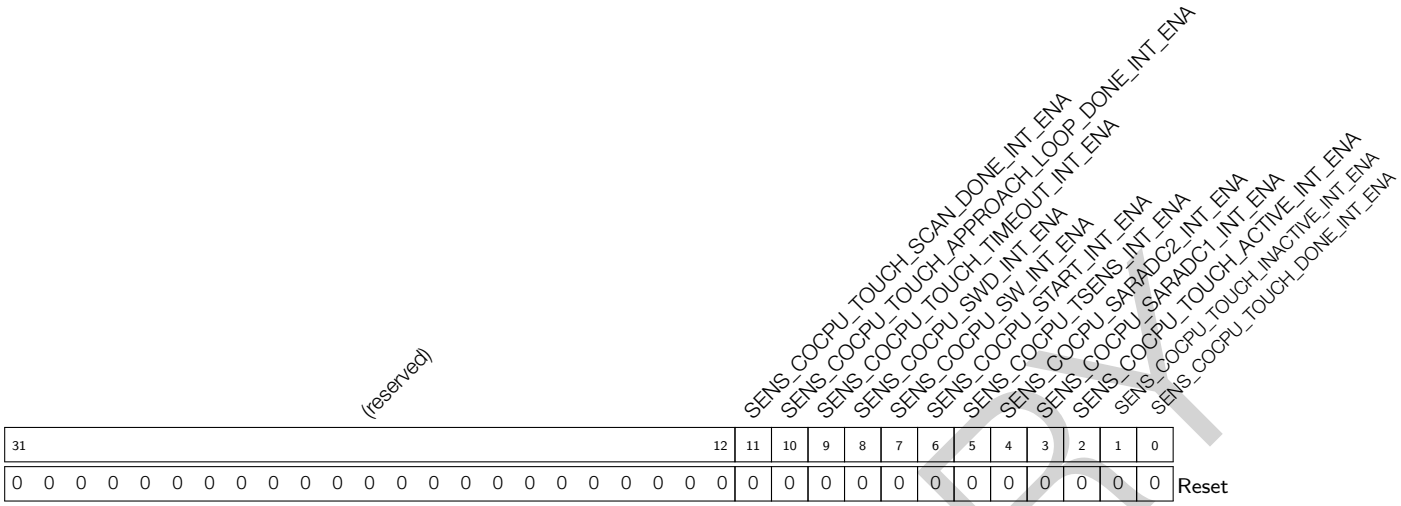
SENS_COCPU_TOUCH_TIMEOUT_INT_RAW TOUCH_TIME_OUT interrupt raw bit. (RO)

SENS_COCPU_TOUCH_APPROACH_LOOP_DONE_INT_RAW TOUCH_APPROACH_LOOP_DONE_INT interrupt raw bit. (RO)

SENS_COCPU_TOUCH_SCAN_DONE_INT_RAW TOUCH_SCAN_DONE_INT interrupt raw bit. (RO)

PRELIMINARY

Register 1.6. SENS_SAR_COCPU_INT_ENA_REG (0x00EC)



SENS_COCPU_TOUCH_DONE_INT_ENA TOUCH_DONE_INT interrupt enable bit. (R/W)

SENS_COCPU_TOUCH_INACTIVE_INT_ENA TOUCH_INACTIVE_INT interrupt enable bit. (R/W)

SENS_COCPU_TOUCH_ACTIVE_INT_ENA TOUCH_ACTIVE_INT interrupt enable bit. (R/W)

SENS_COCPU_SARADC1_INT_ENA SARADC1_DONE_INT interrupt enable bit. (R/W)

SENS_COCPU_SARADC2_INT_ENA SARADC2_DONE_INT interrupt enable bit. (R/W)

SENS_COCPU_TSENS_INT_ENA TSENS_DONE_INT interrupt enable bit. (R/W)

SENS_COCPU_START_INT_ENA RISCV_START_INT interrupt enable bit. (R/W)

SENS_COCPU_SW_INT_ENA SW_INT interrupt enable bit. (R/W)

SENS_COCPU_SWD_INT_ENA SWD_INT interrupt enable bit. (R/W)

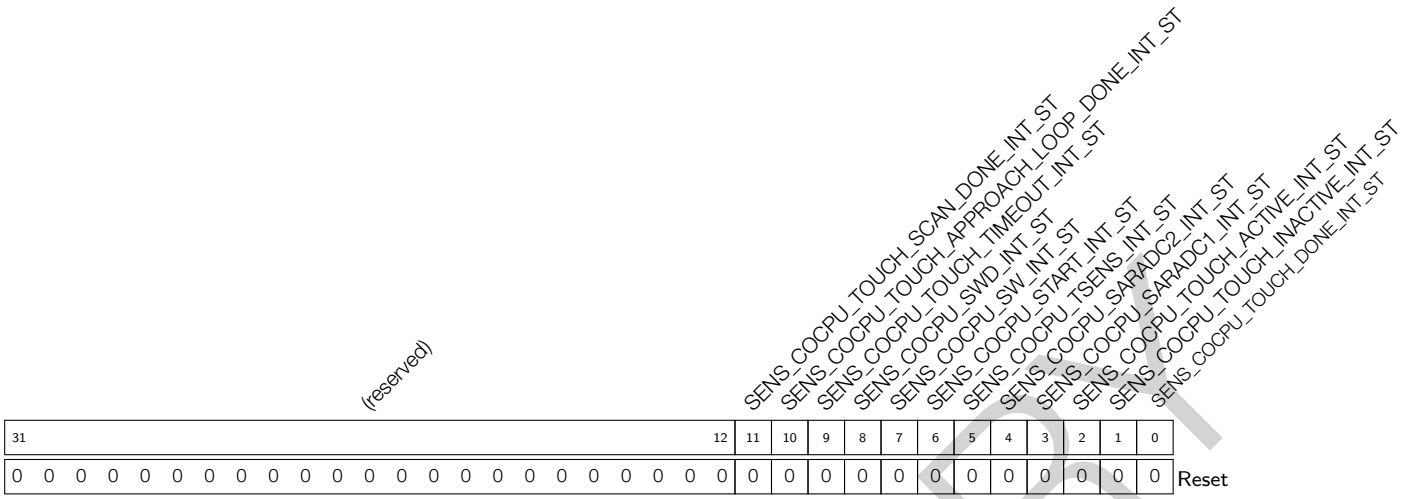
SENS_COCPU_TOUCH_TIMEOUT_INT_ENA TOUCH_TIME_OUT interrupt enable bit. (R/W)

SENS_COCPU_TOUCH_APPROACH_LOOP_DONE_INT_ENA TOUCH_APPROACH_LOOP_DONE_INT interrupt enable bit. (R/W)

SENS_COCPU_TOUCH_SCAN_DONE_INT_ENA TOUCH_SCAN_DONE_INT interrupt enable bit. (R/W)

PRELIMINARY

Register 1.7. SENS_SAR_COCPU_INT_ST_REG (0x00F0)



SENS_COCPU_TOUCH_DONE_INT_ST TOUCH_DONE_INT interrupt status bit. (RO)

SENS_COCPU_TOUCH_INACTIVE_INT_ST TOUCH_INACTIVE_INT interrupt status bit. (RO)

SENS_COCPU_TOUCH_ACTIVE_INT_ST TOUCH_ACTIVE_INT interrupt status bit. (RO)

SENS_COCPU_SARADC1_INT_ST SARADC1_DONE_INT interrupt status bit. (RO)

SENS_COCPU_SARADC2_INT_ST SARADC2_DONE_INT interrupt status bit. (RO)

SENS_COCPU_TSENS_INT_ST TSENS_DONE_INT interrupt status bit. (RO)

SENS_COCPU_START_INT_ST RISCV_START_INT interrupt status bit. (RO)

SENS_COCPU_SW_INT_ST SW_INT interrupt status bit. (RO)

SENS_COCPU_SWD_INT_ST SWD_INT interrupt status bit. (RO)

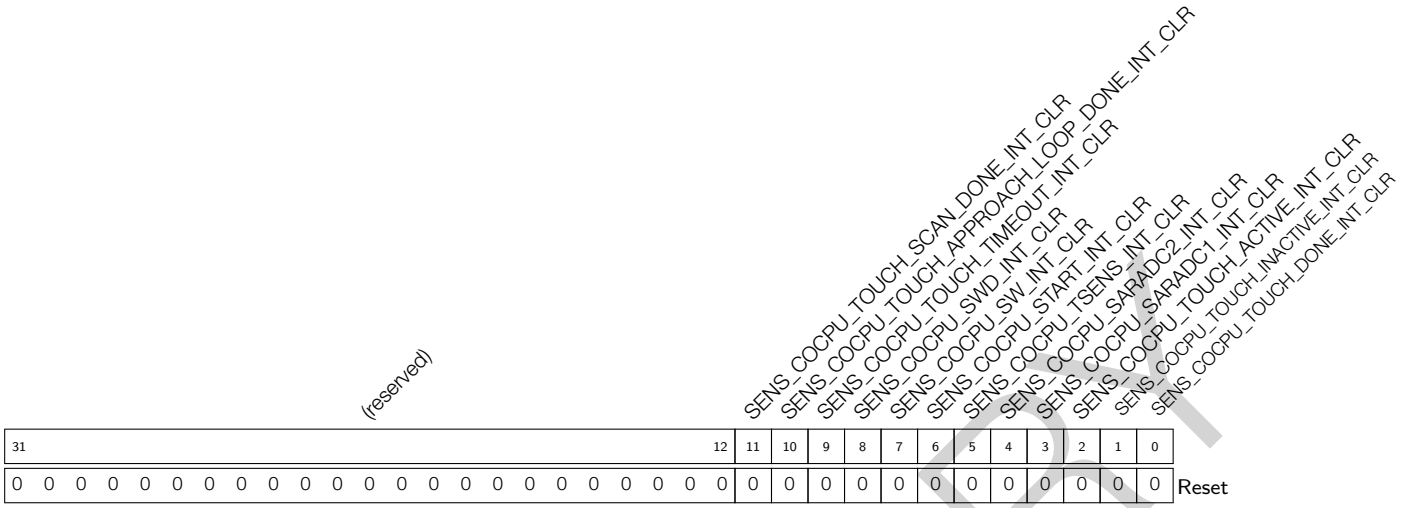
SENS_COCPU_TOUCH_TIMEOUT_INT_ST TOUCH_TIME_OUT interrupt status bit. (RO)

SENS_COCPU_TOUCH_APPROACH_LOOP_DONE_INT_ST TOUCH_APPROACH_LOOP_DONE_INT interrupt status bit. (RO)

SENS_COCPU_TOUCH_SCAN_DONE_INT_ST TOUCH_SCAN_DONE_INT interrupt status bit. (RO)

PRELIMINARY

Register 1.8. SENS_SAR_COCPU_INT_CLR_REG (0x00F4)



SENS_COCPU_TOUCH_DONE_INT_CLR TOUCH_DONE_INT interrupt clear bit. (WO)

SENS_COCPU_TOUCH_INACTIVE_INT_CLR TOUCH_INACTIVE_INT interrupt clear bit. (WO)

SENS_COCPU_TOUCH_ACTIVE_INT_CLR TOUCH_ACTIVE_INT interrupt clear bit. (WO)

SENS_COCPU_SARADC1_INT_CLR SARADC1_DONE_INT interrupt clear bit. (WO)

SENS_COCPU_SARADC2_INT_CLR SARADC2_DONE_INT interrupt clear bit. (WO)

SENS_COCPU_TSENS_INT_CLR TSENS_DONE_INT interrupt clear bit. (WO)

SENS_COCPU_START_INT_CLR RISCV_START_INT interrupt clear bit. (WO)

SENS_COCPU_SW_INT_CLR SW_INT interrupt clear bit. (WO)

SENS_COCPU_SWD_INT_CLR SWD_INT interrupt clear bit. (WO)

SENS_COCPU_TOUCH_TIMEOUT_INT_CLR TOUCH_TIME_OUT interrupt clear bit. (WO)

SENS_COCPU_TOUCH_APPROACH_LOOP_DONE_INT_CLR TOUCH_APPROACH_LOOP_DONE_INT interrupt clear bit. (WO)

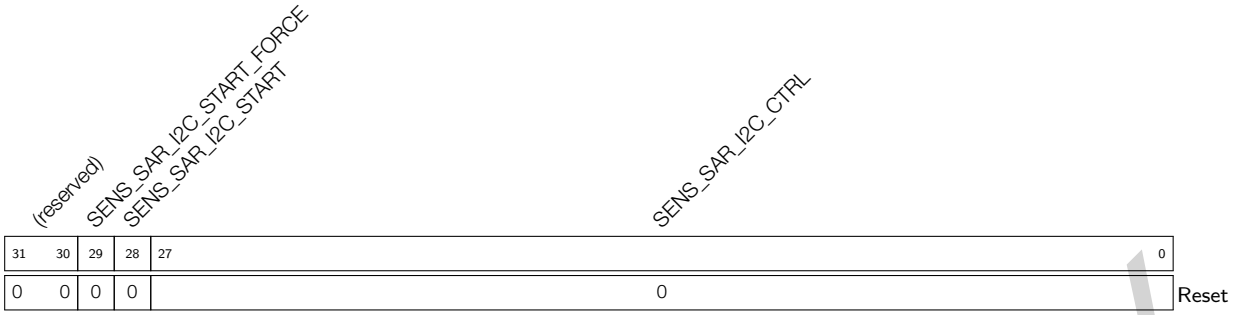
SENS_COCPU_TOUCH_SCAN_DONE_INT_CLR TOUCH_SCAN_DONE_INT interrupt clear bit. (WO)

1.10.3 RTC I2C (RTC_PERI) Registers

The addresses in this section are relative to low-power management base address + 0x0800 provided in Table 3-3 in Chapter 3 *System and Memory*.

PRELIMINARY

Register 1.9. SENS_SAR_I2C_CTRL_REG (0x0058)



SENS_SAR_I2C_CTRL RTC I2C control data; active only when SENS_SAR_I2C_START_FORCE = 1. (R/W)

SENS_SAR_I2C_START Start RTC I2C; active only when SENS_SAR_I2C_START_FORCE = 1. (R/W)

SENS_SAR_I2C_START_FORCE 0: RTC I2C started by FSM; 1: RTC I2C started by software. (R/W)

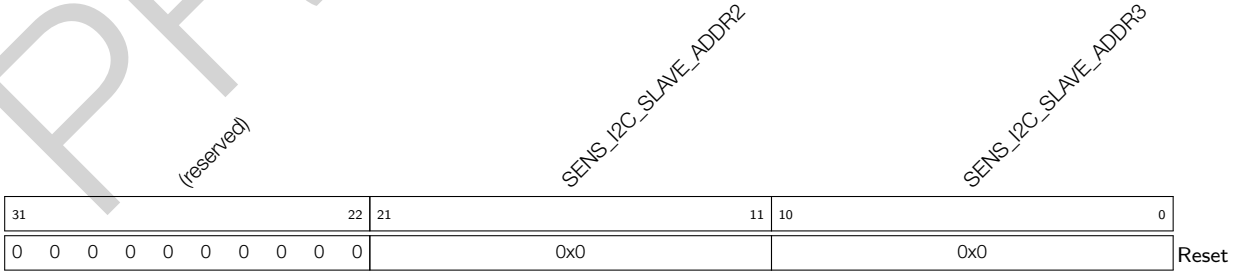
Register 1.10. SENS_SAR_SLAVE_ADDR1_REG (0x0040)



SENS_I2C_SLAVE_ADDR1 RTC I2C slave address 1. (R/W)

SENS_I2C_SLAVE_ADDR0 RTC I2C slave address 0. (R/W)

Register 1.11. SENS_SAR_SLAVE_ADDR2_REG (0x0044)

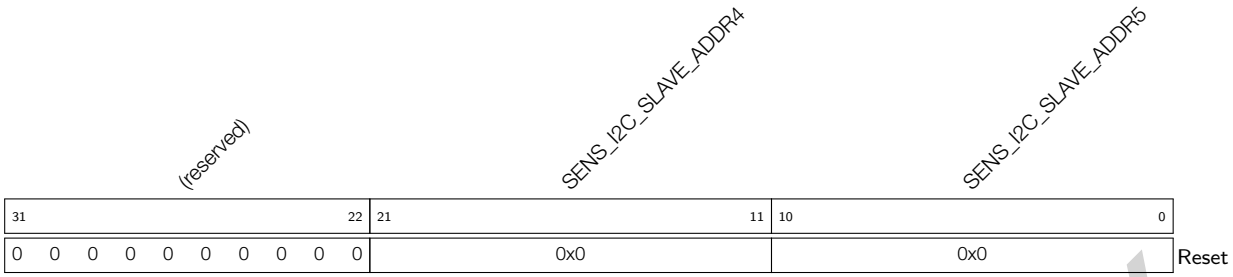


SENS_I2C_SLAVE_ADDR3 RTC I2C slave address 3. (R/W)

SENS_I2C_SLAVE_ADDR2 RTC I2C slave address 2. (R/W)

PRELIMINARY

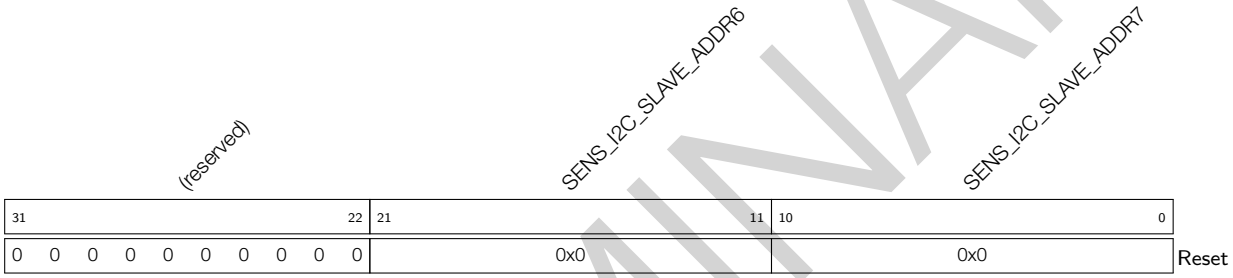
Register 1.12. SENS_SAR_SLAVE_ADDR3_REG (0x0048)



SENS_I2C_SLAVE_ADDR5 RTC I2C slave address 5. (R/W)

SENS_I2C_SLAVE_ADDR4 RTC I2C slave address 4. (R/W)

Register 1.13. SENS_SAR_SLAVE_ADDR4_REG (0x004C)



SENS_I2C_SLAVE_ADDR7 RTC I2C slave address 7. (R/W)

SENS_I2C_SLAVE_ADDR6 RTC I2C slave address 6. (R/W)

1.10.4 RTC I2C (I2C) Registers

The addresses in this section are relative to low-power management base address + 0x0C00 provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 1.14. RTC_I2C_SCL_LOW_REG (0x0000)



RTC_I2C_SCL_LOW_PERIOD This register is used to configure how many clock cycles SCL remains low. (R/W)

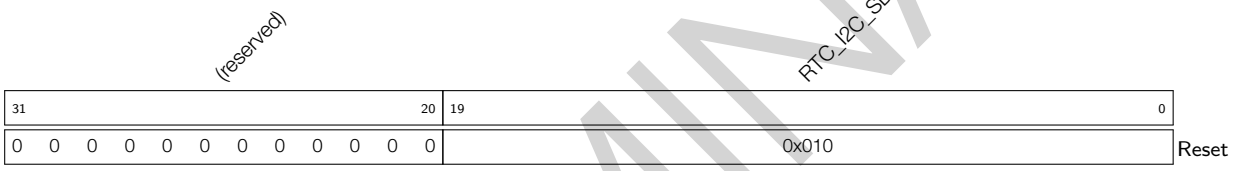
PRELIMINARY

Register 1.15. RTC_I2C_SCL_HIGH_REG (0x0014)



RTC_I2C_SCL_HIGH_PERIOD This register is used to configure how many cycles SCL remains high. (R/W)

Register 1.16. RTC_I2C_SDA_DUTY_REG (0x0018)



RTC_I2C_SDA_DUTY_NUM The number of clock cycles between the SDA switch and the falling edge of SCL. (R/W)

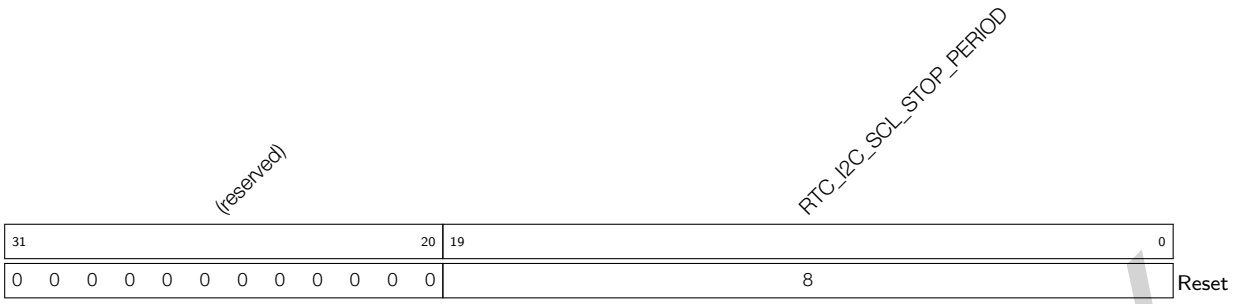
Register 1.17. RTC_I2C_SCL_START_PERIOD_REG (0x001C)



RTC_I2C_SCL_START_PERIOD Number of clock cycles to wait after generating a start condition. (R/W)

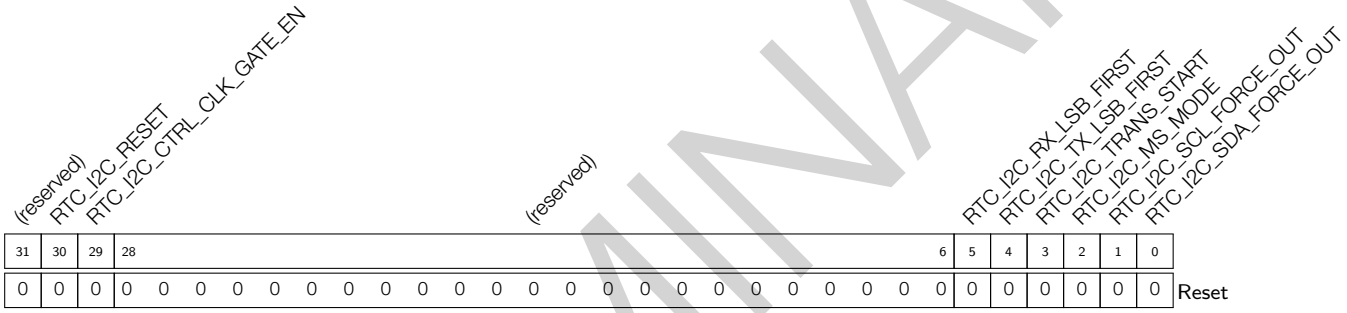
PRELIMINARY

Register 1.18. RTC_I2C_SCL_STOP_PERIOD_REG (0x0020)



RTC_I2C_SCL_STOP_PERIOD Number of clock cycles to wait before generating a stop condition. (R/W)

Register 1.19. RTC_I2C_CTRL_REG (0x0004)



RTC_I2C_SDA_FORCE_OUT SDA output mode. 0: open drain; 1: push pull. (R/W)

RTC_I2C_SCL_FORCE_OUT SCL output mode. 0: open drain; 1: push pull. (R/W)

RTC_I2C_MS_MODE Set this bit to configure RTC I2C as a master. (R/W)

RTC_I2C_TRANS_START Set this bit to 1, RTC I2C starts sending data. (R/W)

RTC_I2C_TX_LSB_FIRST This bit is used to control the sending mode. 0: send data from the most significant bit; 1: send data from the least significant bit. (R/W)

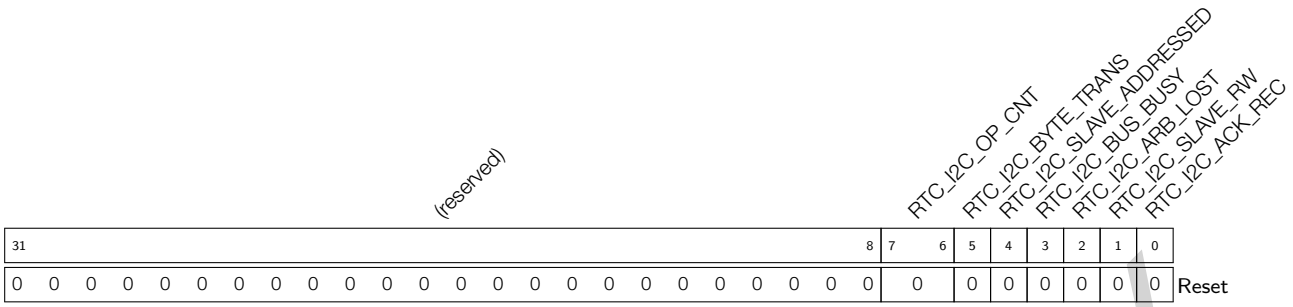
RTC_I2C_RX_LSB_FIRST This bit is used to control the storage mode for received data. 0: receive data from the most significant bit; 1: receive data from the least significant bit. (R/W)

RTC_I2C_CTRL_CLK_GATE_EN RTC I2C controller clock gate. (R/W)

RTC_I2C_RESET RTC I2C software reset. (R/W)

PRELIMINARY

Register 1.20. RTC_I2C_STATUS_REG (0x0008)



RTC_I2C_ACK_REC The received ACK value. 0: ACK; 1: NACK. (RO)

RTC_I2C_SLAVE_RW 0: master writes to slave; 1: master reads from slave. (RO)

RTC_I2C_ARB_LOST When the RTC I2C loses control of SCL line, the register changes to 1. (RO)

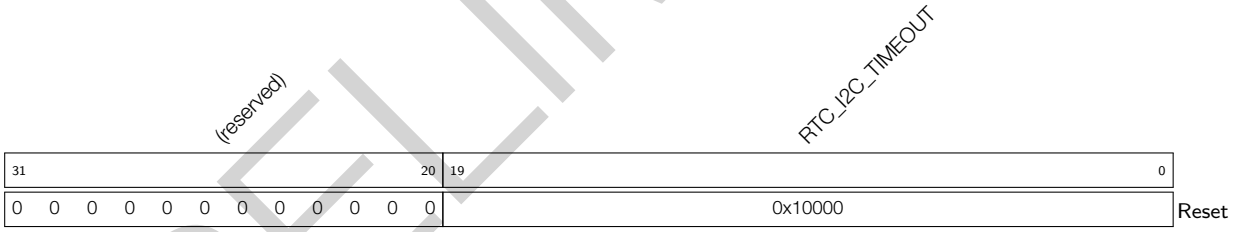
RTC_I2C_BUS_BUSY 0: RTC I2C bus is in idle state; 1: RTC I2C bus is busy transferring data. (RO)

RTC_I2C_SLAVE_ADDRESSED When the address sent by the master matches the address of the slave, then this bit will be set. (RO)

RTC_I2C_BYTE_TRANS This field changes to 1 when one byte is transferred. (RO)

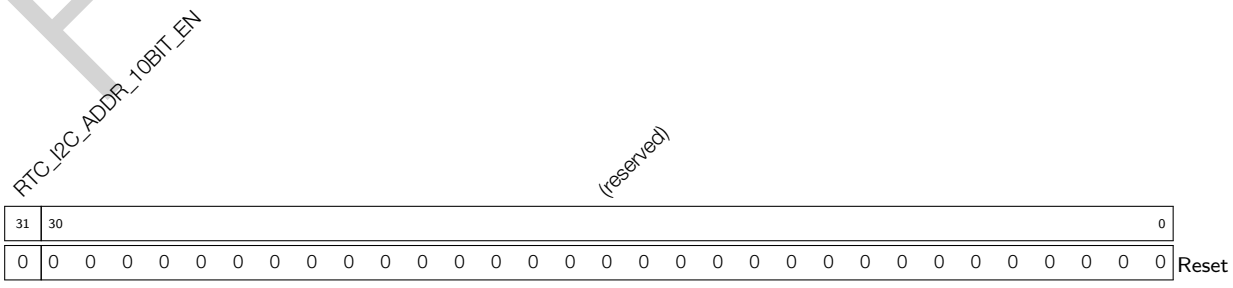
RTC_I2C_OP_CNT Indicate which operation is working. (RO)

Register 1.21. RTC_I2C_TIMEOUT_REG (0x000C)



RTC_I2C_TIMEOUT Timeout threshold. (R/W)

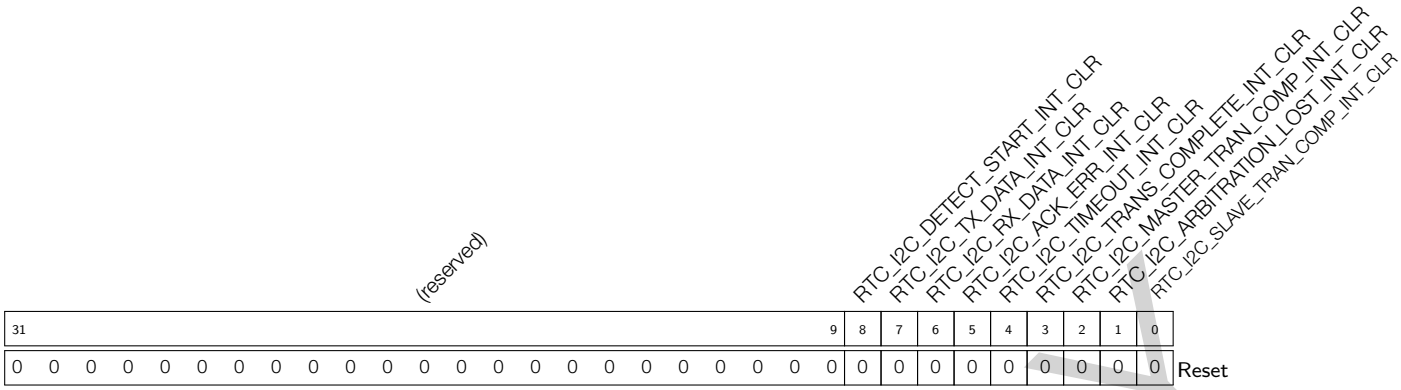
Register 1.22. RTC_I2C_SLAVE_ADDR_REG (0x0010)



RTC_I2C_ADDR_10BIT_EN This field is used to enable the slave 10-bit addressing mode. (R/W)

PRELIMINARY

Register 1.23. RTC_I2C_INT_CLR_REG (0x0024)



RTC_I2C_SLAVE_TRAN_COMP_INT_CLR RTC_I2C_SLAVE_TRAN_COMP_INT interrupt clear bit. (WO)

RTC_I2C_ARBITRATION_LOST_INT_CLR RTC_I2C_ARBITRATION_LOST_INT interrupt clear bit. (WO)

RTC_I2C_MASTER_TRAN_COMP_INT_CLR RTC_I2C_MASTER_TRAN_COMP_INT interrupt clear bit. (WO)

RTC_I2C_TRANS_COMPLETE_INT_CLR RTC_I2C_TRANS_COMPLETE_INT interrupt clear bit. (WO)

RTC_I2C_TIMEOUT_INT_CLR RTC_I2C_TIMEOUT_INT interrupt clear bit. (WO)

RTC_I2C_ACK_ERR_INT_CLR RTC_I2C_ACK_ERR_INT interrupt clear bit. (WO)

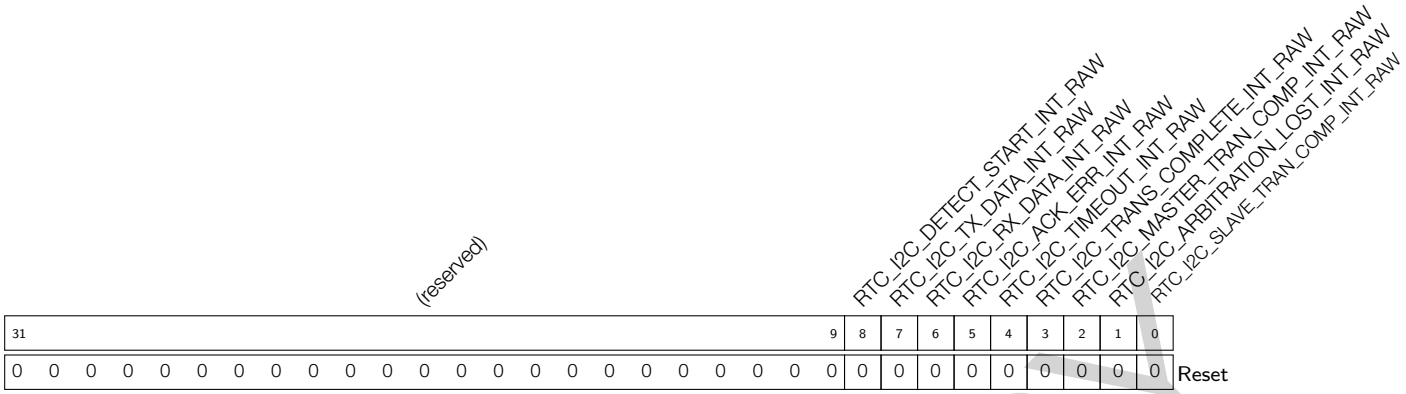
RTC_I2C_RX_DATA_INT_CLR RTC_I2C_RX_DATA_INT interrupt clear bit. (WO)

RTC_I2C_TX_DATA_INT_CLR RTC_I2C_TX_DATA_INT interrupt clear bit. (WO)

RTC_I2C_DETECT_START_INT_CLR RTC_I2C_DETECT_START_INT interrupt clear bit. (WO)

PRELIMINARY

Register 1.24. RTC_I2C_INT_RAW_REG (0x0028)



RTC_I2C_SLAVE_TRAN_COMP_INT_RAW RTC_I2C_SLAVE_TRAN_COMP_INT interrupt raw bit. (RO)

RTC_I2C_ARBITRATION_LOST_INT_RAW RTC_I2C_ARBITRATION_LOST_INT interrupt raw bit. (RO)

RTC_I2C_MASTER_TRAN_COMP_INT_RAW RTC_I2C_MASTER_TRAN_COMP_INT interrupt raw bit. (RO)

RTC_I2C_TRANS_COMPLETE_INT_RAW RTC_I2C_TRANS_COMPLETE_INT interrupt raw bit. (RO)

RTC_I2C_TIMEOUT_INT_RAW RTC_I2C_TIMEOUT_INT interrupt raw bit. (RO)

RTC_I2C_ACK_ERR_INT_RAW RTC_I2C_ACK_ERR_INT interrupt raw bit. (RO)

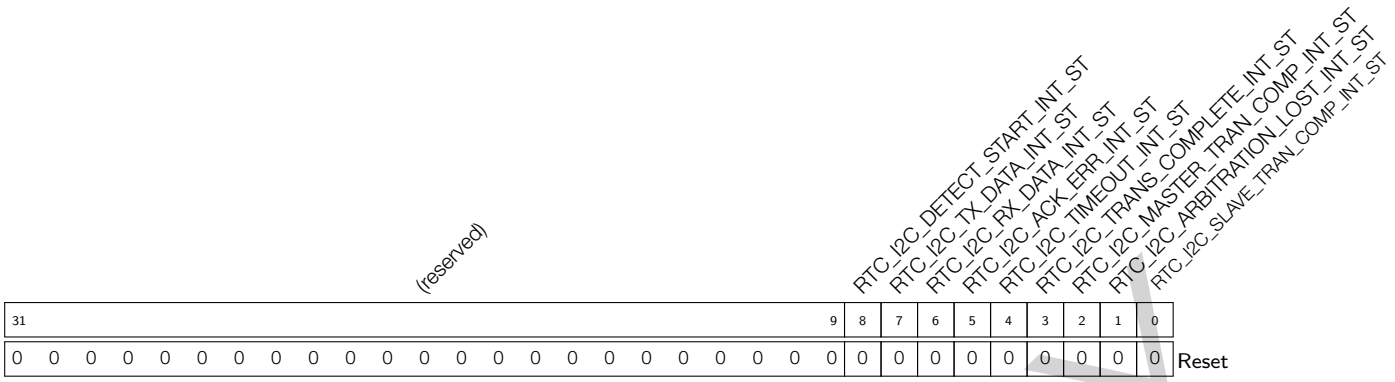
RTC_I2C_RX_DATA_INT_RAW RTC_I2C_RX_DATA_INT interrupt raw bit. (RO)

RTC_I2C_TX_DATA_INT_RAW RTC_I2C_TX_DATA_INT interrupt raw bit. (RO)

RTC_I2C_DETECT_START_INT_RAW RTC_I2C_DETECT_START_INT interrupt raw bit. (RO)

PRELIMINARY

Register 1.25. RTC_I2C_INT_ST_REG (0x002C)



RTC_I2C_SLAVE_TRAN_COMP_INT_ST RTC_I2C_SLAVE_TRAN_COMP_INT interrupt status bit. (RO)

RTC_I2C_ARBITRATION_LOST_INT_ST RTC_I2C_ARBITRATION_LOST_INT interrupt status bit. (RO)

RTC_I2C_MASTER_TRAN_COMP_INT_ST RTC_I2C_MASTER_TRAN_COMP_INT interrupt status bit. (RO)

RTC_I2C_TRANS_COMPLETE_INT_ST RTC_I2C_TRANS_COMPLETE_INT interrupt status bit. (RO)

RTC_I2C_TIMEOUT_INT_ST RTC_I2C_TIMEOUT_INT interrupt status bit. (RO)

RTC_I2C_ACK_ERR_INT_ST RTC_I2C_ACK_ERR_INT interrupt status bit. (RO)

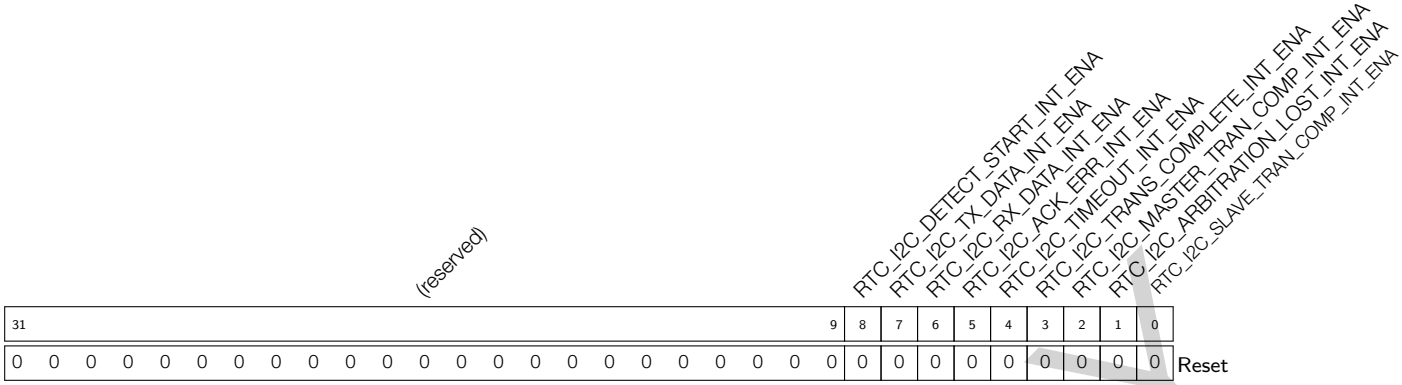
RTC_I2C_RX_DATA_INT_ST RTC_I2C_RX_DATA_INT interrupt status bit. (RO)

RTC_I2C_TX_DATA_INT_ST RTC_I2C_TX_DATA_INT interrupt status bit. (RO)

RTC_I2C_DETECT_START_INT_ST RTC_I2C_DETECT_START_INT interrupt status bit. (RO)

PRELIMINARY

Register 1.26. RTC_I2C_INT_ENA_REG (0x0030)



RTC_I2C_SLAVE_TRAN_COMP_INT_ENA RTC_I2C_SLAVE_TRAN_COMP_INT interrupt enable bit. (R/W)

RTC_I2C_ARBITRATION_LOST_INT_ENA RTC_I2C_ARBITRATION_LOST_INT interrupt enable bit. (R/W)

RTC_I2C_MASTER_TRAN_COMP_INT_ENA RTC_I2C_MASTER_TRAN_COMP_INT interrupt enable bit. (R/W)

RTC_I2C_TRANS_COMPLETE_INT_ENA RTC_I2C_TRANS_COMPLETE_INT interrupt enable bit. (R/W)

RTC_I2C_TIMEOUT_INT_ENA RTC_I2C_TIMEOUT_INT interrupt enable bit. (R/W)

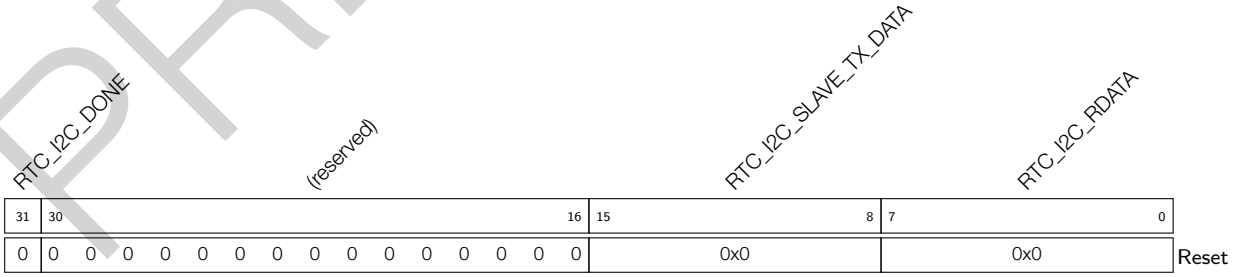
RTC_I2C_ACK_ERR_INT_ENA RTC_I2C_ACK_ERR_INT interrupt enable bit. (R/W)

RTC_I2C_RX_DATA_INT_ENA RTC_I2C_RX_DATA_INT interrupt enable bit. (R/W)

RTC_I2C_TX_DATA_INT_ENA RTC_I2C_TX_DATA_INT interrupt enable bit. (R/W)

RTC_I2C_DETECT_START_INT_ENA RTC_I2C_DETECT_START_INT interrupt enable bit. (R/W)

Register 1.27. RTC_I2C_DATA_REG (0x0034)



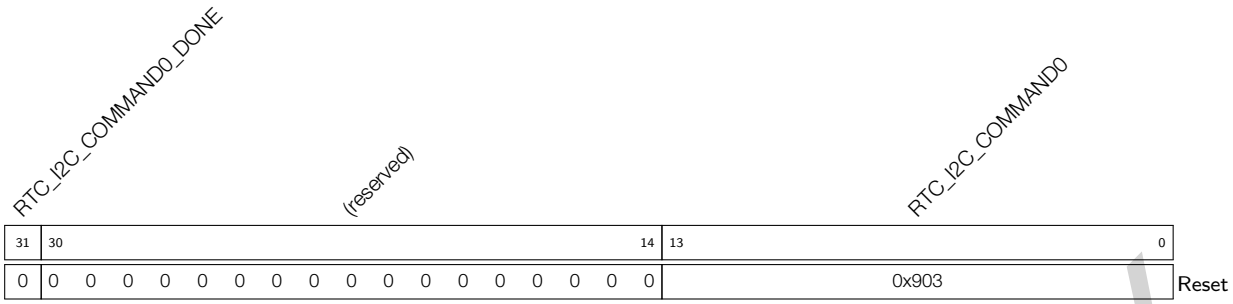
RTC_I2C_RDATA Data received. (RO)

RTC_I2C_SLAVE_TX_DATA The data sent by slave. (R/W)

RTC_I2C_DONE RTC I2C transmission is done. (RO)

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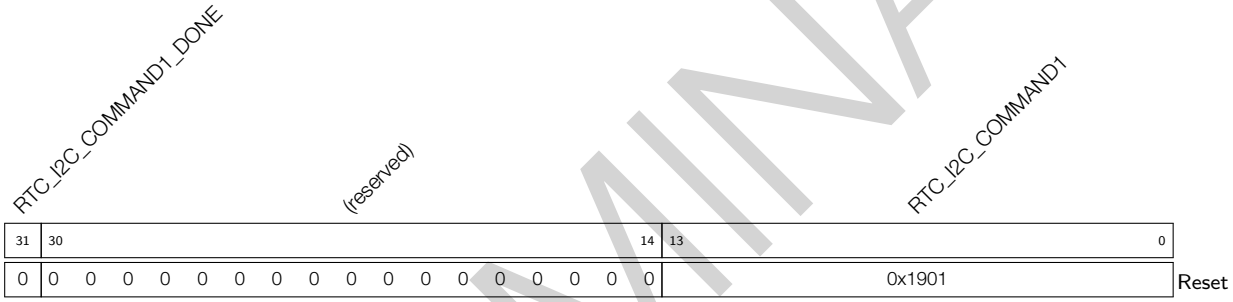
Register 1.28. RTC_I2C_CMD0_REG (0x0038)



RTC_I2C_COMMAND0 Content of command 0. For more information, please refer to the register I2C_COMD0_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND0_DONE When command 0 is done, this bit changes to 1. (RO)

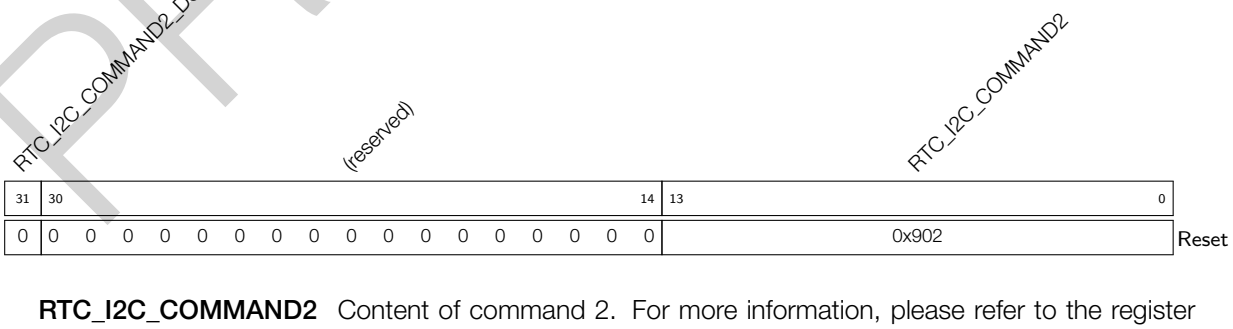
Register 1.29. RTC_I2C_CMD1_REG (0x003C)



RTC_I2C_COMMAND1 Content of command 1. For more information, please refer to the register I2C_COMD1_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND1_DONE When command 1 is done, this bit changes to 1. (RO)

Register 1.30. RTC_I2C_CMD2_REG (0x0040)

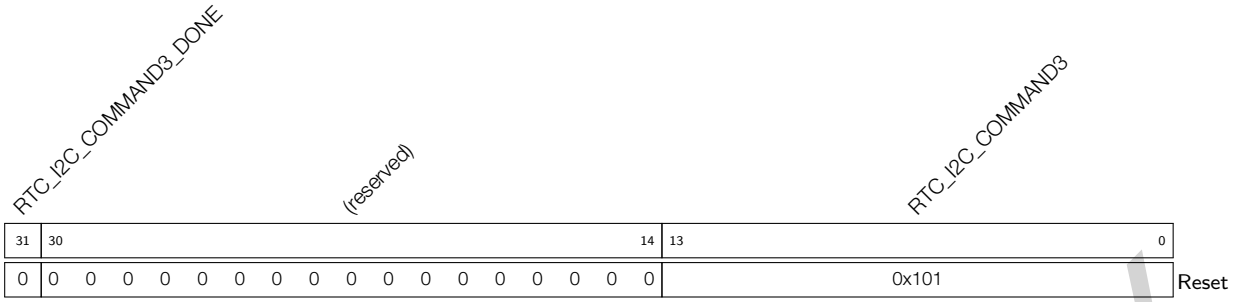


RTC_I2C_COMMAND2 Content of command 2. For more information, please refer to the register I2C_COMD2_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND2_DONE When command 2 is done, this bit changes to 1. (RO)

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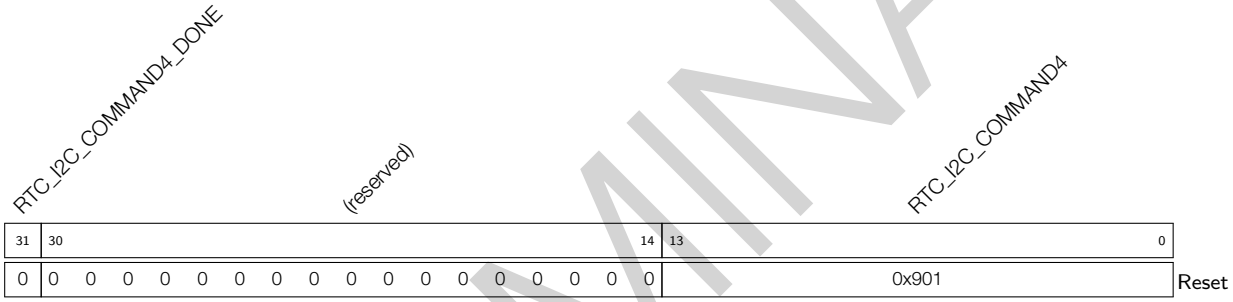
Register 1.31. RTC_I2C_CMD3_REG (0x0044)



RTC_I2C_COMMAND3 Content of command 3. For more information, please refer to the register I2C_COMD3_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND3_DONE When command 3 is done, this bit changes to 1. (RO)

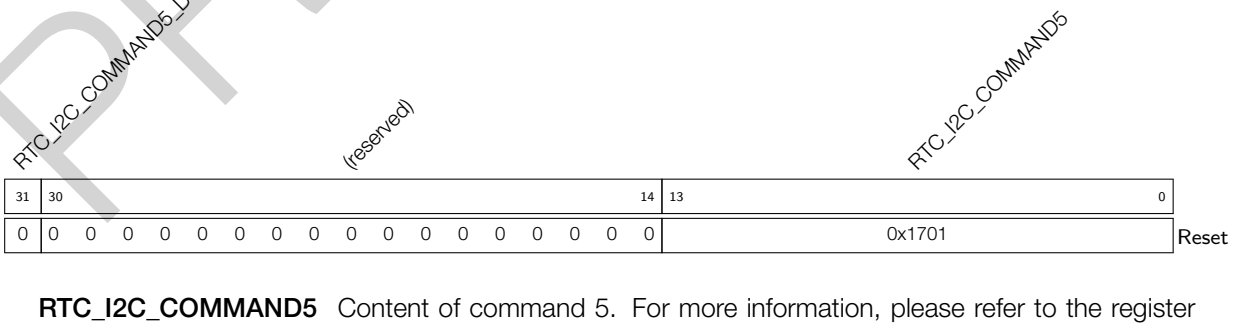
Register 1.32. RTC_I2C_CMD4_REG (0x0048)



RTC_I2C_COMMAND4 Content of command 4. For more information, please refer to the register I2C_COMD4_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND4_DONE When command 4 is done, this bit changes to 1. (RO)

Register 1.33. RTC_I2C_CMD5_REG (0x004C)

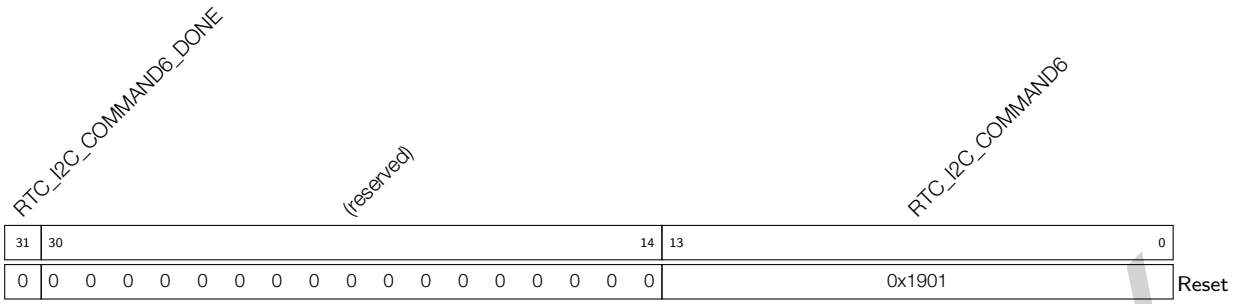


RTC_I2C_COMMAND5 Content of command 5. For more information, please refer to the register I2C_COMD5_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND5_DONE When command 5 is done, this bit changes to 1. (RO)

PRELIMINARY

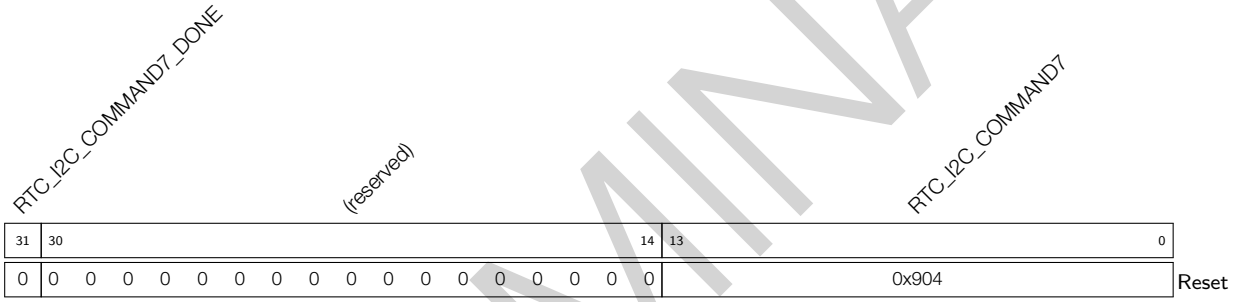
Register 1.34. RTC_I2C_CMD6_REG (0x0050)



RTC_I2C_COMMAND6 Content of command 6. For more information, please refer to the register I2C_COMD6_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND6_DONE When command 6 is done, this bit changes to 1. (RO)

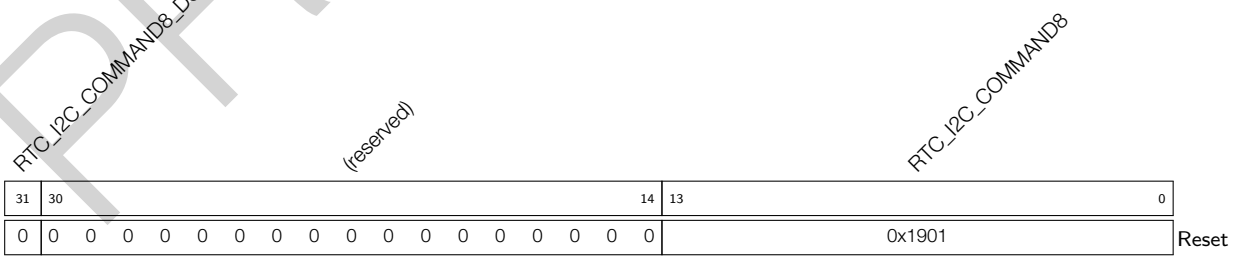
Register 1.35. RTC_I2C_CMD7_REG (0x0054)



RTC_I2C_COMMAND7 Content of command 7. For more information, please refer to the register I2C_COMD7_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND7_DONE When command 7 is done, this bit changes to 1. (RO)

Register 1.36. RTC_I2C_CMD8_REG (0x0058)

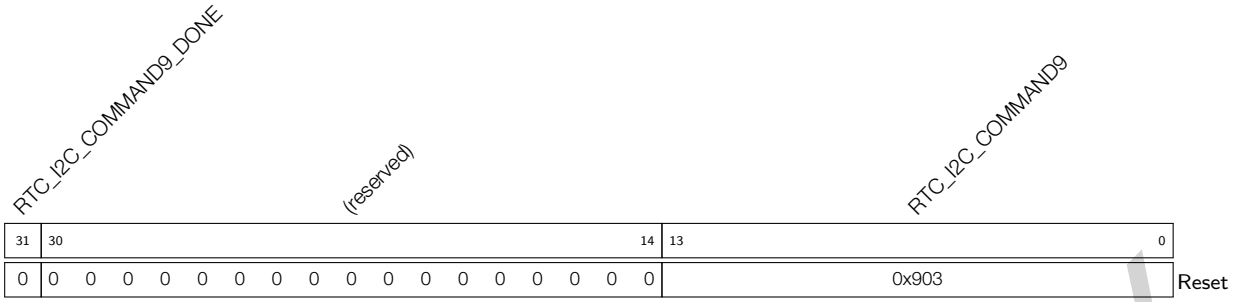


RTC_I2C_COMMAND8 Content of command 8. For more information, please refer to the register I2C_COMD8_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND8_DONE When command 8 is done, this bit changes to 1. (RO)

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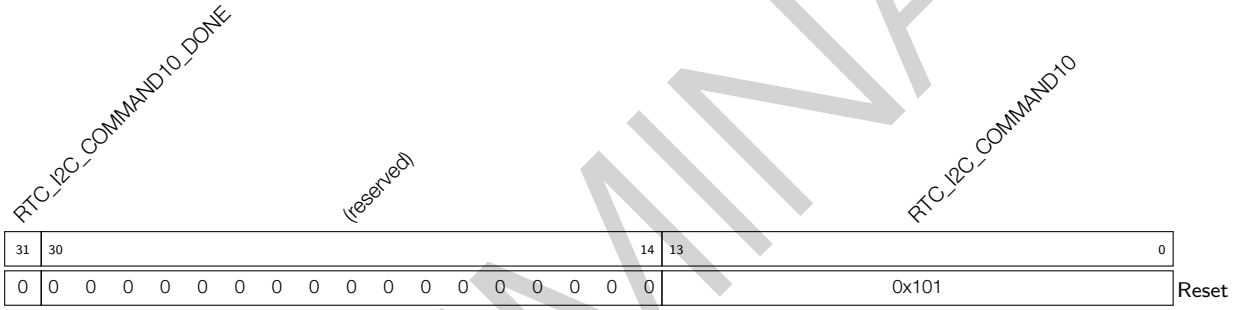
Register 1.37. RTC_I2C_CMD9_REG (0x005C)



RTC_I2C_COMMAND9 Content of command 9. For more information, please refer to the register I2C_COMD9_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND9_DONE When command 9 is done, this bit changes to 1. (RO)

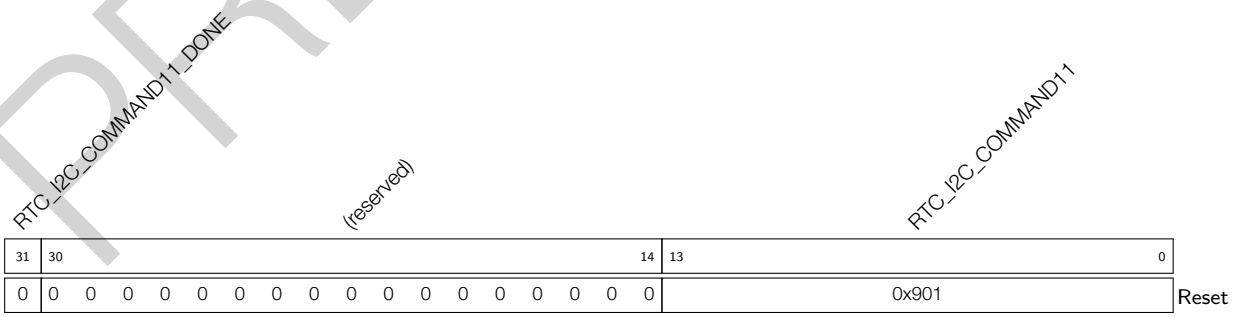
Register 1.38. RTC_I2C_CMD10_REG (0x0060)



RTC_I2C_COMMAND10 Content of command 10. For more information, please refer to the register I2C_COMD10_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND10_DONE When command 10 is done, this bit changes to 1. (RO)

Register 1.39. RTC_I2C_CMD11_REG (0x0064)

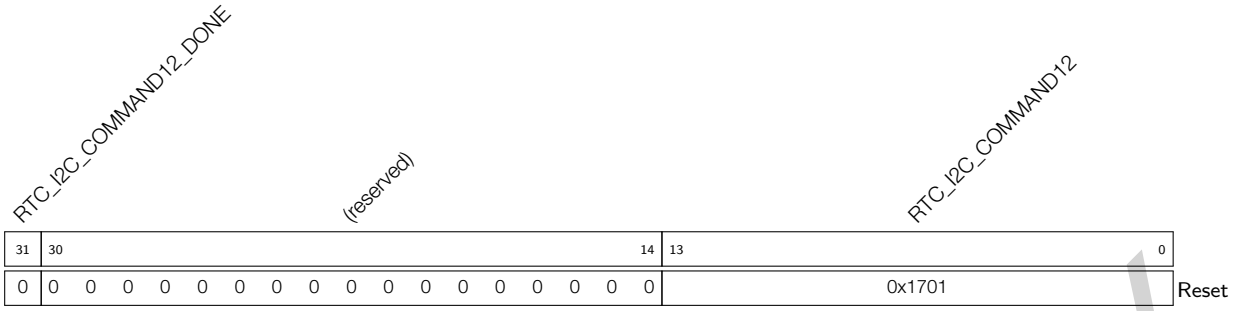


RTC_I2C_COMMAND11 Content of command 11. For more information, please refer to the register I2C_COMD11_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND11_DONE When command 11 is done, this bit changes to 1. (RO)

PRELIMINARY

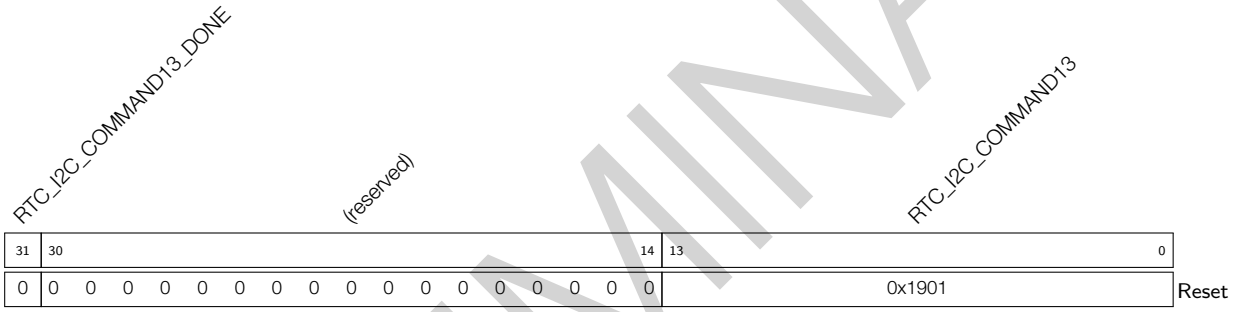
Register 1.40. RTC_I2C_CMD12_REG (0x0068)



RTC_I2C_COMMAND12 Content of command 12. For more information, please refer to the register I2C_COMD12_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND12_DONE When command 12 is done, this bit changes to 1. (RO)

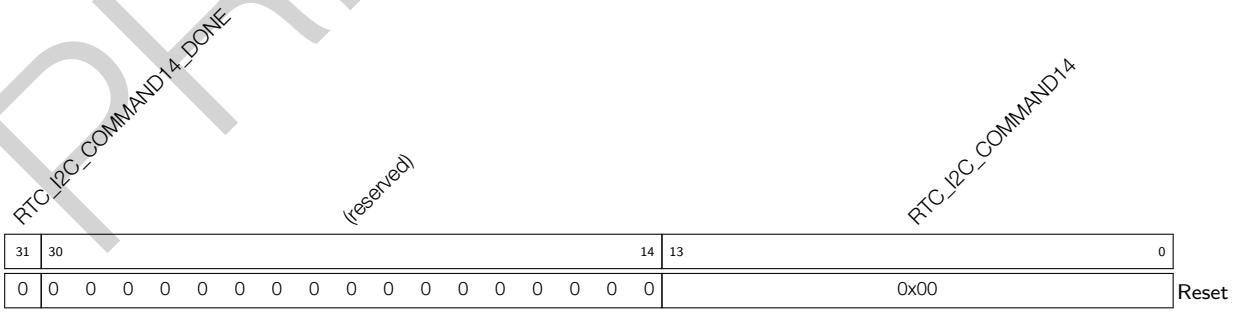
Register 1.41. RTC_I2C_CMD13_REG (0x006C)



RTC_I2C_COMMAND13 Content of command 13. For more information, please refer to the register I2C_COMD13_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND13_DONE When command 13 is done, this bit changes to 1. (RO)

Register 1.42. RTC_I2C_CMD14_REG (0x0070)

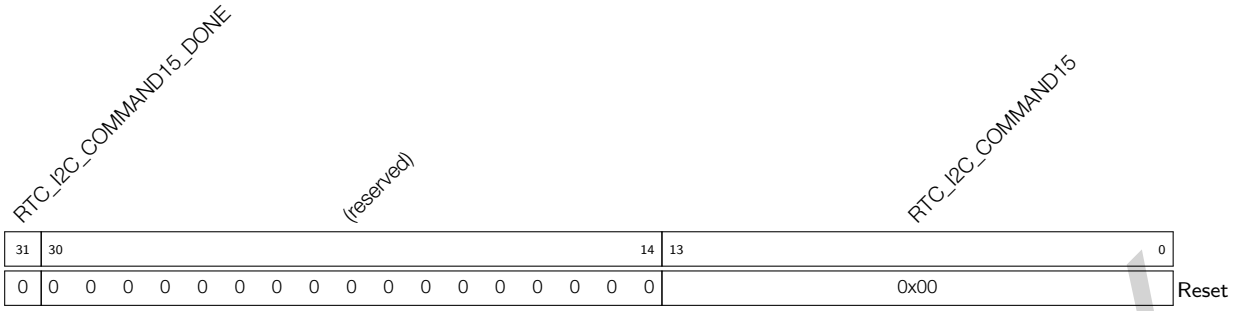


RTC_I2C_COMMAND14 Content of command 14. For more information, please refer to the register I2C_COMD14_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND14_DONE When command 14 is done, this bit changes to 1. (RO)

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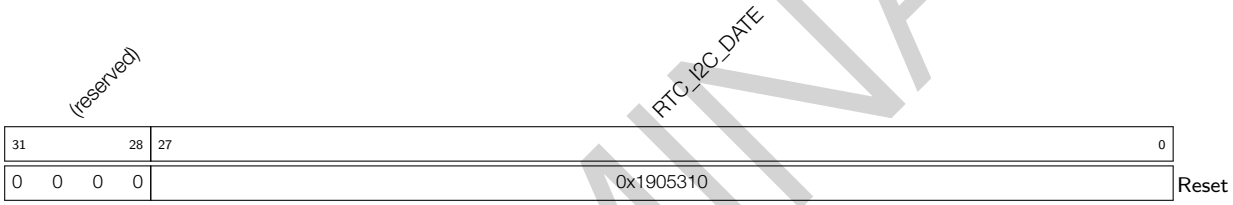
Register 1.43. RTC_I2C_CMD15_REG (0x0074)



RTC_I2C_COMMAND15 Content of command 15. For more information, please refer to the register I2C_COMD15_REG in Chapter I2C Controller. (R/W)

RTC_I2C_COMMAND15_DONE When command 15 is done, this bit changes to 1. (RO)

Register 1.44. RTC_I2C_DATE_REG (0x00FC)



RTC_I2C_DATE Version control register (R/W)

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2 GDMA Controller (GDMA)

2.1 Overview

General Direct Memory Access (GDMA) is a feature that allows peripheral-to-memory, memory-to-peripheral, and memory-to-memory data transfer at a high speed. The CPU is not involved in the GDMA transfer, and therefore it becomes more efficient with less workload.

The GDMA controller in ESP32-S3 has ten independent channels, i.e. five transmit channels and five receive channels. These ten channels are shared by peripherals with GDMA feature, namely SPI2, SPI3, UHCI0, I2S0, I2S1, LCD/CAM, AES, SHA, ADC, and RMT. You can assign the ten channels to any of these peripherals. Every channel supports access to internal RAM or external RAM.

The GDMA controller uses fixed-priority and round-robin channel arbitration schemes to manage peripherals' needs for bandwidth.

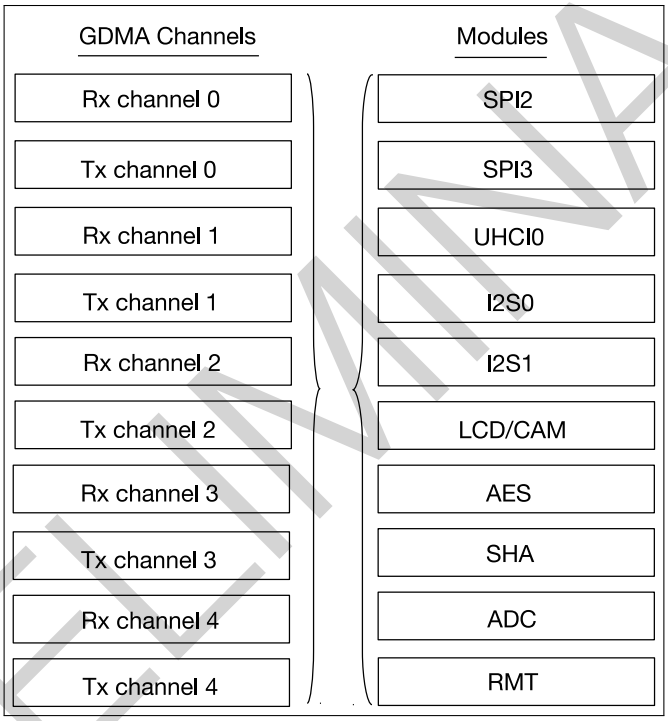


Figure 2-1. Modules with GDMA Feature and GDMA Channels

2.2 Features

The GDMA controller has the following features:

- AHB bus architecture
- Programmable length of data to be transferred in bytes
- Linked list of descriptors
- INCR burst transfer when accessing internal RAM
- Access to an address space of 480 KB at most in internal RAM
- Access to an address spacee of 32 MB at most in external RAM

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- Five transmit channels and five receive channels
- Access to internal and external RAM supported by every channel
- Software-configurable selection of peripheral requesting its service supported by every channel
- Fixed channel priority and round-robin channel arbitration

2.3 Architecture

In ESP32-S3, all modules that need high-speed data transfer support GDMA. The GDMA controller and CPU data bus have access to the same address space in internal and external RAM. Figure 2-2 shows the basic architecture of the GDMA engine.

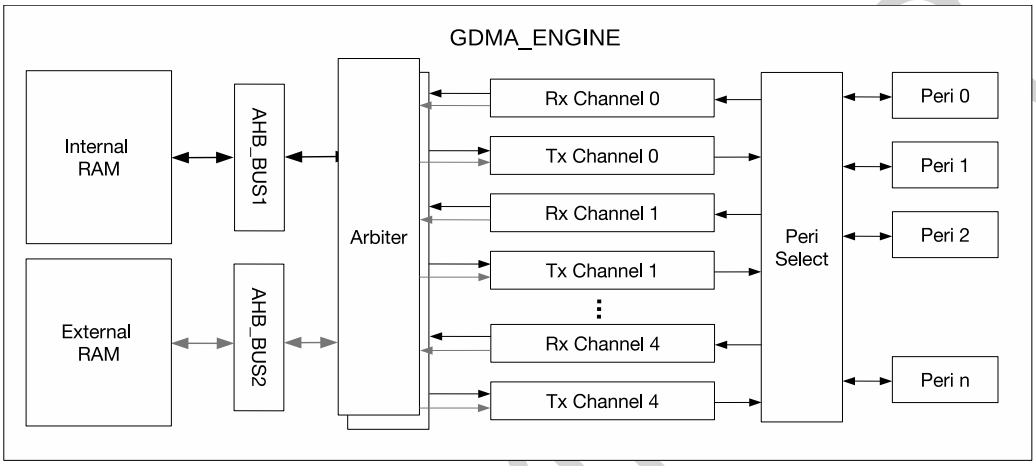


Figure 2-2. GDMA Engine Architecture

The GDMA controller has ten independent channels, i.e. five transmit channels and five receive channels. Every channel can be connected to different peripherals. In other words, channels are general-purpose, shared by peripherals.

The GDMA engine has two independent AHB bus referred to as AHB_BUS1 and AHB_BUS2 respectively. AHB_BUS1 is used to read data from or write data to internal RAM, whereas AHB_BUS2 is used to read data from or write data to external RAM. For available address range of RAM, please see Chapter 3 *System and Memory*.

Software can use the GDMA engine through linked lists. These linked lists, stored in internal RAM, consist of outlink*n* and inlink*n*, where *n* indicates the channel number (ranging from 0 to 4). The GDMA controller reads an outlink*n* (i.e. a linked list of transmit descriptors) from internal RAM and transmits data in corresponding RAM according to the outlink*n*, or reads an inlink*n* (i.e. a linked list of receive descriptors) and stores received data into specific address space in RAM according to the inlink*n*.

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2.4 Functional Description

2.4.1 Linked List

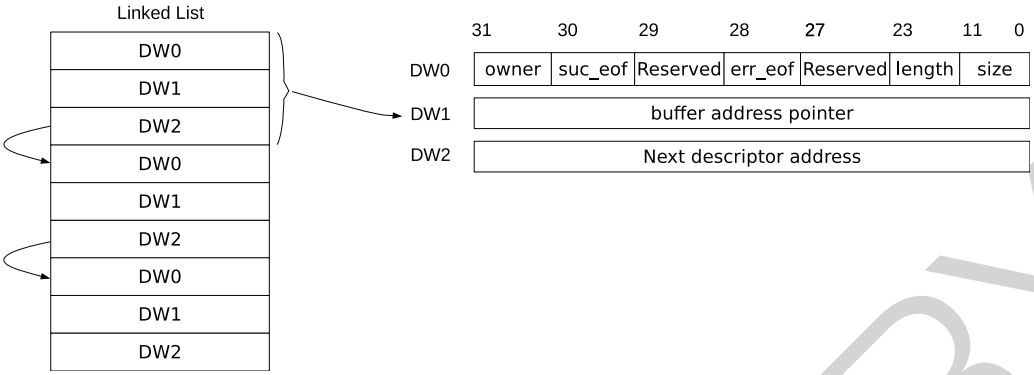


Figure 2-3. Structure of a Linked List

Figure 2-3 shows the structure of a linked list. An outlink and an inlink have the same structure. A linked list is formed by one or more descriptors, and each descriptor consists of three words. Linked lists should be in internal RAM for the GDMA engine to be able to use them. The meaning of each field is as follows:

- Owner (DW0) [31]: Specifies who is allowed to access the buffer that this descriptor points to.
  1'b0: CPU can access the buffer;
  1'b1: The GDMA controller can access the buffer.
  When the GDMA controller stops using the buffer, this bit in a transmit descriptor is automatically cleared by hardware, and this bit in a receive descriptor is automatically cleared by hardware only if GDMA_OUT_AUTO_WRBACK_CH*n* is set to 1. When software loads a linked list, this bit should be set to 1.
  Note: GDMA_OUT is the prefix of transmit channel registers, and GDMA_IN is the prefix of receive channel registers.
- suc_eof (DW0) [30]: Specifies whether this descriptor is the last descriptor in the list.
  1'b0: This descriptor is not the last one;
  1'b1: This descriptor is the last one.
  Software clears suc_eof bit in receive descriptors. When a frame or packet has been received, this bit in the last receive descriptor is set by hardware, and this bit in the last transmit descriptor is set by software.
- Reserved (DW0) [29]: Reserved. Value of this bit does not matter.
- err_eof (DW0) [28]: Specifies whether the received data have errors.
  This bit is used only when UHCI0 uses GDMA to receive data. When an error is detected in the received frame or packet, this bit in the receive descriptor is set to 1 by hardware.
- Reserved (DW0) [27:24]: Reserved.
- Length (DW0) [23:12]: Specifies the number of valid bytes in the buffer that this descriptor points to. This field in a transmit descriptor is written by software and indicates how many bytes can be read from the buffer; this field in a receive descriptor is written by hardware automatically and indicates how many valid bytes have been stored into the buffer.
- Size (DW0) [11:0]: Specifies the size of the buffer that this descriptor points to.

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- Buffer address pointer (DW1): Address of the buffer.
- Next descriptor address (DW2): Address of the next descriptor. If the current descriptor is the last one (suc_eof = 1), this value is 0. This field can only point to internal RAM.

If the length of data received is smaller than the size of the buffer, the GDMA controller will not use available space of the buffer in the next transaction.

2.4.2 Peripheral-to-Memory and Memory-to-Peripheral Data Transfer

The GDMA controller can transfer data from memory to peripheral (transmit) and from peripheral to memory (receive). A transmit channel transfers data in the specified memory location to a peripheral's transmitter via an outlink*n*, whereas a receive channel transfers data received by a peripheral to the specified memory location via an inlink*n*.

Every transmit and receive channel can be connected to any peripheral with GDMA feature. Table 2-1 illustrates how to select the peripheral to be connected via registers. When a channel is connected to a peripheral, the rest channels can not be connected to that peripheral. All transmit and receive channels support access to internal and external RAM. For details, please refer to Section 2.4.8 and Section 2.4.9.

Table 2-1. Selecting Peripherals via Register Configuration

GDMA_PERI_IN_SEL_CH*n* GDMA_PERI_OUT_SEL_CH*n*	Peripheral
0	SPI2
1	SPI3
2	UHCI0
3	I2S0
4	I2S1
5	LCD/CAM
6	AES
7	SHA
8	ADC
9	RMT

2.4.3 Memory-to-Memory Data Transfer

The GDMA controller also allows memory-to-memory data transfer. Such data transfer can be enabled by setting GDMA_MEM_TRANS_EN_CH*n*, which connects the output of transmit channel *n* to the input of receive channel *n*. Note that a transmit channel is only connected to the receive channel with the same number (*n*).

As every transmit and receive channel can be used to access internal and external RAM, there are four data transfer modes:

- from internal RAM to internal RAM
- from internal RAM to external RAM
- from external RAM to internal RAM
- from external RAM to external RAM

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2.4.4 Channel Buffer

Every transmit and receive channel contains FIFOs at three levels, i.e. L1FIFO, L2FIFO, and L3FIFO. As Figure 2-4 shows, L1FIFO is close to the memory, L3FIFO is close to peripherals, and L2FIFO falls in between L1FIFO and L3FIFO. L1FIFO, L2FIFO and L3FIFO have fixed depth: 24, 128, and 16 bytes, respectively.

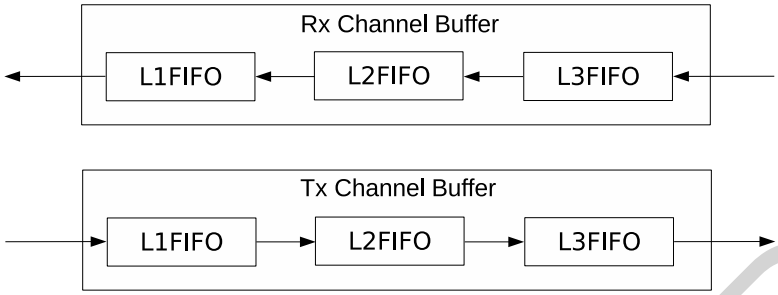


Figure 2-4. Channel Buffer

2.4.5 Enabling GDMA

Software uses the GDMA controller through linked lists. When the GDMA controller receives data, software loads an inlink, configures GDMA_INLINK_ADDR_CH*n* field with address of the first receive descriptor, and sets GDMA_INLINK_START_CH*n* bit to enable GDMA. When the GDMA controller transmits data, software loads an outlink, prepares data to be transmitted, configures GDMA_OUTLINK_ADDR_CH*n* field with address of the first transmit descriptor, and sets GDMA_OUTLINK_START_CH*n* bit to enable GDMA. GDMA_INLINK_START_CH*n* bit and GDMA_OUTLINK_START_CH*n* bit are cleared automatically by hardware.

In some cases, you may want to append more descriptors to a DMA transfer that is already started. Naively, it would seem to be possible to do this by clearing the EOF bit of the final descriptor in the existing list and setting its next descriptor address pointer field (DW2) to the first descriptor of the to-be-added list. However, this strategy fails if the existing DMA transfer is almost or entirely finished. Instead, the GDMA engine has specialized logic to make sure a DMA transfer can be continued or restarted: if it is still ongoing, it will make sure to take the appended descriptors into account; if the transfer has already finished, it will restart with the new descriptors. This is implemented in the Restart function.

When using the Restart function, software needs to rewrite the address of the first descriptor in the new list to DW2 of the last descriptor in the loaded list, and set GDMA_INLINK_RESTART_CH*n* bit or GDMA_OUTLINK_RESTART_CH*n* bit (these two bits are cleared automatically by hardware). As shown in Figure 2-5, by doing so hardware can obtain the address of the first descriptor in the new list when reading the last descriptor in the loaded list, and then read the new list.

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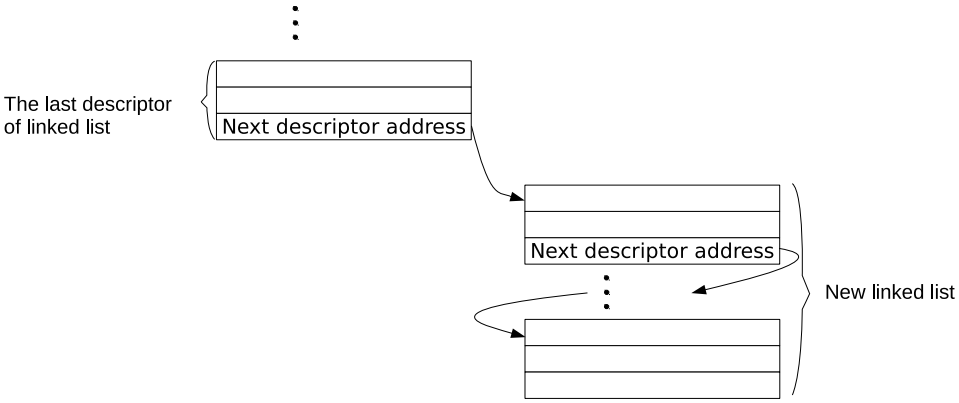


Figure 2-5. Relationship among Linked Lists

2.4.6 Linked List Reading Process

Once configured and enabled by software, the GDMA controller starts to read the linked list from internal RAM. The GDMA performs checks on descriptors in the linked list. Only if the descriptors pass the checks, will the corresponding GDMA channel transfer data. If the descriptors fail any of the checks, hardware will trigger descriptor error interrupt (either GDMA_IN_DSCR_ERR_CH*n*_INT or GDMA_OUT_DSCR_ERR_CH*n*_INT), and the channel will halt.

The checks performed on descriptors are:

- Owner bit check when GDMA_IN_CHECK_OWNER_CH*n* or GDMA_OUT_CHECK_OWNER_CH*n* is set to 1. If the owner bit is 0, the buffer is accessed by the CPU. In this case, the owner bit fails the check. The owner bit will not be checked if GDMA_IN_CHECK_OWNER_CH*n* or GDMA_OUT_CHECK_OWNER_CH*n* is 0;
- Buffer address pointer (DW1) check. If the buffer address pointer points to 0x3FC88000 ~ 0x3FCFFFFF or 0x3C000000 ~ 0x3DFFFFFF (please refer to Section 2.4.8), it passes the check.

After software detects a descriptor error interrupt, it must reset the corresponding channel, and enable GDMA by setting GDMA_OUTLINK_START_CH*n* or GDMA_INLINK_START_CH*n* bit.

Note: The third word (DW2) in a descriptor can only point to a location in internal RAM, given that the third word points to the next descriptor to use and that all descriptors must be in internal memory.

2.4.7 EOF

The GDMA controller uses EOF (end of frame) flags to indicate the end of data frame or packet transmission.

Before the GDMA controller transmits data, GDMA_OUT_TOTAL_EOF_CH*n*_INT_ENA bit should be set to enable GDMA_OUT_TOTAL_EOF_CH*n*_INT interrupt. If data in the buffer pointed by the last descriptor (with EOF) have been transmitted, a GDMA_OUT_TOTAL_EOF_CH*n*_INT interrupt is generated.

Before the GDMA controller receives data, GDMA_IN_SUC_EOF_CH*n*_INT_ENA bit should be set to enable GDMA_IN_SUC_EOF_CH*n*_INT interrupt. If a data frame or packet has been received successfully, a GDMA_IN_SUC_EOF_CH*n*_INT interrupt is generated. In addition, when GDMA channel is connected to UHCI0, the GDMA controller also supports GDMA_IN_ERR_CH*n*_EOF_INT interrupt. This interrupt is enabled by setting GDMA_IN_ERR_EOF_CH*n*_INT_ENA bit, and it indicates that a data frame or packet has been received with errors.

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When detecting a GDMA_OUT_TOTAL_EOF_CH*n*_INT or a GDMA_IN_SUC_EOF_CH*n*_INT interrupt, software can record the value of GDMA_OUT_EOF_DES_ADDR_CH*n* or GDMA_IN_SUC_EOF_DES_ADDR_CH*n* field, i.e. address of the last descriptor. Therefore, software can tell which descriptors have been used and reclaim them.

Note: In this chapter, EOF of transmit descriptors refers to suc_eof, while EOF of receive descriptors refers to both suc_eof and err_eof.

2.4.8 Accessing Internal RAM

Any transmit and receive channels of GDMA can access 0x3FC88000 ~ 0x3FCFFFFF in internal RAM. To improve data transfer efficiency, GDMA can send data in burst mode, which is disabled by default. This mode is enabled for receive channels by setting GDMA_IN_DATA_BURST_EN_CH*n*, and enabled for transmit channels by setting GDMA_OUT_DATA_BURST_EN_CH*n*.

Table 2-2. Descriptor Field Alignment Requirements for Accessing Internal RAM

Inlink/Outlink	Burst Mode	Size	Length	Buffer Address Pointer
Inlink	0	—	—	—
	1	Word-aligned	—	Word-aligned
Outlink	0	—	—	—
	1	—	—	—

Table 2-2 lists the requirements for descriptor field alignment when GDMA accesses internal RAM.

When burst mode is disabled, size, length, and buffer address pointer in both transmit and receive descriptors do not need to be word-aligned. That is to say, GDMA can read data of specified length (1 ~ 4095 bytes) from any start addresses in the accessible address range, or write received data of the specified length (1 ~ 4095 bytes) to any contiguous addresses in the accessible address range.

When burst mode is enabled, size, length, and buffer address pointer in transmit descriptors are also not necessarily word-aligned. However, size and buffer address pointer in receive descriptors except length should be word-aligned.

2.4.9 Accessing External RAM

Any transmit and receive channels of GDMA can access 0x3C000000 ~ 0x3DFFFFFF in external RAM. GDMA can send data only in burst mode. The number of data bytes to transfer in one burst is defined as block size. Block size can be 16 bytes, 32 bytes or 64 bytes, configured via GDMA_IN_EXT_MEM_BK_SIZE_CH*n* for transmit channels and GDMA_OUT_EXT_MEM_BK_SIZE_CH*n* for receive channels.

Table 2-3. Descriptor Field Alignment Requirements for Accessing External RAM

Inlink/Outlink	Size	Length	Buffer Address Pointer
Inlink	Block-aligned	—	Block-aligned
Outlink	—	—	—

Table 2-3 lists the requirements for descriptor field alignment when GDMA accesses internal RAM. Size, length, and buffer address pointer in transmit descriptors do not need to be aligned. However, size and buffer address pointer in receive descriptors except length should be aligned with block size. Table 2-4 illustrates the value of

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GDMA_IN_EXT_MEM_BK_SIZE_CH*n* or GDMA_OUT_EXT_MEM_BK_SIZE_CH*n* bit when fields in linked list descriptors are 16-byte, 32-byte and 64-byte aligned respectively.

Table 2-4. Relationship Between Configuration Register, Block Size and Alignment

GDMA_IN_EXT_MEM_BK_SIZE_CH*n* or GDMA_OUT_EXT_MEM_BK_SIZE_CH*n*	Block Size	Alignment
0	16 bytes	16-byte aligned
1	32 bytes	32-byte aligned
2	64 bytes	64-byte aligned

Note: For receive descriptors, if the data length received are not aligned with block size, GDMA will pad the data received with 0 until they are aligned to initiate burst transfer. You can read the length field in receive descriptors to obtain the length of valid data received.

2.4.10 External RAM Access Permissions

GDMA in ESP32-S3 has a permission control module for access to external RAM. As Figure 2-6 shows, the permission control module divided the 32 MB external RAM into four areas through three configurable boundaries, namely boundary 0, boundary 1, and boundary 2.

- Area 0: 0x3C000000 ~ boundary 0 (include 0x3C000000 but exclude boundary 0)
- Area 1: boundary 0 ~ boundary 1 (include boundary 0 but exclude boundary 1)
- Area 2: boundary 1 ~ boundary 2 (include boundary 1 but exclude boundary 2)
- Area 3: boundary 2 ~ 0x3DFFFFFF (include boundary 0)

Boundary 0, 1, and 2 are configured via PMS_EDMA_BOUNDARY_0, PMS_EDMA_BOUNDARY_1, and PMS_EDMA_BOUNDARY_2, respectively. For details about these fields, please refer to Chapter 13 *Permission Control (PMS)*. The unit of these fields is 4 KB. For example, if PMS_EDMA_BOUNDARY_0 is 0x80, the address of boundary 0 should be 0x3C000000 + 0x80 * 4 KB = 3c080000, in which 0x3C000000 is the starting address of accessible external RAM.

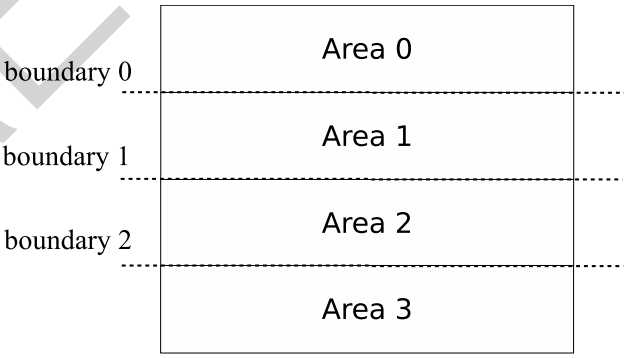


Figure 2-6. Dividing External RAM into Areas

All peripherals with GDMA feature (i.e. SPI2, SPI3, UHCI0, I2S0, I2S1, LCD/CAM, AES, SHA, ADC, and RMT) do not have access permissions for Area 0 and Area 3, but their permissions for Area 1 and Area 2 can be independently managed. The permission control module contains registers to manage such access permissions for Area 1 and Area 2. For example, the PMS_EDMA_PMS_SPI2_ATTR1 field configures SPI2's permissions to

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read and write Area 1. Specifically, when bit 0 of this field is 1, SPI2 is granted read permission; when bit 1 of this field is 1, SPI2 is granted write permission. Likewise, the PMS_EDMA_PMS_SPI2_ATTR2 field configures SPI2's permissions to read and write Area 2.

Access violations are logged and can trigger the GDMA_ETXMEN_REJECT_INT interrupt. You can check the address where the address violation occurs, the peripheral involved, channel number and read or write attribute via GDMA_ETXMEM_REJECT_ADDR, GDMA_ETXMEN_REJECT_PERI_NUM, GDMA_ETXMEN_REJECT_CHANNEL_NUM, and GDMA_ETXMEM_REJECT_ATTR respectively.

2.4.11 Seamless Access to Internal and External RAM

In some application scenarios, a data frame or packet contains data from both internal RAM and external RAM. To ensure real-time data processing, GDMA is designed in such a way that some descriptors in the linked list can be used to access internal RAM, while the other descriptors in the same linked list can be used to access external RAM. This design allows seamless access to internal and external RAM.

2.4.12 Arbitration

To ensure timely response to peripherals running at a high speed with low latency (such as SPI, LCD/CAM), the GDMA controller implements a fixed-priority channel arbitration scheme. That is to say, each channel can be assigned a priority from 0 ~ 9. The larger the number, the higher the priority, and the more timely the response. When several channels are assigned the same priority, the GDMA controller adopts a round-robin arbitration scheme.

Please note that the overall throughput of peripherals with GDMA feature cannot exceed the maximum bandwidth of the GDMA, so that requests from low-priority peripherals can be responded to.

2.5 GDMA Interrupts

- GDMA_OUT_TOTAL_EOF_CH*n*_INT: Triggered when all data corresponding to a linked list (including multiple descriptors) have been sent via transmit channel *n*.
- GDMA_IN_DSCR_EMPTY_CH*n*_INT: Triggered when the size of the buffer pointed by receive descriptors is smaller than the length of data to be received via receive channel *n*.
- GDMA_OUT_DSCR_ERR_CH*n*_INT: Triggered when an error is detected in a transmit descriptor on transmit channel *n*.
- GDMA_IN_DSCR_ERR_CH*n*_INT: Triggered when an error is detected in a receive descriptor on receive channel *n*.
- GDMA_OUT_EOF_CH*n*_INT: Triggered when EOF in a transmit descriptor is 1 and data corresponding to this descriptor have been sent via transmit channel *n*. If GDMA_OUT_EOF_MODE_CH*n* is 0, this interrupt will be triggered when the last byte of data corresponding to this descriptor enters GDMA's transmit channel; if GDMA_OUT_EOF_MODE_CH*n* is 1, this interrupt is triggered when the last byte of data is taken from GDMA's transmit channel.
- GDMA_OUT_DONE_CH*n*_INT: Triggered when all data corresponding to a transmit descriptor have been sent via transmit channel *n*.
- GDMA_IN_ERR_EOF_CH*n*_INT: Triggered when an error is detected in the data frame or packet received via receive channel *n*. This interrupt is used only for UHCI0 peripheral (UART0 or UART1).

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- GDMA_IN_SUC_EOF_CH*n*_INT: Triggered when a data frame or packet has been received via receive channel *n*.
- GDMA_IN_DONE_CH*n*_INT: Triggered when all data corresponding to a receive descriptor have been received via receive channel *n*.

2.6 Programming Procedures

2.6.1 Programming Procedures for GDMA's Transmit Channel

To transmit data, GDMA's transmit channel should be configured by software as follows:

1. Set GDMA_OUT_RST_CH*n* first to 1 and then to 0, to reset the state machine of GDMA's transmit channel and FIFO pointer;
2. Load an outlink, and configure GDMA_OUTLINK_ADDR_CH*n* with address of the first transmit descriptor;
3. Configure GDMA_PERI_OUT_SEL_CH*n* with the value corresponding to the peripheral to be connected, as shown in Table 2-1;
4. Set GDMA_OUTLINK_START_CH*n* to enable GDMA's transmit channel for data transfer;
5. Configure and enable the corresponding peripheral (SPI2, SPI3, UHCI0 (UART0, UART1, or UART2), I2S0, I2S1, AES, SHA, and ADC). See details in individual chapters of these peripherals;
6. Wait for GDMA_OUT_EOF_CH*n*_INT interrupt, which indicates the completion of data transfer.

2.6.2 Programming Procedures for GDMA's Receive Channel

To receive data, GDMA's receive channel should be configured by software as follows:

1. Set GDMA_IN_RST_CH*n* first to 1 and then to 0, to reset the state machine of GDMA's receive channel and FIFO pointer;
2. Load an inlink, and configure GDMA_INLINK_ADDR_CH*n* with address of the first receive descriptor;
3. Configure GDMA_PERI_IN_SEL_CH*n* with the value corresponding to the peripheral to be connected, as shown in Table 2-1;
4. Set GDMA_INLINK_START_CH*n* to enable GDMA's receive channel for data transfer;
5. Configure and enable the corresponding peripheral (SPI2, SPI3, UHCI0 (UART0, UART1, or UART2), I2S0, I2S1, AES, SHA, and ADC). See details in individual chapters of these peripherals;
6. Wait for GDMA_IN_SUC_EOF_CH*n*_INT interrupt, which indicates that a data frame or packet has been received.

2.6.3 Programming Procedures for Memory-to-Memory Transfer

To transfer data from one memory location to another, GDMA should be configured by software as follows:

1. Set GDMA_OUT_RST_CH*n* first to 1 and then to 0, to reset the state machine of GDMA's transmit channel and FIFO pointer;
2. Set GDMA_IN_RST_CH*n* first to 1 and then to 0, to reset the state machine of GDMA's receive channel and FIFO pointer;

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3. Load an outlink, and configure GDMA_OUTLINK_ADDR_CH*n* with address of the first transmit descriptor;
4. Load an inlink, and configure GDMA_INLINK_ADDR_CH*n* with address of the first receive descriptor;
5. Set GDMA_MEM_TRANS_EN_CH*n* to enable memory-to-memory transfer;
6. Set GDMA_OUTLINK_START_CH*n* to enable GDMA's transmit channel for data transfer;
7. Set GDMA_INLINK_START_CH*n* to enable GDMA's receive channel for data transfer;
8. Wait for GDMA_IN_SUC_EOF_CH*n*_INT interrupt, which indicates that which indicates that a data transaction has been completed.

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2.7 Register Summary

The addresses in this section are relative to GDMA base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
Configuration Registers			
GDMA_IN_CONF0_CH0_REG	Configuration register 0 of RX channel 0	0x0000	R/W
GDMA_IN_CONF1_CH0_REG	Configuration register 1 of RX channel 0	0x0004	R/W
GDMA_IN_POP_CH0_REG	Pop control register of RX channel 0	0x001C	varies
GDMA_IN_LINK_CH0_REG	Link descriptor configuration and control register of RX channel 0	0x0020	varies
GDMA_OUT_CONF0_CH0_REG	Configuration register 0 of TX channel 0	0x0060	R/W
GDMA_OUT_CONF1_CH0_REG	Configuration register 1 of TX channel 0	0x0064	R/W
GDMA_OUT_PUSH_CH0_REG	Push control register of RX channel 0	0x007C	varies
GDMA_OUT_LINK_CH0_REG	Link descriptor configuration and control register of TX channel 0	0x0080	varies
GDMA_IN_CONF0_CH1_REG	Configuration register 0 of RX channel 1	0x00C0	R/W
GDMA_IN_CONF1_CH1_REG	Configuration register 1 of RX channel 1	0x00C4	R/W
GDMA_IN_POP_CH1_REG	Pop control register of RX channel 1	0x00DC	varies
GDMA_IN_LINK_CH1_REG	Link descriptor configuration and control register of RX channel 1	0x00E0	varies
GDMA_OUT_CONF0_CH1_REG	Configuration register 0 of TX channel 1	0x0120	R/W
GDMA_OUT_CONF1_CH1_REG	Configuration register 1 of TX channel 1	0x0124	R/W
GDMA_OUT_PUSH_CH1_REG	Push control register of RX channel 1	0x013C	varies
GDMA_OUT_LINK_CH1_REG	Link descriptor configuration and control register of TX channel 1	0x0140	varies
GDMA_IN_CONF0_CH2_REG	Configuration register 0 of RX channel 2	0x0180	R/W
GDMA_IN_CONF1_CH2_REG	Configuration register 1 of RX channel 2	0x0184	R/W
GDMA_IN_POP_CH2_REG	Pop control register of RX channel 2	0x019C	varies
GDMA_IN_LINK_CH2_REG	Link descriptor configuration and control register of RX channel 2	0x01A0	varies
GDMA_OUT_CONF0_CH2_REG	Configuration register 0 of TX channel 2	0x01E0	R/W
GDMA_OUT_CONF1_CH2_REG	Configuration register 1 of TX channel 2	0x01E4	R/W
GDMA_OUT_PUSH_CH2_REG	Push control register of RX channel 2	0x01FC	varies
GDMA_OUT_LINK_CH2_REG	Link descriptor configuration and control register of TX channel 2	0x0200	varies
GDMA_IN_CONF0_CH3_REG	Configuration register 0 of RX channel 3	0x0240	R/W
GDMA_IN_CONF1_CH3_REG	Configuration register 1 of RX channel 3	0x0244	R/W
GDMA_IN_POP_CH3_REG	Pop control register of RX channel 3	0x025C	varies
GDMA_IN_LINK_CH3_REG	Link descriptor configuration and control register of RX channel 3	0x0260	varies
GDMA_OUT_CONF0_CH3_REG	Configuration register 0 of TX channel 3	0x02A0	R/W
GDMA_OUT_CONF1_CH3_REG	Configuration register 1 of TX channel 3	0x02A4	R/W
GDMA_OUT_PUSH_CH3_REG	Push control register of RX channel 3	0x02BC	varies

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Name	Description	Address	Access
GDMA_OUT_LINK_CH3_REG	Link descriptor configuration and control register of TX channel 3	0x02C0	varies
GDMA_IN_CONF0_CH4_REG	Configuration register 0 of RX channel 4	0x0300	R/W
GDMA_IN_CONF1_CH4_REG	Configuration register 1 of RX channel 4	0x0304	R/W
GDMA_IN_POP_CH4_REG	Pop control register of RX channel 4	0x031C	varies
GDMA_IN_LINK_CH4_REG	Link descriptor configuration and control register of RX channel 4	0x0320	varies
GDMA_OUT_CONF0_CH4_REG	Configuration register 0 of TX channel 4	0x0360	R/W
GDMA_OUT_CONF1_CH4_REG	Configuration register 1 of TX channel 4	0x0364	R/W
GDMA_OUT_PUSH_CH4_REG	Push control register of RX channel 4	0x037C	varies
GDMA_OUT_LINK_CH4_REG	Link descriptor configuration and control register of TX channel 4	0x0380	varies
GDMA_PD_CONF_REG	reserved	0x03C4	R/W
GDMA_MISC_CONF_REG	Miscellaneous register	0x03C8	R/W
Interrupt Registers			
GDMA_IN_INT_RAW_CH0_REG	Raw status interrupt of RX channel 0	0x0008	R/WTC/SS
GDMA_IN_INT_ST_CH0_REG	Masked interrupt of RX channel 0	0x000C	RO
GDMA_IN_INT_ENA_CH0_REG	Interrupt enable bits of RX channel 0	0x0010	R/W
GDMA_IN_INT_CLR_CH0_REG	Interrupt clear bits of RX channel 0	0x0014	WT
GDMA_OUT_INT_RAW_CH0_REG	Raw status interrupt of TX channel 0	0x0068	R/WTC/SS
GDMA_OUT_INT_ST_CH0_REG	Masked interrupt of TX channel 0	0x006C	RO
GDMA_OUT_INT_ENA_CH0_REG	Interrupt enable bits of TX channel 0	0x0070	R/W
GDMA_OUT_INT_CLR_CH0_REG	Interrupt clear bits of TX channel 0	0x0074	WT
GDMA_IN_INT_RAW_CH1_REG	Raw status interrupt of RX channel 1	0x00C8	R/WTC/SS
GDMA_IN_INT_ST_CH1_REG	Masked interrupt of RX channel 1	0x00CC	RO
GDMA_IN_INT_ENA_CH1_REG	Interrupt enable bits of RX channel 1	0x00D0	R/W
GDMA_IN_INT_CLR_CH1_REG	Interrupt clear bits of RX channel 1	0x00D4	WT
GDMA_OUT_INT_RAW_CH1_REG	Raw status interrupt of TX channel 1	0x0128	R/WTC/SS
GDMA_OUT_INT_ST_CH1_REG	Masked interrupt of TX channel 1	0x012C	RO
GDMA_OUT_INT_ENA_CH1_REG	Interrupt enable bits of TX channel 1	0x0130	R/W
GDMA_OUT_INT_CLR_CH1_REG	Interrupt clear bits of TX channel 1	0x0134	WT
GDMA_IN_INT_RAW_CH2_REG	Raw status interrupt of RX channel 2	0x0188	R/WTC/SS
GDMA_IN_INT_ST_CH2_REG	Masked interrupt of RX channel 2	0x018C	RO
GDMA_IN_INT_ENA_CH2_REG	Interrupt enable bits of RX channel 2	0x0190	R/W
GDMA_IN_INT_CLR_CH2_REG	Interrupt clear bits of RX channel 2	0x0194	WT
GDMA_OUT_INT_RAW_CH2_REG	Raw status interrupt of TX channel 2	0x01E8	R/WTC/SS
GDMA_OUT_INT_ST_CH2_REG	Masked interrupt of TX channel 2	0x01EC	RO
GDMA_OUT_INT_ENA_CH2_REG	Interrupt enable bits of TX channel 2	0x01F0	R/W
GDMA_OUT_INT_CLR_CH2_REG	Interrupt clear bits of TX channel 2	0x01F4	WT
GDMA_IN_INT_RAW_CH3_REG	Raw status interrupt of RX channel 3	0x0248	R/WTC/SS
GDMA_IN_INT_ST_CH3_REG	Masked interrupt of RX channel 3	0x024C	RO
GDMA_IN_INT_ENA_CH3_REG	Interrupt enable bits of RX channel 3	0x0250	R/W
GDMA_IN_INT_CLR_CH3_REG	Interrupt clear bits of RX channel 3	0x0254	WT

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Name	Description	Address	Access
GDMA_OUT_INT_RAW_CH3_REG	Raw status interrupt of TX channel 3	0x02A8	R/WTC/SS
GDMA_OUT_INT_ST_CH3_REG	Masked interrupt of TX channel 3	0x02AC	RO
GDMA_OUT_INT_ENA_CH3_REG	Interrupt enable bits of TX channel 3	0x02B0	R/W
GDMA_OUT_INT_CLR_CH3_REG	Interrupt clear bits of TX channel 3	0x02B4	WT
GDMA_IN_INT_RAW_CH4_REG	Raw status interrupt of RX channel 4	0x0308	R/WTC/SS
GDMA_IN_INT_ST_CH4_REG	Masked interrupt of RX channel 4	0x030C	RO
GDMA_IN_INT_ENA_CH4_REG	Interrupt enable bits of RX channel 4	0x0310	R/W
GDMA_IN_INT_CLR_CH4_REG	Interrupt clear bits of RX channel 4	0x0314	WT
GDMA_OUT_INT_RAW_CH4_REG	Raw status interrupt of TX channel 4	0x0368	R/WTC/SS
GDMA_OUT_INT_ST_CH4_REG	Masked interrupt of TX channel 4	0x036C	RO
GDMA_OUT_INT_ENA_CH4_REG	Interrupt enable bits of TX channel 4	0x0370	R/W
GDMA_OUT_INT_CLR_CH4_REG	Interrupt clear bits of TX channel 4	0x0374	WT
GDMA_EXTMEM_REJECT_INT_RAW_REG	Raw interrupt status of external RAM permission	0x03FC	R/WTC/SS
GDMA_EXTMEM_REJECT_INT_ST_REG	Masked interrupt status of external RAM permission	0x0400	RO
GDMA_EXTMEM_REJECT_INT_ENA_REG	Interrupt enable bits of external RAM permission	0x0404	R/W
GDMA_EXTMEM_REJECT_INT_CLR_REG	Interrupt clear bits of external RAM permission	0x0408	WT
Status Registers			
GDMA_INFIFO_STATUS_CH0_REG	Receive FIFO status of RX channel 0	0x0018	RO
GDMA_IN_STATE_CH0_REG	Receive status of RX channel 0	0x0024	RO
GDMA_IN_SUC_EOF_DES_ADDR_CH0_REG	Inlink descriptor address when EOF occurs of RX channel 0	0x0028	RO
GDMA_IN_ERR_EOF_DES_ADDR_CH0_REG	Inlink descriptor address when errors occur of RX channel 0	0x002C	RO
GDMA_IN_DSCR_CH0_REG	Current inlink descriptor address of RX channel 0	0x0030	RO
GDMA_IN_DSCR_BF0_CH0_REG	The last inlink descriptor address of RX channel 0	0x0034	RO
GDMA_IN_DSCR_BF1_CH0_REG	The second-to-last inlink descriptor address of RX channel 0	0x0038	RO
GDMA_OUTFIFO_STATUS_CH0_REG	Transmit FIFO status of TX channel 0	0x0078	RO
GDMA_OUT_STATE_CH0_REG	Transmit status of TX channel 0	0x0084	RO
GDMA_OUT_EOF_DES_ADDR_CH0_REG	Outlink descriptor address when EOF occurs of TX channel 0	0x0088	RO
GDMA_OUT_EOF_BFR_DES_ADDR_CH0_REG	The last outlink descriptor address when EOF occurs of TX channel 0	0x008C	RO
GDMA_OUT_DSCR_CH0_REG	Current inlink descriptor address of TX channel 0	0x0090	RO
GDMA_OUT_DSCR_BF0_CH0_REG	The last inlink descriptor address of TX channel 0	0x0094	RO

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Name	Description	Address	Access
GDMA_OUT_DSCR_BF1_CH0_REG	The second-to-last inlink descriptor address of TX channel 0	0x0098	RO
GDMA_INFIFO_STATUS_CH1_REG	Receive FIFO status of RX channel 1	0x00D8	RO
GDMA_IN_STATE_CH1_REG	Receive status of RX channel 1	0x00E4	RO
GDMA_IN_SUC_EOF_DES_ADDR_CH1_REG	Inlink descriptor address when EOF occurs of RX channel 1	0x00E8	RO
GDMA_IN_ERR_EOF_DES_ADDR_CH1_REG	Inlink descriptor address when errors occur of RX channel 1	0x00EC	RO
GDMA_IN_DSCR_CH1_REG	Current inlink descriptor address of RX channel 1	0x00F0	RO
GDMA_IN_DSCR_BF0_CH1_REG	The last inlink descriptor address of RX channel 1	0x00F4	RO
GDMA_IN_DSCR_BF1_CH1_REG	The second-to-last inlink descriptor address of RX channel 1	0x00F8	RO
GDMA_OUTFIFO_STATUS_CH1_REG	Transmit FIFO status of TX channel 1	0x0138	RO
GDMA_OUT_STATE_CH1_REG	Transmit status of TX channel 1	0x0144	RO
GDMA_OUT_EOF_DES_ADDR_CH1_REG	Outlink descriptor address when EOF occurs of TX channel 1	0x0148	RO
GDMA_OUT_EOF_BFR_DES_ADDR_CH1_REG	The last outlink descriptor address when EOF occurs of TX channel 1	0x014C	RO
GDMA_OUT_DSCR_CH1_REG	Current inlink descriptor address of TX channel 1	0x0150	RO
GDMA_OUT_DSCR_BF0_CH1_REG	The last inlink descriptor address of TX channel 1	0x0154	RO
GDMA_OUT_DSCR_BF1_CH1_REG	The second-to-last inlink descriptor address of TX channel 1	0x0158	RO
GDMA_INFIFO_STATUS_CH2_REG	Receive FIFO status of RX channel 2	0x0198	RO
GDMA_IN_STATE_CH2_REG	Receive status of RX channel 2	0x01A4	RO
GDMA_IN_SUC_EOF_DES_ADDR_CH2_REG	Inlink descriptor address when EOF occurs of RX channel 2	0x01A8	RO
GDMA_IN_ERR_EOF_DES_ADDR_CH2_REG	Inlink descriptor address when errors occur of RX channel 2	0x01AC	RO
GDMA_IN_DSCR_CH2_REG	Current inlink descriptor address of RX channel 2	0x01B0	RO
GDMA_IN_DSCR_BF0_CH2_REG	The last inlink descriptor address of RX channel 2	0x01B4	RO
GDMA_IN_DSCR_BF1_CH2_REG	The second-to-last inlink descriptor address of RX channel 2	0x01B8	RO
GDMA_OUTFIFO_STATUS_CH2_REG	Transmit FIFO status of TX channel 2	0x01F8	RO
GDMA_OUT_STATE_CH2_REG	Transmit status of TX channel 2	0x0204	RO
GDMA_OUT_EOF_DES_ADDR_CH2_REG	Outlink descriptor address when EOF occurs of TX channel 2	0x0208	RO
GDMA_OUT_EOF_BFR_DES_ADDR_CH2_REG	The last outlink descriptor address when EOF occurs of TX channel 2	0x020C	RO

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Name	Description	Address	Access
GDMA_OUT_DSCR_CH2_REG	Current inlink descriptor address of TX channel 2	0x0210	RO
GDMA_OUT_DSCR_BF0_CH2_REG	The last inlink descriptor address of TX channel 2	0x0214	RO
GDMA_OUT_DSCR_BF1_CH2_REG	The second-to-last inlink descriptor address of TX channel 2	0x0218	RO
GDMA_INFIFO_STATUS_CH3_REG	Receive FIFO status of RX channel 3	0x0258	RO
GDMA_IN_STATE_CH3_REG	Receive status of RX channel 3	0x0264	RO
GDMA_IN_SUC_EOF_DES_ADDR_CH3_REG	Inlink descriptor address when EOF occurs of RX channel 3	0x0268	RO
GDMA_IN_ERR_EOF_DES_ADDR_CH3_REG	Inlink descriptor address when errors occur of RX channel 3	0x026C	RO
GDMA_IN_DSCR_CH3_REG	Current inlink descriptor address of RX channel 3	0x0270	RO
GDMA_IN_DSCR_BF0_CH3_REG	The last inlink descriptor address of RX channel 3	0x0274	RO
GDMA_IN_DSCR_BF1_CH3_REG	The second-to-last inlink descriptor address of RX channel 3	0x0278	RO
GDMA_OUTFIFO_STATUS_CH3_REG	Transmit FIFO status of TX channel 3	0x02B8	RO
GDMA_OUT_STATE_CH3_REG	Transmit status of TX channel 3	0x02C4	RO
GDMA_OUT_EOF_DES_ADDR_CH3_REG	Outlink descriptor address when EOF occurs of TX channel 3	0x02C8	RO
GDMA_OUT_EOF_BFR_DES_ADDR_CH3_REG	The last outlink descriptor address when EOF occurs of TX channel 3	0x02CC	RO
GDMA_OUT_DSCR_CH3_REG	Current inlink descriptor address of TX channel 3	0x02D0	RO
GDMA_OUT_DSCR_BF0_CH3_REG	The last inlink descriptor address of TX channel 3	0x02D4	RO
GDMA_OUT_DSCR_BF1_CH3_REG	The second-to-last inlink descriptor address of TX channel 3	0x02D8	RO
GDMA_INFIFO_STATUS_CH4_REG	Receive FIFO status of RX channel 4	0x0318	RO
GDMA_IN_STATE_CH4_REG	Receive status of RX channel 4	0x0324	RO
GDMA_IN_SUC_EOF_DES_ADDR_CH4_REG	Inlink descriptor address when EOF occurs of RX channel 4	0x0328	RO
GDMA_IN_ERR_EOF_DES_ADDR_CH4_REG	Inlink descriptor address when errors occur of RX channel 4	0x032C	RO
GDMA_IN_DSCR_CH4_REG	Current inlink descriptor address of RX channel 4	0x0330	RO
GDMA_IN_DSCR_BF0_CH4_REG	The last inlink descriptor address of RX channel 4	0x0334	RO
GDMA_IN_DSCR_BF1_CH4_REG	The second-to-last inlink descriptor address of RX channel 4	0x0338	RO
GDMA_OUTFIFO_STATUS_CH4_REG	Transmit FIFO status of TX channel 4	0x0378	RO
GDMA_OUT_STATE_CH4_REG	Transmit status of TX channel 4	0x0384	RO

PRELIMINARY

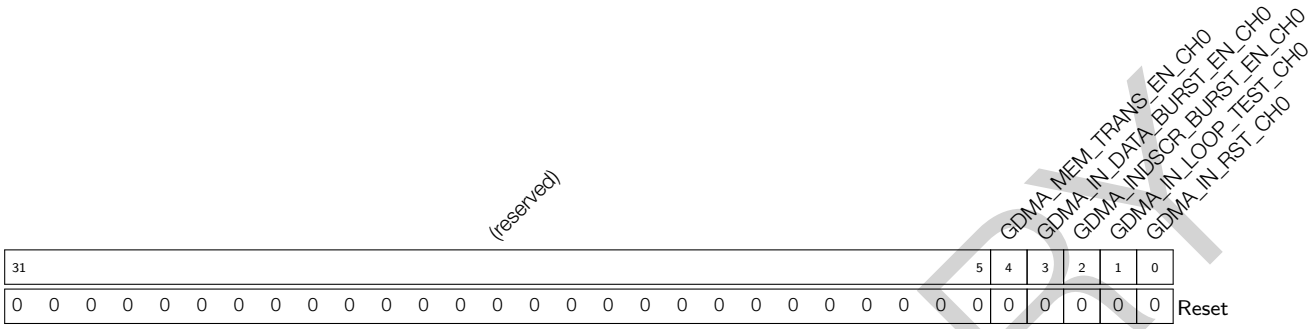
Name	Description	Address	Access
GDMA_OUT_EOF_DES_ADDR_CH4_REG	Outlink descriptor address when EOF occurs of TX channel 4	0x0388	RO
GDMA_OUT_EOF_BFR_DES_ADDR_CH4_REG	The last outlink descriptor address when EOF occurs of TX channel 4	0x038C	RO
GDMA_OUT_DSCR_CH4_REG	Current inlink descriptor address of TX channel 4	0x0390	RO
GDMA_OUT_DSCR_BF0_CH4_REG	The last inlink descriptor address of TX channel 4	0x0394	RO
GDMA_OUT_DSCR_BF1_CH4_REG	The second-to-last inlink descriptor address of TX channel 4	0x0398	RO
Priority Registers			
GDMA_IN_PRI_CH0_REG	Priority register of RX channel 0	0x0044	R/W
GDMA_OUT_PRI_CH0_REG	Priority register of TX channel 0	0x00A4	R/W
GDMA_IN_PRI_CH1_REG	Priority register of RX channel 1	0x0104	R/W
GDMA_OUT_PRI_CH1_REG	Priority register of TX channel 1	0x0164	R/W
GDMA_IN_PRI_CH2_REG	Priority register of RX channel 2	0x01C4	R/W
GDMA_OUT_PRI_CH2_REG	Priority register of TX channel 2	0x0224	R/W
GDMA_IN_PRI_CH3_REG	Priority register of RX channel 3	0x0284	R/W
GDMA_OUT_PRI_CH3_REG	Priority register of TX channel 3	0x02E4	R/W
GDMA_IN_PRI_CH4_REG	Priority register of RX channel 4	0x0344	R/W
GDMA_OUT_PRI_CH4_REG	Priority register of TX channel 4	0x03A4	R/W
Peripheral Selection Registers			
GDMA_IN_PERI_SEL_CH0_REG	Peripheral selection of RX channel 0	0x0048	R/W
GDMA_OUT_PERI_SEL_CH0_REG	Peripheral selection of TX channel 0	0x00A8	R/W
GDMA_IN_PERI_SEL_CH1_REG	Peripheral selection of RX channel 1	0x0108	R/W
GDMA_OUT_PERI_SEL_CH1_REG	Peripheral selection of TX channel 1	0x0168	R/W
GDMA_IN_PERI_SEL_CH2_REG	Peripheral selection of RX channel 2	0x01C8	R/W
GDMA_OUT_PERI_SEL_CH2_REG	Peripheral selection of TX channel 2	0x0228	R/W
GDMA_IN_PERI_SEL_CH3_REG	Peripheral selection of RX channel 3	0x0288	R/W
GDMA_OUT_PERI_SEL_CH3_REG	Peripheral selection of TX channel 3	0x02E8	R/W
GDMA_IN_PERI_SEL_CH4_REG	Peripheral selection of RX channel 4	0x0348	R/W
GDMA_OUT_PERI_SEL_CH4_REG	Peripheral selection of TX channel 4	0x03A8	R/W
Permission Status Registers			
GDMA_EXTMEM_REJECT_ADDR_REG	External RAM address where access violation occurs	0x03F4	RO
GDMA_EXTMEM_REJECT_ST_REG	Status of external RAM where access violation occurs	0x03F8	RO
Version Register			
GDMA_DATE_REG	Version control register	0x040C	R/W

PRELIMINARY

2.8 Registers

The addresses in this section are relative to GDMA base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 2.1. GDMA_IN_CONF0_CH*n*_REG (*n*: 0-4) (0x0000+192n*)**



GDMA_IN_RST_CH*n* This bit is used to reset GDMA channel 0 RX FSM and RX FIFO pointer. (R/W)

GDMA_IN_LOOP_TEST_CH*n* Reserved. (R/W)

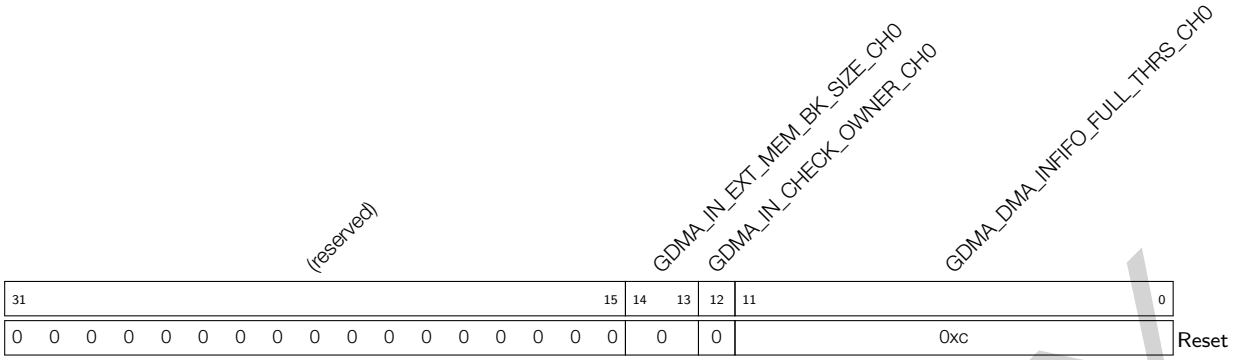
GDMA_INDSCR_BURST_EN_CH*n* Set this bit to 1 to enable INCR burst transfer for RX channel 0 reading descriptor when accessing internal RAM. (R/W)

GDMA_IN_DATA_BURST_EN_CH*n* Set this bit to 1 to enable INCR burst transfer for RX channel 0 receiving data when accessing internal RAM. (R/W)

GDMA_MEM_TRANS_EN_CH*n* Set this bit 1 to enable automatic transmitting data from memory to memory via GDMA. (R/W)

PRELIMINARY

Register 2.2. GDMA_IN_CONF1_CH*n*_REG (*n*: 0-4) (0x0004+192n*)**

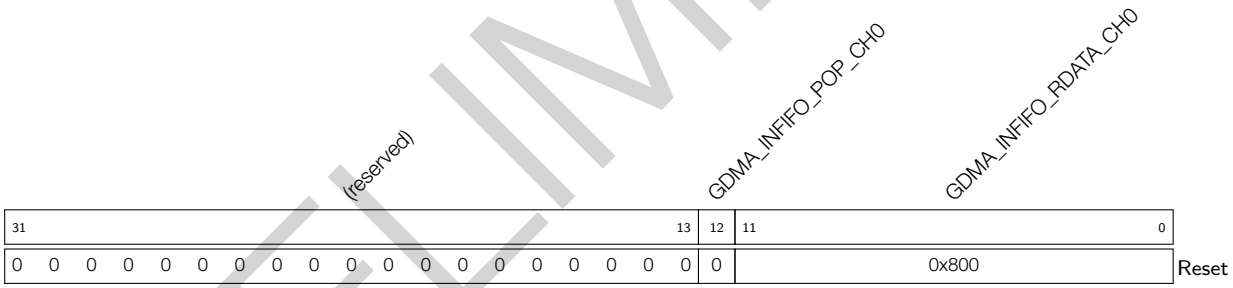


GDMA_DMA_INFIFO_FULL_THRS_CH*n* This register is used to generate the GDMA_INFIFO_FULL_WM_INT interrupt when RX channel 0 received byte number in RX FIFO is up to the value of the register. (R/W)

GDMA_IN_CHECK_OWNER_CH*n* Set this bit to enable checking the owner attribute of the descriptor. (R/W)

GDMA_IN_EXT_MEM_BK_SIZE_CH*n* Block size of RX channel 0 when GDMA access external RAM. 0: 16 bytes; 1: 32 bytes; 2: 64 bytes; 3: Reserved. (R/W)

Register 2.3. GDMA_IN_POP_CH*n*_REG (*n*: 0-4) (0x001C+192n*)**

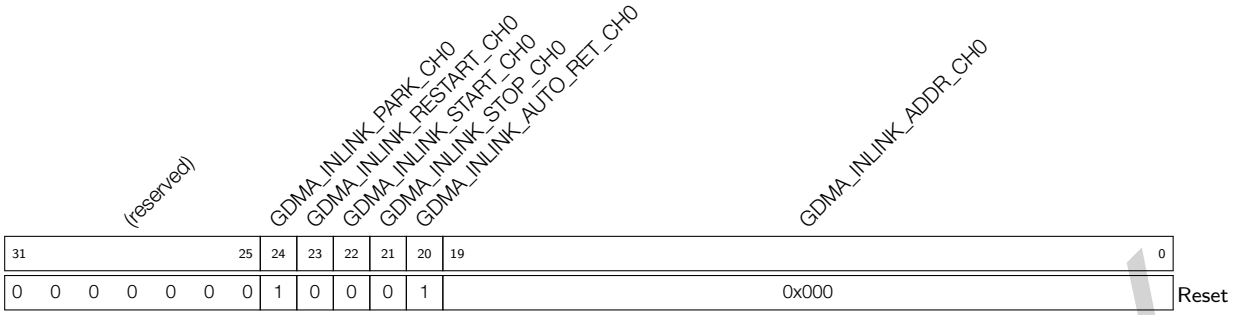


GDMA_INFIFO_RDATA_CH*n* This register stores the data popping from GDMA FIFO (intended for debugging). (RO)

GDMA_INFIFO_POP_CH*n* Set this bit to pop data from GDMA FIFO (intended for debugging). (R/W/SC)

PRELIMINARY

Register 2.4. GDMA_IN_LINK_CH*n*_REG (*n*: 0-4) (0x0020+192n*)**



GDMA_INLINK_ADDR_CH*n* This register stores the 20 least significant bits of the first receive descriptor's address. (R/W)

GDMA_INLINK_AUTO_RET_CH*n* Set this bit to return to current receive descriptor's address, when there are some errors in current receiving data. (R/W)

GDMA_INLINK_STOP_CH*n* Set this bit to stop GDMA's receive channel from receiving data. (R/W/SC)

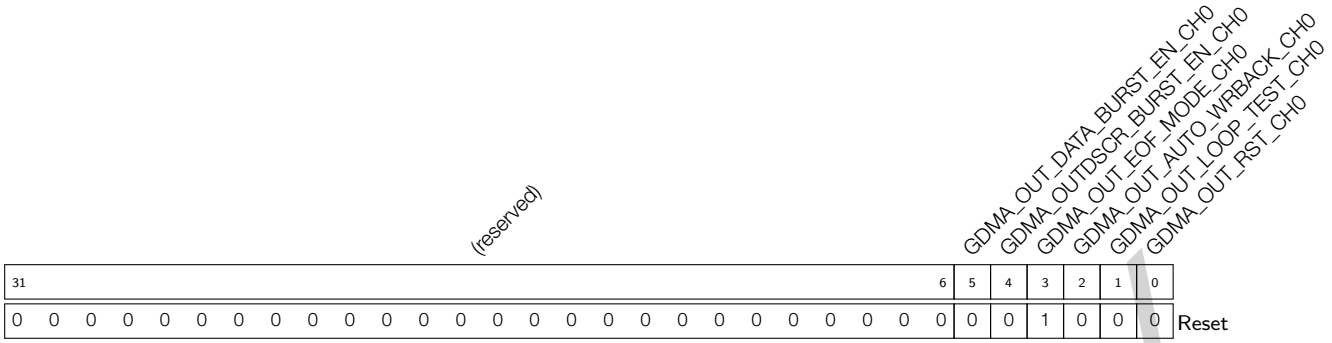
GDMA_INLINK_START_CH*n* Set this bit to enable GDMA's receive channel for data transfer. (R/W/SC)

GDMA_INLINK_RESTART_CH*n* Set this bit to mount a new receive descriptor. (R/W/SC)

GDMA_INLINK_PARK_CH*n* 1: the receive descriptor's FSM is in idle state; 0: the receive descriptor's FSM is working. (RO)

PRELIMINARY

Register 2.5. GDMA_OUT_CONF0_CH*n*_REG (*n*: 0-4) (0x0060+192n*)**



GDMA_OUT_RST_CH*n* This bit is used to reset GDMA channel 0 TX FSM and TX FIFO pointer. (R/W)

GDMA_OUT_LOOP_TEST_CH*n* Reserved. (R/W)

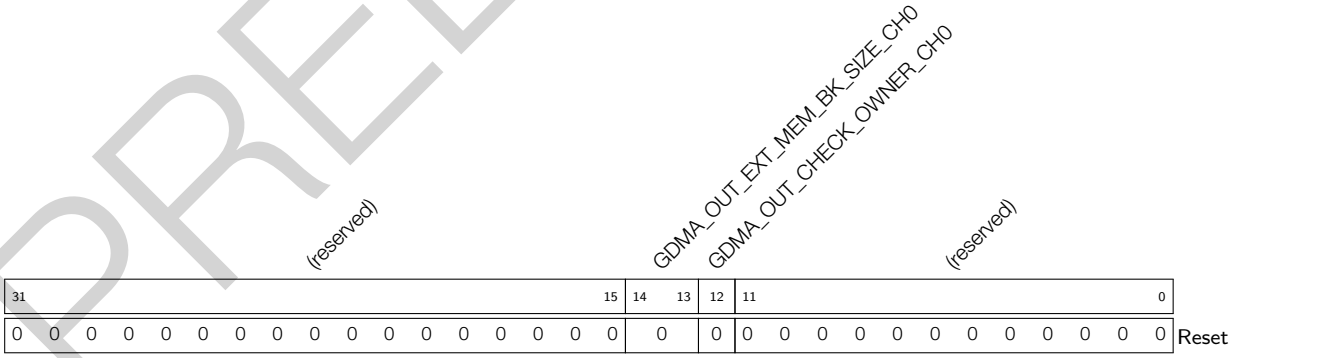
GDMA_OUT_AUTO_WRBACK_CH*n* Set this bit to enable automatic outlink-writeback when all the data in TX FIFO has been transmitted. (R/W)

GDMA_OUT_EOF_MODE_CH*n* EOF flag generation mode when transmitting data. 1: EOF flag for TX channel 0 is generated when data need to transmit has been popped from FIFO in GDMA. (R/W)

GDMA_OUTDSCR_BURST_EN_CH*n* Set this bit to 1 to enable INCR burst transfer for TX channel 0 reading descriptor when accessing internal RAM. (R/W)

GDMA_OUT_DATA_BURST_EN_CH*n* Set this bit to 1 to enable INCR burst transfer for TX channel 0 transmitting data when accessing internal RAM. (R/W)

Register 2.6. GDMA_OUT_CONF1_CH*n*_REG (*n*: 0-4) (0x0064+192n*)**

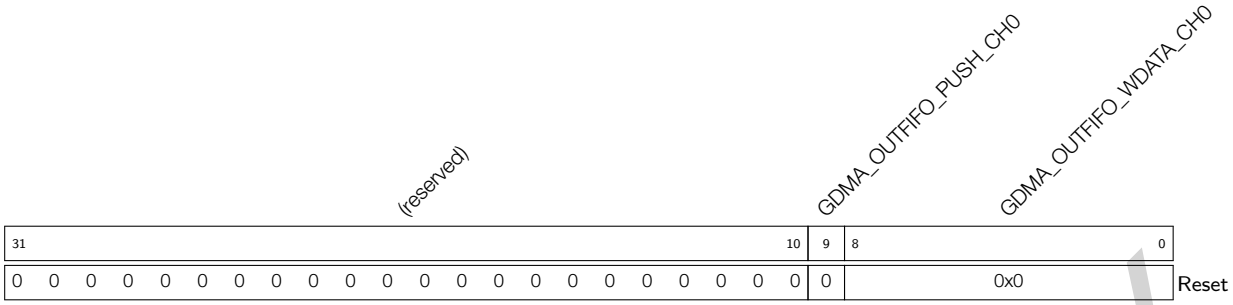


GDMA_OUT_CHECK_OWNER_CH*n* Set this bit to enable checking the owner attribute of the descriptor. (R/W)

GDMA_OUT_EXT_MEM_BK_SIZE_CH*n* Block size of TX channel 0 when GDMA access external RAM. 0: 16 bytes; 1: 32 bytes; 2: 64 bytes; 3: Reserved. (R/W)

PRELIMINARY

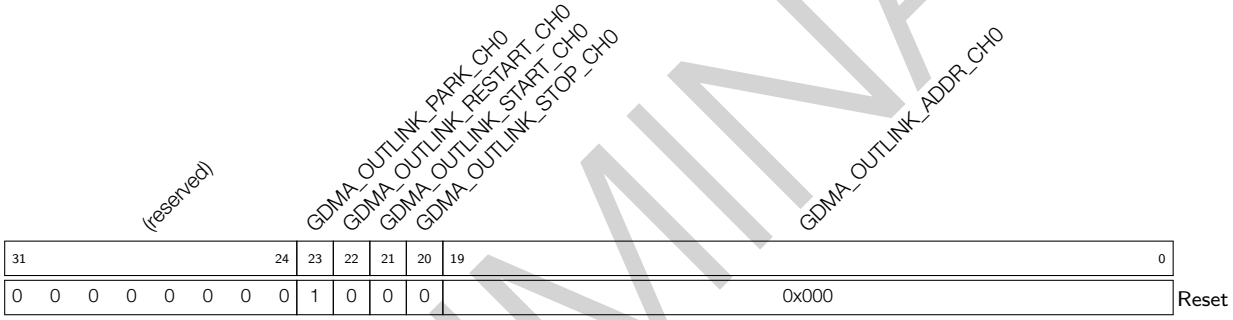
Register 2.7. GDMA_OUT_PUSH_CH*n*_REG (*n*: 0-4) (0x007C+192n*)**



GDMA_OUTFIFO_WDATA_CH*n* This register stores the data that need to be pushed into GDMA FIFO. (R/W)

GDMA_OUTFIFO_PUSH_CH*n* Set this bit to push data into GDMA FIFO. (R/W/SC)

Register 2.8. GDMA_OUT_LINK_CH*n*_REG (*n*: 0-4) (0x0080+192n*)**



GDMA_OUTLINK_ADDR_CH*n* This register stores the 20 least significant bits of the first transmit descriptor's address. (R/W)

GDMA_OUTLINK_STOP_CH*n* Set this bit to stop GDMA's transmit channel from transferring data. (R/W/SC)

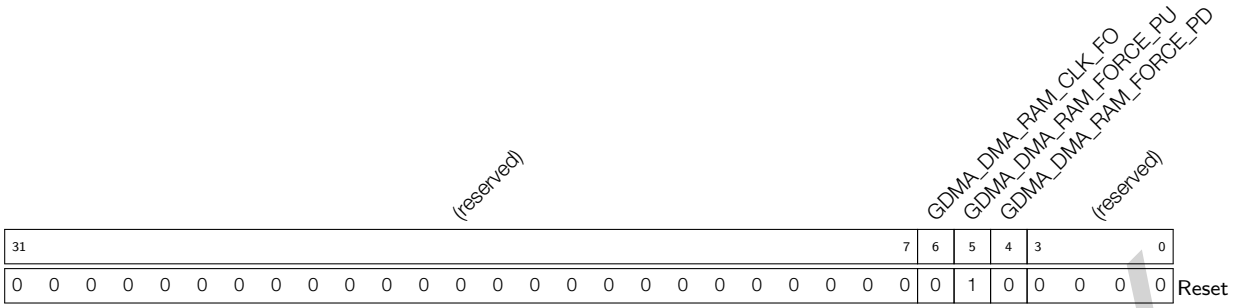
GDMA_OUTLINK_START_CH*n* Set this bit to enable GDMA's transmit channel for data transfer. (R/W/SC)

GDMA_OUTLINK_RESTART_CH*n* Set this bit to restart a new outlink from the last address. (R/W/SC)

GDMA_OUTLINK_PARK_CH*n* 1: the transmit descriptor's FSM is in idle state; 0: the transmit descriptor's FSM is working. (RO)

PRELIMINARY

Register 2.9. GDMA_PD_CONF_REG (0x03C4)

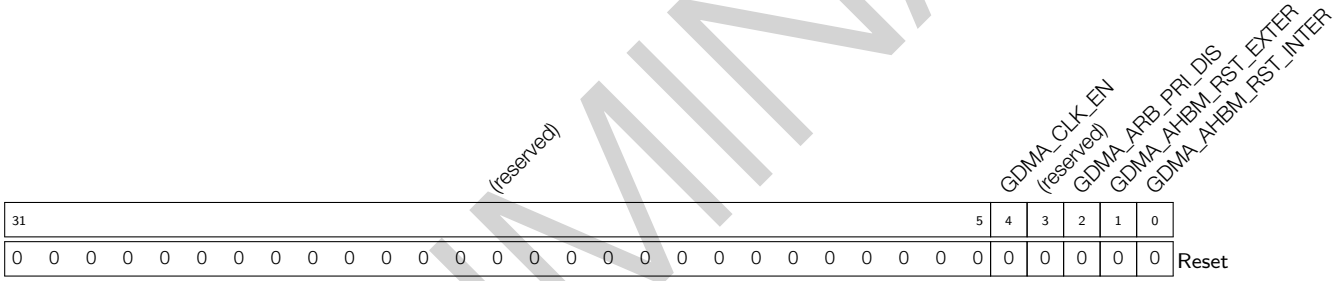


GDMA_DMA_RAM_FORCE_PD Set this bit to force power down GDMA internal memory. (R/W)

GDMA_DMA_RAM_FORCE_PU Set this bit to force power up GDMA internal memory. (R/W)

GDMA_DMA_RAM_CLK_FO 1: Force to open the clock and bypass the gate-clock when accessing the RAM in GDMA; 0: A gate-clock will be used when accessing the RAM in GDMA. (R/W)

Register 2.10. GDMA_MISC_CONF_REG (0x03C8)



GDMA_AHBM_RST_INTER Set this bit, then clear this bit to reset the internal AHB FSM. (R/W)

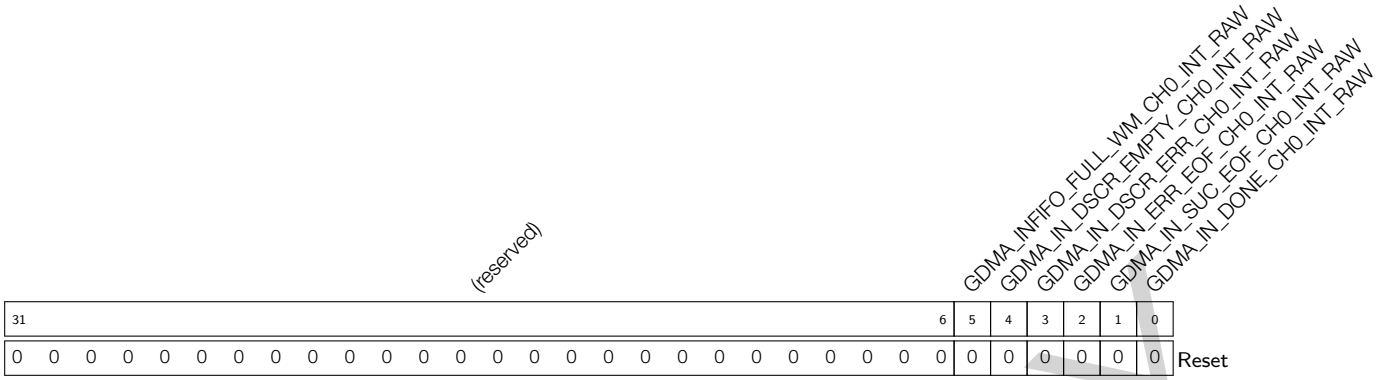
GDMA_AHBM_RST_EXTER Set this bit, then clear this bit to reset the external AHB FSM. (R/W)

GDMA_ARB_PRI_DIS Set this bit to disable priority arbitration function. (R/W)

GDMA_CLK_EN 1: Force clock on for registers; 0: Support clock only when application writes registers. (R/W)

PRELIMINARY

Register 2.11. GDMA_IN_INT_RAW_CH*n*_REG (*n*: 0-4) (0x0008+192n*)**



GDMA_IN_DONE_CH*n*_INT_RAW The raw interrupt bit turns to high level when the last data pointed by one receive descriptor has been received for RX channel 0. (R/WTC/SS)

GDMA_IN_SUC_EOF_CH*n*_INT_RAW The raw interrupt bit turns to high level when the last data pointed by one receive descriptor has been received for RX channel 0. For UHCI0, the raw interrupt bit turns to high level when the last data pointed by one receive descriptor has been received and no data error is detected for RX channel 0. (R/WTC/SS)

GDMA_IN_ERR_EOF_CH*n*_INT_RAW The raw interrupt bit turns to high level when data error is detected only in the case that the peripheral is UHCI0 for RX channel 0. For other peripherals, this raw interrupt is reserved. (R/WTC/SS)

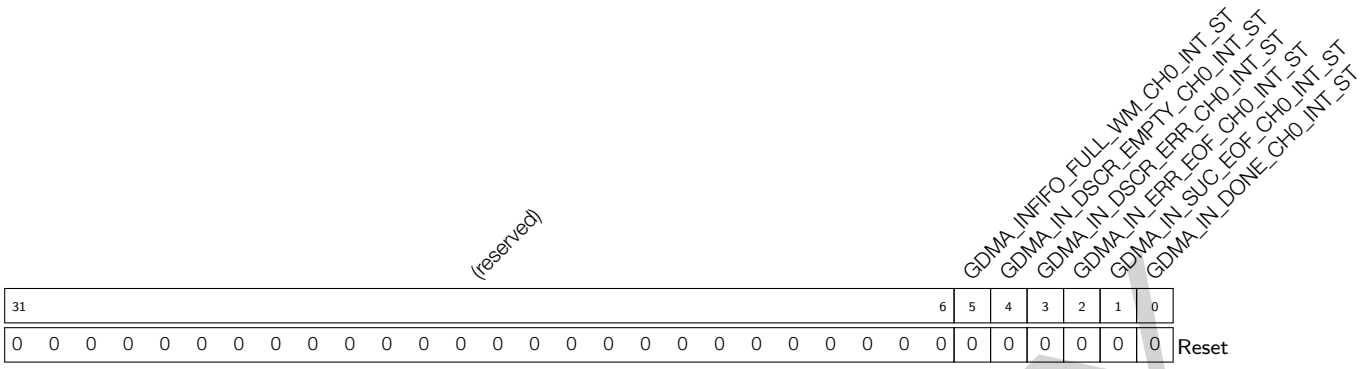
GDMA_IN_DSCR_ERR_CH*n*_INT_RAW The raw interrupt bit turns to high level when detecting receive descriptor error, including owner error, the second and third word error of receive descriptor for RX channel 0. (R/WTC/SS)

GDMA_IN_DSCR_EMPTY_CH*n*_INT_RAW The raw interrupt bit turns to high level when RX FIFO pointed by inlink is full and receiving data is not completed, but there is no more inlink for RX channel 0. (R/WTC/SS)

GDMA_INFIFO_FULL_WM_CH*n*_INT_RAW The raw interrupt bit turns to high level when received data byte number is up to threshold configured by GDMA_DMA_INFIFO_FULL_THRS_CH0 in RX FIFO of RX channel 0. (R/WTC/SS)

PRELIMINARY

Register 2.12. GDMA_IN_INT_ST_CH*n*_REG (*n*: 0-4) (0x000C+192n*)**



GDMA_IN_DONE_CH*n*_INT_ST The raw interrupt status bit for the GDMA_IN_DONE_CH_INT interrupt. (RO)

GDMA_IN_SUC_EOF_CH*n*_INT_ST The raw interrupt status bit for the GDMA_IN_SUC_EOF_CH_INT interrupt. (RO)

GDMA_IN_ERR_EOF_CH*n*_INT_ST The raw interrupt status bit for the GDMA_IN_ERR_EOF_CH_INT interrupt. (RO)

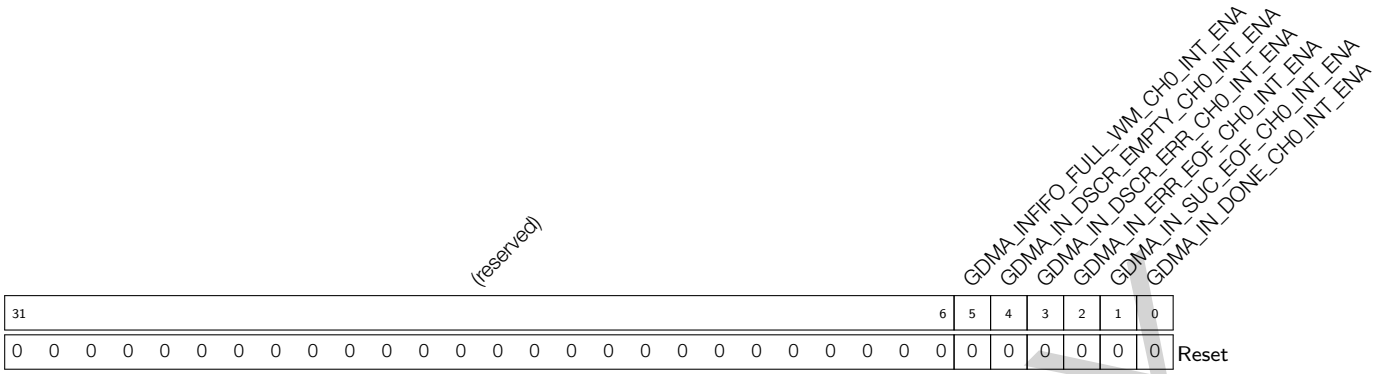
GDMA_IN_DSCR_ERR_CH*n*_INT_ST The raw interrupt status bit for the GDMA_IN_DSCR_ERR_CH_INT interrupt. (RO)

GDMA_IN_DSCR_EMPTY_CH*n*_INT_ST The raw interrupt status bit for the GDMA_IN_DSCR_EMPTY_CH_INT interrupt. (RO)

GDMA_INFIFO_FULL_WM_CH*n*_INT_ST The raw interrupt status bit for the GDMA_INFIFO_FULL_WM_CH_INT interrupt. (RO)

PRELIMINARY

Register 2.13. GDMA_IN_INT_ENA_CH*n*_REG (*n*: 0-4) (0x0010+192n*)**



GDMA_IN_DONE_CH*n*_INT_ENA The interrupt enable bit for the GDMA_IN_DONE_CH_INT interrupt. (R/W)

GDMA_IN_SUC_EOF_CH*n*_INT_ENA The interrupt enable bit for the GDMA_IN_SUC_EOF_CH_INT interrupt. (R/W)

GDMA_IN_ERR_EOF_CH*n*_INT_ENA The interrupt enable bit for the GDMA_IN_ERR_EOF_CH_INT interrupt. (R/W)

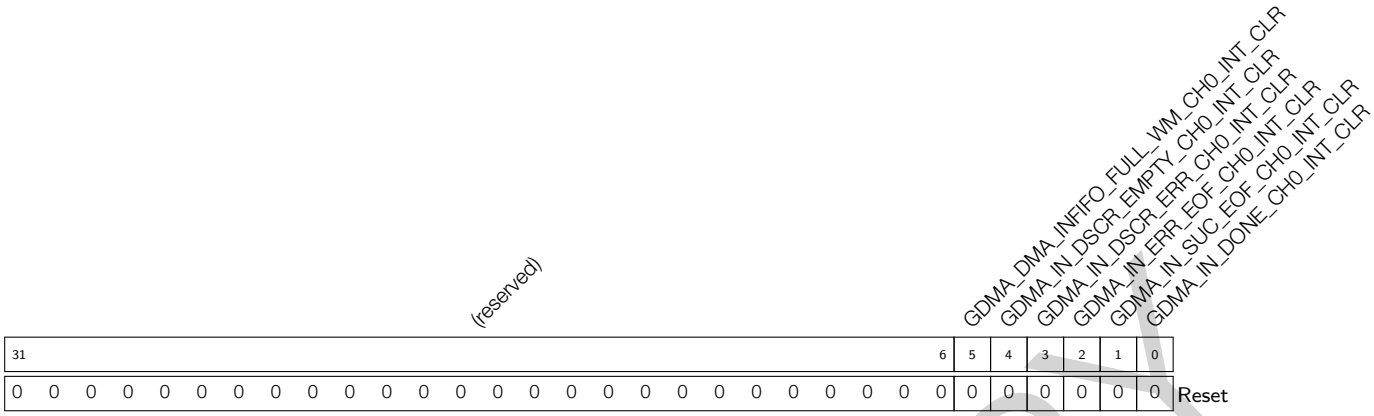
GDMA_IN_DSCR_ERR_CH*n*_INT_ENA The interrupt enable bit for the GDMA_IN_DSCR_ERR_CH_INT interrupt. (R/W)

GDMA_IN_DSCR_EMPTY_CH*n*_INT_ENA The interrupt enable bit for the GDMA_IN_DSCR_EMPTY_CH_INT interrupt. (R/W)

GDMA_INFIFO_FULL_WM_CH*n*_INT_ENA The interrupt enable bit for the GDMA_INFIFO_FULL_WM_CH_INT interrupt. (R/W)

PRELIMINARY

Register 2.14. GDMA_IN_INT_CLR_CH*n*_REG (*n*: 0-4) (0x0014+192n*)**



GDMA_IN_DONE_CH*n*_INT_CLR Set this bit to clear the GDMA_IN_DONE_CH_INT interrupt. (WT)

GDMA_IN_SUC_EOF_CH*n*_INT_CLR Set this bit to clear the GDMA_IN_SUC_EOF_CH_INT interrupt. (WT)

GDMA_IN_ERR_EOF_CH*n*_INT_CLR Set this bit to clear the GDMA_IN_ERR_EOF_CH_INT interrupt. (WT)

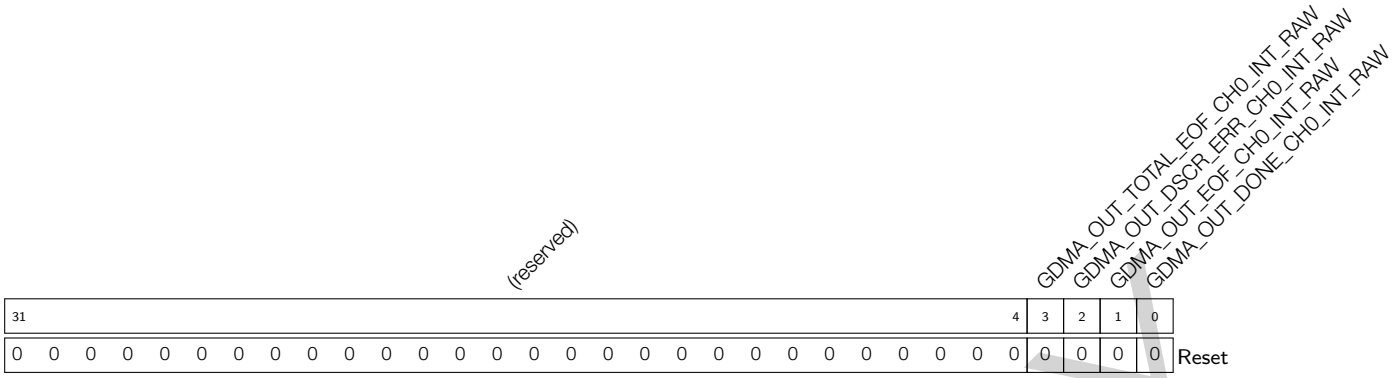
GDMA_IN_DSCR_ERR_CH*n*_INT_CLR Set this bit to clear the GDMA_IN_DSCR_ERR_CH_INT interrupt. (WT)

GDMA_IN_DSCR_EMPTY_CH*n*_INT_CLR Set this bit to clear the GDMA_IN_DSCR_EMPTY_CH_INT interrupt. (WT)

GDMA_DMA_INFIFO_FULL_WM_CH*n*_INT_CLR Set this bit to clear the GDMA_INFIFO_FULL_WM_CH_INT interrupt. (WT)

PRELIMINARY

Register 2.15. GDMA_OUT_INT_RAW_CH*n*_REG (*n*: 0-4) (0x0068+192n*)**



GDMA_OUT_DONE_CH*n*_INT_RAW The raw interrupt bit turns to high level when the last data pointed by one transmit descriptor has been transmitted to peripherals for TX channel 0. (R/WTC/SS)

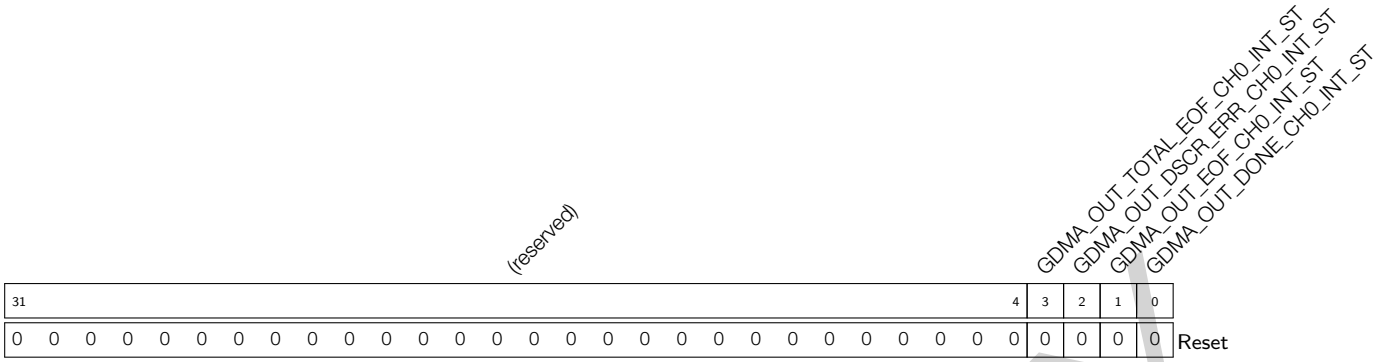
GDMA_OUT_EOF_CH*n*_INT_RAW The raw interrupt bit turns to high level when the last data pointed by one transmit descriptor has been read from memory for TX channel 0. (R/WTC/SS)

GDMA_OUT_DSCR_ERR_CH*n*_INT_RAW The raw interrupt bit turns to high level when detecting transmit descriptor error, including owner error, the second and third word error of transmit descriptor for TX channel 0. (R/WTC/SS)

GDMA_OUT_TOTAL_EOF_CH*n*_INT_RAW The raw interrupt bit turns to high level when data corresponding a outlink (includes one descriptor or few descriptors) is transmitted out for TX channel 0. (R/WTC/SS)

PRELIMINARY

Register 2.16. GDMA_OUT_INT_ST_CH*n*_REG (*n*: 0-4) (0x006C+192n*)**



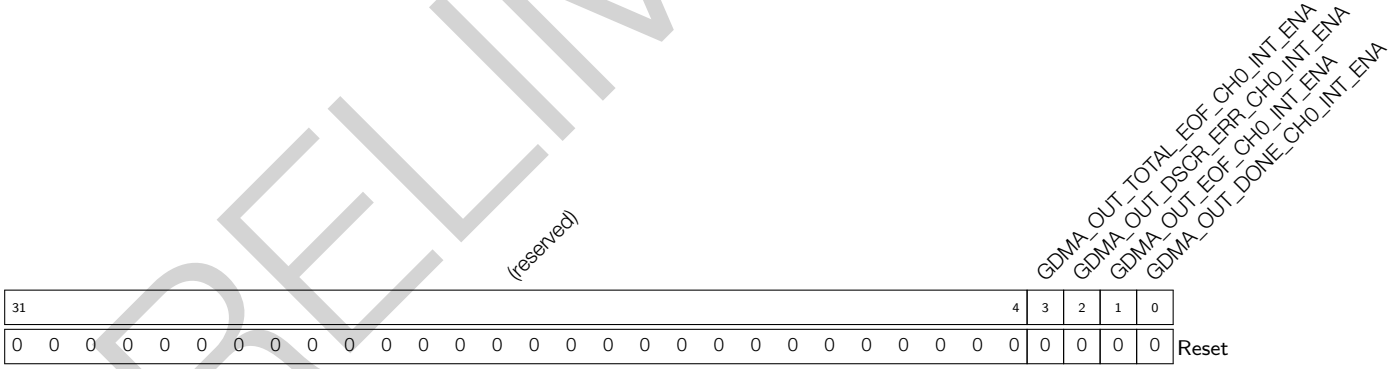
GDMA_OUT_DONE_CH*n*_INT_ST The raw interrupt status bit for the GDMA_OUT_DONE_CH_INT interrupt. (RO)

GDMA_OUT_EOF_CH*n*_INT_ST The raw interrupt status bit for the GDMA_OUT_EOF_CH_INT interrupt. (RO)

GDMA_OUT_DSCR_ERR_CH*n*_INT_ST The raw interrupt status bit for the GDMA_OUT_DSCR_ERR_CH_INT interrupt. (RO)

GDMA_OUT_TOTAL_EOF_CH*n*_INT_ST The raw interrupt status bit for the GDMA_OUT_TOTAL_EOF_CH_INT interrupt. (RO)

Register 2.17. GDMA_OUT_INT_ENA_CH*n*_REG (*n*: 0-4) (0x0070+192n*)**



GDMA_OUT_DONE_CH*n*_INT_ENA The interrupt enable bit for the GDMA_OUT_DONE_CH_INT interrupt. (R/W)

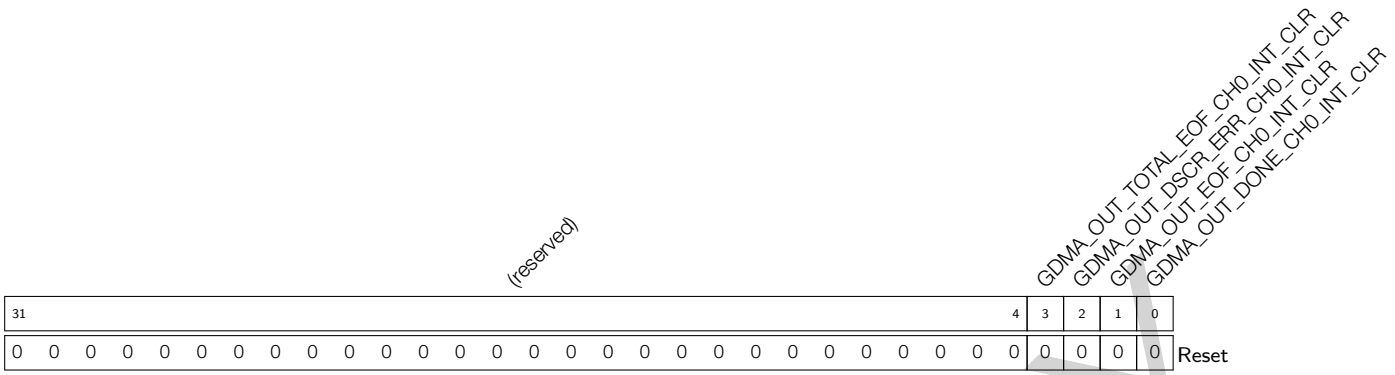
GDMA_OUT_EOF_CH*n*_INT_ENA The interrupt enable bit for the GDMA_OUT_EOF_CH_INT interrupt. (R/W)

GDMA_OUT_DSCR_ERR_CH*n*_INT_ENA The interrupt enable bit for the GDMA_OUT_DSCR_ERR_CH_INT interrupt. (R/W)

GDMA_OUT_TOTAL_EOF_CH*n*_INT_ENA The interrupt enable bit for the GDMA_OUT_TOTAL_EOF_CH_INT interrupt. (R/W)

PRELIMINARY

Register 2.18. GDMA_OUT_INT_CLR_CH*n*_REG (*n*: 0-4) (0x0074+192n*)**



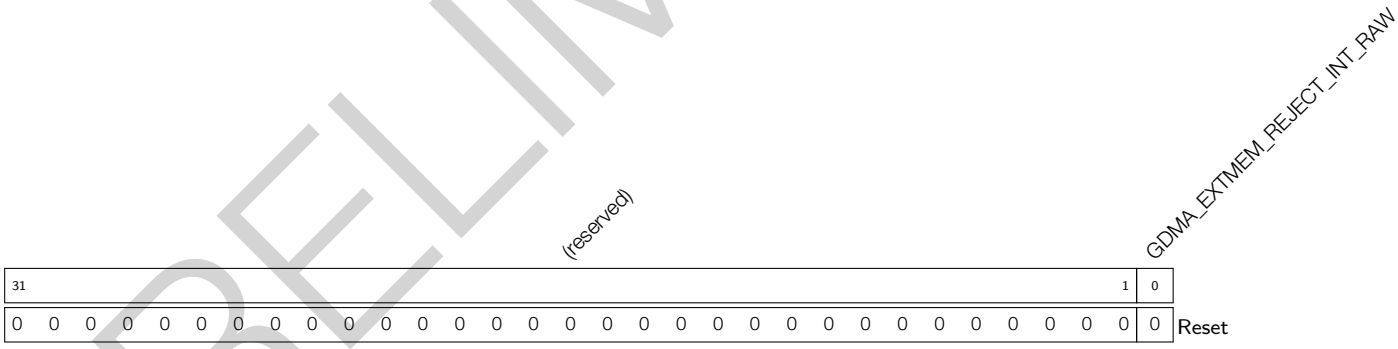
GDMA_OUT_DONE_CH*n*_INT_CLR Set this bit to clear the GDMA_OUT_DONE_CH_INT interrupt. (WT)

GDMA_OUT_EOF_CH*n*_INT_CLR Set this bit to clear the GDMA_OUT_EOF_CH_INT interrupt. (WT)

GDMA_OUT_DSCR_ERR_CH*n*_INT_CLR Set this bit to clear the GDMA_OUT_DSCR_ERR_CH_INT interrupt. (WT)

GDMA_OUT_TOTAL_EOF_CH*n*_INT_CLR Set this bit to clear the GDMA_OUT_TOTAL_EOF_CH_INT interrupt. (WT)

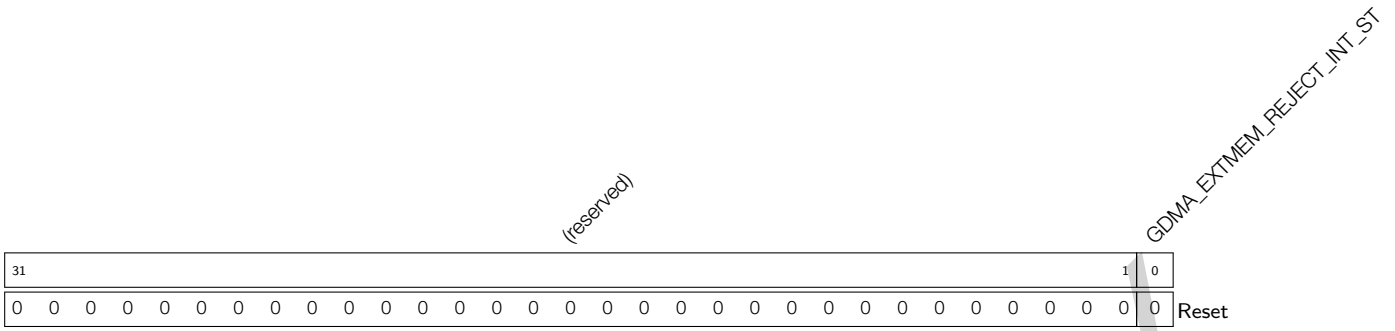
Register 2.19. GDMA_EXTMEM_REJECT_INT_RAW_REG (0x03FC)



GDMA_EXTMEM_REJECT_INT_RAW The raw interrupt bit turns to high level when accessing external RAM is rejected by permission control. (R/WTC/SS)

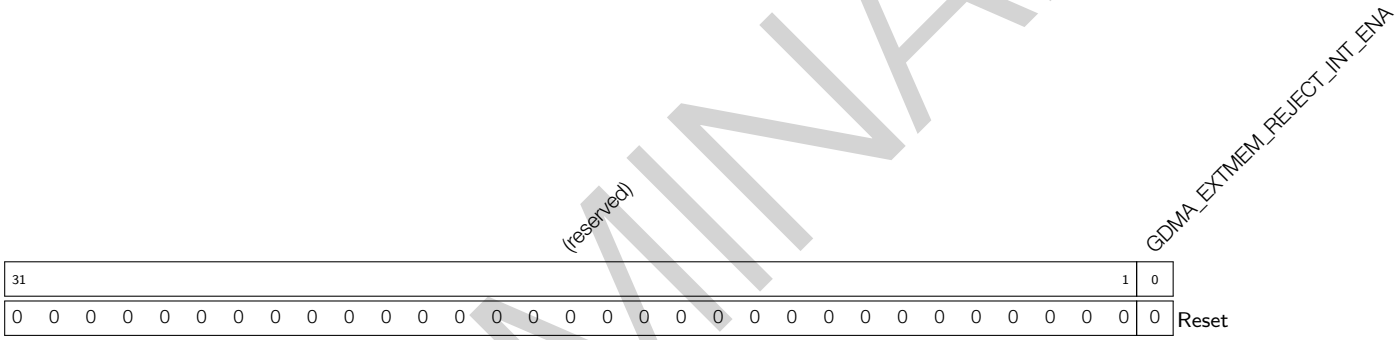
PRELIMINARY

Register 2.20. GDMA_EXTMEM_REJECT_INT_ST_REG (0x0400)



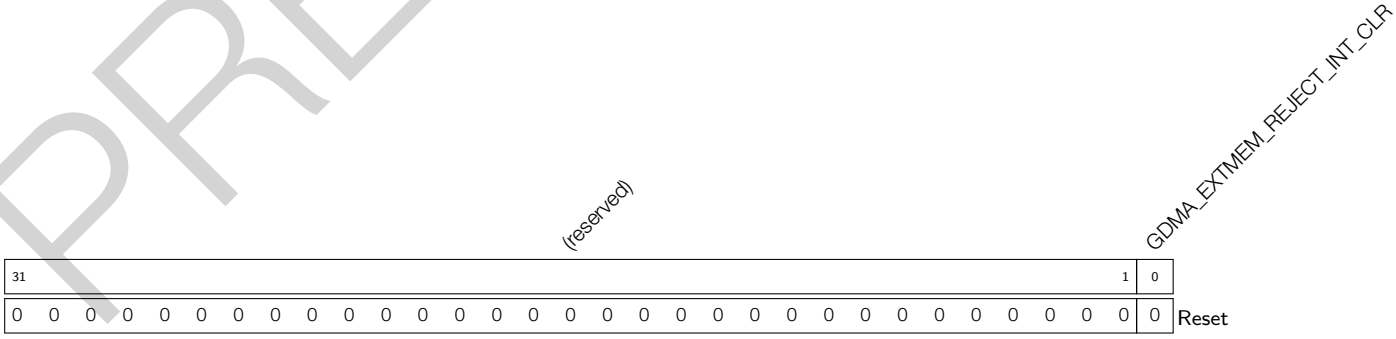
GDMA_EXTMEM_REJECT_INT_ST The raw interrupt status bit for the GDMA_EXTMEM_REJECT_INT interrupt. (RO)

Register 2.21. GDMA_EXTMEM_REJECT_INT_ENA_REG (0x0404)



GDMA_EXTMEM_REJECT_INT_ENA The interrupt enable bit for the GDMA_EXTMEM_REJECT_INT interrupt. (R/W)

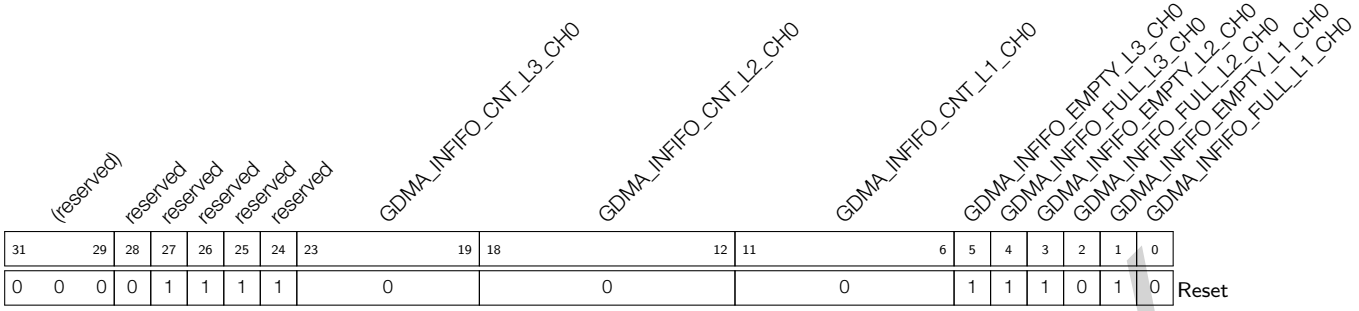
Register 2.22. GDMA_EXTMEM_REJECT_INT_CLR_REG (0x0408)



GDMA_EXTMEM_REJECT_INT_CLR Set this bit to clear the GDMA_EXTMEM_REJECT_INT interrupt. (WT)

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Register 2.23. GDMA_INFIFO_STATUS_CH*n*_REG (*n*: 0-4) (0x0018+192n*)**



GDMA_INFIFO_FULL_L1_CH*n* L1 RX FIFO full signal for RX channel 0. (RO)

GDMA_INFIFO_EMPTY_L1_CH*n* L1 RX FIFO empty signal for RX channel 0. (RO)

GDMA_INFIFO_FULL_L2_CH*n* L2 RX FIFO full signal for RX channel 0. (RO)

GDMA_INFIFO_EMPTY_L2_CH*n* L2 RX FIFO empty signal for RX channel 0. (RO)

GDMA_INFIFO_FULL_L3_CH*n* L3 RX FIFO full signal for RX channel 0. (RO)

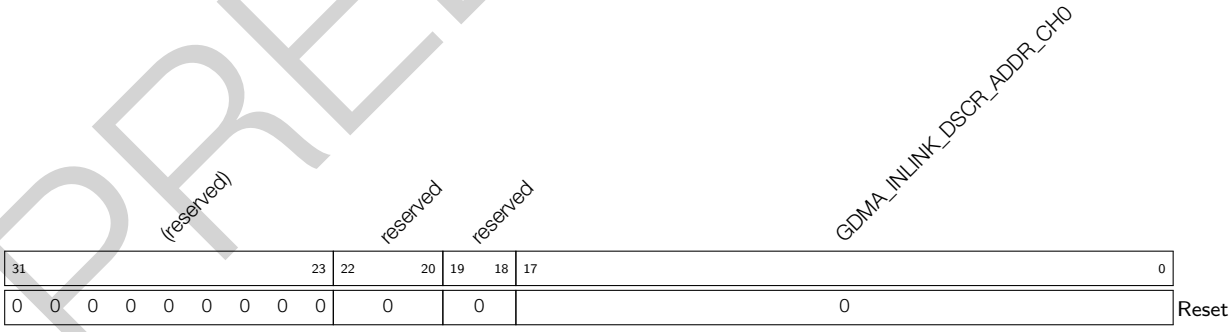
GDMA_INFIFO_EMPTY_L3_CH*n* L3 RX FIFO empty signal for RX channel 0. (RO)

GDMA_INFIFO_CNT_L1_CH*n* The register stores the byte number of the data in L1 RX FIFO for RX channel 0. (RO)

GDMA_INFIFO_CNT_L2_CH*n* The register stores the byte number of the data in L2 RX FIFO for RX channel 0. (RO)

GDMA_INFIFO_CNT_L3_CH*n* The register stores the byte number of the data in L3 RX FIFO for RX channel 0. (RO)

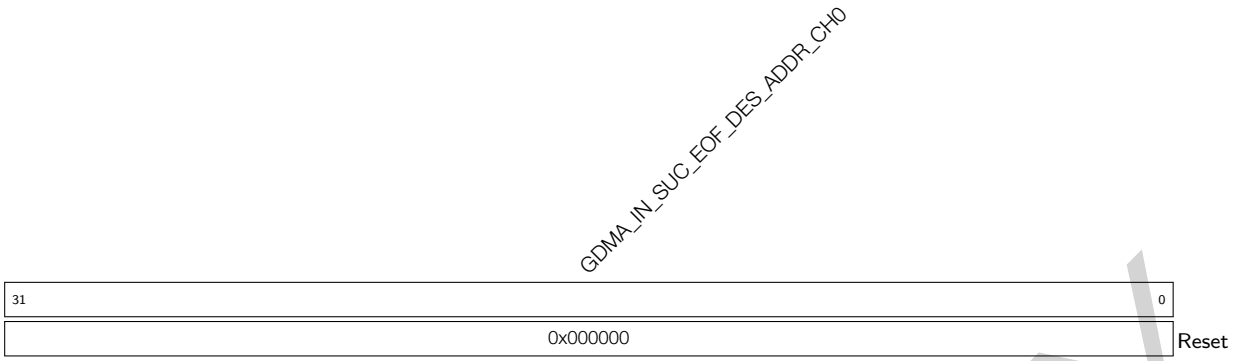
Register 2.24. GDMA_IN_STATE_CH*n*_REG (*n*: 0-4) (0x0024+192n*)**



GDMA_INLINK_DSCR_ADDR_CH*n* This register stores the current receive descriptor's address. (RO)

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Register 2.25. GDMA_IN_SUC_EOF_DES_ADDR_CH*n*_REG (*n*: 0-4) (0x0028+192n*)**



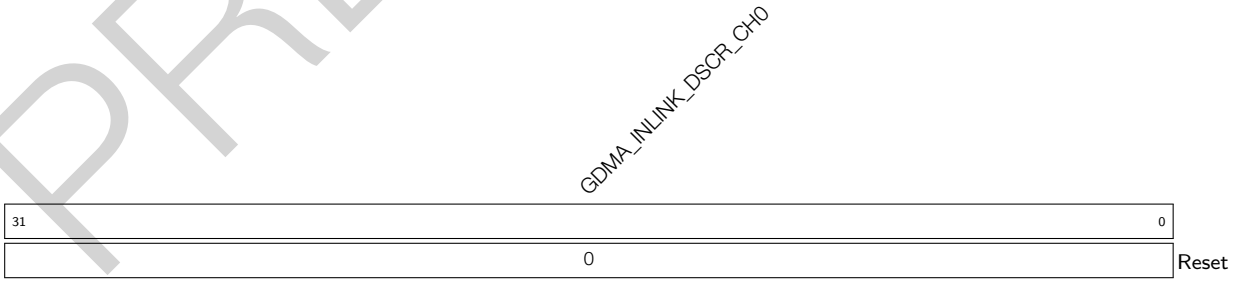
GDMA_IN_SUC_EOF_DES_ADDR_CH*n* This register stores the address of the receive descriptor when the EOF bit in this descriptor is 1. (RO)

Register 2.26. GDMA_IN_ERR_EOF_DES_ADDR_CH*n*_REG (*n*: 0-4) (0x002C+192n*)**



GDMA_IN_ERR_EOF_DES_ADDR_CH*n* This register stores the address of the receive descriptor when there are some errors in current receiving data. Only used when peripheral is UHCI0. (RO)

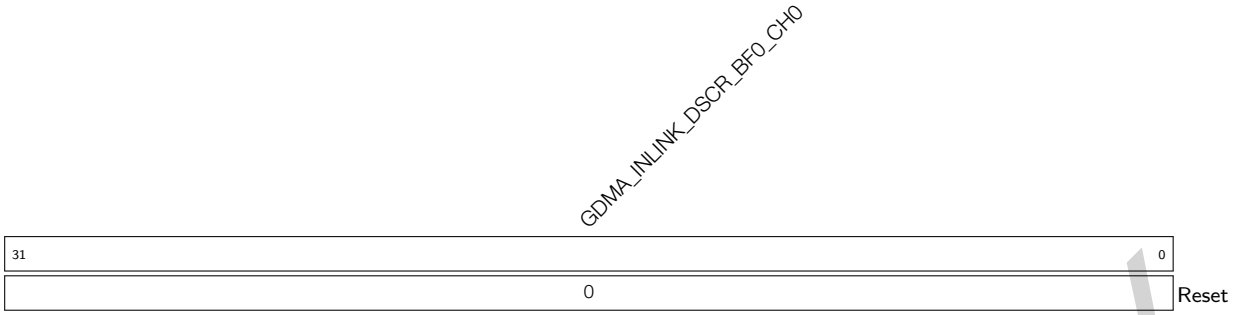
Register 2.27. GDMA_IN_DSCR_CH*n*_REG (*n*: 0-4) (0x0030+192n*)**



GDMA_INLINK_DSCR_CH*n* The address of the current receive descriptor x. (RO)

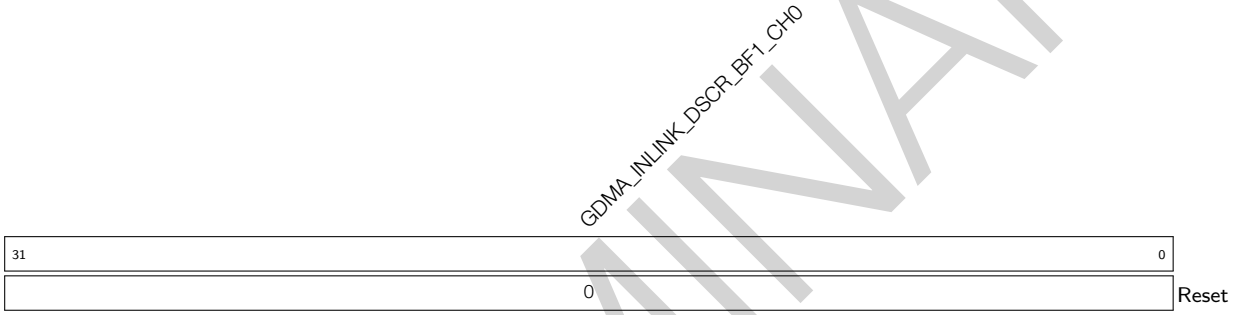
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Register 2.28. GDMA_IN_DSCR_BF0_CH*n*_REG (*n*: 0-4) (0x0034+192n*)**



GDMA_INLINK_DSCR_BF0_CH*n* The address of the last receive descriptor x-1. (RO)

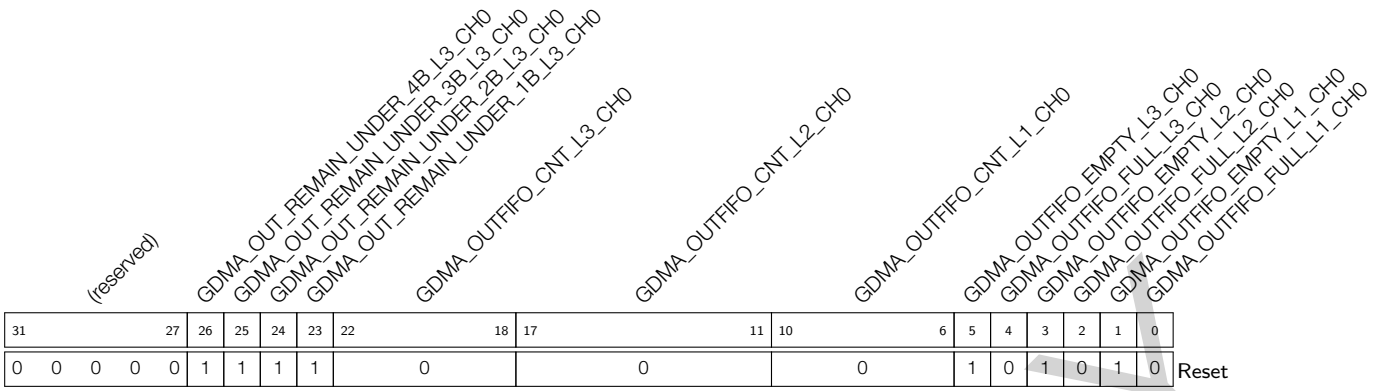
Register 2.29. GDMA_IN_DSCR_BF1_CH*n*_REG (*n*: 0-4) (0x0038+192n*)**



GDMA_INLINK_DSCR_BF1_CH*n* The address of the second-to-last receive descriptor x-2. (RO)

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Register 2.30. GDMA_OUTFIFO_STATUS_CH*n*_REG (*n*: 0-4) (0x0078+192n*)**



GDMA_OUTFIFO_FULL_L1_CH*n* L1 TX FIFO full signal for TX channel 0. (RO)

GDMA_OUTFIFO_EMPTY_L1_CH*n* L1 TX FIFO empty signal for TX channel 0. (RO)

GDMA_OUTFIFO_FULL_L2_CH*n* L2 TX FIFO full signal for TX channel 0. (RO)

GDMA_OUTFIFO_EMPTY_L2_CH*n* L2 TX FIFO empty signal for TX channel 0. (RO)

GDMA_OUTFIFO_FULL_L3_CH*n* L3 TX FIFO full signal for TX channel 0. (RO)

GDMA_OUTFIFO_EMPTY_L3_CH*n* L3 TX FIFO empty signal for TX channel 0. (RO)

GDMA_OUTFIFO_CNT_L1_CH*n* The register stores the byte number of the data in L1 TX FIFO for TX channel 0. (RO)

GDMA_OUTFIFO_CNT_L2_CH*n* The register stores the byte number of the data in L2 TX FIFO for TX channel 0. (RO)

GDMA_OUTFIFO_CNT_L3_CH*n* The register stores the byte number of the data in L3 TX FIFO for TX channel 0. (RO)

GDMA_OUT_REMAIN_UNDER_1B_L3_CH*n* Reserved. (RO)

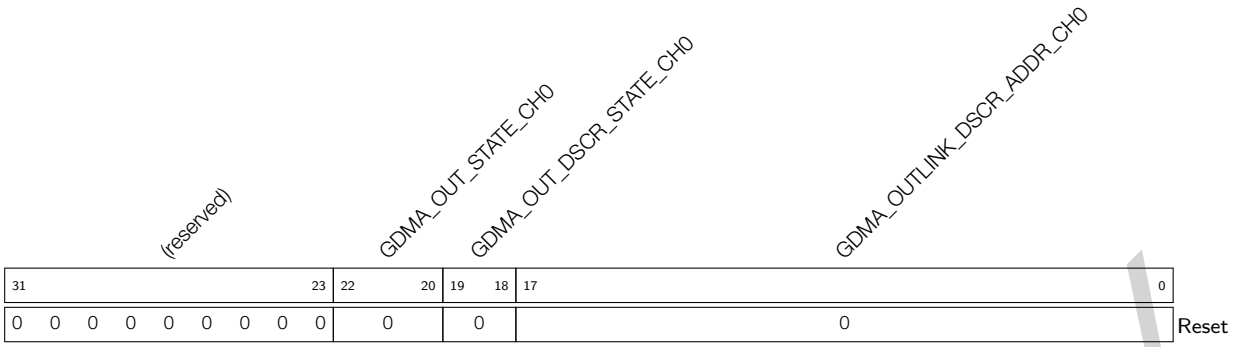
GDMA_OUT_REMAIN_UNDER_2B_L3_CH*n* Reserved. (RO)

GDMA_OUT_REMAIN_UNDER_3B_L3_CH*n* Reserved. (RO)

GDMA_OUT_REMAIN_UNDER_4B_L3_CH*n* Reserved. (RO)

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Register 2.31. GDMA_OUT_STATE_CH*n*_REG (*n*: 0-4) (0x0084+192n*)**

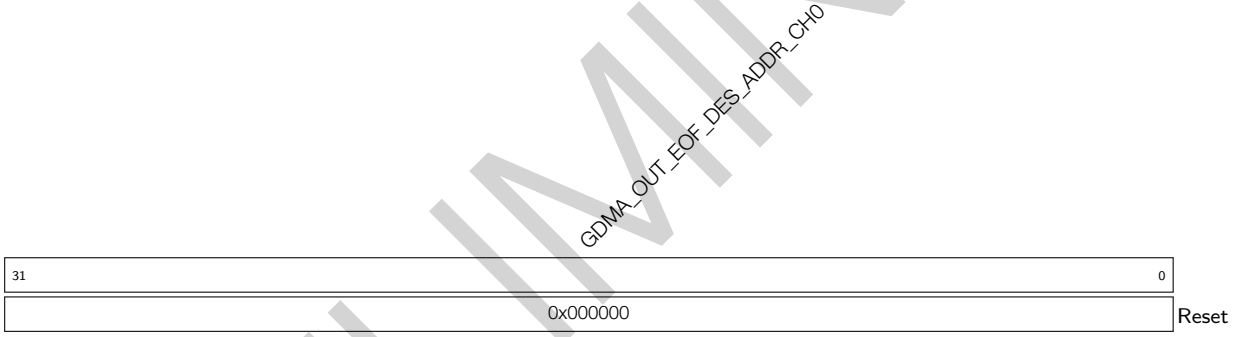


GDMA_OUTLINK_DSCR_ADDR_CH*n* This register stores the current transmit descriptor's address. (RO)

GDMA_OUT_DSCR_STATE_CH*n* Reserved. (RO)

GDMA_OUT_STATE_CH*n* Reserved. (RO)

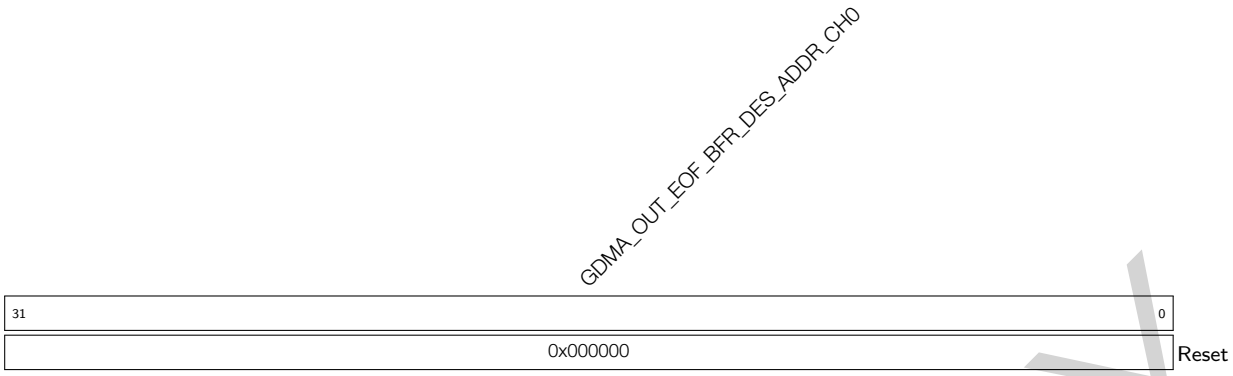
Register 2.32. GDMA_OUT_EOF_DES_ADDR_CH*n*_REG (*n*: 0-4) (0x0088+192n*)**



GDMA_OUT_EOF_DES_ADDR_CH*n* This register stores the address of the transmit descriptor when the EOF bit in this descriptor is 1. (RO)

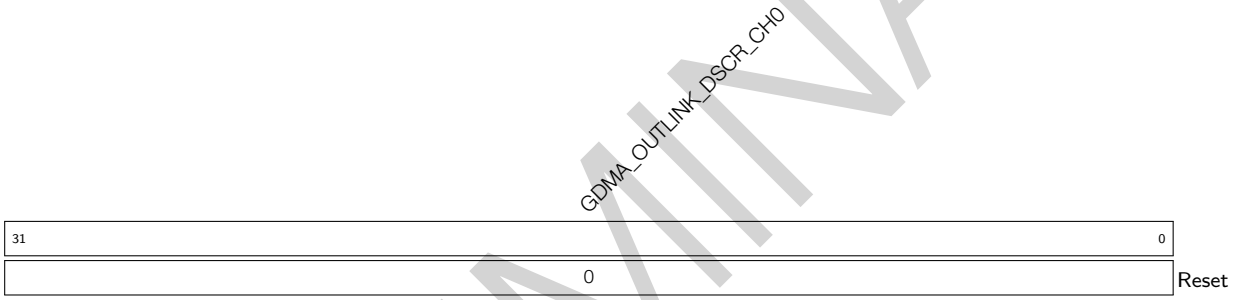
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Register 2.33. GDMA_OUT_EOF_BFR_DES_ADDR_CH*n*_REG (*n*: 0-4) (0x008C+192n*)**



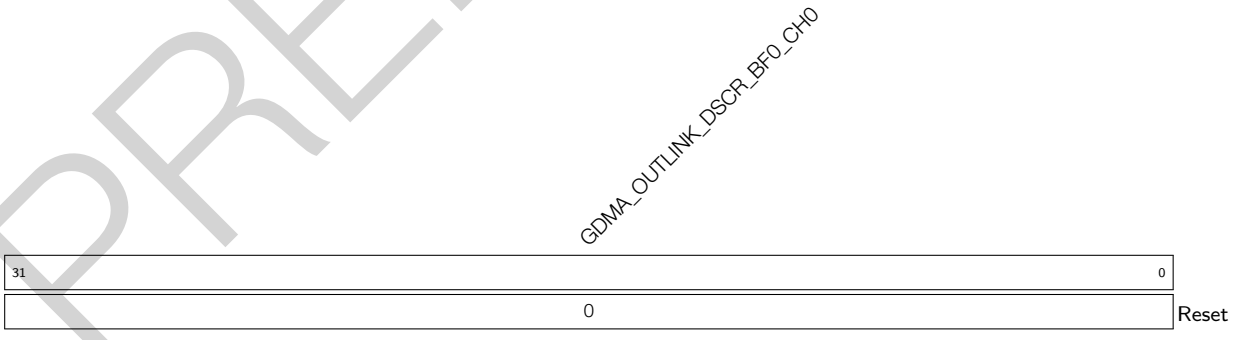
GDMA_OUT_EOF_BFR_DES_ADDR_CH*n* This register stores the address of the transmit descriptor before the last transmit descriptor. (RO)

Register 2.34. GDMA_OUT_DSCR_CH*n*_REG (*n*: 0-4) (0x0090+192n*)**



GDMA_OUTLINK_DSCR_CH*n* The address of the current transmit descriptor y. (RO)

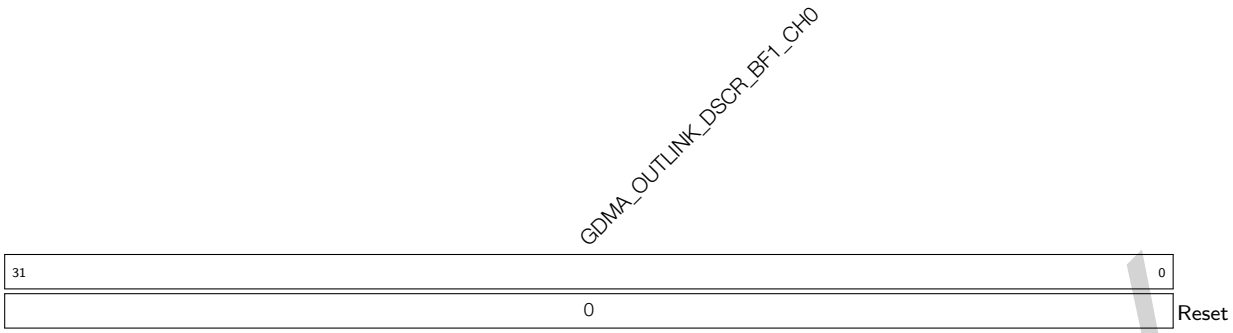
Register 2.35. GDMA_OUT_DSCR_BF0_CH*n*_REG (*n*: 0-4) (0x0094+192n*)**



GDMA_OUTLINK_DSCR_BF0_CH*n* The address of the last transmit descriptor y-1. (RO)

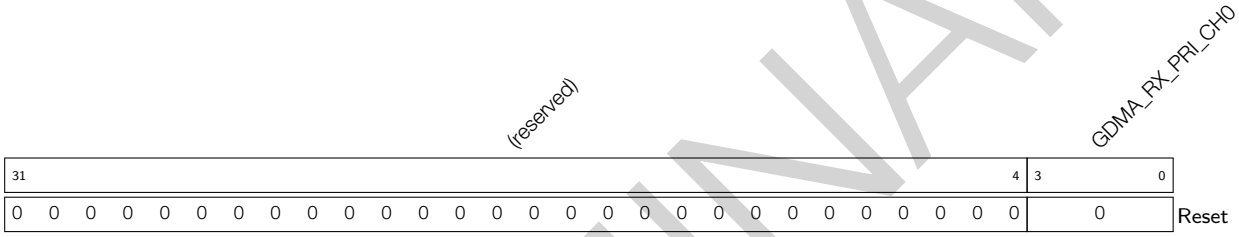
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Register 2.36. GDMA_OUT_DSCR_BF1_CH*n*_REG (*n*: 0-4) (0x0098+192n*)**



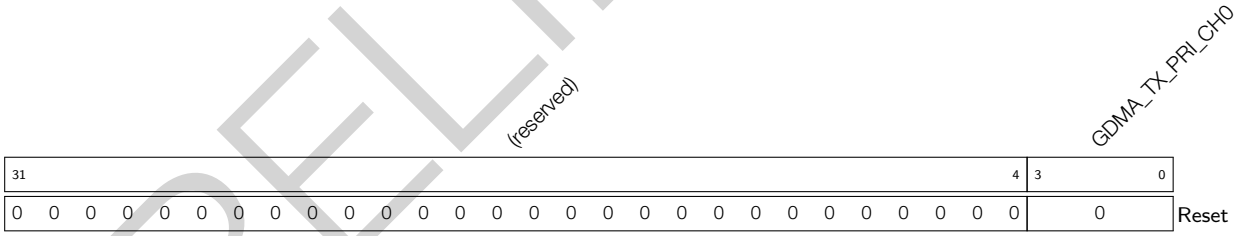
GDMA_OUTLINK_DSCR_BF1_CH*n* The address of the second-to-last receive descriptor x-2. (RO)

Register 2.37. GDMA_IN_PRI_CH*n*_REG (*n*: 0-4) (0x0044+192n*)**



GDMA_RX_PRI_CH*n* The priority of RX channel 0. The larger the value, the higher the priority. (R/W)

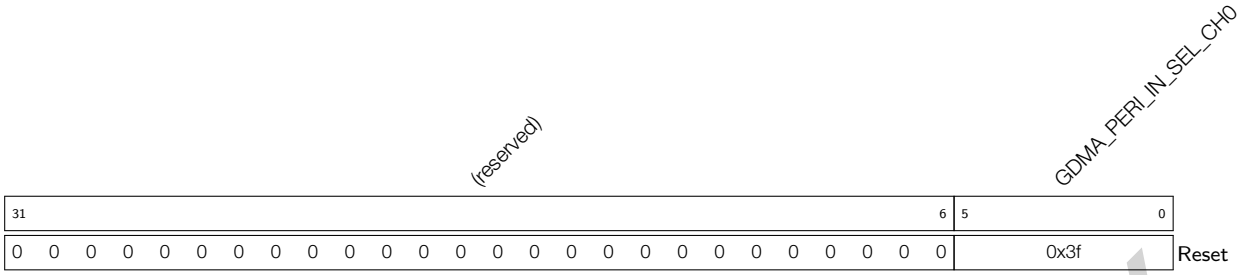
Register 2.38. GDMA_OUT_PRI_CH*n*_REG (*n*: 0-4) (0x00A4+192n*)**



GDMA_TX_PRI_CH*n* The priority of TX channel 0. The larger the value, the higher the priority. (R/W)

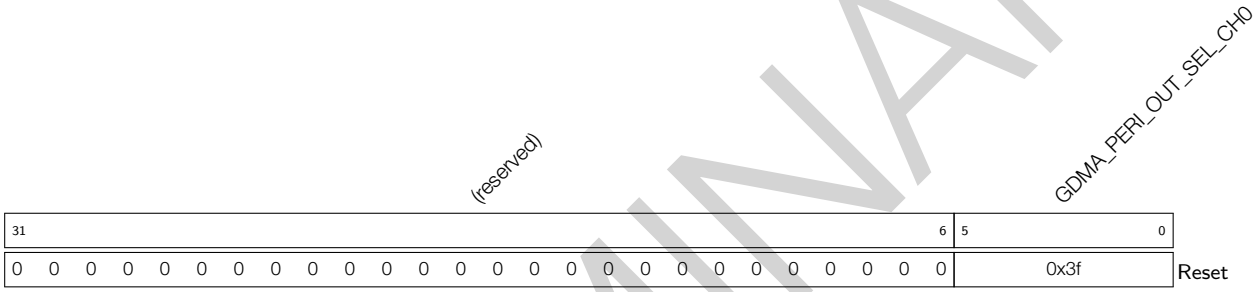
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Register 2.39. GDMA_IN_PERI_SEL_CH*n*_REG (*n*: 0-4) (0x0048+192n*)**



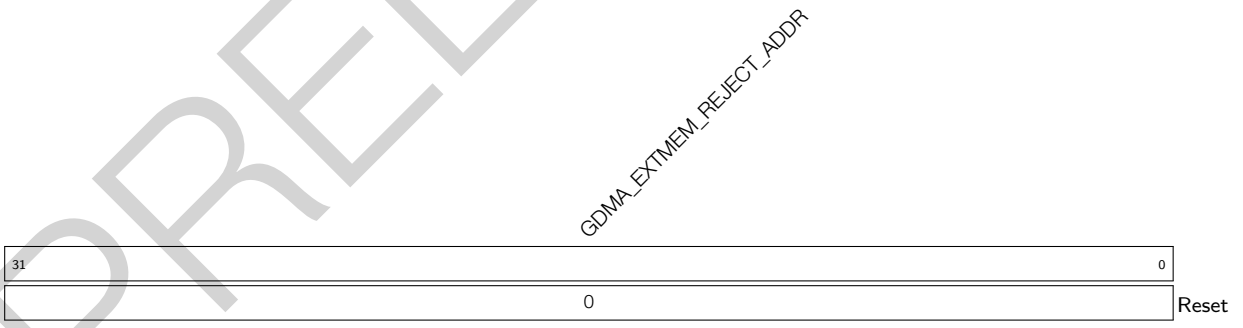
GDMA_PERI_IN_SEL_CH*n* This register is used to select peripheral for RX channel 0. 0: SPI2; 1: SPI3; 2: UHCI0; 3: I2S0; 4: I2S1; 5: LCD_CAM; 6: AES; 7: SHA; 8: ADC_DAC; 9: RMT. (R/W)

Register 2.40. GDMA_OUT_PERI_SEL_CH*n*_REG (*n*: 0-4) (0x00A8+192n*)**



GDMA_PERI_OUT_SEL_CH*n* This register is used to select peripheral for TX channel 0. 0: SPI2; 1: SPI3; 2: UHCI0; 3: I2S0; 4: I2S1; 5: LCD_CAM; 6: AES; 7: SHA; 8: ADC_DAC; 9: RMT. (R/W)

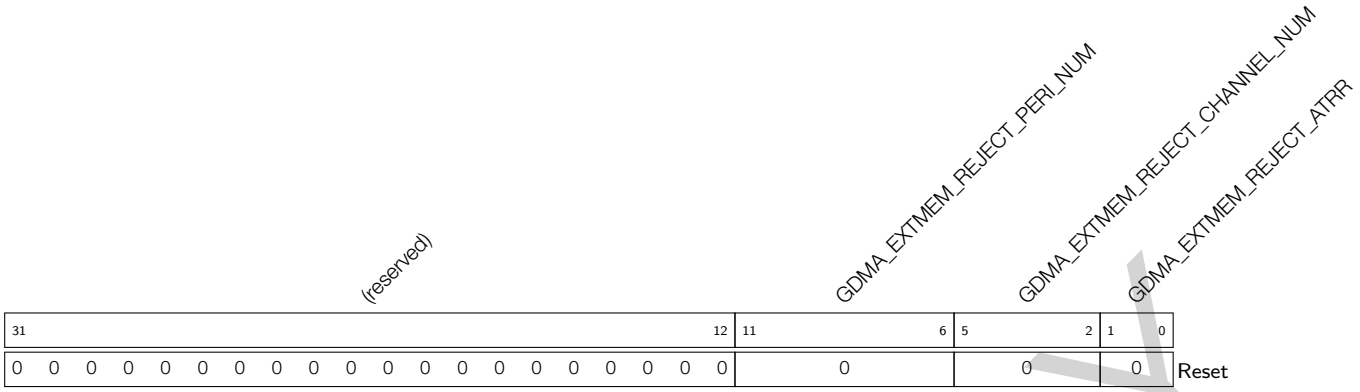
Register 2.41. GDMA_EXTMEM_REJECT_ADDR_REG (0x03F4)



GDMA_EXTMEM_REJECT_ADDR This register store the first address rejected by permission control when accessing external RAM. (RO)

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Register 2.42. GDMA_EXTMEM_REJECT_ST_REG (0x03F8)

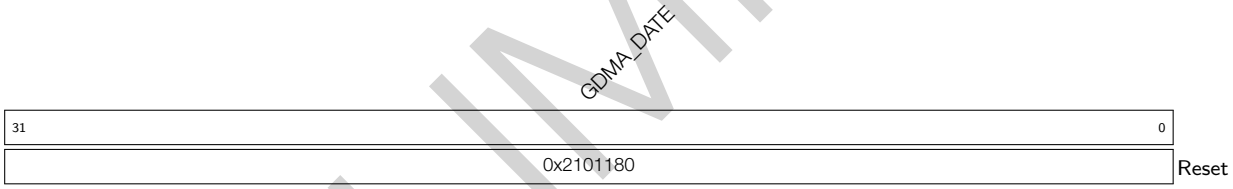


GDMA_EXTMEM_REJECT_ATRR Read or write attribute of the rejected access. Bit 0: if this bit is 1, the rejected access is READ. Bit 1: if this bit is 1, the rejected access is WRITE. (RO)

GDMA_EXTMEM_REJECT_CHANNEL_NUM This field indicates the channel used for the rejected access. (RO)

GDMA_EXTMEM_REJECT_PERI_NUM This bit indicates the peripheral whose access was rejected. (RO)

Register 2.43. GDMA_DATE_REG (0x040C)



GDMA_DATE This is the version control register. (R/W)

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3 System and Memory

3.1 Overview

The ESP32-S3 is a dual-core system with two Harvard Architecture Xtensa® LX7 CPUs. All internal memory, external memory, and peripherals are located on the CPU buses.

3.2 Features

- **Address Space**
  - 848 KB of internal memory address space accessed from the instruction bus
  - 560 KB of internal memory address space accessed from the data bus
  - 836 KB of peripheral address space
  - 32 MB of external memory virtual address space accessed from the instruction bus
  - 32 MB external memory virtual address space accessed from the data bus
  - 480 KB of internal DMA address space
  - 32 MB of external DMA address space
- **Internal Memory**
  - 384 KB Internal ROM
  - 512 KB Internal SRAM
  - 8 KB RTC FAST Memory
  - 8 KB RTC SLOW Memory
- **External Memory**
  - Supports up to 1 GB external flash
  - Supports up to 1 GB external RAM
- **Peripheral Space**
  - 45 modules/peripherals in total
- **GDMA**
  - 11 GDMA-supported modules/peripherals

Figure 3-1 illustrates the system structure and address mapping.

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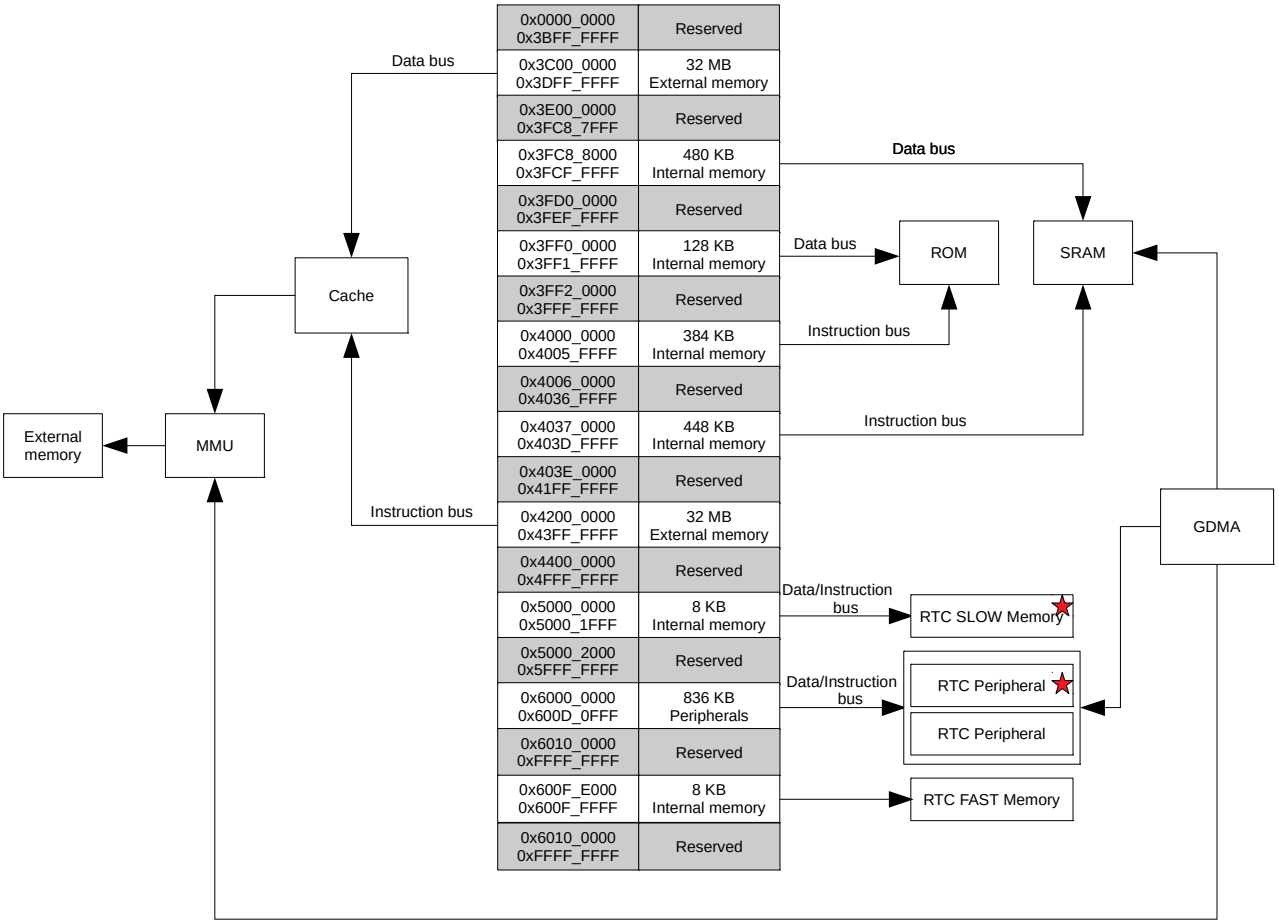


Figure 3-1. System Structure and Address Mapping

Note:

- The address space with gray background is not available to users.
- The memory or peripheral marked with a red pentagram can be accessed by the ULP co-processor.
- The range of addresses available in the address space may be larger than the actual available memory of a particular type.

3.3 Functional Description

3.3.1 Address Mapping

The system contains two Harvard Architecture Xtensa® LX7 CPUs, and both can access the same range of address space.

Addresses below 0x4000_0000 are accessed using the data bus. Addresses in the range of 0x4000_0000 ~ 0x4FFF_FFFF are accessed using the instruction bus. Addresses over and including 0x5000_0000 are shared by both data bus and instruction bus.

Both data bus and instruction bus are little-endian. The CPU can access data via the data bus using single-byte, double-byte, 4-byte and 16-byte alignment. The CPU can also access data via the instruction bus, but only in

4-byte aligned manner; non-aligned data access will cause a CPU exception.

The CPU can:

- directly access the internal memory via both data bus and instruction bus;
- directly access the external memory which is mapped into the address space via cache;
- directly access modules/peripherals via data bus.

Figure 3-1 lists the address ranges on the data bus and instruction bus and their corresponding target memory.

Some internal and external memory can be accessed via both data bus and instruction bus. In such cases, the CPU can access the same memory using multiple addresses.

3.3.2 Internal Memory

The ESP32-S3 consists of the following three types of internal memory:

- Internal ROM (384 KB): The internal ROM is a read-only memory and cannot be programmed. Internal ROM contains the ROM code (software instructions and some software read-only data) of some low level system software.
- Internal SRAM (512 KB): The Internal Static RAM (SRAM) is a volatile memory that can be quickly accessed by the CPU (generally within a single CPU clock cycle).
  - A part of the SRAM can be configured to operate as a cache for external memory access, which cannot be accessed by CPU in such case.
  - Some parts of the SRAM can only be accessed via the CPU's instruction bus.
  - Some parts of the SRAM can only be accessed via the CPU's data bus.
  - Some parts of the SRAM can be accessed via both the CPU's instruction bus and the CPU's data bus.
- RTC Memory (16 KB): The RTC (Real Time Clock) memory implemented as Static RAM (SRAM) and thus is volatile. However, RTC memory has the added feature of being persistent throughout deep sleep (i.e., the RTC memory retains its values throughout deep sleep).
  - RTC FAST Memory (8 KB): RTC FAST memory can only be accessed by the CPU, and cannot be accessed by the ULP co-processor. It is generally used to store instructions and data that needs to persist across a deep sleep.
  - RTC SLOW Memory (8 KB): The RTC SLOW memory can be accessed by both the CPU and the ULP co-processor, and thus is generally used to store instructions and share data between the CPU and the ULP co-processor.

Based on the three different types of internal memory described above, the internal memory of the ESP32-S3 is split into four segments: Internal ROM (384 KB), Internal SRAM (512 KB), RTC FAST Memory (8 KB) and RTC SLOW Memory (8 KB). However, within each segment, there may be different bus access restrictions (e.g., some parts of the segment may only be accessible by the CPU's instruction bus). Therefore, some segments are also further divided down into parts. Table 3-1 describes each part of internal memory and their address ranges on the data bus and/or instruction bus.

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Table 3-1. Internal Memory Address Mapping

Bus Type	Boundary Address		Size (KB)	Target
	Low Address	High Address		
Data bus	0x3FF0_0000	0x3FF1_FFFF	128	Internal ROM 1
	0x3FC8_0000	0x3FCE_FFFF	416	Internal SRAM 1
	0x3FCF_0000	0x3FCF_FFFF	64	Internal SRAM 2
Instruction bus	0x4000_0000	0x4003_FFFF	256	Internal ROM 0
	0x4004_0000	0x4005_FFFF	128	Internal ROM 1
	0x4037_0000	0x4037_7FFF	32	Internal SRAM 0
	0x4037_8000	0x403D_FFFF	416	Internal SRAM 1
Data/Instruction bus	0x5000_0000	0x5000_1FFF	8	RTC SLOW Memory
	0x600F_E000	0x600F_FFFF	8	RTC FAST Memory

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Note:

All of the internal memories are managed by Permission Control module. An internal memory can only be accessed when it is allowed by Permission Control, then the internal memory can be available to the CPU. For more information about Permission Control, please refer to Chapter 13 *Permission Control (PMS)*.

1. Internal ROM 0

Internal ROM 0 is a 256 KB, read-only memory space, addressed by the CPU only through the instruction bus, as shown in Table 3-1.

2. Internal ROM 1

Internal ROM 1 is a 128 KB, read-only memory space, addressed by the CPU through the instruction bus via 0x4004_0000 ~ 0x4005_FFFF or through the data bus via 0x3FF0_0000 ~ 0x3FF1_FFFF in the same order, as shown in Table 3-1.

This means, for example, address 0x4005_0000 and 0x3FF0_0000 correspond to the same word, 0x4005_0004 and 0x3FF0_0004 correspond to the same word, 0x4005_0008 and 0x3FF0_0008 correspond to the same word, etc (same below).

3. Internal SRAM 0

Internal SRAM 0 is a 32 KB, read-and-write memory space, addressed by the CPU through the instruction bus, as shown in Table 3-1.

A 16 KB or the total 32 KB of this memory space can be configured as instruction cache (ICache) to store instructions or read-only data of the external memory. In this case, the occupied memory space cannot be accessed by the CPU, while the remaining can still can be accessed by the CPU.

4. Internal SRAM 1

Internal SRAM 1 is a 416 KB, read-and-write memory space, addressed by the CPU through the data bus or instruction bus in the same order, as shown in Table 3-1.

The total 416 KB memory space comprises multiple 8 KB and 16 KB memory (sub-memory) blocks. A memory block (up to 16 KB) can be used as a Trace Memory, in which case this block can still be accessed by the CPU.

5. Internal SRAM 2

Internal SRAM 2 is a 64 KB, read-and-write memory space, addressed by the CPU through the data bus, as shown in Table 3-1.

A 32 KB or the total 64 KB can be configured as data cache (DCache) to cache data of the external memory. The space used as DCache cannot be accessed by the CPU, while the remaining space can still be accessed by the CPU.

6. RTC FAST Memory

RTC FAST Memory is a 8 KB, read-and-write SRAM, addressed by the CPU through the data/instruction bus via the shared address 0x600F_E000 ~ 0x600F_FFFF, as described in Table 3-1.

7. RTC SLOW Memory

RTC SLOW Memory is a 8 KB, read-and-write SRAM, addressed by the CPU through the data/instruction bus via shared address 0x5000_E000 ~ 0x5001_FFFF, as described in Table 3-1.

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RTC SLOW Memory can also be used as a peripheral addressable to the CPU via 0x6002_1000 ~ 0x6002_2FFF.

3.3.3 External Memory

ESP32-S3 supports SPI, Dual SPI, Quad SPI, Octal SPI, QPI, and OPI interfaces that allow connection to external flash and RAM. It also supports hardware encryption and decryption based on XTS_AES algorithm to protect users' programs and data in the external flash and RAM.

3.3.3.1 External Memory Address Mapping

The CPU accesses the external memory via the cache. According to information inside the MMU (Memory Management Unit), the cache maps the CPU's instruction/data bus address into a physical address of the external flash and RAM. Due to this address mapping, ESP32-S3 can address up to 1 GB external flash and 1 GB external RAM.

Using the cache, ESP32-S3 is able to support the following address space mappings at a time:

- Up to 32 MB instruction bus address space can be mapped to the external flash or RAM as individual 64 KB blocks via the ICache. 4-byte aligned reads and fetches are supported.
- Up to 32 MB data bus address space can be mapped to the external RAM as individual 64 KB blocks via the DCache. Single-byte, double-byte, 4-byte, 16-byte aligned reads and writes are supported. This address space can also be mapped to the external flash or RAM for read operations only.

Table 3-2 lists the mapping between the cache and the corresponding address ranges on the data bus and instruction bus.

Table 3-2. External Memory Address Mapping

Bus Type	Boundary Address		Size (MB)	Target
	Low Address	High Address		
Data bus	0x3C00_0000	0x3DFF_FFFF	32	DCache
Instruction bus	0x4200_0000	0x43FF_FFFF	32	ICache

Note:

Only if the CPU obtains permission for accessing the external memory, can it be responded for memory access. For more detailed information about permission control, please refer to Chapter 13 *Permission Control (PMS)*.

3.3.3.2 Cache

As shown in Figure 3-2, ESP32-S3 has a dual-core-shared ICache and DCache structure, which allows prompt response upon simultaneous requests from the instruction bus and data bus. Some internal memory space can be used as cache (see Internal SRAM 0 and Internal SRAM 2 in Section 3.3.2).

When the instruction bus of two cores initiate a request on ICache simultaneously, the arbiter determines which core gets the access to the ICache first; when the data bus of two cores initiate a request on DCache simultaneously, the arbiter determines which gets the access to the DCache first. When a cache miss occurs, the cache controller will initiate a request to the external memory. When ICache and DCache initiate requests on the

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external memory simultaneously, the arbiter determines which gets the access to the external memory first. The size of ICache can be configured to 16 KB or 32 KB, while its block size can be configured to 16 B or 32 B. When an ICache is configured to 32 KB, its block cannot be 16 B. The size of DCache can be configured to 32 KB or 64 KB, while its block size can be configured to 16 B, 32 B or 64 B. When a DCache is configured to 64 KB, its block cannot be 16 B.

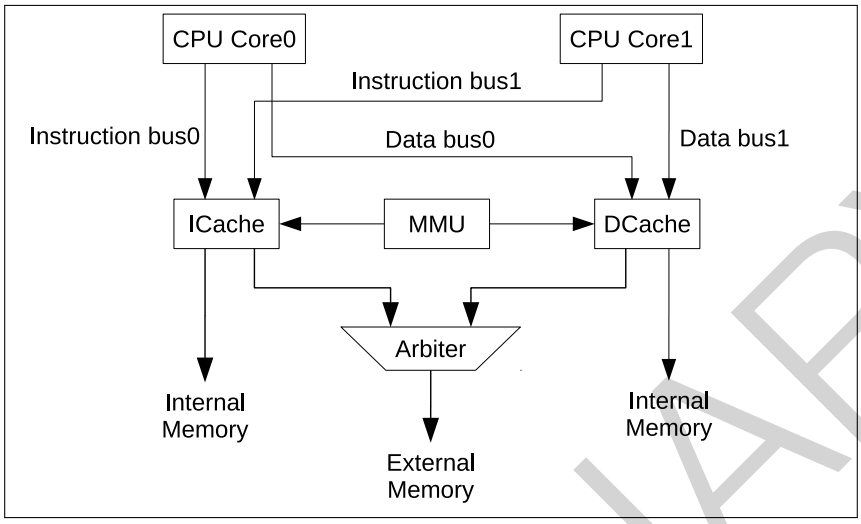


Figure 3-2. Cache Structure

3.3.3.3 Cache Operations

ESP32-S3 caches support the following operations:

1. **Write-Back**: This operation is used to clear the dirty bits in dirty blocks and update the new data to the external memory. After the write-back operation finished, both the external memory and the cache are bearing the new data. The CPU can then read/write the data directly from the cache. Only DCache has this function.

   If the data in the cache is newer than the one stored in the external memory, then the new data will be considered as a dirty block. The cache tracks these dirty blocks through their dirty bits. When the dirty bits of a data are cleared, the cache will consider the data as new.

2. **Clean**: This operation is used to clear dirty bits in the dirty block, without updating data to the external memory. After the clean operation finish, there will still be old data stored in the external memory, while the cache keeps the new one (but the cache does not know about this). The CPU can then read/write the data directly from the cache. Only DCache has this function.

3. **Invalidate**: This operation is used to remove valid data in the cache. Even if the data is a dirty block mentioned above, it will not be updated to the external memory. But for the non-dirty data, it will be only stored in the external memory after this operation. The CPU needs to access the external memory in order to read/write this data. As for the dirty blocks, they will be totally lost with only old data in the external memory after this operation. There are two types of invalidate operation: automatic invalidation (Auto-Invalidate) and manual invalidation (Manual-Invalidate). Manual-Invalidate is performed only on data in the specified area in the cache, while Auto-Invalidate is performed on all data in the cache. Both ICache and DCache have this function.

4. **Preload**: This operation is to load instructions and data into the cache in advance. The minimum unit of

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preload-operation is one block. There are two types of preload-operation: manual preload (Manual-Preload) and automatic preload (Auto-Preload). Manual-Preload means that the hardware prefetches a piece of continuous data according to the virtual address specified by the software. Auto-Preload means the hardware prefetches a piece of continuous data according to the current address where the cache hits or misses (depending on configuration). Both ICache and DCache have this function.

5. **Lock/Unlock**: The lock operation is used to prevent the data in the cache from being easily replaced. There are two types of lock: prelock and manual lock. When prelock is enabled, the cache locks the data in the specified area when filling the missing data to cache memory, while the data outside the specified area will not be locked. When manual lock is enabled, the cache checks the data that is already in the cache memory and locks the data only if it falls in the specified area, and leaves the data outside the specified area unlocked. When there are missing data, the cache will replace the data in the unlocked way first, so the data in the locked way is always stored in the cache and will not be replaced. But when all ways within the cache are locked, the cache will replace data, as if it was not locked. Unlocking is the reverse of locking, except that it only can be done manually. Both ICache and DCache have this function.

   Please note that the writing-back, cleaning and Manual-Invalidate operations will only work on the unlocked data. If you expect to perform such operations on the locked data, please unlock them first.

3.3.4 GDMA Address Space

The GDMA (General Direct Memory Access) peripheral in ESP32-S3 can provide DMA (Direct Memory Access) services including:

- Data transfers between different locations of internal memory;
- Data transfers between internal memory and external memory;
- Data transfers between different locations of external memory.

GDMA uses the same addresses as the CPU's data bus to access Internal SRAM 1 and Internal SRAM 2. Specifically, GDMA uses address range 0x3FC8_8000 ~ 0x3FCE_FFFF to access Internal SRAM 1 and 0x3FCF_0000 ~ 0x3FCF_FFFF to access Internal SRAM 2. Note that GDMA cannot access the internal memory occupied by cache.

In addition, GDMA can access the external memory (only RAM) via the same address as CPU accessing DCache (0x3C00_0000 ~ 0x3DFF_FFFF). When DCache and GDMA access the external memory simultaneously, the software needs to make sure the data is consistent.

Besides, some peripherals/modules of the ESP32-S3 can work together with GDMA. In these cases, GDMA can provide the following powerful services for them:

- Data transfers between modules/peripherals and internal memory;
- Data transfers between modules/peripherals and external memory.

There are 11 peripherals/modules that can work together with GDMA. As shown in Figure 3-3, these 11 vertical lines in turn correspond to these 11 peripherals/modules with GDMA function, the horizontal line represents a certain channel of GDMA (can be any channel), and the intersection of the vertical line and the horizontal line indicates that a peripheral/module has the ability to access the corresponding channel of GDMA. If there are multiple intersections on the same line, it means that these peripherals/modules cannot enable the GDMA function at the same time.

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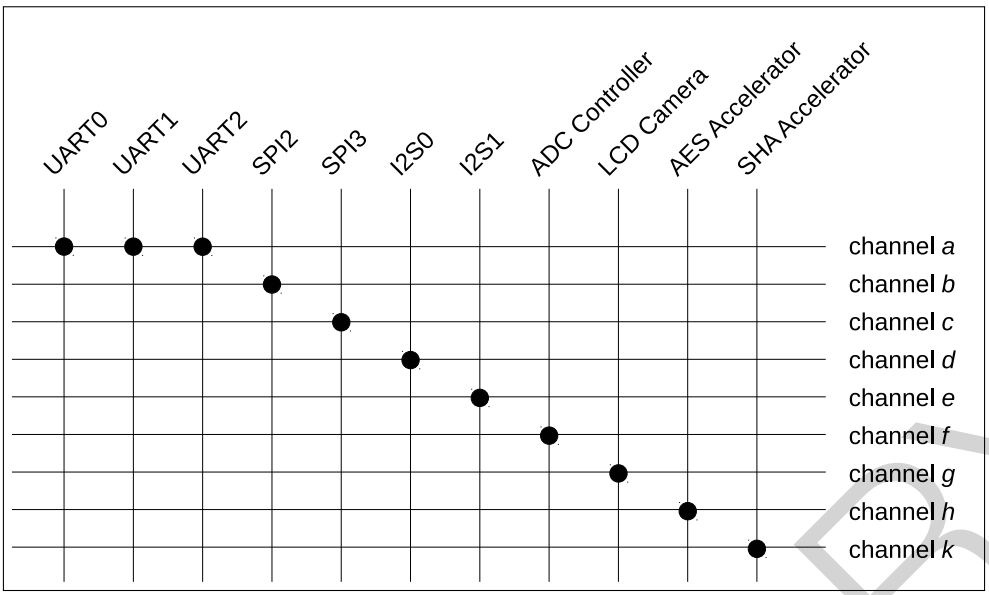


Figure 3-3. Peripherals/modules that can work with GDMA

These peripherals/modules can access any memory available to GDMA. For more information, please refer to Chapter 2 *GDMA Controller (GDMA)*.

Note:

When accessing a memory via GDMA, a corresponding access permission is needed, otherwise this access may fail. For more information about permission control, please refer to Chapter 13 *Permission Control (PMS)*.

3.3.5 Modules/Peripherals

The CPU can access modules/peripherals via 0x6000_0000 ~ 0x600D_0FFF shared by the data/instruction bus.

3.3.5.1 Module/Peripheral Address Mapping

Table 3-3 lists all the modules/peripherals and their respective address ranges. Note that the address space of specific modules/peripherals is defined by "Boundary Address" (including both Low Address and High Address).

Table 3-3. Module/Peripheral Address Mapping

Target	Boundary Address		Size (KB)	Notes
	Low Address	High Address		
UART Controller 0	0x6000_0000	0x6000_0FFF	4	
Reserved	0x6000_1000	0x6000_1FFF		
SPI Controller 1	0x6000_2000	0x6000_2FFF	4	
SPI Controller 0	0x6000_3000	0x6000_3FFF	4	
GPIO	0x6000_4000	0x6000_4FFF	4	
Reserved	0x6000_5000	0x6000_6FFF		

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Table 3-3 – cont'd from previous page

Target	Boundary Address		Size (KB)	Notes
	Low Address	High Address		
eFuse Controller	0x6000_7000	0x6000_7FFF	4	
Low-Power Management	0x6000_8000	0x6000_8FFF	4	
IO MUX	0x6000_9000	0x6000_9FFF	4	
Reserved	0x6000_A000	0x6000_EFFF		
I2S Controller 0	0x6000_F000	0x6000_FFFF	4	
UART Controller 1	0x6001_0000	0x6001_0FFF	4	
Reserved	0x6001_1000	0x6001_2FFF		
I2C Controller 0	0x6001_3000	0x6001_3FFF	4	
UHCI0	0x6001_4000	0x6001_4FFF	4	
Reserved	0x6001_5000	0x6001_5FFF		
Remote Control Peripheral	0x6001_6000	0x6001_6FFF	4	
Pulse Count Controller	0x6001_7000	0x6001_7FFF	4	
Reserved	0x6001_8000	0x6001_8FFF		
LED PWM Controller	0x6001_9000	0x6001_9FFF	4	
Reserved	0x6001_A000	0x6001_DFFF		
Motor Control PWM 0	0x6001_E000	0x6001_EFFF	4	
Timer Group 0	0x6001_F000	0x6001_FFFF	4	
Timer Group 1	0x6002_0000	0x6002_0FFF	4	
RTC SLOW Memory	0x6002_1000	0x6002_2FFF	8	
System Timer	0x6002_3000	0x6002_3FFF	4	
SPI Controller 2	0x6002_4000	0x6002_4FFF	4	
SPI Controller 3	0x6002_5000	0x6002_5FFF	4	
APB Controller	0x6002_6000	0x6002_6FFF	4	
I2C Controller 1	0x6002_7000	0x6002_7FFF	4	
SD/MMC Host Controller	0x6002_8000	0x6002_8FFF	4	
Reserved	0x6002_9000	0x6002_AFFF		
Two-wire Automotive Interface	0x6002_B000	0x6002_BFFF	4	
Motor Control PWM 1	0x6002_C000	0x6002_CFFF	4	
I2S Controller 1	0x6002_D000	0x6002_DFFF	4	
UART controller 2	0x6002_E000	0x6002_EFFF	4	
Reserved	0x6002_F000	0x6003_7FFF		
USB Serial/JTAG Controller	0x6003_8000	0x6003_8FFF	4	
USB External Control registers	0x6003_9000	0x6003_9FFF	4	1
AES Accelerator	0x6003_A000	0x6003_AFFF	4	
SHA Accelerator	0x6003_B000	0x6003_BFFF	4	
RSA Accelerator	0x6003_C000	0x6003_CFFF	4	
Digital Signature	0x6003_D000	0x6003_DFFF	4	
HMAC Accelerator	0x6003_E000	0x6003_EFFF	4	
GDMA Controller	0x6003_F000	0x6003_FFFF	4	
ADC Controller	0x6004_0000	0x6004_0FFF	4	
Camera-LCD Controller	0x6004_1000	0x6004_1FFF	4	

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Table 3-3 – cont'd from previous page

Target	Boundary Address		Size (KB)	Notes
	Low Address	High Address		
Reserved	0x6004_2000	0x6007_FFFF		
USB core registers	0x6008_0000	0x600B_FFFF	256	1
System Registers	0x600C_0000	0x600C_0FFF	4	
Sensitive Register	0x600C_1000	0x600C_1FFF	4	
Interrupt Matrix	0x600C_2000	0x600C_2FFF	4	
Reserved	0x600C_3000	0x600C_3FFF		
Configure Cache	0x600C_4000	0x600C_BFFF	32	
External Memory Encryption and Decryption	0x600C_C000	0x600C_CFFF	4	
Reserved	0x600C_D000	0x600C_DFFF		
Debug Assist	0x600C_E000	0x600C_EFFF	4	
Reserved	0x600C_F000	0x600C_FFFF		
World Controller	0x600D_0000	0x600D_0FFF	4	

Note:

1. The address space in this module/peripheral is not continuous.
2. The CPU needs to obtain the access permission to a certain module/peripheral when initiating a request to access it, otherwise it may fail. For more information of permission control, please see Chapter 13 *Permission Control (PMS)*.

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4 eFuse Controller

4.1 Overview

The ESP32-S3 contains a 4-Kbit eFuse to store parameters. These parameters are burned and read by an eFuse Controller. Once an eFuse bit is programmed to 1, it can never be reverted to 0. The eFuse controller programs individual bits of parameters in eFuse according to users configurations. Some of these parameters can be read by users using the eFuse controller. If read-protection for some data is not enabled, that data is readable from outside the chip. If read-protection is enabled, that data can not be read from outside the chip. In all cases, however, some keys stored in eFuse can still be used internally by hardware cryptography modules such as Digital Signature, HMAC, etc., without exposing this data to the outside world.

4.2 Features

- 4-Kbit in total, with 1792 bits available for users
- One-time programmable storage
- Configurable write protection
- Configurable read protection
- Various hardware encoding schemes protect against data corruption

4.3 Functional Description

4.3.1 Structure

The eFuse data is organized in 11 blocks (BLOCK0 ~ BLOCK10). BLOCK0 has 640 bits in totall. BLOCK1 has 288 bits and each block of BLOCK2 ~ 10 has 352 bits.

BLOCK0, which holds most parameters, has 25 bits that are readable but useless to users (the details are showed in Section 4.3.2), and 29 further bits are reserved for future use.

Table 4-1 lists all the parameters in BLOCK0 and their offsets, bit widths, as well as information on whether they can be used by hardware, which bits are write-protected, and corresponding descriptions.

The **EFUSE_WR_DIS** parameter is used to disable the writing of other parameters, while **EFUSE_RD_DIS** is used to disable users from reading BLOCK4 ~ BLOCK10. For more information on these two parameters, please see Section 4.3.1.1 and Section 4.3.1.2.

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Table 4-1. Parameters in eFuse BLOCK0

Parameters	Bit Width	Accessible by Hardware	Programming-Protection by EFUSE_WR_DIS Bit Number	Description
EFUSE_WR_DIS	32	Y	N/A	Disable writing of individual eFuses.
EFUSE_RD_DIS	7	Y	0	Disable users from reading eFuse blocks BLOCK4 ~ 10.
EFUSE_DIS_ICACHE	1	Y	2	Disable ICache.
EFUSE_DIS_DCACHE	1	Y	2	Disable DCache.
EFUSE_DIS_DOWNLOAD_ICACHE	1	Y	2	Disable ICache in Download mode.
EFUSE_DIS_DOWNLOAD_DCACHE	1	Y	2	Disable DCache in Download mode.
EFUSE_DIS_FORCE_DOWNLOAD	1	Y	2	Disable chip from force-entering Download mode.
EFUSE_DIS_USB_OTG	1	Y	2	Disable USB OTG.
EFUSE_DIS_TWAI	1	Y	2	Disable TWAI Controller.
EFUSE_DIS_APP_CPU	1	Y	2	Disable APP CPU.
EFUSE_SOFT_DIS_JTAG	3	Y	31	Disable JTAG by programming odd number of bits. If JTAG is disabled by this way, users can re-enable JTAG via HMAC peripheral.
EFUSE_DIS_PAD_JTAG	1	Y	2	Hardware Disable JTAG permanently.
EFUSE_DIS_DOWNLOAD_ MANUAL_ENCRYPT	1	Y	2	Disable flash encryption in Download boot mode.
EFUSE_USB_EXCHG_PINS	1	Y	30	Swap USB D+/D- pins. Note: The eFuse has a design flaw and does **not** move the pullup (needed to detect USB speed), resulting in the PC thinking the chip is a low-speed device, which stops communication. For detailed information, please refer to Chapter 29 *USB Serial/JTAG Controller (USB_SERIAL_JTAG)*.
EFUSE_EXT_PHY_ENABLE	1	N	30	Enable external USB PHY.
EFUSE_VDD_SPI_XPD	1	Y	3	Power up the VDD_SPI regulator if EFUSE_VDD_SPI_FORCE is 1.

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Table 4-1 – cont'd from previous page

Parameters	Bit Width	Accessible by Hardware	Programming-Protection by EFUSE_WR_DIS Bit Number	Description
EFUSE_VDD_SPI_TIEH	1	Y	3	Select voltage for VDD_SPI if VDD_SPI_FORCE is 1. 0: connect VDD_SPI to 1.8 V LDO; 1: connect VDD_SPI to VDD_RTC_IO.
EFUSE_VDD_SPI_FORCE	1	Y	3	Set to use EFUSE_VDD_SPI_XPD and EFUSE_VDD_SPI_TIEH to configure VDD_SPI LDO.
EFUSE_WDT_DELAY_SEL	2	Y	3	Select RTC WDT timeout threshold.
EFUSE_SPI_BOOT_CRYPT_CNT	3	Y	4	Enable SPI boot encryption and decryption. This feature is enabled when an odd number of bits is set in this parameter, otherwise it is disabled.
EFUSE_SECURE_BOOT_KEY_ REVOKE0	1	N	5	Revoke the first secure boot key when enabled.
EFUSE_SECURE_BOOT_KEY_ REVOKE1	1	N	6	Revoke the second secure boot key when enabled.
EFUSE_SECURE_BOOT_KEY_ REVOKE2	1	N	7	Revoke the third secure boot key when enabled.
EFUSE_KEY_PURPOSE_0	4	Y	8	Key0 purpose, see Table 4-2.
EFUSE_KEY_PURPOSE_1	4	Y	9	Key1 purpose, see Table 4-2.
EFUSE_KEY_PURPOSE_2	4	Y	10	Key2 purpose, see Table 4-2.
EFUSE_KEY_PURPOSE_3	4	Y	11	Key3 purpose, see Table 4-2.
EFUSE_KEY_PURPOSE_4	4	Y	12	Key4 purpose, see Table 4-2.
EFUSE_KEY_PURPOSE_5	4	Y	13	Key5 purpose, see Table 4-2.
EFUSE_SECURE_BOOT_EN	1	N	15	Enable secure boot.
EFUSE_SECURE_BOOT_AGG RESSIVE_REVOKE	1	N	16	Enable aggressive Secure boot key revocation mode.
EFUSE_DIS_USB_JTAG	1	Y	2	Set to disable the function of usb_serial_jtag that switch usb to jtag.
EFUSE_DIS_USB_SERIAL_JTAG	1	Y	2	Set to disable usb_serial_jtag module.
EFUSE_STRAP_JTAG_SEL	1	Y	2	Enable selection between usb_to_jtag or pad_to_jtag through GPIO3. 0: pad_to_jtag; 1: usb_to_jtag.

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Table 4-1 – cont'd from previous page

Parameters	Bit Width	Accessible by Hardware	Programming-Protection by EFUSE_WR_DIS Bit Number	Description
EFUSE_USB_PHY_SEL	1	Y	2	Select internal/external PHY for USB OTG and usb_serial_jtag. 0: internal PHY for usb_serial_jtag, external PHY for USB OTG; 1: internal PHY for USB OTG, external PHY for usb_serial_jtag.
EFUSE_FLASH_TPUW	4	N	18	Configure flash startup delay after SoC being powered up (the unit is ms/2). When the value is 15, delay will be 7.5 ms.
EFUSE_DIS_DOWNLOAD_MODE	1	N	18	Disable all download boot modes.
EFUSE_DIS_LEGACY_SPI_BOOT	1	N	18	Disable Legacy SPI boot mode.
EFUSE_DIS_USB_PRINT	1	N	18	Disable USB printing.
EFUSE_FLASH_ECC_MODE	1	N	18	Set ECC mode for SPI flash. 0: 16-to-18-byte mode; 1: 16-to-17-byte mode.
EFUSE_DIS_USB_SERIAL_JTAG_DOWNLOAD_MODE	1	N	18	Disable download through USB-Serial-JTAG.
EFUSE_ENABLE_SECURITY_ DOWNLOAD	1	N	18	Enable UART secure download mode (read/write flash only).
EFUSE_UART_PRINT_CONTROL	2	N	18	Set UART boot message output mode. 2'b00: Force print; 2'b01: Low-level print, controlled by GPIO46; 2'b10: High-level print, controlled by GPIO46; 2'b11: Print force disabled.
EFUSE_PIN_POWER_SELECTION	1	N	18	Select power for GPIO33 ~ GPIO37. 0: VDD3P3_CPU; 1: VDD_SPI.
EFUSE_FLASH_TYPE	1	N	18	Flash type. 0: 4 data lines; 1: 8 data lines.
EFUSE_FLASH_PAGE_SIZE	2	N	18	Set the page size of flash.
EFUSE_FLASH_ECC_EN	1	N	18	Enable ECC function in Flash boot mode.
EFUSE_FORCE_SEND_RESUME	1	N	18	Force ROM code to send an SPI flash resume command during SPI boot.
EFUSE_SECURE_VERSION	16	N	18	Secure version (used by ESP-IDF anti-rollback feature).
EFUSE_DIS_USB_OTG_DOWNLOAD_MODE	1	N	19	Disable download through USB-OTG.

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Table 4-2 lists all key purpose and their values. Setting the eFuse parameter EFUSE_KEY_PURPOSE_*n* declares the purpose of KEY*n* (*n*: 0 ~ 5).

Table 4-2. Secure Key Purpose Values

Key Purpose Values	Purposes
0	User purposes
1	Reserved
2	XTS_AES_256_KEY_1 (flash/SRAM encryption and decryption)
3	XTS_AES_256_KEY_2 (flash/SRAM encryption and decryption)
4	XTS_AES_128_KEY (flash/SRAM encryption and decryption)
5	HMAC Downstream mode
6	JTAG in HMAC Downstream mode
7	Digital Signature peripheral in HMAC Downstream mode
8	HMAC Upstream mode
9	SECURE_BOOT_DIGEST0 (secure boot key digest)
10	SECURE_BOOT_DIGEST1 (secure boot key digest)
11	SECURE_BOOT_DIGEST2 (secure boot key digest)

Table 4-3 provides the details of parameters in BLOCK1 ~ BLOCK10.

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Table 4-3. Parameters in BLOCK1 to BLOCK10

BLOCK	Parameters	Bit Width	Accessible by Hardware	Write Protection by EFUSE_WR_DIS Bit Number	Read Protection by EFUSE_RD_DIS Bit Number	Description
BLOCK1	EFUSE_MAC	48	N	20	N/A	MAC address
	EFUSE_SPI_PAD_CONFIGURE	[0:5]	N	20	N/A	CLK
		[6:11]	N	20	N/A	Q (D1)
		[12:17]	N	20	N/A	D (D0)
		[18:23]	N	20	N/A	CS
		[24:29]	N	20	N/A	HD (D3)
		[30:35]	N	20	N/A	WP (D2)
		[36:41]	N	20	N/A	DQS
		[42:47]	N	20	N/A	D4
		[48:53]	N	20	N/A	D5
		[54:59]	N	20	N/A	D6
		[60:65]	N	20	N/A	D7
	EFUSE_WAFER_VERSION	[0:2]	N	20	N/A	System data
	EFUSE_PKG_VERSION	[0:2]	N	20	N/A	System data
	EFUSE_SYS_DATA_PART0	72	N	20	N/A	System data
BLOCK2	EFUSE_OPTIONAL_UNIQUE_ID	128	N	20	N/A	System data
	EFUSE_SYS_DATA_PART1	128	N	21	N/A	System data
BLOCK2	EFUSE_SYS_DATA_PART1	256	N	21	N/A	System data
BLOCK3	EFUSE_USR_DATA	256	N	22	N/A	User data
BLOCK4	EFUSE_KEY0_DATA	256	Y	23	0	KEY0 or user data
BLOCK5	EFUSE_KEY1_DATA	256	Y	24	1	KEY1 or user data
BLOCK6	EFUSE_KEY2_DATA	256	Y	25	2	KEY2 or user data
BLOCK7	EFUSE_KEY3_DATA	256	Y	26	3	KEY3 or user data
BLOCK8	EFUSE_KEY4_DATA	256	Y	27	4	KEY4 or user data
BLOCK9	EFUSE_KEY5_DATA	256	Y	28	5	KEY5 or user data

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Table 4-3 – cont'd from previous page

BLOCK	Parameters	Bit Width	Accessible by Hardware	Write Protection by EFUSE_WR_DIS Bit Number	Read Protection by EFUSE_RD_DIS Bit Number	Description
BLOCK10	EFUSE_SYS_DATA_PART2	256	N	29	6	System data

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Among these blocks, BLOCK4 ~ 9 store KEY0 ~ 5, respectively. Up to six 256-bit keys can be written into eFuse. Whenever a key is written, its purpose value should also be written (see table 4-2). For example, when a key for the JTAG function in HMAC Downstream mode is written to KEY3 (i.e., BLOCK7), its key purpose value 6 should also be written to EFUSE_KEY_PURPOSE_3.

BLOCK1 ~ BLOCK10 use the RS coding scheme, so there are some restrictions on writing to these parameters. For more detailed information, please refer to Section 4.3.1.3 and 4.3.2.

4.3.1.1 EFUSE_WR_DIS

Parameter EFUSE_WR_DIS determines whether individual eFuse parameters are write-protected. After EFUSE_WR_DIS has been programmed, execute an eFuse read operation to let the new values take effect (see Section 4.3.3).

Column "Write Protection by EFUSE_WR_DIS Bit Number" in Table 4-1 and Table 4-3 list the specific bits in EFUSE_WR_DIS that disable writing.

When the write protection bit of a parameter is set to 0, it means that this parameter is not write-protected and can be programmed.

Setting the write protection bit of a parameter to 1 enables write-protection for it and none of its bits can be modified afterwards. Non-programmed bits always remain 0 while programmed bits always remain 1.

4.3.1.2 EFUSE_RD_DIS

Only the eFuse blocks BLOCK4 ~ BLOCK10 can be individually read protected to prevent any access from outside the chip, as shown in column "Read Protection by EFUSE_RD_DIS Bit Number" of Table 4-3. After EFUSE_RD_DIS has been programmed, execute an eFuse read operation to let the new values take effect (see Section 4.3.3).

If a bit in EFUSE_RD_DIS is 0, then the eFuse block can be read by users; if a bit in EFUSE_RD_DIS is 1, then the parameter controlled by this bit is user read protected.

Other parameters that are not in BLOCK4 ~ BLOCK10 can always be read by users.

When BLOCK4 ~ BLOCK10 are set to be read-protected, the data in these blocks are not readable by users, but they can still be used internally by hardware cryptography modules, if the EFUSE_KEY_PURPOSE_*n* bit is set accordingly.

4.3.1.3 Data Storage

According to the different types of eFuse bits, eFuse controller use two hardware encoding schemes to protect eFuse bits from corruption.

All BLOCK0 parameters except for EFUSE_WR_DIS are stored with four backups, meaning each bit is stored four times. This scheme is transparent to the user. This encoding scheme is invisible for users.

BLOCK1 ~ BLOCK10 store key data and some parameters and use RS (44, 32) coding scheme that supports up to 6 bytes of automatic error correction. The primitive polynomial of RS (44, 32) is
$p(x) = x^8 + x^4 + x^3 + x^2 + 1$.

The shift register circuit shown in Figure 4-1 and 4-2 processes 32 data bytes using RS (44, 32). This coding scheme encodes 32 bytes of data into 44 bytes:

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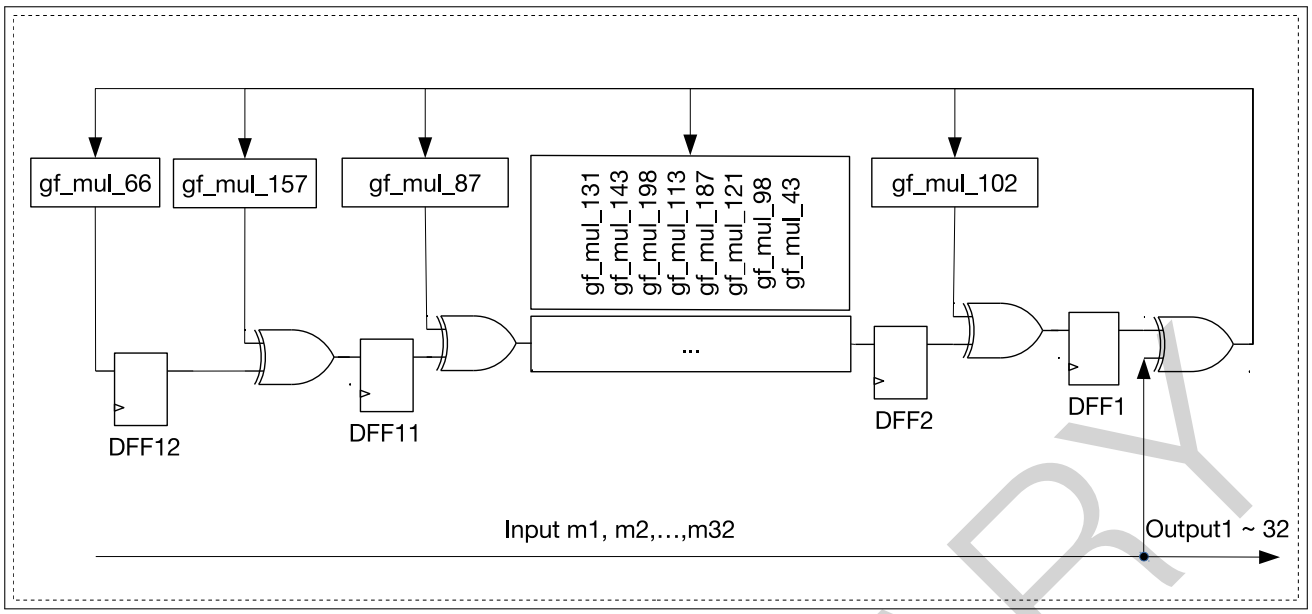


Figure 4-1. Shift Register Circuit (output of first 32 bytes)

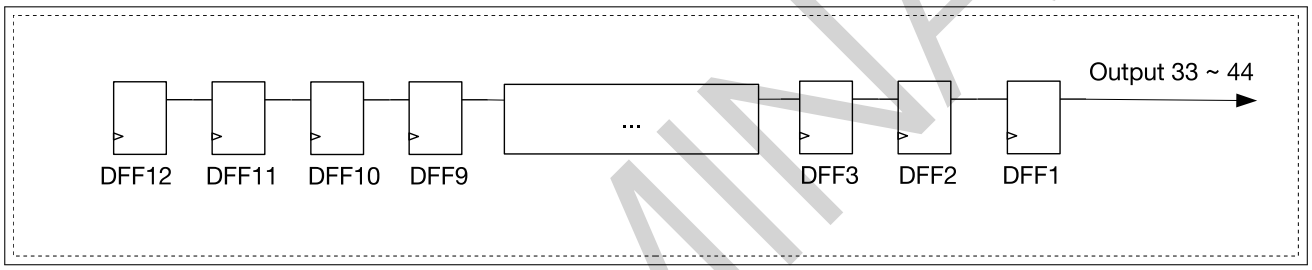


Figure 4-2. Shift Register Circuit (output of last 12 bytes)

- Bytes [0:31] are the data bytes itself
- Bytes [32:43] are the encoded parity bytes stored in 8-bit flip-flops DFF1, DFF2, ..., DFF12 (gf_mul_n, where n is an integer, is the result of multiplying a byte of data ...)

After that, the hardware burns into eFuse the 44-byte codeword consisting of the data bytes followed by the parity bytes.

When the eFuse block is read back, the eFuse controller automatically decodes the codeword and applies error correction if needed.

Because the RS check codes are generated on the entire 256-bit eFuse block, each block can only be written once.

4.3.2 Programming of Parameters

The eFuse controller can only program eFuse parameters of one block at a time. BLOCK0 ~ BLOCK10 share the same address range to store the parameters to be programmed. Configure parameter EFUSE_BLK_NUM to indicate which block should be programmed.

Before programming, make sure the eFuse programming voltage VDDQ is configured correctly as described in Section 4.3.4.

Programming BLOCK0

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When EFUSE_BLK_NUM is set to 0, BLOCK0 will be programmed. Register EFUSE_PGM_DATA0_REG stores EFUSE_WR_DIS. Registers EFUSE_PGM_DATA1_REG ~ EFUSE_PGM_DATA5_REG store the information of parameters to be programmed. Note that 25 bits are readable but useless to users and must always be set to 0 in the programming registers. The specific bits are:

- EFUSE_PGM_DATA1_REG[27:31]
- EFUSE_PGM_DATA1_REG[21:24]
- EFUSE_PGM_DATA2_REG[7:15]
- EFUSE_PGM_DATA2_REG[0:3]
- EFUSE_PGM_DATA3_REG[26:27]
- EFUSE_PGM_DATA4_REG[30]

Data in registers EFUSE_PGM_DATA6_REG ~ EFUSE_PGM_DATA7_REG and EFUSE_PGM_CHECK_VALUE0_REG ~ EFUSE_PGM_CHECK_VALUE2_REG are ignored when programming BLOCK0.

Programming BLOCK1

When EFUSE_BLK_NUM is set to 1, registers EFUSE_PGM_DATA0_REG ~ EFUSE_PGM_DATA5_REG store the BLOCK1 parameters to be programmed. Registers EFUSE_PGM_CHECK_VALUE0_REG ~ EFUSE_PGM_DATA2_REG store the corresponding RS check codes. Data in registers EFUSE_PGM_DATA6_REG ~ EFUSE_PGM_DATA7_REG is ignored when programming BLOCK1, and the RS check codes will be calculated with these bits all treated as 0.

Programming BLOCK2 ~ 10

When EFUSE_BLK_NUM is set to 2 ~ 10, registers EFUSE_PGM_DATA0_REG ~ EFUSE_PGM_DATA7_REG store the parameters to be programmed to this block. Registers EFUSE_PGM_CHECK_VALUE0_REG ~ EFUSE_PGM_CHECK_VALUE2_REG store the corresponding RS check codes.

Programming process

The process of programming parameters is as follows:

1. Write the block number to EFUSE_BLK_NUM to determine the block to be programmed.
2. Write parameters to be programmed to registers EFUSE_PGM_DATA0_REG ~ EFUSE_PGM_DATA7_REG and the corresponding checksum values to EFUSE_PGM_CHECK_VALUE0_REG ~ EFUSE_PGM_CHECK_VALUE2_REG.
3. Configure the field EFUSE_OP_CODE of register EFUSE_CONF_REG to 0x5A5A.
4. Configure the field EFUSE_PGM_CMD of register EFUSE_CMD_REG to 1.
5. Poll register EFUSE_CMD_REG until it is 0x0, or wait for a PGM_DONE interrupt. For more information on how to identify a PGM_DONE interrupt, please see the end of Section 4.3.3.
6. In order to avoid programming content leakage, please clear the parameters in EFUSE_PGM_DATA0_REG ~ EFUSE_PGM_DATA7_REG and EFUSE_PGM_CHECK_VALUE0_REG ~ EFUSE_PGM_CHECK_VALUE2_REG.
7. Trigger an eFuse read operation (see Section 4.3.3) to update eFuse registers with the new values.

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8. Check error record registers. If the values read in error record registers are not 0, the programming process should be performed again following above steps 1 ~ 7. Please check the following error record registers for different eFuse blocks:
    - BLOCK0: EFUSE_RD_REPEAT_ERR0_REG ~ EFUSE_RD_REPEAT_ERR4_REG
    - BLOCK1: EFUSE_RD_RS_ERR0_REG[2:0], EFUSE_RD_RS_ERR0_REG[7]
    - BLOCK2: EFUSE_RD_RS_ERR0_REG[6:4], EFUSE_RD_RS_ERR0_REG[11]
    - BLOCK3: EFUSE_RD_RS_ERR0_REG[10:8], EFUSE_RD_RS_ERR0_REG[15]
    - BLOCK4: EFUSE_RD_RS_ERR0_REG[14:12], EFUSE_RD_RS_ERR0_REG[19]
    - BLOCK5: EFUSE_RD_RS_ERR0_REG[18:16], EFUSE_RD_RS_ERR0_REG[23]
    - BLOCK6: EFUSE_RD_RS_ERR0_REG[22:20], EFUSE_RD_RS_ERR0_REG[27]
    - BLOCK7: EFUSE_RD_RS_ERR0_REG[26:24], EFUSE_RD_RS_ERR0_REG[31]
    - BLOCK8: EFUSE_RD_RS_ERR0_REG[30:28], EFUSE_RD_RS_ERR1_REG[3]
    - BLOCK9: EFUSE_RD_RS_ERR1_REG[2:0], EFUSE_RD_RS_ERR1_REG[2:0][7]
    - BLOCK10: EFUSE_RD_RS_ERR1_REG[2:0][6:4]

Limitations

In BLOCK0, each bit can be programmed separately. However, we recommend to minimize programming cycles and program all the bits of a parameter in one programming action. In addition, after all parameters controlled by a certain bit of EFUSE_WR_DIS are programmed, that bit should be immediately programmed. The programming of parameters controlled by a certain bit of EFUSE_WR_DIS, and the programming of the bit itself can even be completed at the same time. Repeated programming of already programmed bits is strictly forbidden, otherwise, programming errors will occur.

BLOCK1 cannot be programmed by users as it has been programmed at manufacturing.

BLOCK2 ~ 10 can only be programmed once. Repeated programming is not allowed.

4.3.3 User Read of Parameters

Users cannot read eFuse bits directly. The eFuse Controller hardware reads all eFuse bits and stores the results to their corresponding registers in its memory space. Then, users can read eFuse bits by reading the registers that start with EFUSE_RD_. Details are provided in Table 4-4.

Table 4-4. Registers Information

BLOCK	Read Registers	Registers When Programming This Block
0	EFUSE_RD_WR_DIS_REG	EFUSE_PGM_DATA0_REG
0	EFUSE_RD_REPEAT_DATA0 ~ 4_REG	EFUSE_PGM_DATA1 ~ 5_REG
1	EFUSE_RD_MAC_SPI_SYS_0 ~ 5_REG	EFUSE_PGM_DATA0 ~ 5_REG
2	EFUSE_RD_SYS_PART1_0 ~ 7_REG	EFUSE_PGM_DATA0 ~ 7_REG
3	EFUSE_RD_USR_DATA0 ~ 7_REG	EFUSE_PGM_DATA0 ~ 7_REG
4 ~ 9	EFUSE_RD_KEY*n*_DATA0 ~ 7_REG (*n*: 0 ~ 5)	EFUSE_PGM_DATA0 ~ 7_REG
10	EFUSE_RD_SYS_PART2_0 ~ 7_REG	EFUSE_PGM_DATA0 ~ 7_REG

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Updating eFuse read registers

The eFuse Controller reads internal eFuses to update corresponding registers. This read operation happens on system reset and can also be triggered manually by users as needed (e.g., if new eFuse values have been programmed). The process of triggering a read operation by users is as follows:

1. Configure the field EFUSE_OP_CODE in register EFUSE_CONF_REG to 0x5AA5.
2. Configure the field EFUSE_READ_CMD in register EFUSE_CMD_REG to 1.
3. Poll register EFUSE_CMD_REG until it is 0x0, or wait for a READ_DONE interrupt. Information on how to identify a READ_DONE interrupt is provided below in this section.
4. users reads the values of each parameter from memory.

The eFuse read registers will hold all values until the next read operation.

Error detection

Error record registers allow users to detect if there are any inconsistencies in the stored backup eFuse parameters.

Registers EFUSE_RD_REPEAT_ERR0 ~ 3_REG indicate if there are any errors of programmed parameters (except for EFUSE_WR_DIS) in BLOCK0 (value 1 indicates an error is detected, and the bit becomes invalid; value 0 indicates no error).

Registers EFUSE_RD_RS_ERR0 ~ 1_REG store the number of corrected bytes as well as the result of RS decoding during eFuse reading BLOCK1 ~ BLOCK10.

The values of above registers will be updated every time after the eFuse read registers have been updated.

Identifying the completion of a program/read operation

The methods to identify the completion of a program/read operation are described below. Please note that bit 1 corresponds to a program operation, and bit 0 corresponds to a read operation.

- Method one:
  1. Poll bit 1/0 in register EFUSE_INT_RAW_REG until it becomes 1, which represents the completion of a program/read operation.
- Method two:
  1. Set bit 1/0 in register EFUSE_INT_ENA_REG to 1 to enable the eFuse Controller to post a PGM_DONE or READ_DONE interrupt.
  2. Configure the Interrupt Matrix to enable the CPU to respond to eFuse interrupt signals, see Chapter 8 *Interrupt Matrix (INTERRUPT)*.
  3. Wait for the PGM/READ_DONE interrupt.
  4. Set bit 1/0 in register EFUSE_INT_CLR_REG to 1 to clear the PGM/READ_DONE interrupt.

Note

When eFuse controller updating its registers, it will use EFUSE_PGM_DATA*n*_REG (n=0 1 ..,7) again to store data. So please do not write important data into these registers before this updating process initiated.

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During the chip boot process, eFuse controller will update eFuse data into registers which can be accessed by users automatically. You can get programmed eFuse data by reading corresponding registers. Thus, it is no need to update eFuse read registers in such case.

4.3.4 eFuse VDDQ Timing

The eFuse Controller operates with 20 MHz, one cycle is 50 ns, and its programming voltage VDDQ should be configured as follows:

- EFUSE_DAC_NUM (store the rising period of VDDQ): The default value of VDDQ is 2.5 V and the voltage increases by 0.01 V in each clock cycle. Thus, the default value of this parameter is 255;
- EFUSE_DAC_CLK_DIV (the clock divisor of VDDQ): The clock period to program VDDQ should be larger than 1 μs;
- EFUSE_PWR_ON_NUM (the power-up time for VDDQ): The programming voltage should be stabilized after this time, which means the value of this parameter should be configured to exceed the value of EFUSE_DAC_CLK_DIV multiply by EFUSE_DAC_NUM;
- EFUSE_PWR_OFF_NUM (the power-out time for VDDQ): The value of this parameter should be larger than 10 μs.

Table 4-5. Configuration of Default VDDQ Timing Parameters

EFUSE_DAC_NUM	EFUSE_DAC_CLK_DIV	EFUSE_PWR_ON_NUM	EFUSE_PWR_OFF_NUM
0xFF	0x28	0x3000	0x190

4.3.5 The Use of Parameters by Hardware Modules

Some hardware modules are directly connected to the eFuse peripheral in order to use the parameters listed in Table 4-1 and Table 4-3, specifically those marked with "Y" in columns "Accessible by Hardware". Users cannot intervene in this process.

4.3.6 Interrupts

- PGM_DONE interrupt: Triggered when eFuse programming has finished. Set EFUSE_PGM_DONE_INT_ENA to enable this interrupt;
- READ_DONE interrupt: Triggered when eFuse reading has finished. Set EFUSE_READ_DONE_INT_ENA to enable this interrupt.

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4.4 Register Summary

The addresses in this section are relative to eFuse Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

07

Name	Description	Address	Access
PGM Data Register			
EFUSE_PGM_DATA0_REG	Register 0 that stores data to be programmed	0x0000	R/W
EFUSE_PGM_DATA1_REG	Register 1 that stores data to be programmed	0x0004	R/W
EFUSE_PGM_DATA2_REG	Register 2 that stores data to be programmed	0x0008	R/W
EFUSE_PGM_DATA3_REG	Register 3 that stores data to be programmed	0x000C	R/W
EFUSE_PGM_DATA4_REG	Register 4 that stores data to be programmed	0x0010	R/W
EFUSE_PGM_DATA5_REG	Register 5 that stores data to be programmed	0x0014	R/W
EFUSE_PGM_DATA6_REG	Register 6 that stores data to be programmed	0x0018	R/W
EFUSE_PGM_DATA7_REG	Register 7 that stores data to be programmed	0x001C	R/W
EFUSE_PGM_CHECK_VALUE0_REG	Register 0 that stores the RS code to be programmed	0x0020	R/W
EFUSE_PGM_CHECK_VALUE1_REG	Register 1 that stores the RS code to be programmed	0x0024	R/W
EFUSE_PGM_CHECK_VALUE2_REG	Register 2 that stores the RS code to be programmed	0x0028	R/W
Read Data Register			
EFUSE_RD_WR_DIS_REG	BLOCK0 data register 0	0x002C	RO
EFUSE_RD_REPEAT_DATA0_REG	BLOCK0 data register 1	0x0030	RO
EFUSE_RD_REPEAT_DATA1_REG	BLOCK0 data register 2	0x0034	RO
EFUSE_RD_REPEAT_DATA2_REG	BLOCK0 data register 3	0x0038	RO
EFUSE_RD_REPEAT_DATA3_REG	BLOCK0 data register 4	0x003C	RO
EFUSE_RD_REPEAT_DATA4_REG	BLOCK0 data register 5	0x0040	RO
EFUSE_RD_MAC_SPI_SYS_0_REG	BLOCK1 data register 0	0x0044	RO
EFUSE_RD_MAC_SPI_SYS_1_REG	BLOCK1 data register 1	0x0048	RO
EFUSE_RD_MAC_SPI_SYS_2_REG	BLOCK1 data register 2	0x004C	RO
EFUSE_RD_MAC_SPI_SYS_3_REG	BLOCK1 data register 3	0x0050	RO
EFUSE_RD_MAC_SPI_SYS_4_REG	BLOCK1 data register 4	0x0054	RO
EFUSE_RD_MAC_SPI_SYS_5_REG	BLOCK1 data register 5	0x0058	RO
EFUSE_RD_SYS_PART1_DATA0_REG	Register 0 of BLOCK2 (system)	0x005C	RO
EFUSE_RD_SYS_PART1_DATA1_REG	Register 1 of BLOCK2 (system)	0x0060	RO
EFUSE_RD_SYS_PART1_DATA2_REG	Register 2 of BLOCK2 (system)	0x0064	RO
EFUSE_RD_SYS_PART1_DATA3_REG	Register 3 of BLOCK2 (system)	0x0068	RO
EFUSE_RD_SYS_PART1_DATA4_REG	Register 4 of BLOCK2 (system)	0x006C	RO
EFUSE_RD_SYS_PART1_DATA5_REG	Register 5 of BLOCK2 (system)	0x0070	RO
EFUSE_RD_SYS_PART1_DATA6_REG	Register 6 of BLOCK2 (system)	0x0074	RO
EFUSE_RD_SYS_PART1_DATA7_REG	Register 7 of BLOCK2 (system)	0x0078	RO
EFUSE_RD_USR_DATA0_REG	Register 0 of BLOCK3 (user)	0x007C	RO
EFUSE_RD_USR_DATA1_REG	Register 1 of BLOCK3 (user)	0x0080	RO

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Name	Description	Address	Access
EFUSE_RD_USR_DATA2_REG	Register 2 of BLOCK3 (user)	0x0084	RO
EFUSE_RD_USR_DATA3_REG	Register 3 of BLOCK3 (user)	0x0088	RO
EFUSE_RD_USR_DATA4_REG	Register 4 of BLOCK3 (user)	0x008C	RO
EFUSE_RD_USR_DATA5_REG	Register 5 of BLOCK3 (user)	0x0090	RO
EFUSE_RD_USR_DATA6_REG	Register 6 of BLOCK3 (user)	0x0094	RO
EFUSE_RD_USR_DATA7_REG	Register 7 of BLOCK3 (user)	0x0098	RO
EFUSE_RD_KEY0_DATA0_REG	Register 0 of BLOCK4 (KEY0)	0x009C	RO
EFUSE_RD_KEY0_DATA1_REG	Register 1 of BLOCK4 (KEY0)	0x00A0	RO
EFUSE_RD_KEY0_DATA2_REG	Register 2 of BLOCK4 (KEY0)	0x00A4	RO
EFUSE_RD_KEY0_DATA3_REG	Register 3 of BLOCK4 (KEY0)	0x00A8	RO
EFUSE_RD_KEY0_DATA4_REG	Register 4 of BLOCK4 (KEY0)	0x00AC	RO
EFUSE_RD_KEY0_DATA5_REG	Register 5 of BLOCK4 (KEY0)	0x00B0	RO
EFUSE_RD_KEY0_DATA6_REG	Register 6 of BLOCK4 (KEY0)	0x00B4	RO
EFUSE_RD_KEY0_DATA7_REG	Register 7 of BLOCK4 (KEY0)	0x00B8	RO
EFUSE_RD_KEY1_DATA0_REG	Register 0 of BLOCK5 (KEY1)	0x00BC	RO
EFUSE_RD_KEY1_DATA1_REG	Register 1 of BLOCK5 (KEY1)	0x00C0	RO
EFUSE_RD_KEY1_DATA2_REG	Register 2 of BLOCK5 (KEY1)	0x00C4	RO
EFUSE_RD_KEY1_DATA3_REG	Register 3 of BLOCK5 (KEY1)	0x00C8	RO
EFUSE_RD_KEY1_DATA4_REG	Register 4 of BLOCK5 (KEY1)	0x00CC	RO
EFUSE_RD_KEY1_DATA5_REG	Register 5 of BLOCK5 (KEY1)	0x00D0	RO
EFUSE_RD_KEY1_DATA6_REG	Register 6 of BLOCK5 (KEY1)	0x00D4	RO
EFUSE_RD_KEY1_DATA7_REG	Register 7 of BLOCK5 (KEY1)	0x00D8	RO
EFUSE_RD_KEY2_DATA0_REG	Register 0 of BLOCK6 (KEY2)	0x00DC	RO
EFUSE_RD_KEY2_DATA1_REG	Register 1 of BLOCK6 (KEY2)	0x00E0	RO
EFUSE_RD_KEY2_DATA2_REG	Register 2 of BLOCK6 (KEY2)	0x00E4	RO
EFUSE_RD_KEY2_DATA3_REG	Register 3 of BLOCK6 (KEY2)	0x00E8	RO
EFUSE_RD_KEY2_DATA4_REG	Register 4 of BLOCK6 (KEY2)	0x00EC	RO
EFUSE_RD_KEY2_DATA5_REG	Register 5 of BLOCK6 (KEY2)	0x00F0	RO
EFUSE_RD_KEY2_DATA6_REG	Register 6 of BLOCK6 (KEY2)	0x00F4	RO
EFUSE_RD_KEY2_DATA7_REG	Register 7 of BLOCK6 (KEY2)	0x00F8	RO
EFUSE_RD_KEY3_DATA0_REG	Register 0 of BLOCK7 (KEY3)	0x00FC	RO
EFUSE_RD_KEY3_DATA1_REG	Register 1 of BLOCK7 (KEY3)	0x0100	RO
EFUSE_RD_KEY3_DATA2_REG	Register 2 of BLOCK7 (KEY3)	0x0104	RO
EFUSE_RD_KEY3_DATA3_REG	Register 3 of BLOCK7 (KEY3)	0x0108	RO
EFUSE_RD_KEY3_DATA4_REG	Register 4 of BLOCK7 (KEY3)	0x010C	RO
EFUSE_RD_KEY3_DATA5_REG	Register 5 of BLOCK7 (KEY3)	0x0110	RO
EFUSE_RD_KEY3_DATA6_REG	Register 6 of BLOCK7 (KEY3)	0x0114	RO
EFUSE_RD_KEY3_DATA7_REG	Register 7 of BLOCK7 (KEY3)	0x0118	RO
EFUSE_RD_KEY4_DATA0_REG	Register 0 of BLOCK8 (KEY4)	0x011C	RO
EFUSE_RD_KEY4_DATA1_REG	Register 1 of BLOCK8 (KEY4)	0x0120	RO
EFUSE_RD_KEY4_DATA2_REG	Register 2 of BLOCK8 (KEY4)	0x0124	RO
EFUSE_RD_KEY4_DATA3_REG	Register 3 of BLOCK8 (KEY4)	0x0128	RO
EFUSE_RD_KEY4_DATA4_REG	Register 4 of BLOCK8 (KEY4)	0x012C	RO

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Name	Description	Address	Access
EFUSE_RD_KEY4_DATA5_REG	Register 5 of BLOCK8 (KEY4)	0x0130	RO
EFUSE_RD_KEY4_DATA6_REG	Register 6 of BLOCK8 (KEY4)	0x0134	RO
EFUSE_RD_KEY4_DATA7_REG	Register 7 of BLOCK8 (KEY4)	0x0138	RO
EFUSE_RD_KEY5_DATA0_REG	Register 0 of BLOCK9 (KEY5)	0x013C	RO
EFUSE_RD_KEY5_DATA1_REG	Register 1 of BLOCK9 (KEY5)	0x0140	RO
EFUSE_RD_KEY5_DATA2_REG	Register 2 of BLOCK9 (KEY5)	0x0144	RO
EFUSE_RD_KEY5_DATA3_REG	Register 3 of BLOCK9 (KEY5)	0x0148	RO
EFUSE_RD_KEY5_DATA4_REG	Register 4 of BLOCK9 (KEY5)	0x014C	RO
EFUSE_RD_KEY5_DATA5_REG	Register 5 of BLOCK9 (KEY5)	0x0150	RO
EFUSE_RD_KEY5_DATA6_REG	Register 6 of BLOCK9 (KEY5)	0x0154	RO
EFUSE_RD_KEY5_DATA7_REG	Register 7 of BLOCK9 (KEY5)	0x0158	RO
EFUSE_RD_SYS_PART2_DATA0_REG	Register 0 of BLOCK10 (system)	0x015C	RO
EFUSE_RD_SYS_PART2_DATA1_REG	Register 1 of BLOCK10 (system)	0x0160	RO
EFUSE_RD_SYS_PART2_DATA2_REG	Register 2 of BLOCK10 (system)	0x0164	RO
EFUSE_RD_SYS_PART2_DATA3_REG	Register 3 of BLOCK10 (system)	0x0168	RO
EFUSE_RD_SYS_PART2_DATA4_REG	Register 4 of BLOCK10 (system)	0x016C	RO
EFUSE_RD_SYS_PART2_DATA5_REG	Register 5 of BLOCK10 (system)	0x0170	RO
EFUSE_RD_SYS_PART2_DATA6_REG	Register 6 of BLOCK10 (system)	0x0174	RO
EFUSE_RD_SYS_PART2_DATA7_REG	Register 7 of BLOCK10 (system)	0x0178	RO
Report Register			
EFUSE_RD_REPEAT_ERR0_REG	Programming error record register 0 of BLOCK0	0x017C	RO
EFUSE_RD_REPEAT_ERR1_REG	Programming error record register 1 of BLOCK0	0x0180	RO
EFUSE_RD_REPEAT_ERR2_REG	Programming error record register 2 of BLOCK0	0x0184	RO
EFUSE_RD_REPEAT_ERR3_REG	Programming error record register 3 of BLOCK0	0x0188	RO
EFUSE_RD_REPEAT_ERR4_REG	Programming error record register 4 of BLOCK0	0x0190	RO
EFUSE_RD_RS_ERR0_REG	Programming error record register 0 of BLOCK1 ~ 10	0x01C0	RO
EFUSE_RD_RS_ERR1_REG	Programming error record register 1 of BLOCK1 ~ 10	0x01C4	RO
Configuration Register			
EFUSE_CLK_REG	eFuse clock configuration register	0x01C8	R/W
EFUSE_CONF_REG	eFuse operation mode configuration register	0x01CC	R/W
EFUSE_CMD_REG	eFuse command register	0x01D4	varies
EFUSE_DAC_CONF_REG	Controls the eFuse programming voltage	0x01E8	R/W
EFUSE_RD_TIM_CONF_REG	Configures read timing parameters	0x01EC	R/W
EFUSE_WR_TIM_CONF1_REG	Configuration register 1 of eFuse programming timing parameters	0x01F4	R/W
EFUSE_WR_TIM_CONF2_REG	Configuration register 2 of eFuse programming timing parameters	0x01F8	R/W
Status Register			
EFUSE_STATUS_REG	eFuse status register	0x01D0	RO
Interrupt Register			
EFUSE_INT_RAW_REG	eFuse raw interrupt register	0x01D8	R/WC/SS

PRELIMINARY

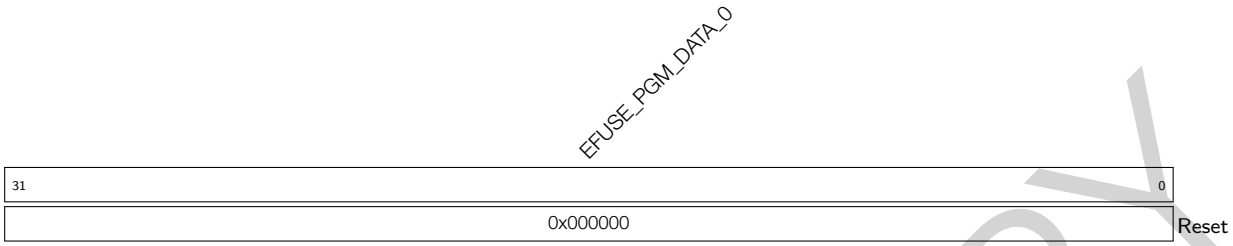
Name	Description	Address	Access
EFUSE_INT_ST_REG	eFuse interrupt status register	0x01DC	RO
EFUSE_INT_ENA_REG	eFuse interrupt enable register	0x01E0	R/W
EFUSE_INT_CLR_REG	eFuse interrupt clear register	0x01E4	WO
Version Register			
EFUSE_DATE_REG	Version control register	0x01FC	R/W

PRELIMINARY

4.5 Registers

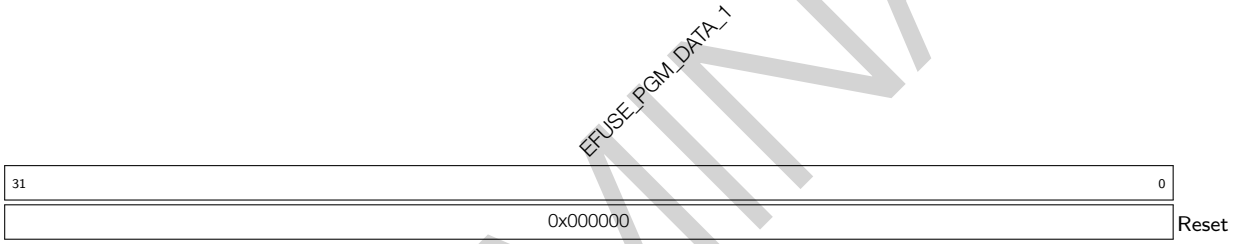
The addresses in this section are relative to eFuse Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 4.1. EFUSE_PGM_DATA0_REG (0x0000)



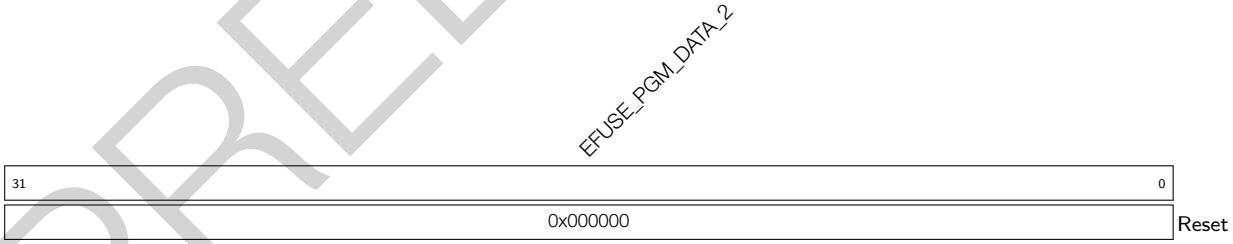
EFUSE_PGM_DATA_0 The content of the 0th 32-bit data to be programmed. (R/W)

Register 4.2. EFUSE_PGM_DATA1_REG (0x0004)



EFUSE_PGM_DATA_1 The content of the first 32-bit data to be programmed. (R/W)

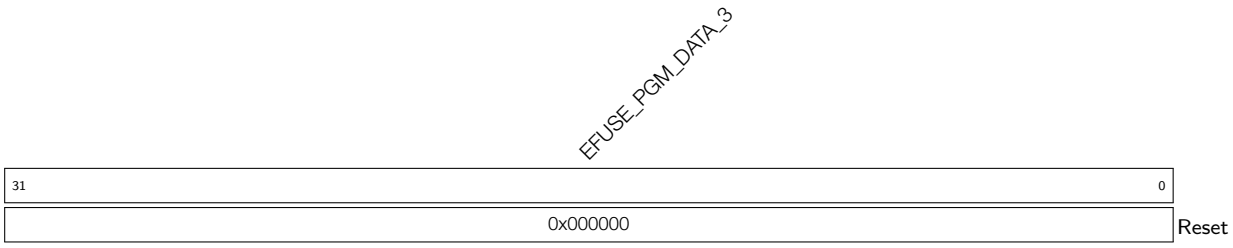
Register 4.3. EFUSE_PGM_DATA2_REG (0x0008)



EFUSE_PGM_DATA_2 The content of the second 32-bit data to be programmed. (R/W)

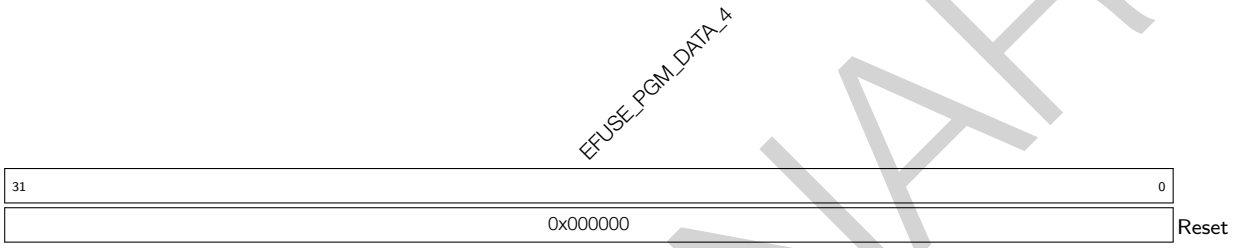
PRELIMINARY

Register 4.4. EFUSE_PGM_DATA3_REG (0x000C)



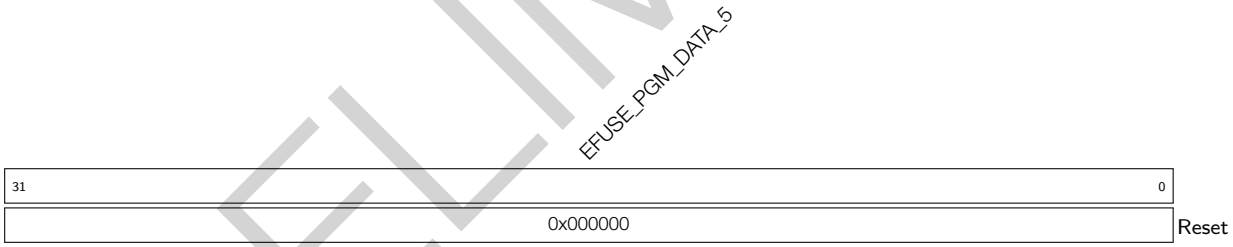
EFUSE_PGM_DATA_3 The content of the 3rd 32-bit data to be programmed. (R/W)

Register 4.5. EFUSE_PGM_DATA4_REG (0x0010)



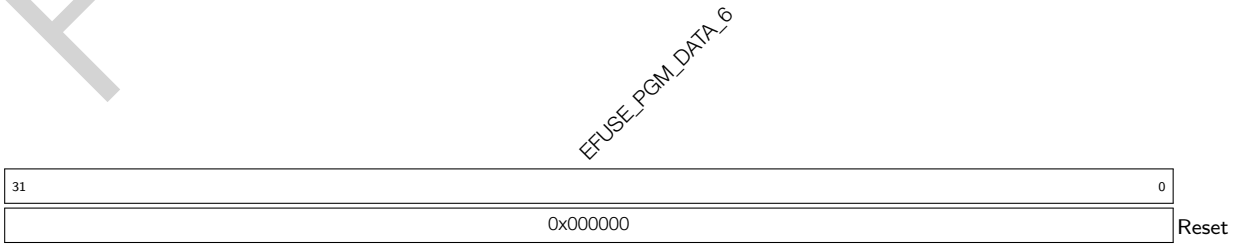
EFUSE_PGM_DATA_4 The content of the 4th 32-bit data to be programmed. (R/W)

Register 4.6. EFUSE_PGM_DATA5_REG (0x0014)



EFUSE_PGM_DATA_5 The content of the 5th 32-bit data to be programmed. (R/W)

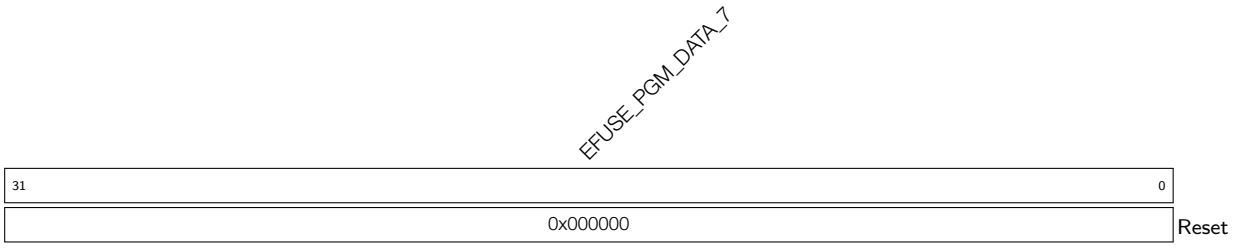
Register 4.7. EFUSE_PGM_DATA6_REG (0x0018)



EFUSE_PGM_DATA_6 The content of the 6th 32-bit data to be programmed. (R/W)

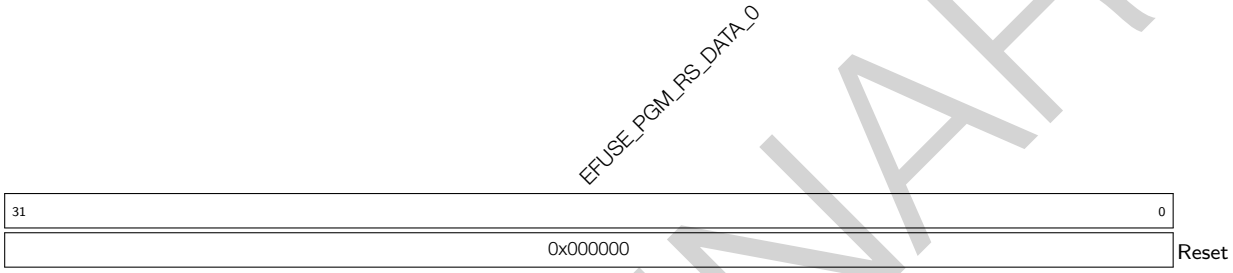
PRELIMINARY

Register 4.8. EFUSE_PGM_DATA7_REG (0x001C)



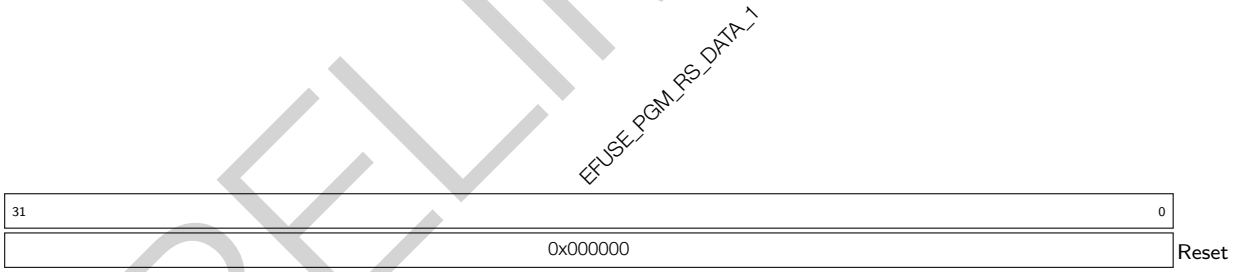
EFUSE_PGM_DATA_7 The content of the 7th 32-bit data to be programmed. (R/W)

Register 4.9. EFUSE_PGM_CHECK_VALUE0_REG (0x0020)



EFUSE_PGM_RS_DATA_0 The content of the 0th 32-bit RS code to be programmed. (R/W)

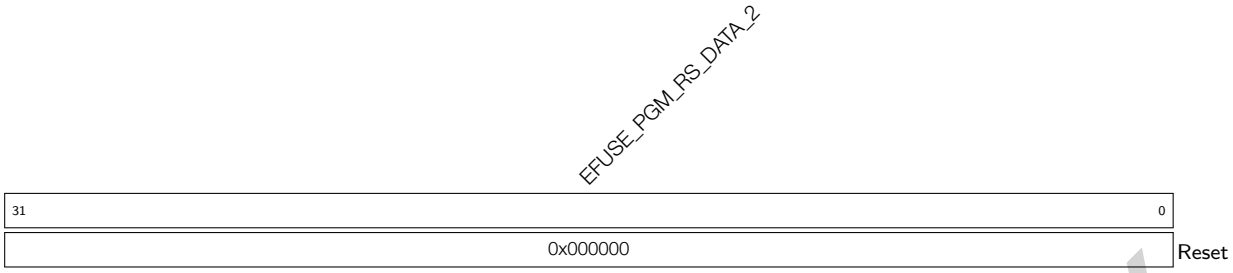
Register 4.10. EFUSE_PGM_CHECK_VALUE1_REG (0x0024)



EFUSE_PGM_RS_DATA_1 The content of the first 32-bit RS code to be programmed. (R/W)

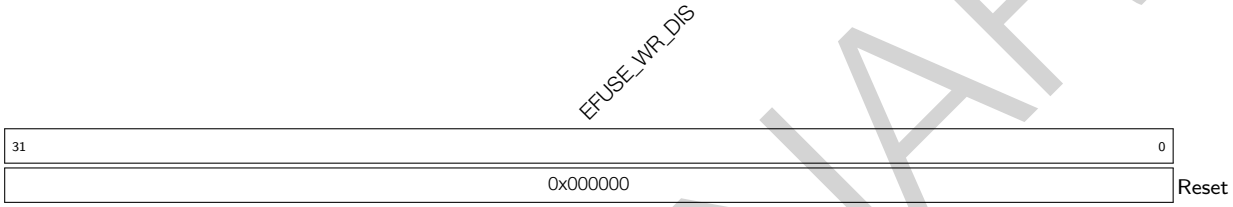
PRELIMINARY

Register 4.11. EFUSE_PGM_CHECK_VALUE2_REG (0x0028)



EFUSE_PGM_RS_DATA_2 The content of the second 32-bit RS code to be programmed. (R/W)

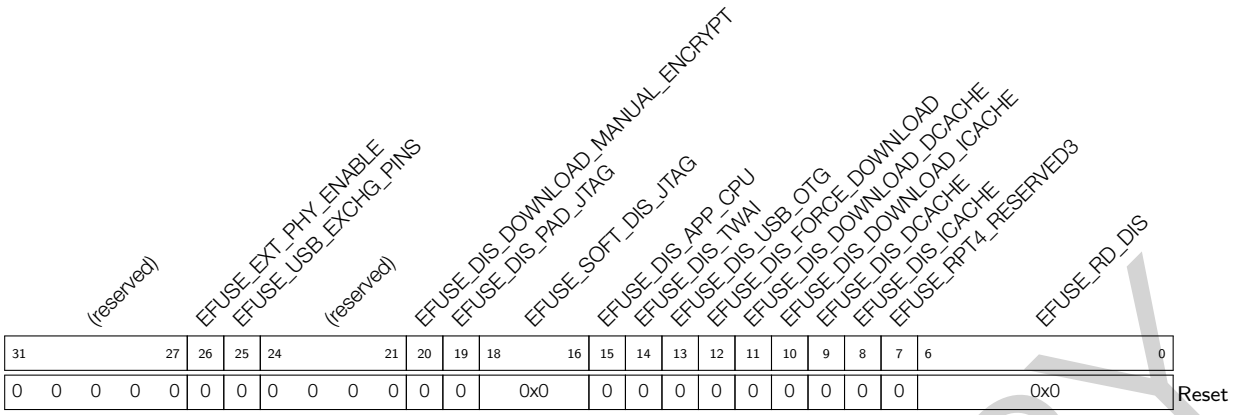
Register 4.12. EFUSE_RD_WR_DIS_REG (0x002C)



EFUSE_WR_DIS Disable programming of individual eFuses. (RO)

PRELIMINARY

Register 4.13. EFUSE_RD_REPEAT_DATA0_REG (0x0030)



EFUSE_RD_DIS This bit be set to disable users reading from BlOCK4 ~ 10. (RO)

EFUSE_RPT4_RESERVED3 Reserved (used four backups method). (RO)

EFUSE_DIS_ICACHE This bit be set to disable Icache. (RO)

EFUSE_DIS_DCACHE This bit be set to disable Dcache. (RO)

EFUSE_DIS_DOWNLOAD_ICACHE This bit be set to disable Icache in download mode (boot_mode[3:0] is 0, 1, 2, 3, 6, 7). (RO)

EFUSE_DIS_DOWNLOAD_DCACHE This bit be set to disable Dcache in download mode (boot_mode[3:0] is 0, 1, 2, 3, 6, 7). (RO)

EFUSE_DIS_FORCE_DOWNLOAD This bit be set to disable the function that forces chip into download mode. (RO)

EFUSE_DIS_USB_OTG This bit be set to disable USB OTG function. (RO)

EFUSE_DIS_TWAI This bit be set to disable TWAI function. (RO)

EFUSE_DIS_APP_CPU This bit be set to disable app cpu. (RO)

EFUSE_SOFT_DIS_JTAG These bits be set (odd number of bits set to 1 means disable) to disable JTAG with soft-disable method so that users can re-enable JTAG by HMAC module again. (RO)

EFUSE_DIS_PAD_JTAG This bit be set to disable JTAG permanently. (RO)

EFUSE_DIS_DOWNLOAD_MANUAL_ENCRYPT This bit be set to disable flash encryption when in download boot modes. (RO)

EFUSE_USB_EXCHG_PINS This bit be set to swap USB D+ and D- pins. (RO)

Note: The eFuse has a design flaw and does **not** move the pullup (needed to detect USB speed), resulting in the PC thinking the chip is a low-speed device, which stops communication. For detailed information, please refer to Chapter 29 *USB Serial/JTAG Controller (USB_SERIAL_JTAG)*.

EFUSE_EXT_PHY_ENABLE This bit be set to enable external PHY. (RO)

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Register 4.14. EFUSE_RD_REPEAT_DATA1_REG (0x0034)



EFUSE_VDD_SPI_XPD This bit be set to means SPI regulator power up. (RO)

EFUSE_VDD_SPI_TIEH SPI regulator output is short connected to VDD3P3_RTC_IO. (RO)

EFUSE_VDD_SPI_FORCE This bit be set to force using the parameters in eFuse to configure VDD_SPI. (RO)

EFUSE_WDT_DELAY_SEL Selects RTC watchdog timeout threshold, in unit of slow clock cycle. 00: 40000, 01: 80000, 10: 160000, 11:320000. (RO)

EFUSE_SPI_BOOT_CRYPT_CNT This bit be set to enable SPI boot encrypt/decrypt. Odd number of 1: enable. even number of 1: disable. (RO)

EFUSE_SECURE_BOOT_KEY_REVOKE0 This bit be set to revoke first secure boot key. (RO)

EFUSE_SECURE_BOOT_KEY_REVOKE1 This bit be set to revoke second secure boot key. (RO)

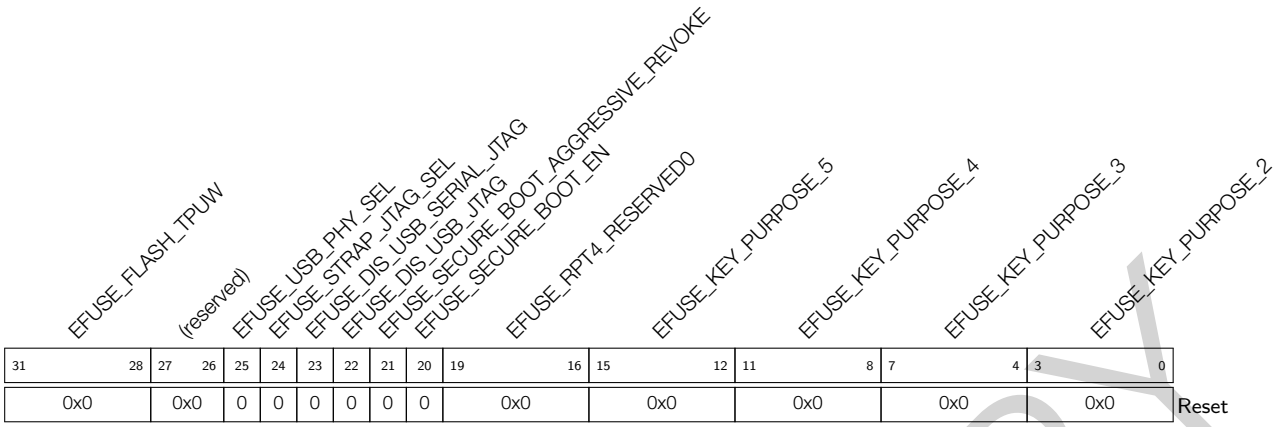
EFUSE_SECURE_BOOT_KEY_REVOKE2 This bit be set to revoke third secure boot key. (RO)

EFUSE_KEY_PURPOSE_0 Purpose of Key0. (RO)

EFUSE_KEY_PURPOSE_1 Purpose of Key1. (RO)

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Register 4.15. EFUSE_RD_REPEAT_DATA2_REG (0x0038)



EFUSE_KEY_PURPOSE_2 Purpose of Key2. (RO)

EFUSE_KEY_PURPOSE_3 Purpose of Key3. (RO)

EFUSE_KEY_PURPOSE_4 Purpose of Key4. (RO)

EFUSE_KEY_PURPOSE_5 Purpose of Key5. (RO)

EFUSE_RPT4_RESERVED0 Reserved (used four backups method). (RO)

EFUSE_SECURE_BOOT_EN This bit be set to enable secure boot. (RO)

EFUSE_SECURE_BOOT_AGGRESSIVE_REVOKE This bit be set to enable aggressive revoke of secure boot keys. (RO)

EFUSE_DIS_USB_JTAG This bit be set to disable USB OTG function that can be switched to JTAG interface. (RO)

EFUSE_DIS_USB_SERIAL_JTAG This bit be set to disable usb_serial_jtag function. (RO)

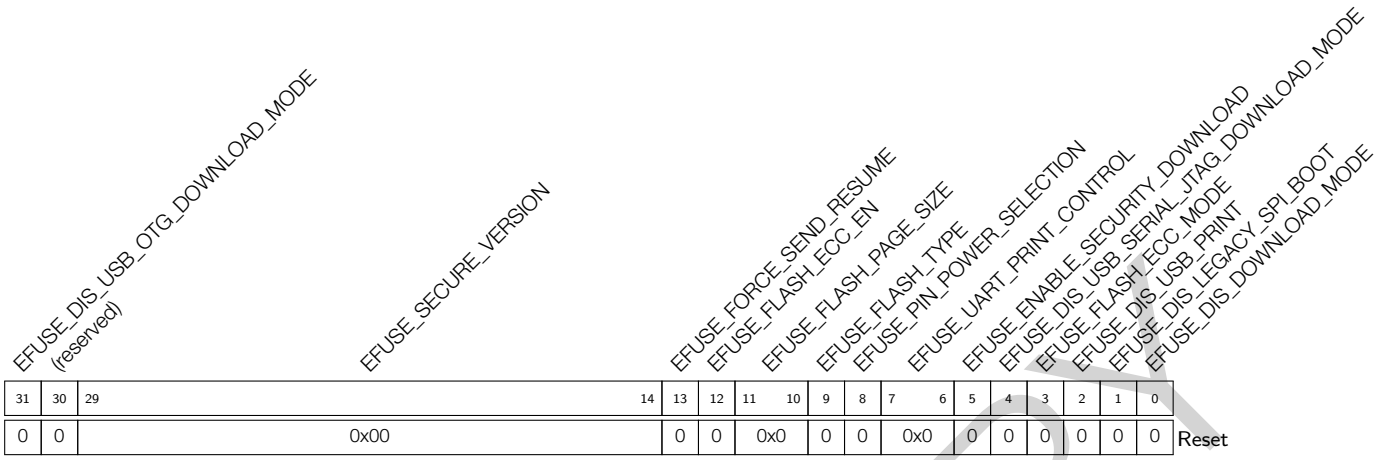
EFUSE_STRAP_JTAG_SEL This bit be set to enable selection between usb_to_jtag and pad_to_jtag through strapping GPIO3 when both reg_dis_usb_jtag and reg_dis_pad_jtag are equal to 0. (RO)

EFUSE_USB_PHY_SEL This bit is used to switch internal PHY and external PHY for USB OTG and USB Serial/JTAG. 0: internal PHY is assigned to USB Serial/JTAG while external PHY is assigned to USB OTG. 1: internal PHY is assigned to USB OTG while external PHY is assigned to USB Serial/JTAG. (RO)

EFUSE_FLASH_TPUW Configures flash waiting time after power-up, in unit of ms. If the value is less than 15, the waiting time is the configurable value. Otherwise, the waiting time is twice the configurable value. (RO)

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Register 4.16. EFUSE_RD_REPEAT_DATA3_REG (0x003C)



EFUSE_DIS_DOWNLOAD_MODE This bit be set to disable download mode (boot_mode[3:0] = 0, 1, 2, 3, 6, 7). (RO)

EFUSE_DIS_LEGACY_SPI_BOOT This bit be set to disable Legacy SPI boot mode (boot_mode[3:0] = 4). (RO)

EFUSE_DIS_USB_PRINT This bit be set to disable USB printing. (RO)

EFUSE_FLASH_ECC_MODE This bit be set to enable ECC mode in ROM, 0: Enable Flash ECC 16-to-18 byte mode in ROM. 1: Use 16-to-17 byte mode in ROM. (RO)

EFUSE_DIS_USB_SERIAL_JTAG_DOWNLOAD_MODE This bit be set to disable download through USB-Serial-JTAG. (RO)

EFUSE_ENABLE_SECURITY_DOWNLOAD This bit be set to enable secure UART download mode. (RO)

EFUSE_UART_PRINT_CONTROL This bit be set for the default UART boot message output mode. 00: Enabled. 01: Enabled when GPIO46 is low at reset. 10: Enabled when GPIO46 is high at reset. 11:disabled. (RO)

EFUSE_PIN_POWER_SELECTION GPIO33 ~ GPIO37 power supply selection while ROM code is executed. 0: VDD3P3_CPU. 1: VDD_SPI. (RO)

EFUSE_FLASH_TYPE Configures the maximum data lines of SPI flash. 0: four lines. 1: eight lines. (RO)

EFUSE_FLASH_PAGE_SIZE Configures flash page size. 0: 256 Byte; 1: 512 Byte; 2: 1 KB; 3: 2 KB. (RO)

EFUSE_FLASH_ECC_EN This bit be set to enable ECC for flash boot. (RO)

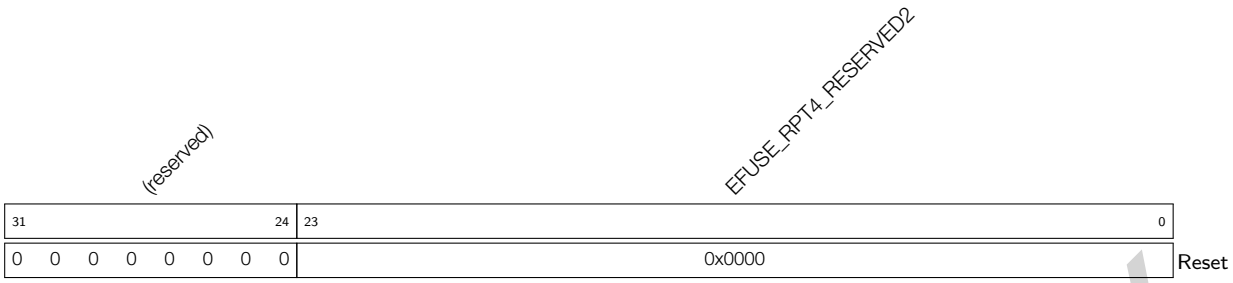
EFUSE_FORCE_SEND_RESUME This bit be set to force ROM code to send a resume command during SPI boot. (RO)

EFUSE_SECURE_VERSION Secure version (used by ESP-IDF anti-rollback feature). (RO)

EFUSE_DIS_USB_OTG_DOWNLOAD_MODE This bit be set to disable download through USB-OTG. (RO)

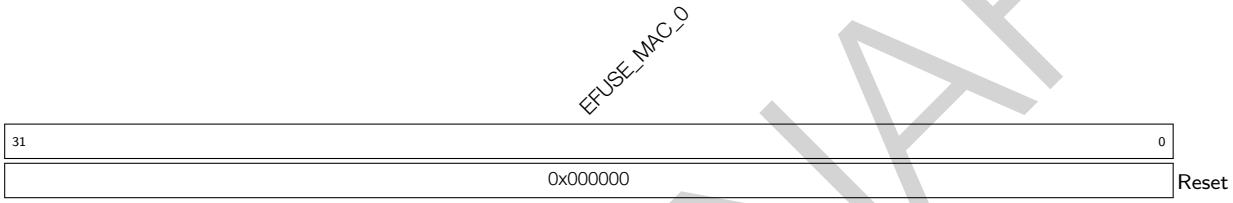
PRELIMINARY

Register 4.17. EFUSE_RD_REPEAT_DATA4_REG (0x0040)



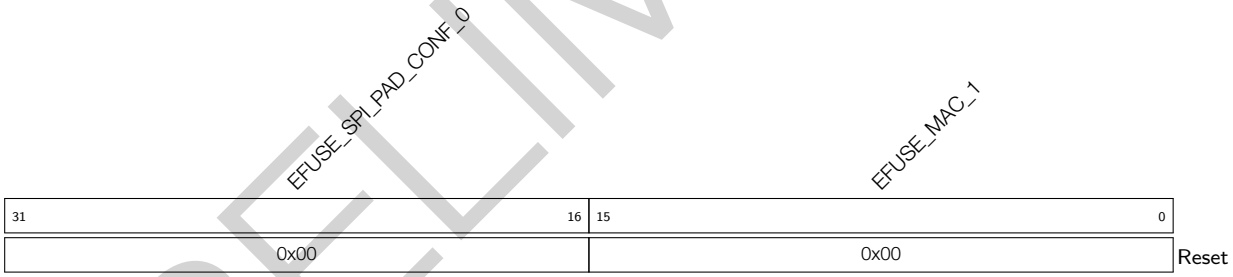
EFUSE_RPT4_RESERVED2 Reserved (used for four backups method). (RO)

Register 4.18. EFUSE_RD_MAC_SPI_SYS_0_REG (0x0044)



EFUSE_MAC_0 Stores the low 32 bits of MAC address. (RO)

Register 4.19. EFUSE_RD_MAC_SPI_SYS_1_REG (0x0048)

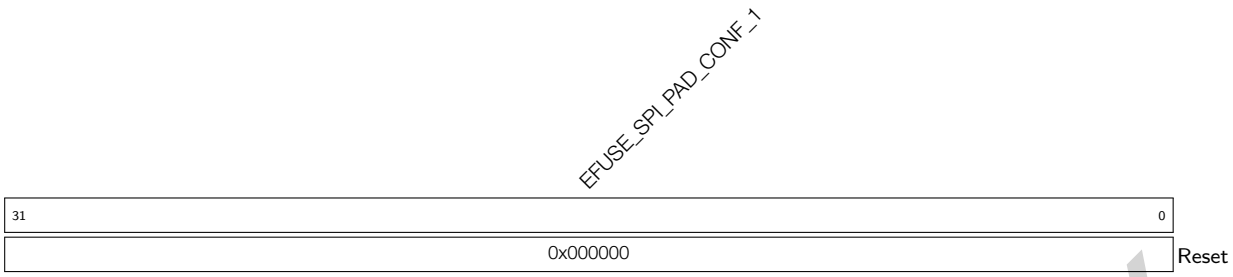


EFUSE_MAC_1 Stores the high 16 bits of MAC address. (RO)

EFUSE_SPI_PAD_CONF_0 Stores the first part of SPI_PAD_CONF. (RO)

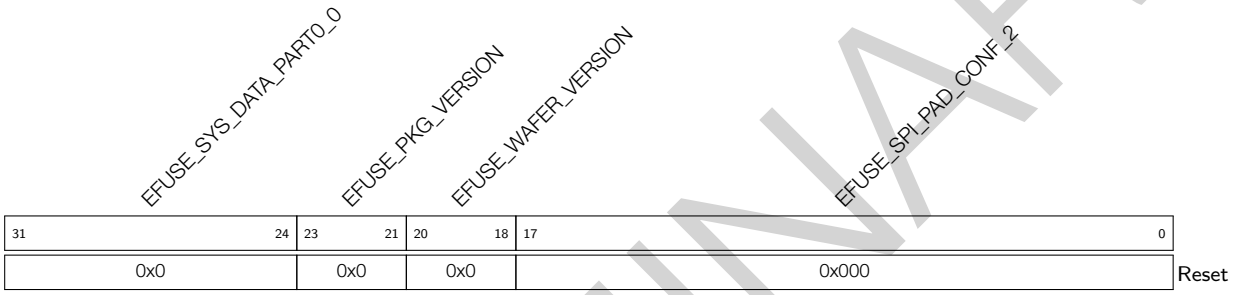
PRELIMINARY

Register 4.20. EFUSE_RD_MAC_SPI_SYS_2_REG (0x004C)



EFUSE_SPI_PAD_CONF_1 Stores the second part of SPI_PAD_CONF. (RO)

Register 4.21. EFUSE_RD_MAC_SPI_SYS_3_REG (0x0050)



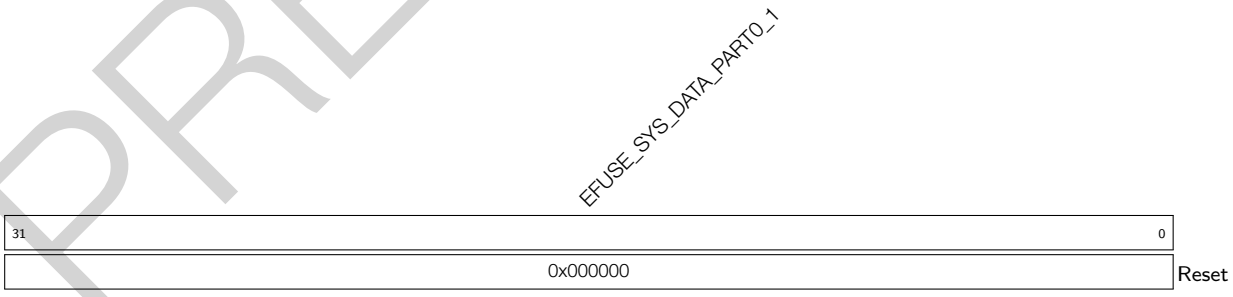
EFUSE_SPI_PAD_CONF_2 Stores the second part of SPI_PAD_CONF. (RO)

EFUSE_WAFER_VERSION Stores wafer version information. (RO)

EFUSE_PKG_VERSION Stores package version information. (RO)

EFUSE_SYS_DATA_PART0_0 Stores the bits 0~7 of the first part of system data. (RO)

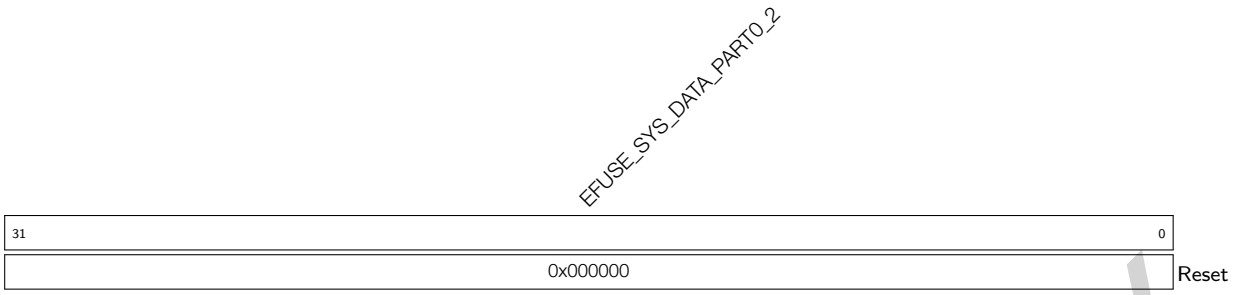
Register 4.22. EFUSE_RD_MAC_SPI_SYS_4_REG (0x0054)



EFUSE_SYS_DATA_PART0_1 Stores the bits 8~39 of the first part of system data. (RO)

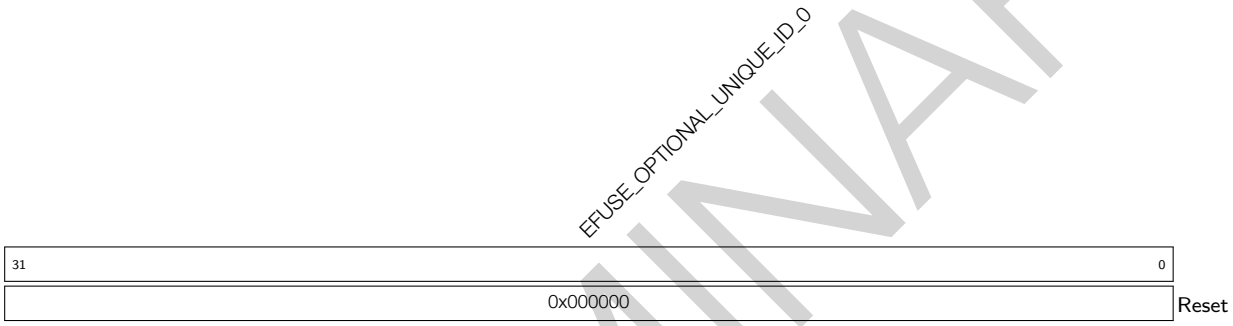
PRELIMINARY

Register 4.23. EFUSE_RD_MAC_SPI_SYS_5_REG (0x0058)



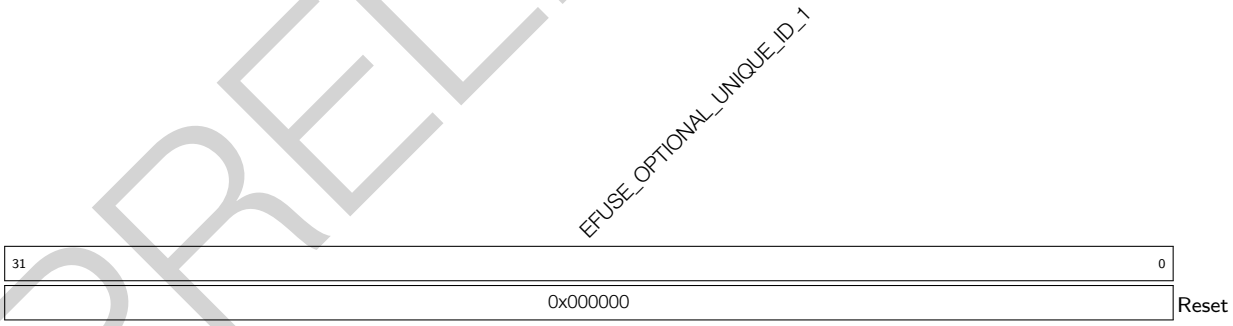
EFUSE_SYS_DATA_PART0_2 Stores the bits 40~71 of the first part of system data. (RO)

Register 4.24. EFUSE_RD_SYS_PART1_DATA0_REG (0x005C)



EFUSE_OPTIONAL_UNIQUE_ID_0 Stores the bits 0~31 of the optional unique id information. (RO)

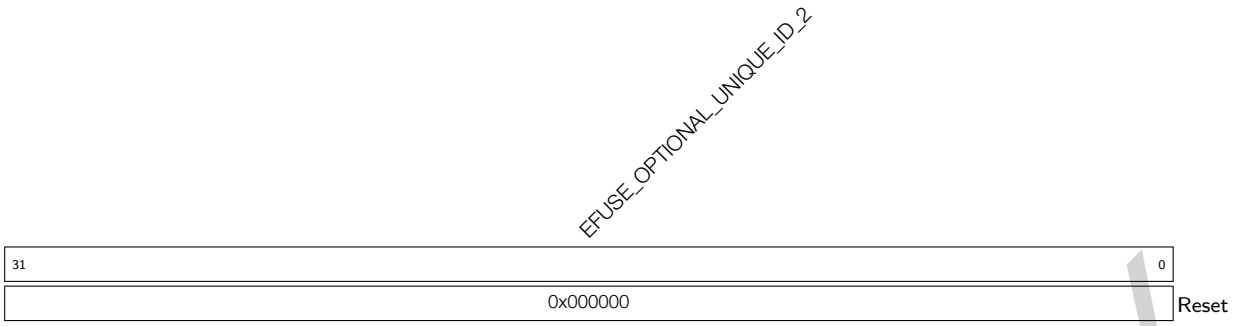
Register 4.25. EFUSE_RD_SYS_PART1_DATA1_REG (0x0060)



EFUSE_OPTIONAL_UNIQUE_ID_1 Stores the bits 32~63 of the optional unique id information. (RO)

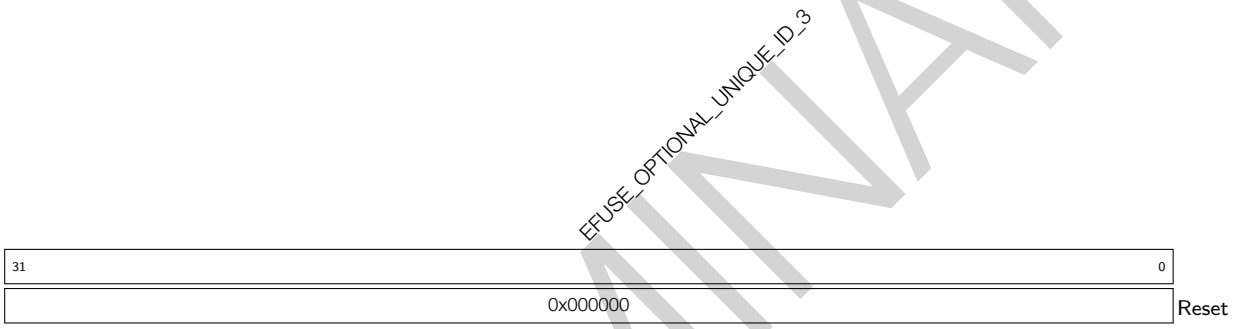
PRELIMINARY

Register 4.26. EFUSE_RD_SYS_PART1_DATA2_REG (0x0064)



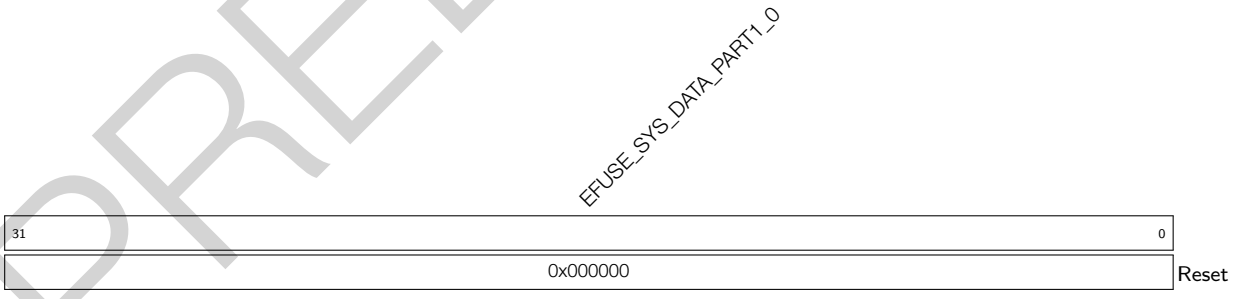
EFUSE_OPTIONAL_UNIQUE_ID_2 Stores the bits 64~95 of the optional unique id information. (RO)

Register 4.27. EFUSE_RD_SYS_PART1_DATA3_REG (0x0068)



EFUSE_OPTIONAL_UNIQUE_ID_3 Stores the bits 96~127 of the optional unique id information. (RO)

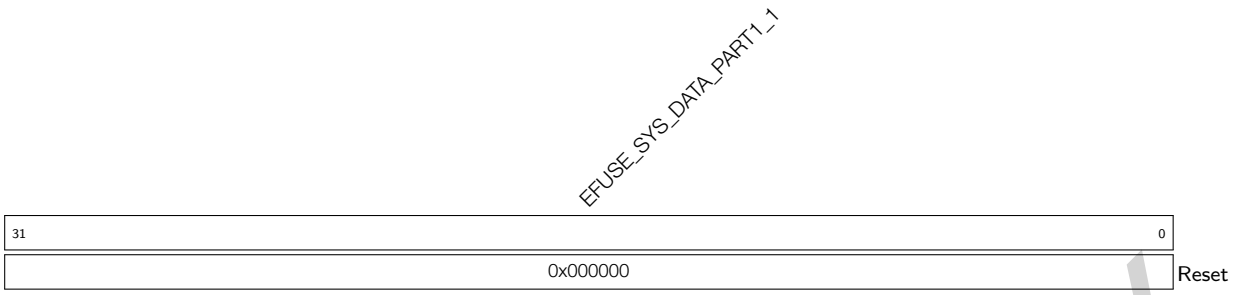
Register 4.28. EFUSE_RD_SYS_PART1_DATA4_REG (0x006C)



EFUSE_SYS_DATA_PART1_0 Stores the first 32 bits of the second part of system data. (RO)

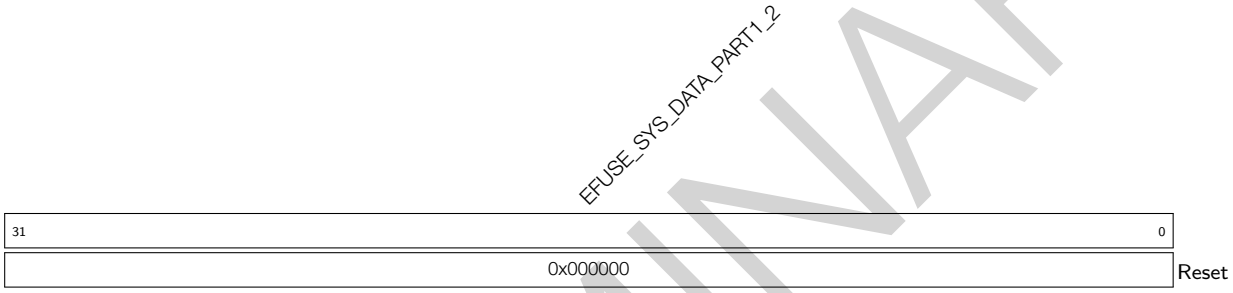
PRELIMINARY

Register 4.29. EFUSE_RD_SYS_PART1_DATA5_REG (0x0070)



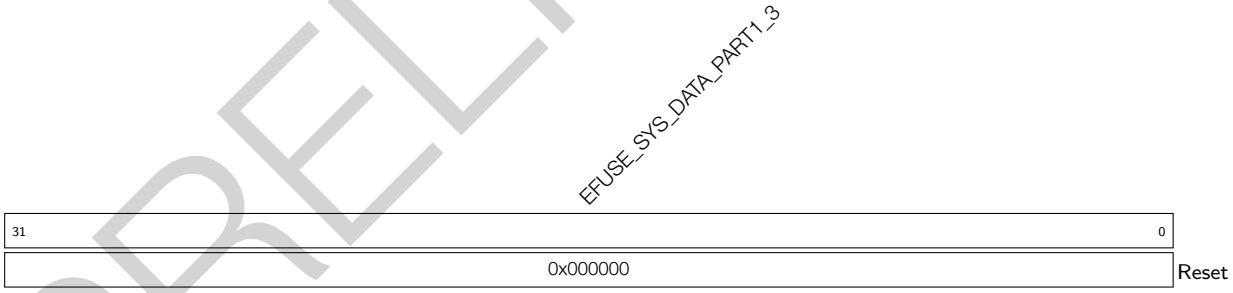
EFUSE_SYS_DATA_PART1_1 Stores the second 32 bits of the seconde part of system data. (RO)

Register 4.30. EFUSE_RD_SYS_PART1_DATA6_REG (0x0074)



EFUSE_SYS_DATA_PART1_2 Stores the third 32 bits of the second part of system data. (RO)

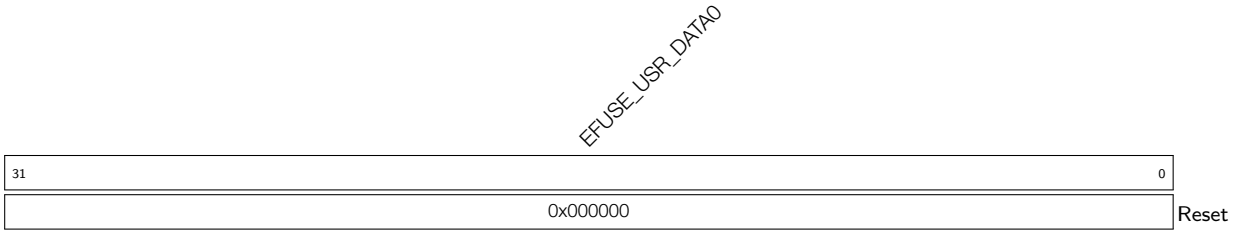
Register 4.31. EFUSE_RD_SYS_PART1_DATA7_REG (0x0078)



EFUSE_SYS_DATA_PART1_3 Stores the fourth 32 bits of the second part of system data. (RO)

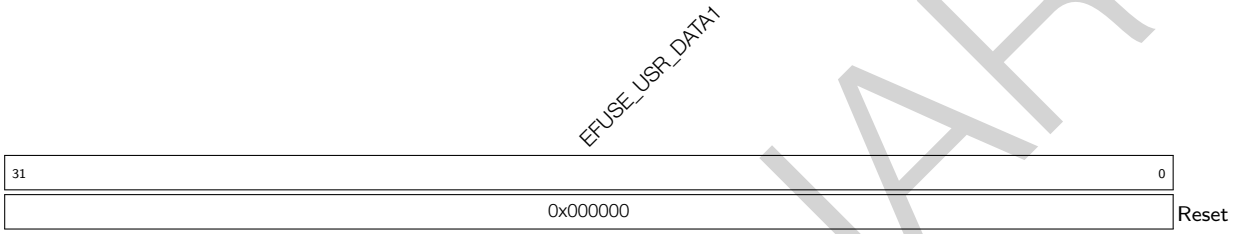
PRELIMINARY

Register 4.32. EFUSE_RD_USR_DATA0_REG (0x007C)



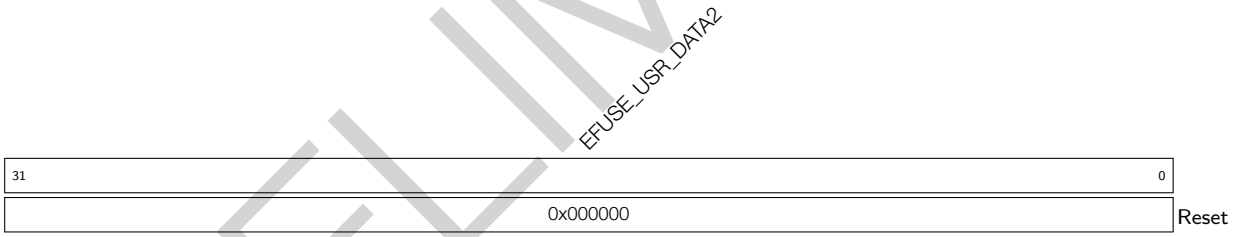
EFUSE_USR_DATA0 Stores the bits [0:31] of BLOCK3 (user). (RO)

Register 4.33. EFUSE_RD_USR_DATA1_REG (0x0080)



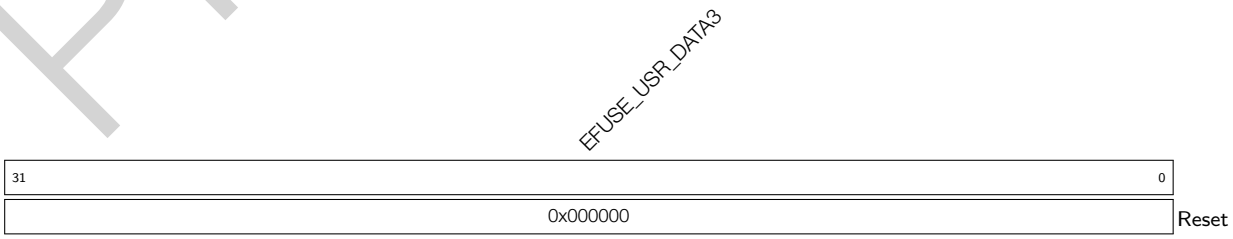
EFUSE_USR_DATA1 Stores the bits [32:63] of BLOCK3 (user). (RO)

Register 4.34. EFUSE_RD_USR_DATA2_REG (0x0084)



EFUSE_USR_DATA2 Stores the bits [64:95] of BLOCK3 (user). (RO)

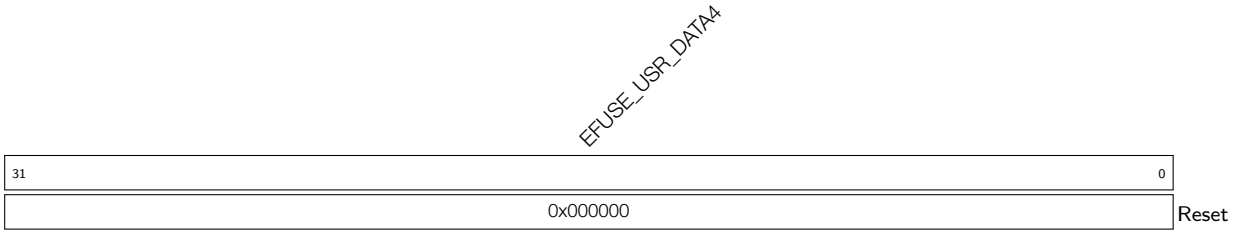
Register 4.35. EFUSE_RD_USR_DATA3_REG (0x0088)



EFUSE_USR_DATA3 Stores the bits [96:127] of BLOCK3 (user). (RO)

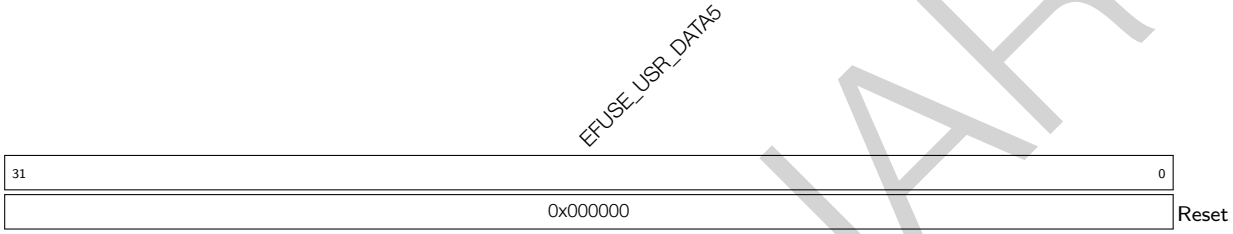
PRELIMINARY

Register 4.36. EFUSE_RD_USR_DATA4_REG (0x008C)



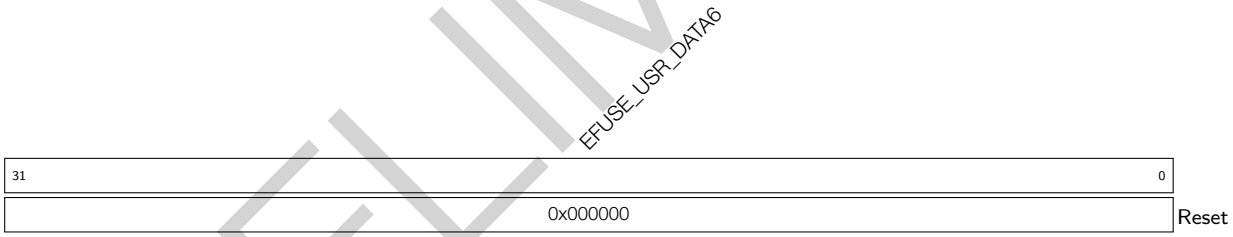
EFUSE_USR_DATA4 Stores the bits [128:159] of BLOCK3 (user). (RO)

Register 4.37. EFUSE_RD_USR_DATA5_REG (0x0090)



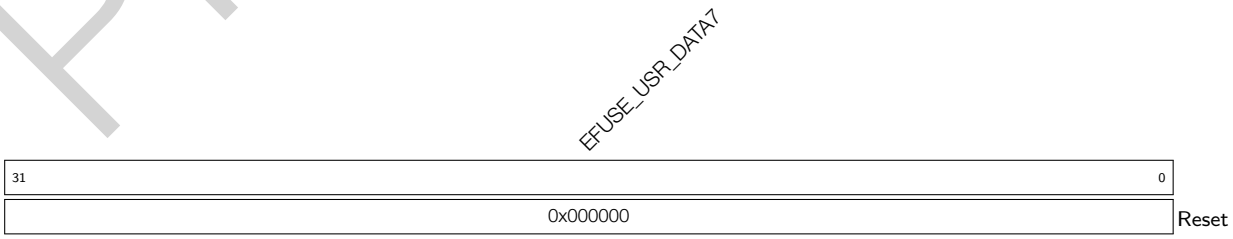
EFUSE_USR_DATA5 Stores the bits [160:191] of BLOCK3 (user). (RO)

Register 4.38. EFUSE_RD_USR_DATA6_REG (0x0094)



EFUSE_USR_DATA6 Stores the bits [192:223] of BLOCK3 (user). (RO)

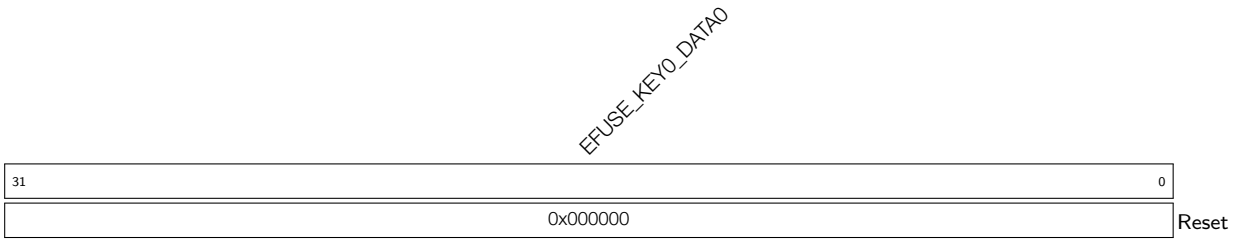
Register 4.39. EFUSE_RD_USR_DATA7_REG (0x0098)



EFUSE_USR_DATA7 Stores the bits [224:255] of BLOCK3 (user). (RO)

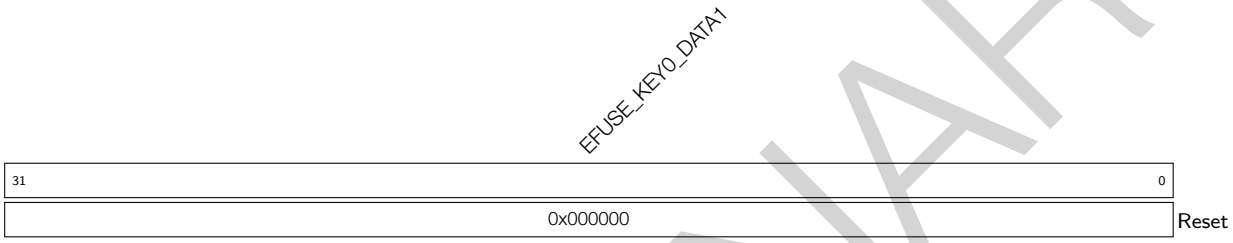
PRELIMINARY

Register 4.40. EFUSE_RD_KEY0_DATA0_REG (0x009C)



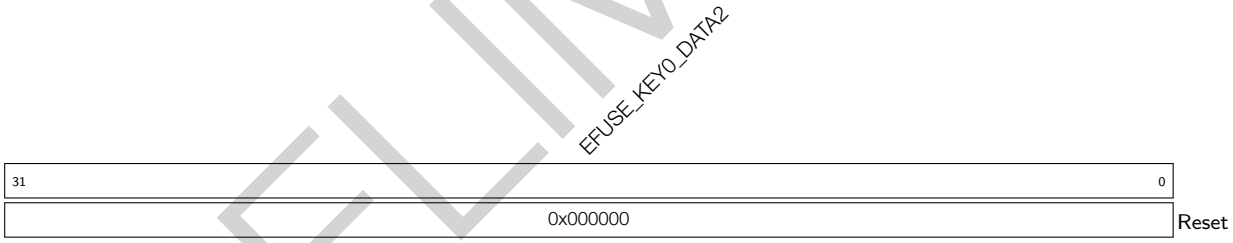
EFUSE_KEY0_DATA0 Stores the first 32 bits of KEY0. (RO)

Register 4.41. EFUSE_RD_KEY0_DATA1_REG (0x00A0)



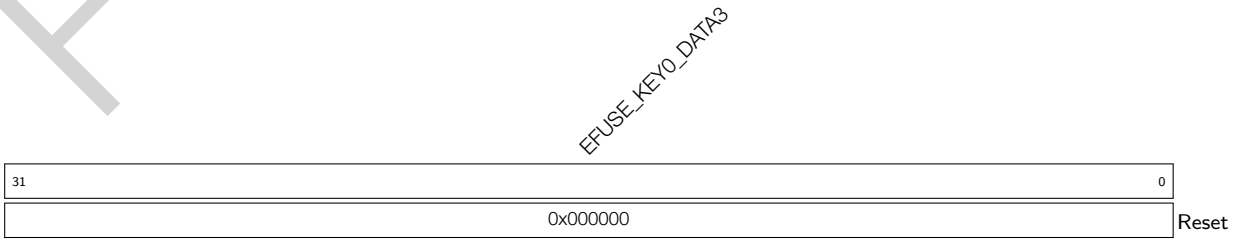
EFUSE_KEY0_DATA1 Stores the second 32 bits of KEY0. (RO)

Register 4.42. EFUSE_RD_KEY0_DATA2_REG (0x00A4)



EFUSE_KEY0_DATA2 Stores the third 32 bits of KEY0. (RO)

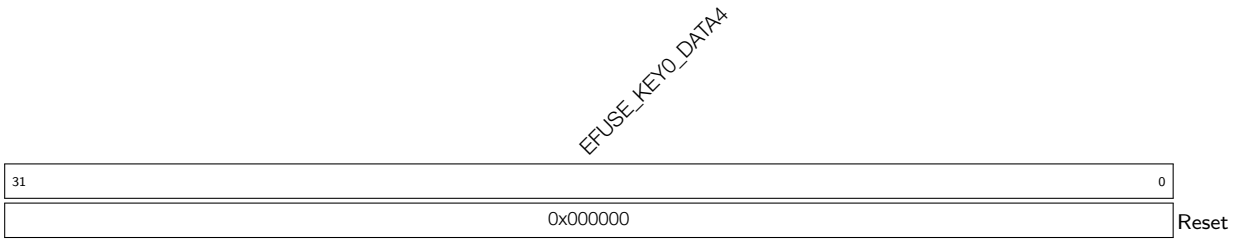
Register 4.43. EFUSE_RD_KEY0_DATA3_REG (0x00A8)



EFUSE_KEY0_DATA3 Stores the fourth 32 bits of KEY0. (RO)

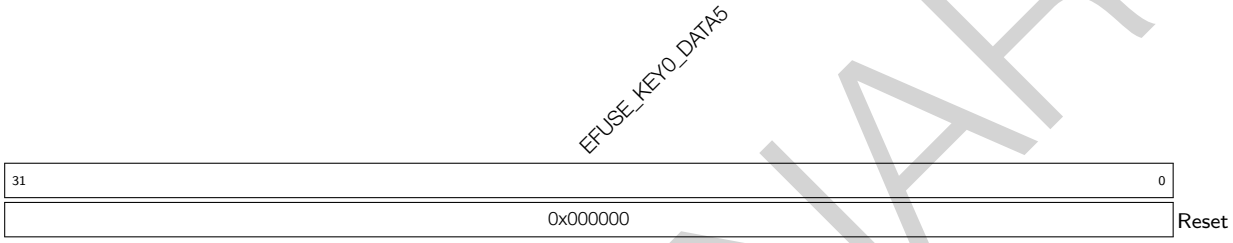
PRELIMINARY

Register 4.44. EFUSE_RD_KEY0_DATA4_REG (0x00AC)



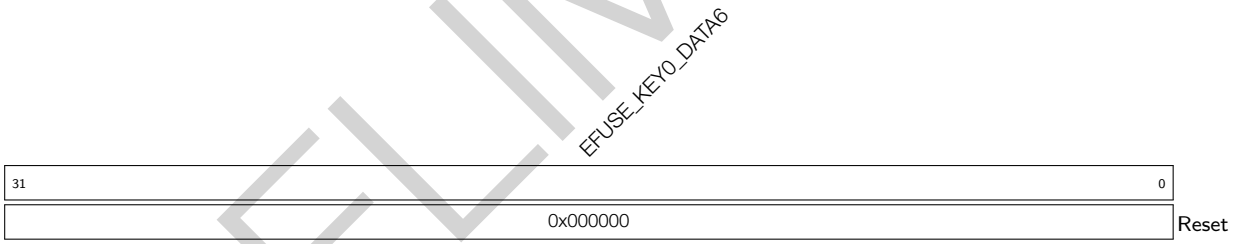
EFUSE_KEY0_DATA4 Stores the fifth 32 bits of KEY0. (RO)

Register 4.45. EFUSE_RD_KEY0_DATA5_REG (0x00B0)



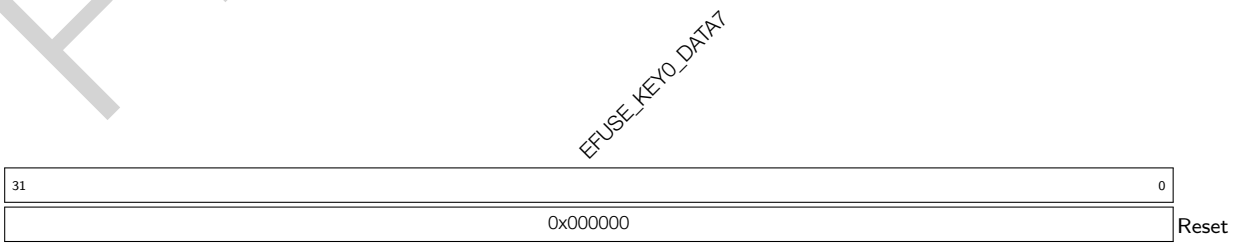
EFUSE_KEY0_DATA5 Stores the sixth 32 bits of KEY0. (RO)

Register 4.46. EFUSE_RD_KEY0_DATA6_REG (0x00B4)



EFUSE_KEY0_DATA6 Stores the seventh 32 bits of KEY0. (RO)

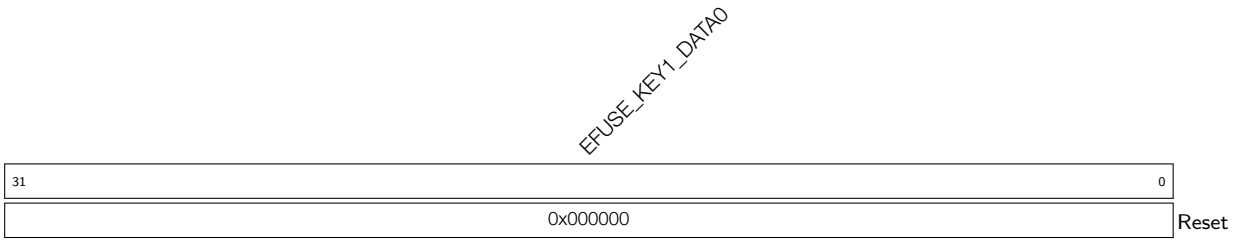
Register 4.47. EFUSE_RD_KEY0_DATA7_REG (0x00B8)



EFUSE_KEY0_DATA7 Stores the eighth 32 bits of KEY0. (RO)

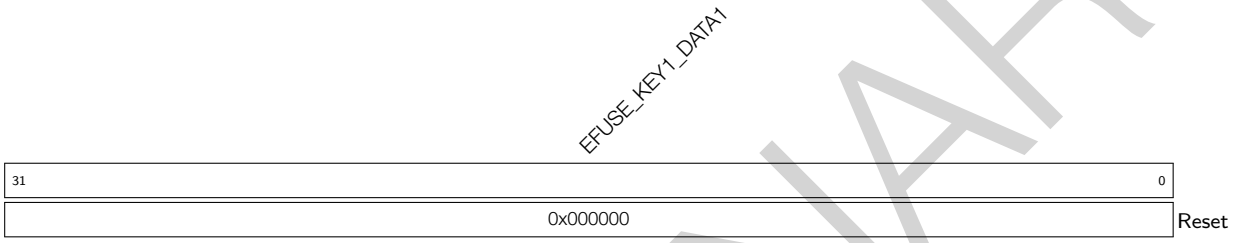
PRELIMINARY

Register 4.48. EFUSE_RD_KEY1_DATA0_REG (0x00BC)



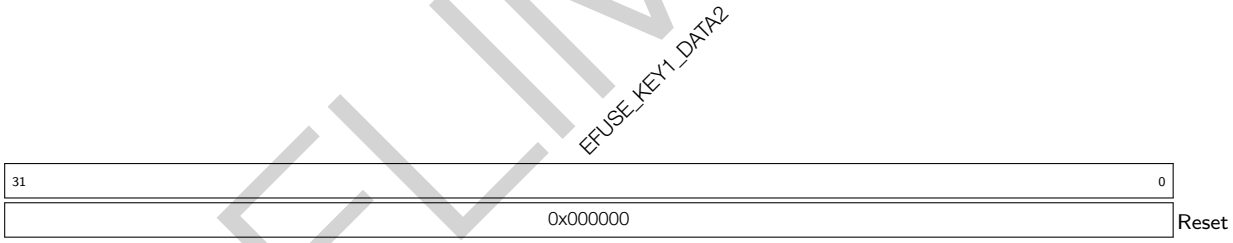
EFUSE_KEY1_DATA0 Stores the first 32 bits of KEY1. (RO)

Register 4.49. EFUSE_RD_KEY1_DATA1_REG (0x00C0)



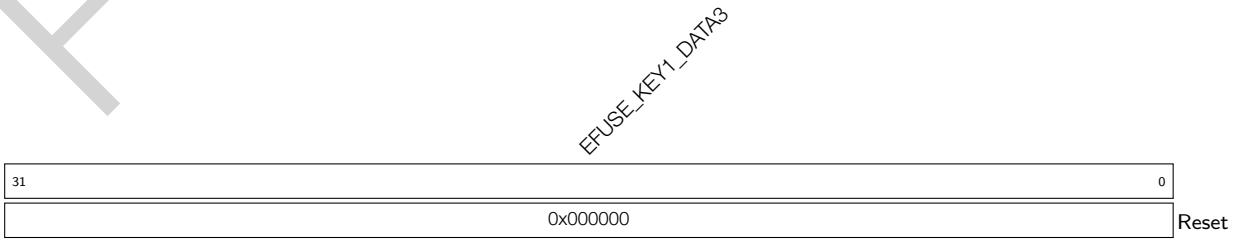
EFUSE_KEY1_DATA1 Stores the second 32 bits of KEY1. (RO)

Register 4.50. EFUSE_RD_KEY1_DATA2_REG (0x00C4)



EFUSE_KEY1_DATA2 Stores the third 32 bits of KEY1. (RO)

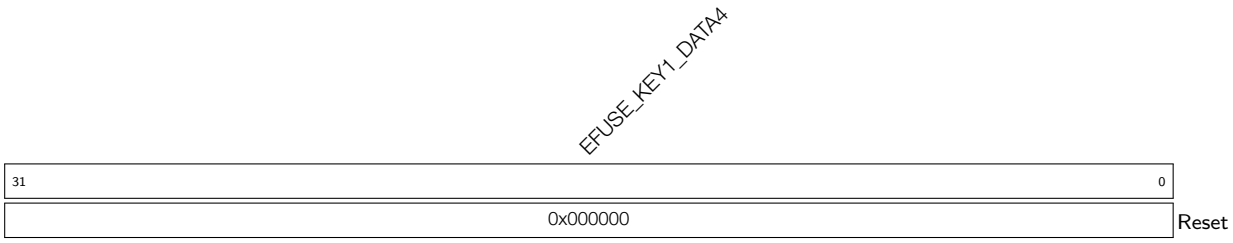
Register 4.51. EFUSE_RD_KEY1_DATA3_REG (0x00C8)



EFUSE_KEY1_DATA3 Stores the fourth 32 bits of KEY1. (RO)

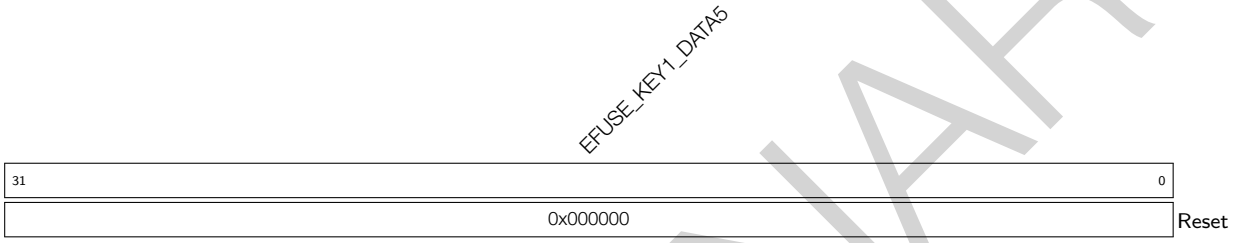
PRELIMINARY

Register 4.52. EFUSE_RD_KEY1_DATA4_REG (0x00CC)



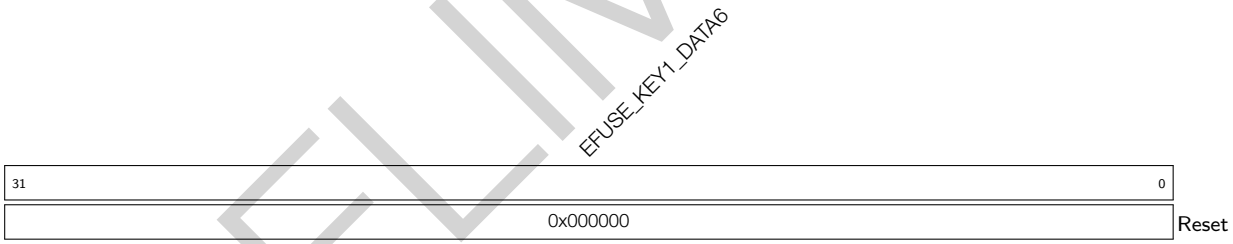
EFUSE_KEY1_DATA4 Stores the fifth 32 bits of KEY1. (RO)

Register 4.53. EFUSE_RD_KEY1_DATA5_REG (0x00D0)



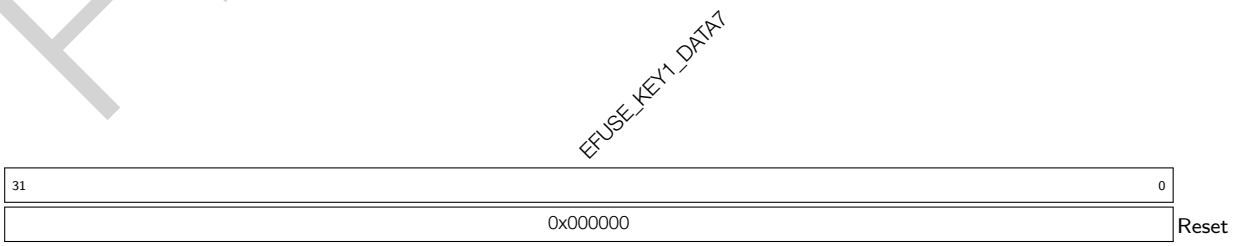
EFUSE_KEY1_DATA5 Stores the sixth 32 bits of KEY1. (RO)

Register 4.54. EFUSE_RD_KEY1_DATA6_REG (0x00D4)



EFUSE_KEY1_DATA6 Stores the seventh 32 bits of KEY1. (RO)

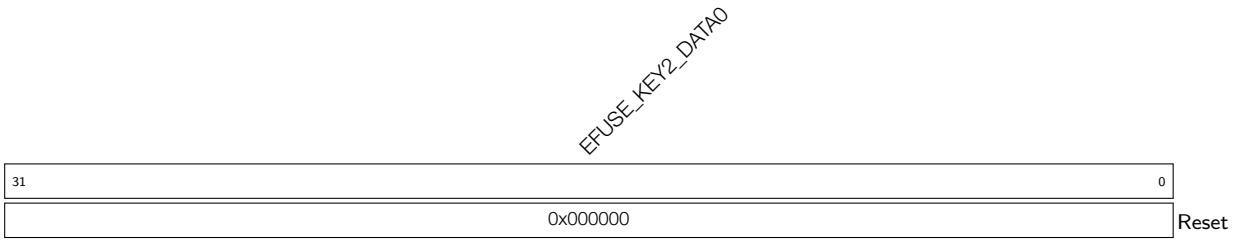
Register 4.55. EFUSE_RD_KEY1_DATA7_REG (0x00D8)



EFUSE_KEY1_DATA7 Stores the eighth 32 bits of KEY1. (RO)

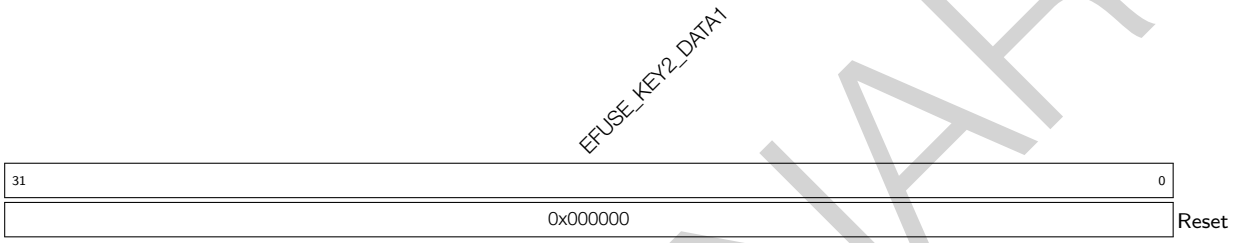
PRELIMINARY

Register 4.56. EFUSE_RD_KEY2_DATA0_REG (0x00DC)



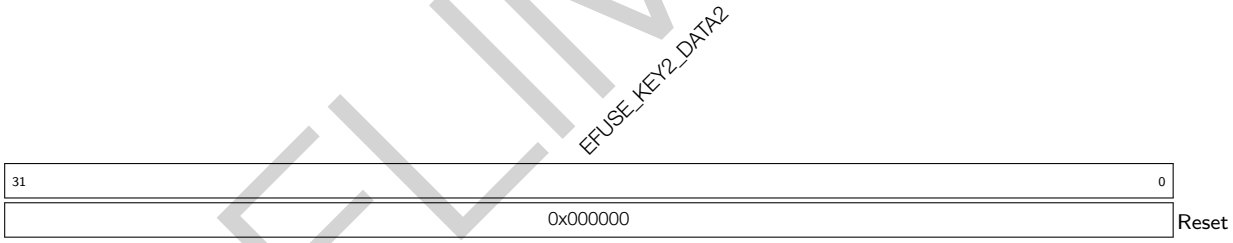
EFUSE_KEY2_DATA0 Stores the first 32 bits of KEY2. (RO)

Register 4.57. EFUSE_RD_KEY2_DATA1_REG (0x00E0)



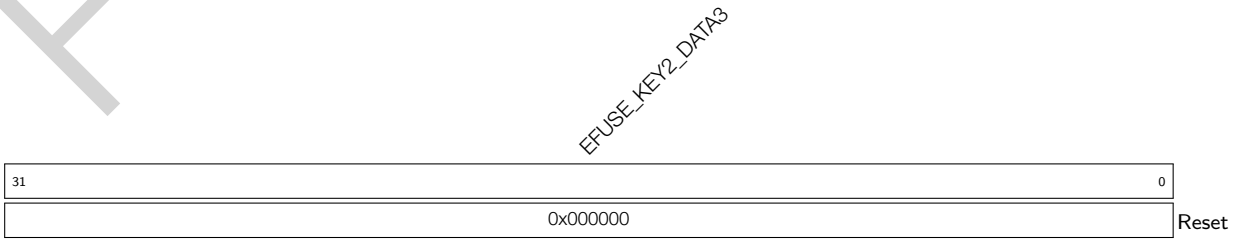
EFUSE_KEY2_DATA1 Stores the second 32 bits of KEY2. (RO)

Register 4.58. EFUSE_RD_KEY2_DATA2_REG (0x00E4)



EFUSE_KEY2_DATA2 Stores the third 32 bits of KEY2. (RO)

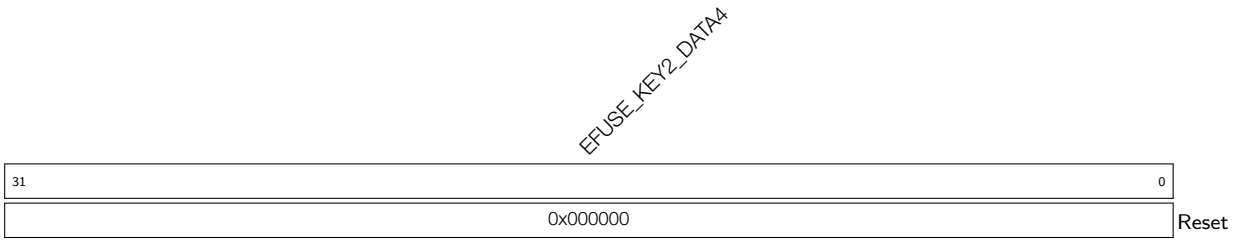
Register 4.59. EFUSE_RD_KEY2_DATA3_REG (0x00E8)



EFUSE_KEY2_DATA3 Stores the fourth 32 bits of KEY2. (RO)

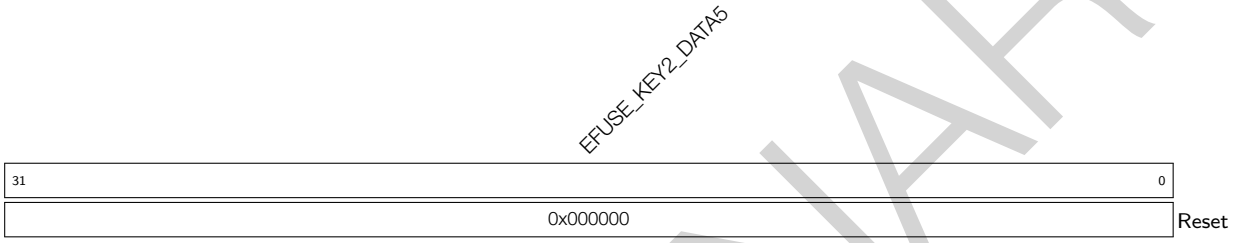
PRELIMINARY

Register 4.60. EFUSE_RD_KEY2_DATA4_REG (0x00EC)



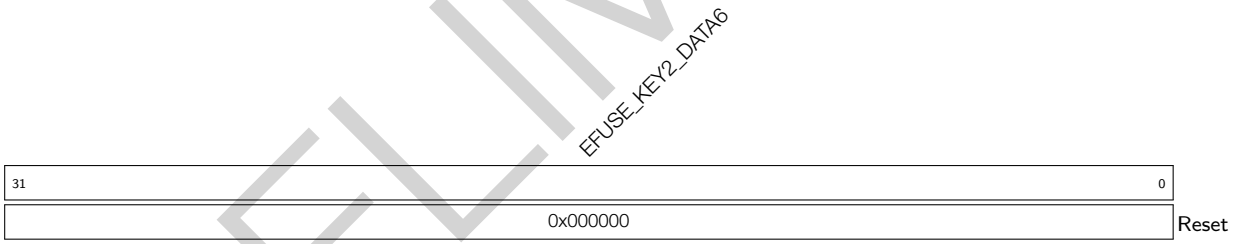
EFUSE_KEY2_DATA4 Stores the fifth 32 bits of KEY2. (RO)

Register 4.61. EFUSE_RD_KEY2_DATA5_REG (0x00F0)



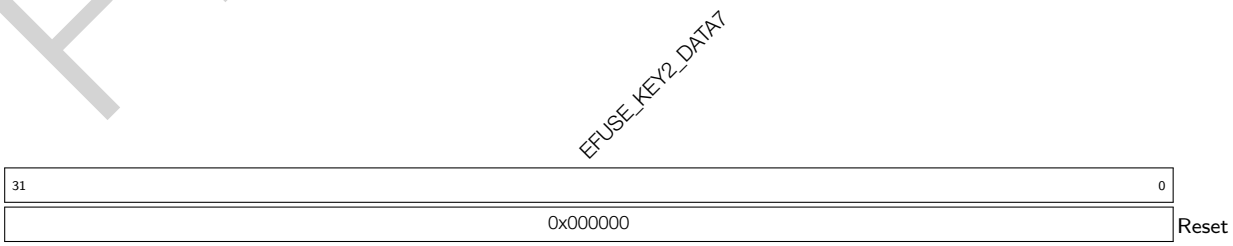
EFUSE_KEY2_DATA5 Stores the sixth 32 bits of KEY2. (RO)

Register 4.62. EFUSE_RD_KEY2_DATA6_REG (0x00F4)



EFUSE_KEY2_DATA6 Stores the seventh 32 bits of KEY2. (RO)

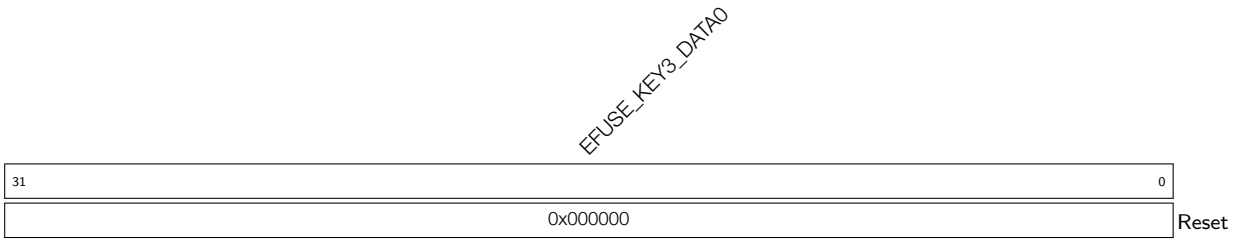
Register 4.63. EFUSE_RD_KEY2_DATA7_REG (0x00F8)



EFUSE_KEY2_DATA7 Stores the eighth 32 bits of KEY2. (RO)

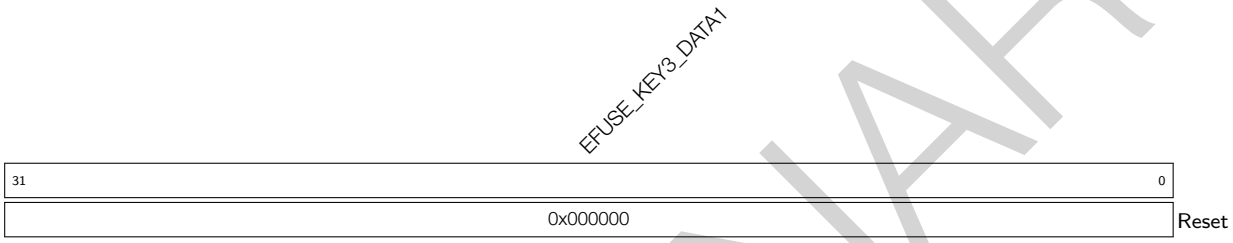
PRELIMINARY

Register 4.64. EFUSE_RD_KEY3_DATA0_REG (0x00FC)



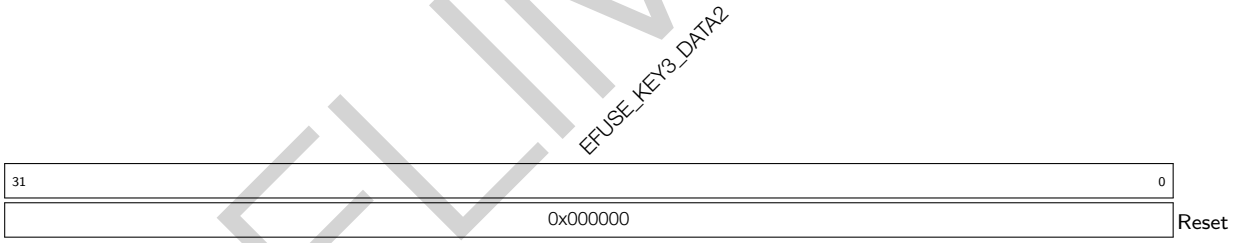
EFUSE_KEY3_DATA0 Stores the first 32 bits of KEY3. (RO)

Register 4.65. EFUSE_RD_KEY3_DATA1_REG (0x0100)



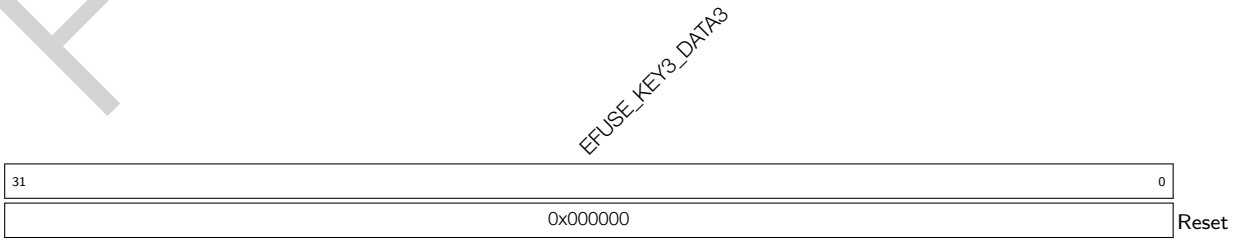
EFUSE_KEY3_DATA1 Stores the second 32 bits of KEY3. (RO)

Register 4.66. EFUSE_RD_KEY3_DATA2_REG (0x0104)



EFUSE_KEY3_DATA2 Stores the third 32 bits of KEY3. (RO)

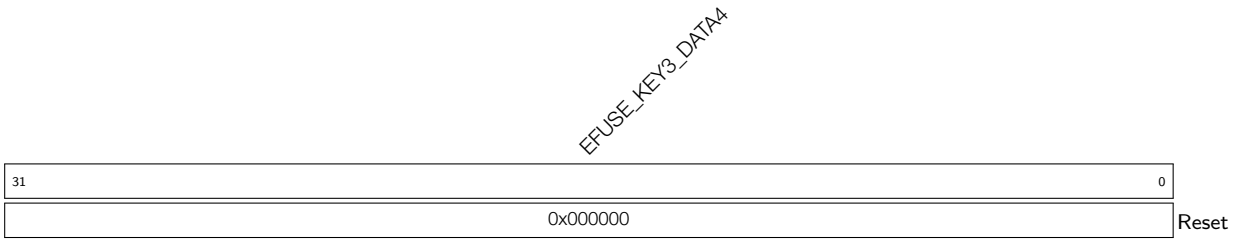
Register 4.67. EFUSE_RD_KEY3_DATA3_REG (0x0108)



EFUSE_KEY3_DATA3 Stores the fourth 32 bits of KEY3. (RO)

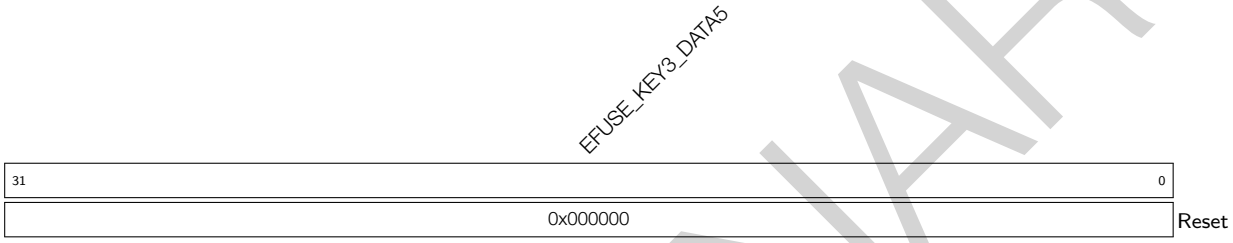
PRELIMINARY

Register 4.68. EFUSE_RD_KEY3_DATA4_REG (0x010C)



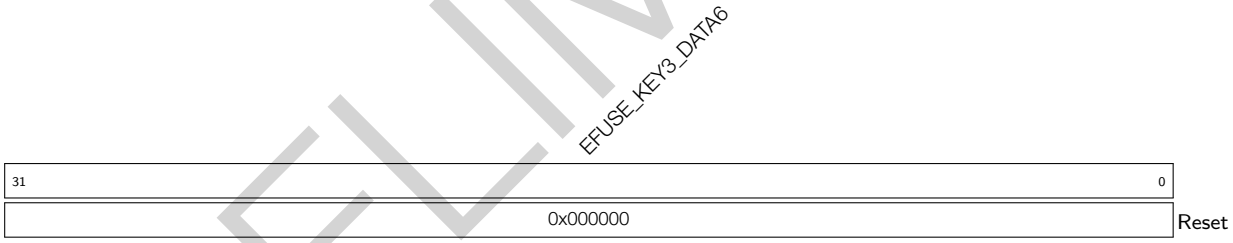
EFUSE_KEY3_DATA4 Stores the fifth 32 bits of KEY3. (RO)

Register 4.69. EFUSE_RD_KEY3_DATA5_REG (0x0110)



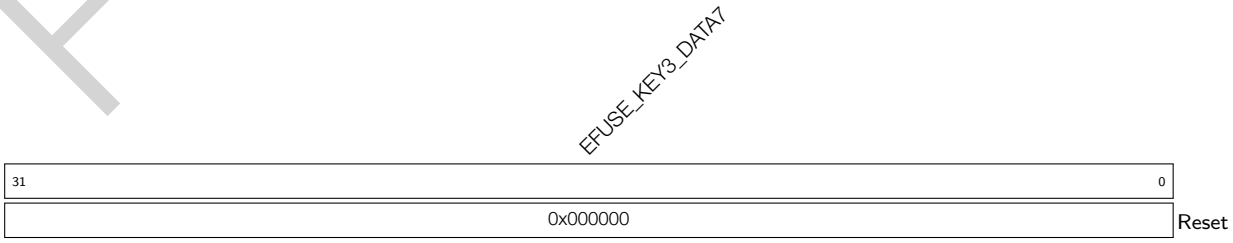
EFUSE_KEY3_DATA5 Stores the sixth 32 bits of KEY3. (RO)

Register 4.70. EFUSE_RD_KEY3_DATA6_REG (0x0114)



EFUSE_KEY3_DATA6 Stores the seventh 32 bits of KEY3. (RO)

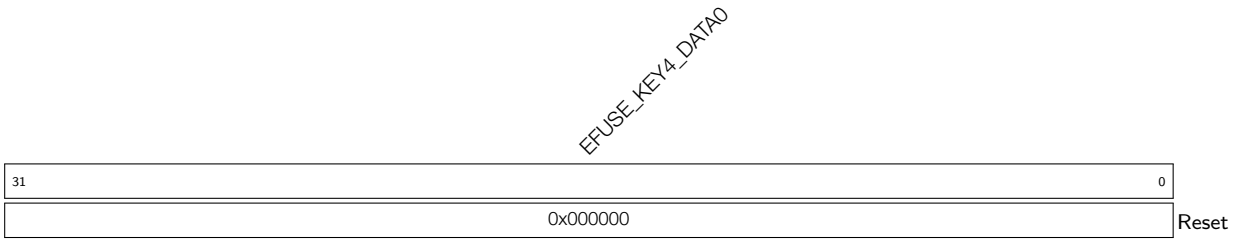
Register 4.71. EFUSE_RD_KEY3_DATA7_REG (0x0118)



EFUSE_KEY3_DATA7 Stores the eighth 32 bits of KEY3. (RO)

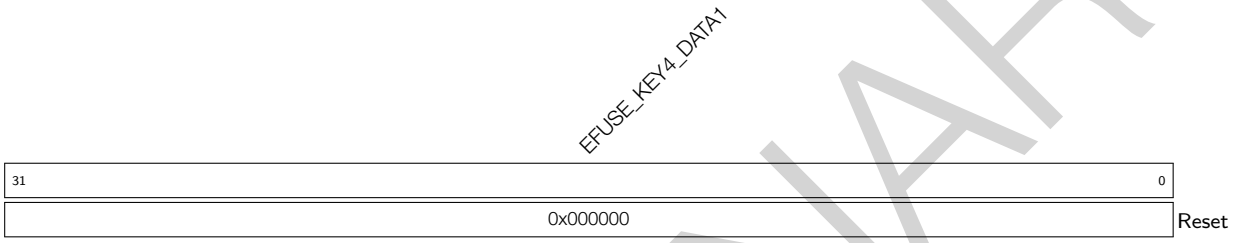
PRELIMINARY

Register 4.72. EFUSE_RD_KEY4_DATA0_REG (0x011C)



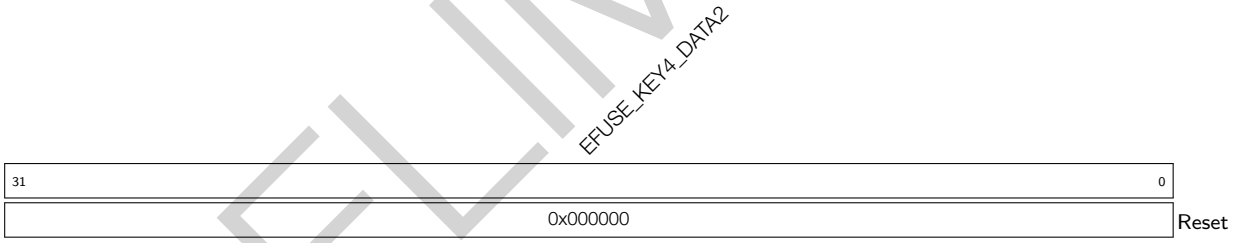
EFUSE_KEY4_DATA0 Stores the first 32 bits of KEY4. (RO)

Register 4.73. EFUSE_RD_KEY4_DATA1_REG (0x0120)



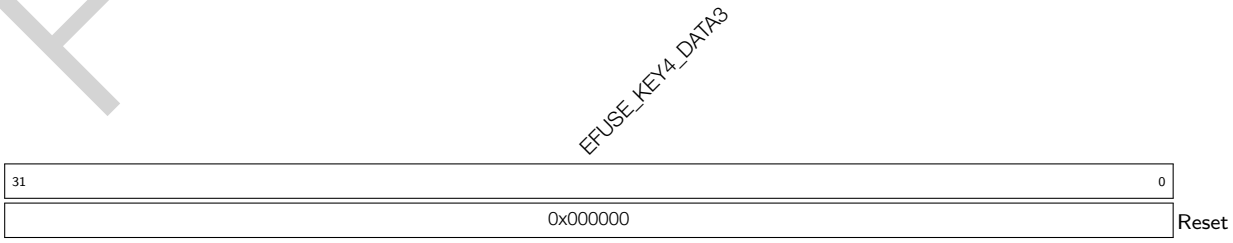
EFUSE_KEY4_DATA1 Stores the second 32 bits of KEY4. (RO)

Register 4.74. EFUSE_RD_KEY4_DATA2_REG (0x0124)



EFUSE_KEY4_DATA2 Stores the third 32 bits of KEY4. (RO)

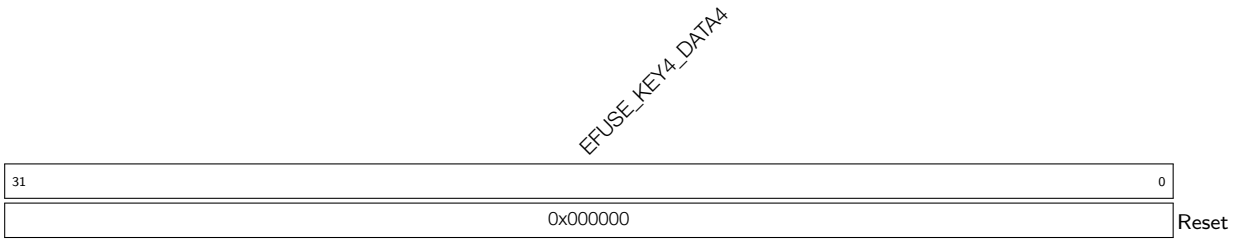
Register 4.75. EFUSE_RD_KEY4_DATA3_REG (0x0128)



EFUSE_KEY4_DATA3 Stores the fourth 32 bits of KEY4. (RO)

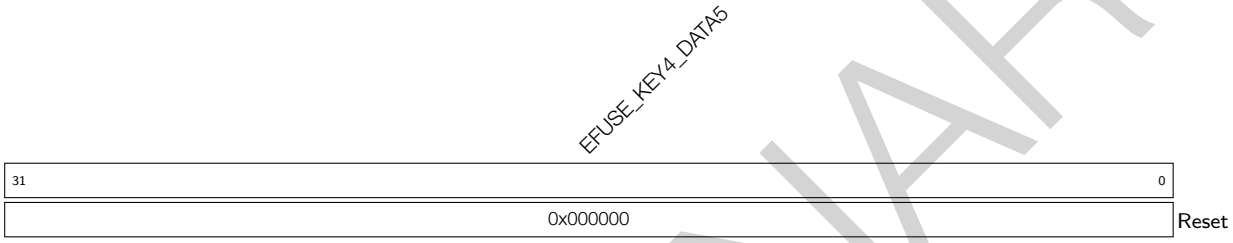
PRELIMINARY

Register 4.76. EFUSE_RD_KEY4_DATA4_REG (0x012C)



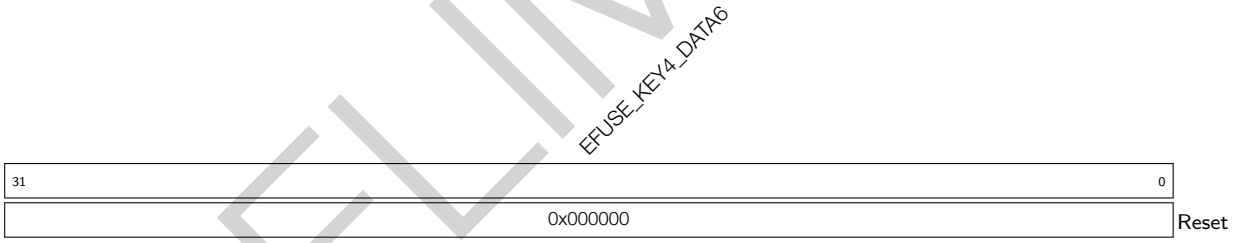
EFUSE_KEY4_DATA4 Stores the fifth 32 bits of KEY4. (RO)

Register 4.77. EFUSE_RD_KEY4_DATA5_REG (0x0130)



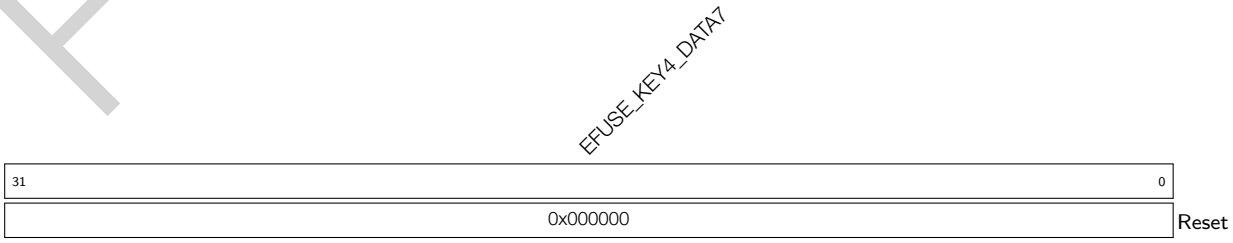
EFUSE_KEY4_DATA5 Stores the sixth 32 bits of KEY4. (RO)

Register 4.78. EFUSE_RD_KEY4_DATA6_REG (0x0134)



EFUSE_KEY4_DATA6 Stores the seventh 32 bits of KEY4. (RO)

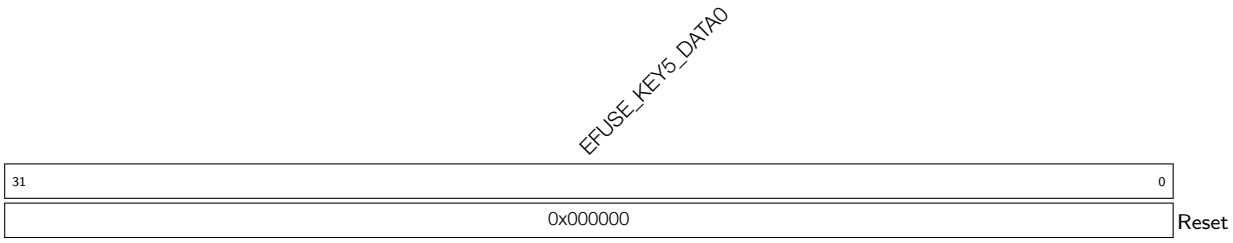
Register 4.79. EFUSE_RD_KEY4_DATA7_REG (0x0138)



EFUSE_KEY4_DATA7 Stores the eighth 32 bits of KEY4. (RO)

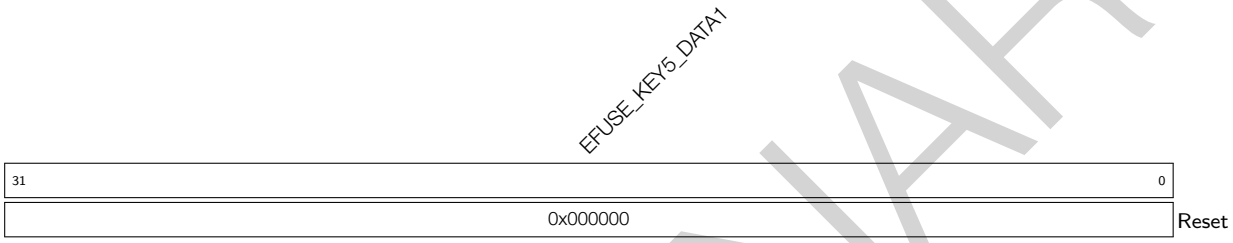
PRELIMINARY

Register 4.80. EFUSE_RD_KEY5_DATA0_REG (0x013C)



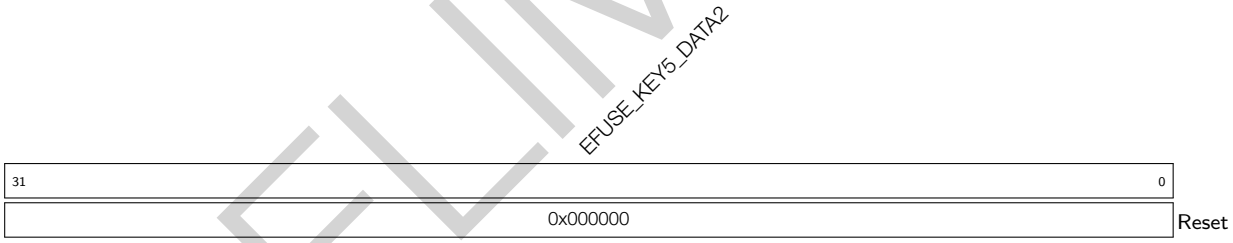
EFUSE_KEY5_DATA0 Stores the first 32 bits of KEY5. (RO)

Register 4.81. EFUSE_RD_KEY5_DATA1_REG (0x0140)



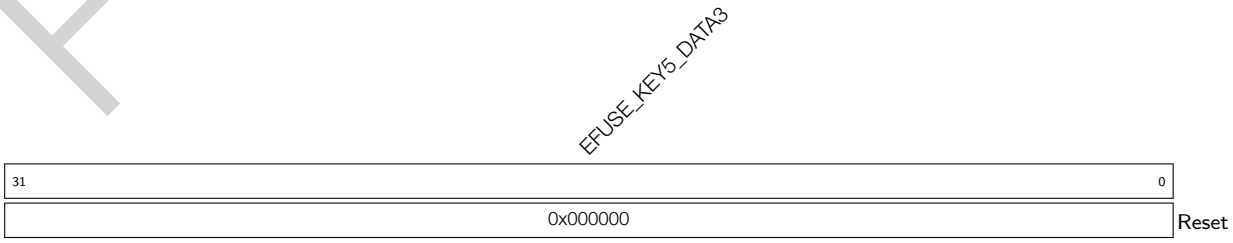
EFUSE_KEY5_DATA1 Stores the second 32 bits of KEY5. (RO)

Register 4.82. EFUSE_RD_KEY5_DATA2_REG (0x0144)



EFUSE_KEY5_DATA2 Stores the third 32 bits of KEY5. (RO)

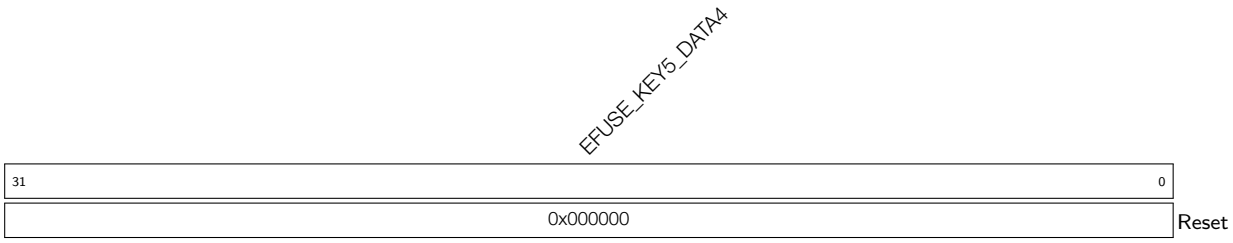
Register 4.83. EFUSE_RD_KEY5_DATA3_REG (0x0148)



EFUSE_KEY5_DATA3 Stores the fourth 32 bits of KEY5. (RO)

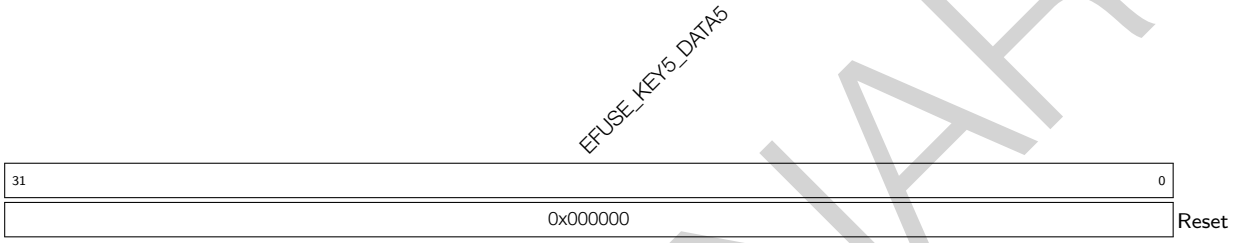
PRELIMINARY

Register 4.84. EFUSE_RD_KEY5_DATA4_REG (0x014C)



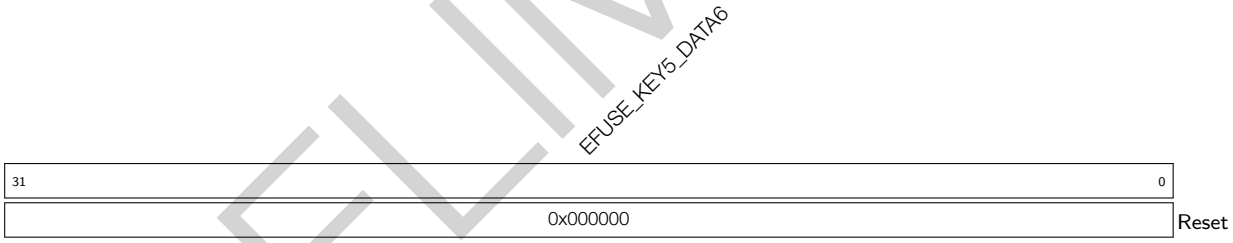
EFUSE_KEY5_DATA4 Stores the fifth 32 bits of KEY5. (RO)

Register 4.85. EFUSE_RD_KEY5_DATA5_REG (0x0150)



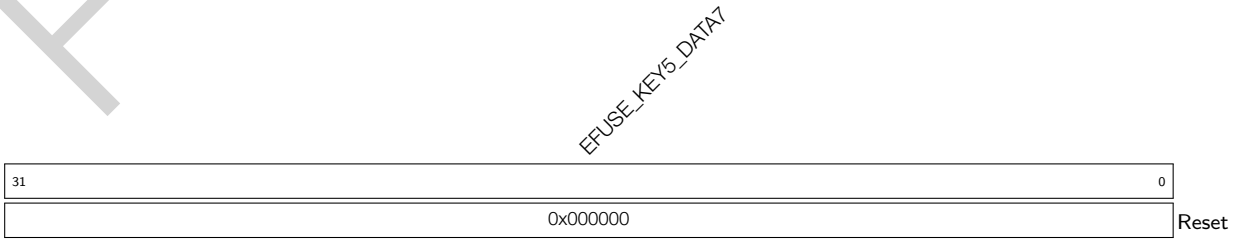
EFUSE_KEY5_DATA5 Stores the sixth 32 bits of KEY5. (RO)

Register 4.86. EFUSE_RD_KEY5_DATA6_REG (0x0154)



EFUSE_KEY5_DATA6 Stores the seventh 32 bits of KEY5. (RO)

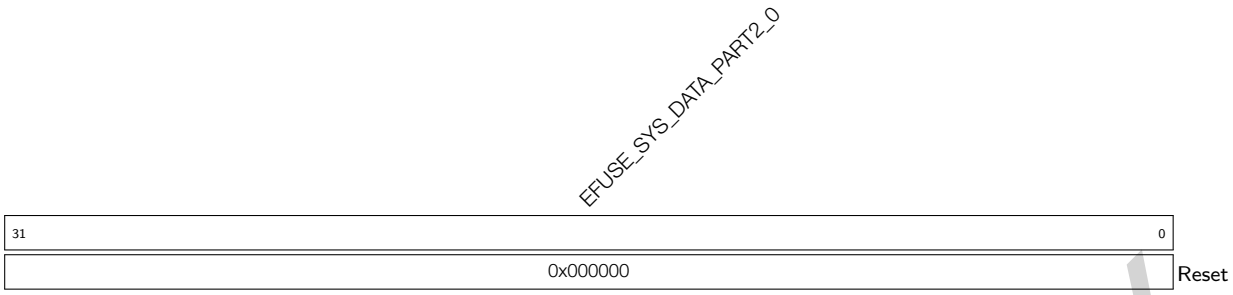
Register 4.87. EFUSE_RD_KEY5_DATA7_REG (0x0158)



EFUSE_KEY5_DATA7 Stores the eighth 32 bits of KEY5. (RO)

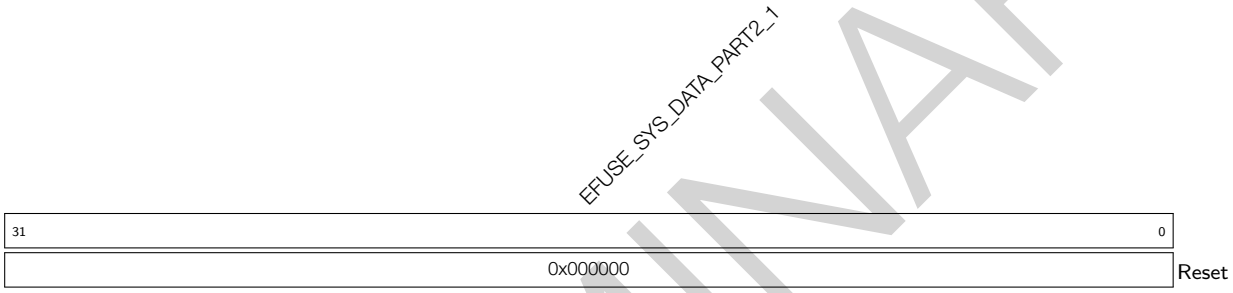
PRELIMINARY

Register 4.88. EFUSE_RD_SYS_PART2_DATA0_REG (0x015C)



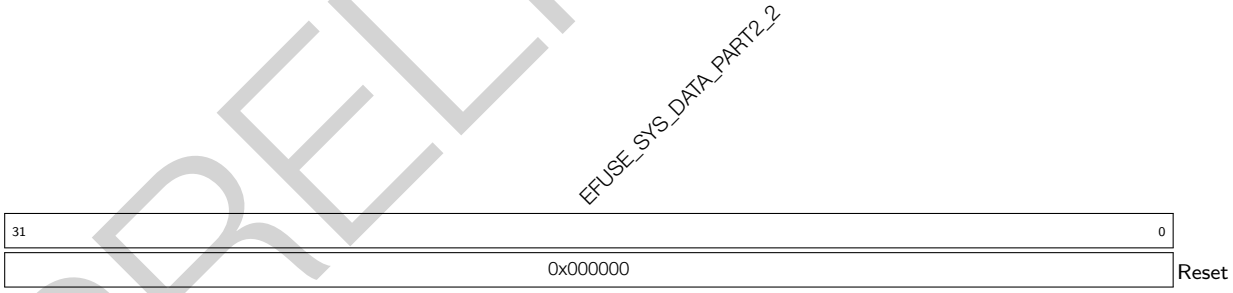
EFUSE_SYS_DATA_PART2_0 Stores the first 32 bits of the third part of system data. (RO)

Register 4.89. EFUSE_RD_SYS_PART2_DATA1_REG (0x0160)



EFUSE_SYS_DATA_PART2_1 Stores the second 32 bits of the third part of system data. (RO)

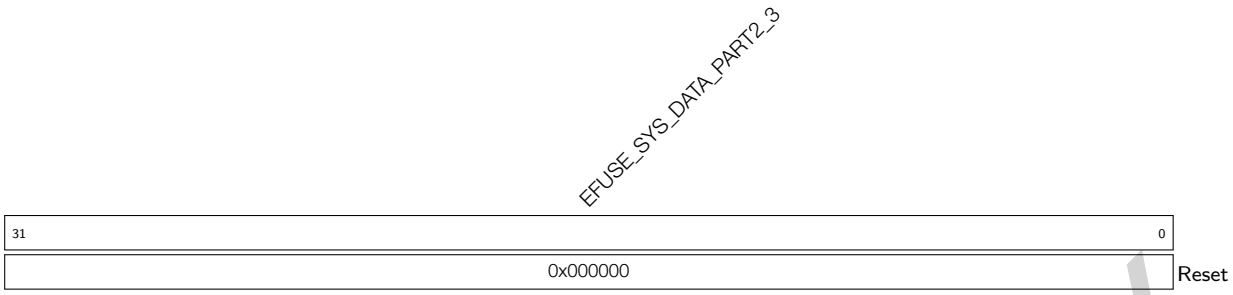
Register 4.90. EFUSE_RD_SYS_PART2_DATA2_REG (0x0164)



EFUSE_SYS_DATA_PART2_2 Stores the third 32 bits of the third part of system data. (RO)

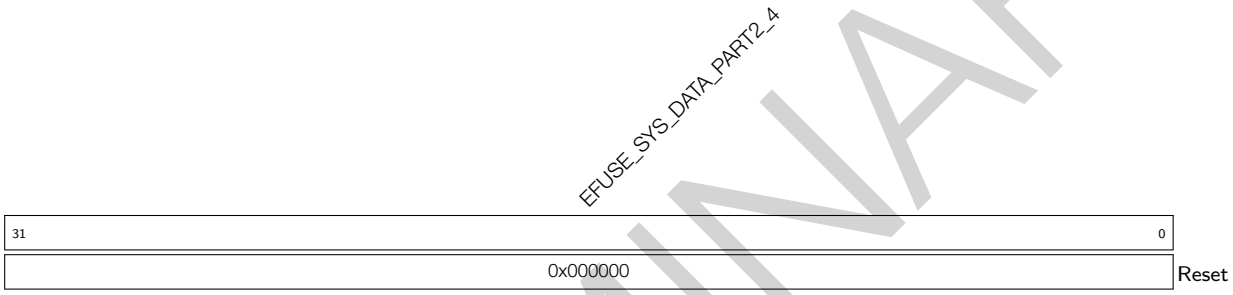
PRELIMINARY

Register 4.91. EFUSE_RD_SYS_PART2_DATA3_REG (0x0168)



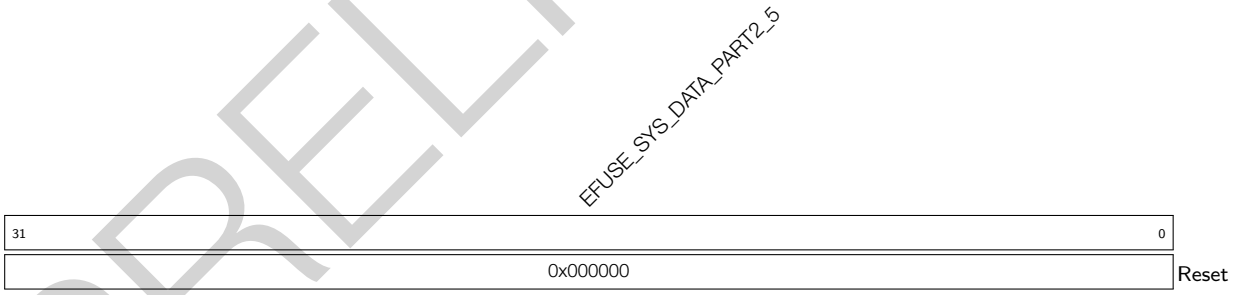
EFUSE_SYS_DATA_PART2_3 Stores the fourth 32 bits of the third part of system data. (RO)

Register 4.92. EFUSE_RD_SYS_PART2_DATA4_REG (0x016C)



EFUSE_SYS_DATA_PART2_4 Stores the fifth 32 bits of the third part of system data. (RO)

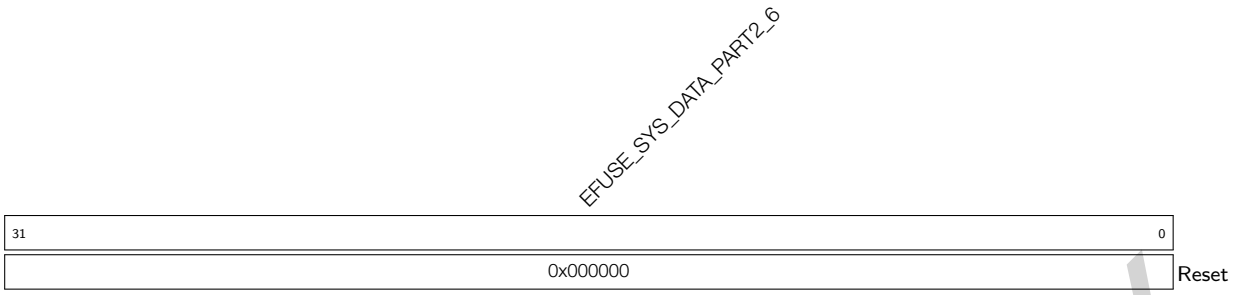
Register 4.93. EFUSE_RD_SYS_PART2_DATA5_REG (0x0170)



EFUSE_SYS_DATA_PART2_5 Stores the sixth 32 bits of the third part of system data. (RO)

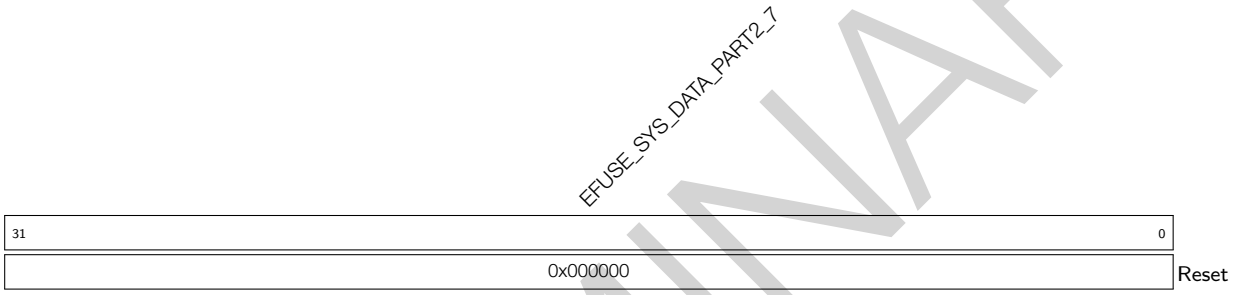
PRELIMINARY

Register 4.94. EFUSE_RD_SYS_PART2_DATA6_REG (0x0174)



EFUSE_SYS_DATA_PART2_6 Stores the seventh 32 bits of the third part of system data. (RO)

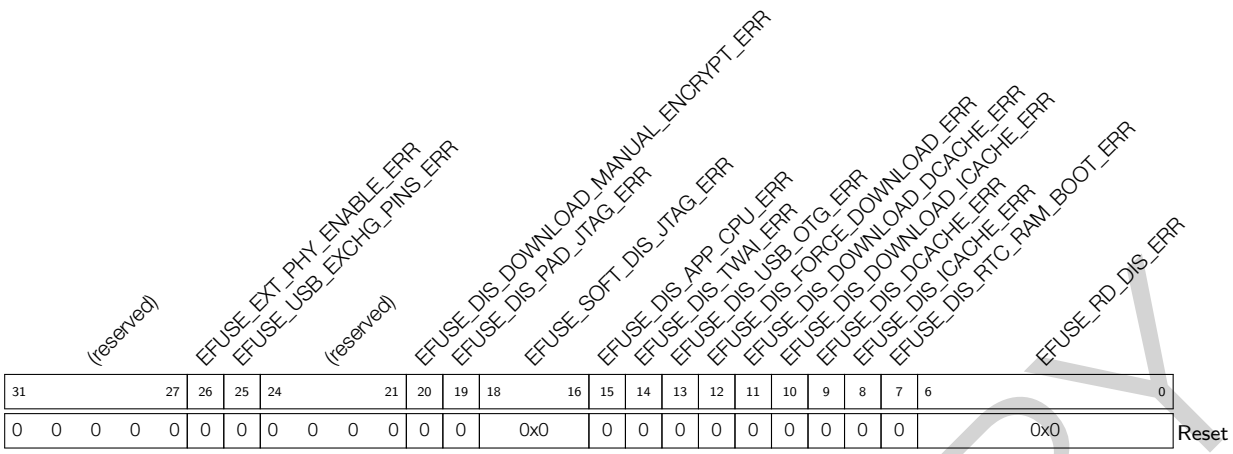
Register 4.95. EFUSE_RD_SYS_PART2_DATA7_REG (0x0178)



EFUSE_SYS_DATA_PART2_7 Stores the eighth 32 bits of the third part of system data. (RO)

PRELIMINARY

Register 4.96. EFUSE_RD_REPEAT_ERR0_REG (0x017C)



EFUSE_RD_DIS_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_RTC_RAM_BOOT_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_ICACHE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_DCACHE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_DOWNLOAD_ICACHE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_DOWNLOAD_DCACHE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_FORCE_DOWNLOAD_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_USB_OTG_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_TWAI_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_APP_CPU_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_SOFT_DIS_JTAG_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_PAD_JTAG_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

Continued on the next page...

PRELIMINARY

Register 4.96. EFUSE_RD_REPEAT_ERR0_REG (0x017C)

Continued from the previous page...

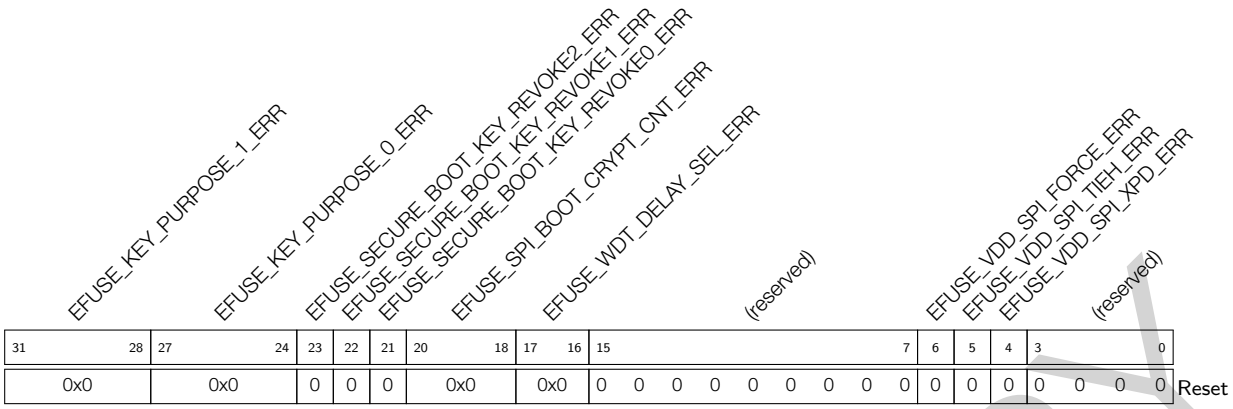
EFUSE_DIS_DOWNLOAD_MANUAL_ENCRYPT_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_USB_EXCHG_PINS_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_EXT_PHY_ENABLE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

PRELIMINARY

Register 4.97. EFUSE_RD_REPEAT_ERR1_REG (0x0180)



EFUSE_VDD_SPI_XPD_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_VDD_SPI_TIEH_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_VDD_SPI_FORCE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_WDT_DELAY_SEL_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_SPI_BOOT_CRYPT_CNT_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_SECURE_BOOT_KEY_REVOKE0_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_SECURE_BOOT_KEY_REVOKE1_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

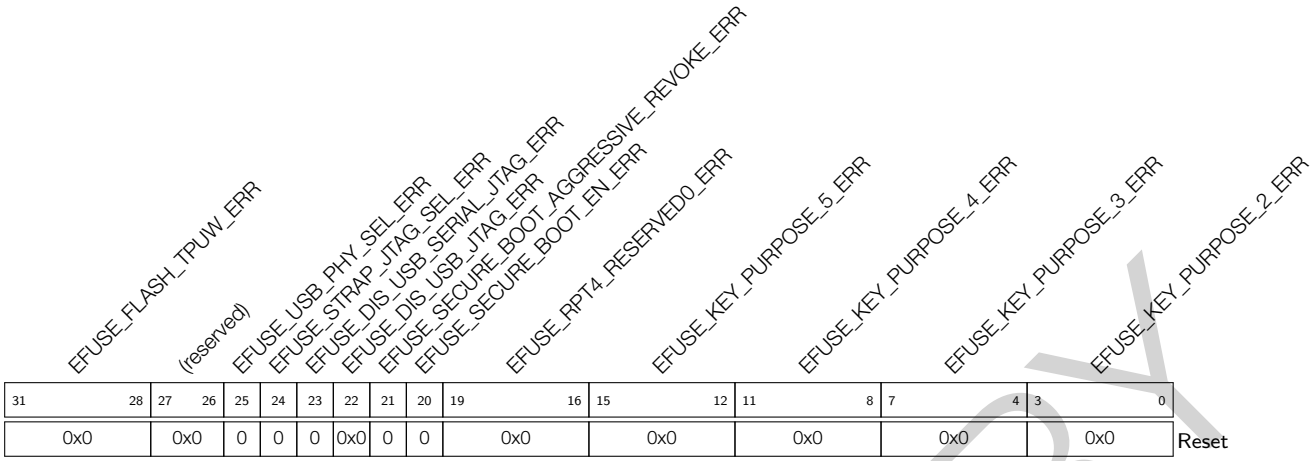
EFUSE_SECURE_BOOT_KEY_REVOKE2_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_KEY_PURPOSE_0_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_KEY_PURPOSE_1_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

PRELIMINARY

Register 4.98. EFUSE_RD_REPEAT_ERR2_REG (0x0184)



EFUSE_KEY_PURPOSE_2_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_KEY_PURPOSE_3_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_KEY_PURPOSE_4_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_KEY_PURPOSE_5_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_RPT4_RESERVED0_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_SECURE_BOOT_EN_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_SECURE_BOOT_AGGRESSIVE_REVOKE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_USB_JTAG_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_USB_SERIAL_JTAG_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

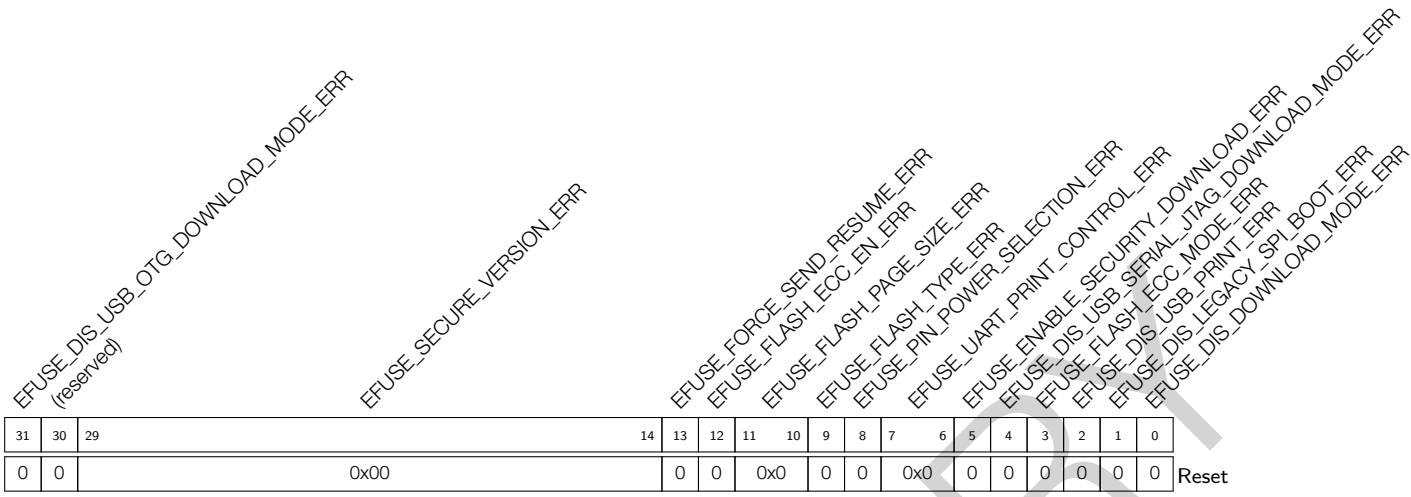
EFUSE_STRAP_JTAG_SEL_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_USB_PHY_SEL_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_FLASH_TPUW_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

PRELIMINARY

Register 4.99. EFUSE_RD_REPEAT_ERR3_REG (0x0188)



EFUSE_DIS_DOWNLOAD_MODE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_LEGACY_SPI_BOOT_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_USB_PRINT_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_FLASH_ECC_MODE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_USB_SERIAL_JTAG_DOWNLOAD_MODE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_ENABLE_SECURITY_DOWNLOAD_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_UART_PRINT_CONTROL_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_PIN_POWER_SELECTION_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_FLASH_TYPE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_FLASH_PAGE_SIZE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_FLASH_ECC_EN_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_FORCE_SEND_RESUME_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

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PRELIMINARY

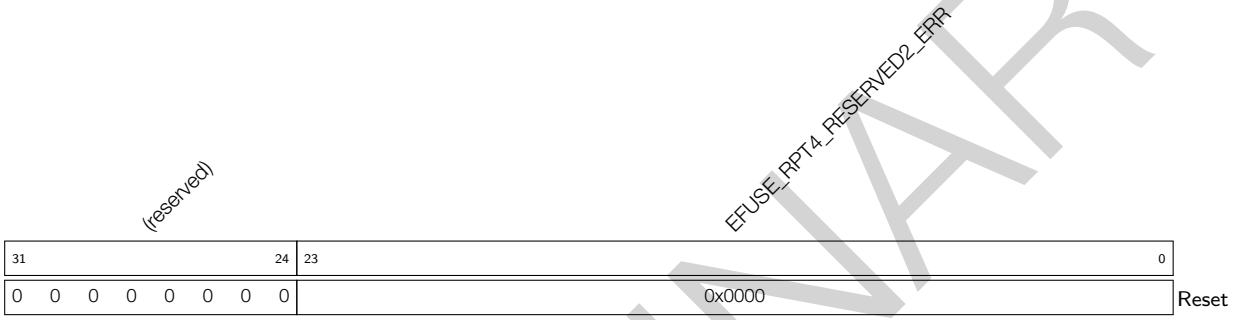
Register 4.99. EFUSE_RD_REPEAT_ERR3_REG (0x0188)

Continued from the previous page...

EFUSE_SECURE_VERSION_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

EFUSE_DIS_USB_OTG_DOWNLOAD_MODE_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

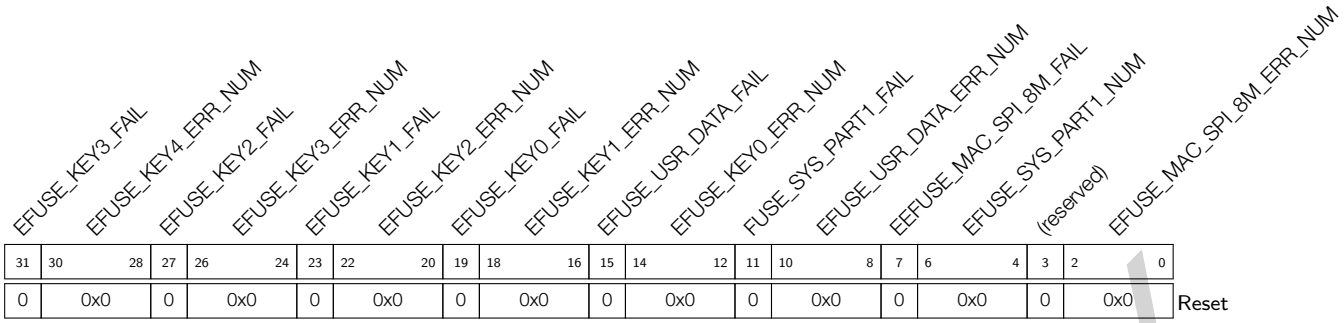
Register 4.100. EFUSE_RD_REPEAT_ERR4_REG (0x018C)



EFUSE_RPT4_RESERVED2_ERR Any bits in this field set to 1 indicate a programming error to corresponding eFuse bit. (RO)

PRELIMINARY

Register 4.101. EFUSE_RD_RS_ERR0_REG (0x01C0)



EFUSE_MAC_SPI_8M_ERR_NUM The value of this field means the number of error bytes during programming Block1. (RO)

EFUSE_SYS_PART1_NUM The value of this field means the number of error bytes during programming Block2. (RO)

EFUSE_MAC_SPI_8M_FAIL 0: Means no failure and that the data of MAC_SPI_8M is reliable 1: Means that programming data of MAC_SPI_8M failed and the number of error bytes is over 6. (RO)

EFUSE_USR_DATA_ERR_NUM The value of this field means the number of error bytes during programming Block3. (RO)

EFUSE_SYS_PART1_FAIL 0: Means no failure and that the data of system part1 is reliable 1: Means that programming data of system part1 failed and the number of error bytes is over 6. (RO)

EFUSE_KEY0_ERR_NUM The value of this field means the number of error bytes during programming Block4. (RO)

EFUSE_USR_DATA_FAIL 0: Means no failure and that the user data is reliable 1: Means that programming user data failed and the number of error bytes is over 6. (RO)

EFUSE_KEY1_ERR_NUM The value of this field means the number of error bytes during programming Block5. (RO)

EFUSE_KEY0_FAIL 0: Means no failure and that the data of key0 is reliable 1: Means that programming key0 failed and the number of error bytes is over 6. (RO)

EFUSE_KEY2_ERR_NUM The value of this field means the number of error bytes during programming Block6. (RO)

EFUSE_KEY1_FAIL 0: Means no failure and that the data of key1 is reliable 1: Means that programming key1 failed and the number of error bytes is over 6. (RO)

EFUSE_KEY3_ERR_NUM The value of this field means the number of error bytes during programming Block7. (RO)

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PRELIMINARY

Register 4.101. EFUSE_RD_RS_ERR0_REG (0x01C0)

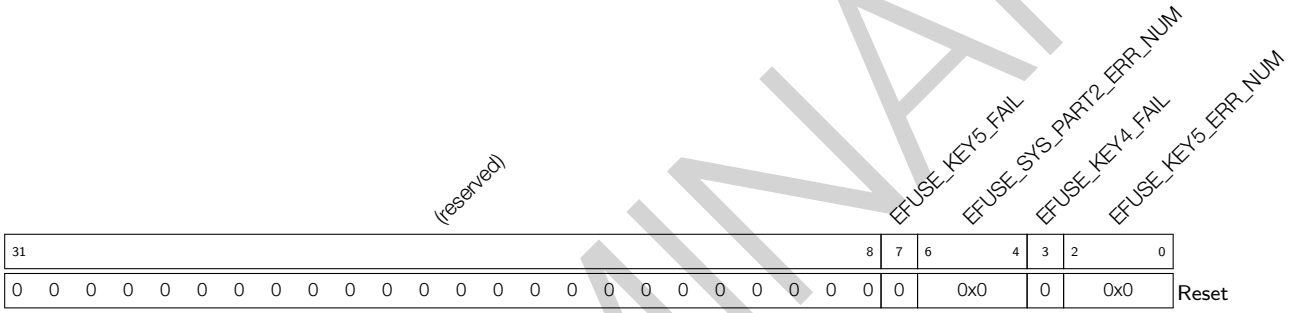
Continued from the previous page...

EFUSE_KEY2_FAIL 0: Means no failure and that the data of key2 is reliable 1: Means that programming key2 failed and the number of error bytes is over 6. (RO)

EFUSE_KEY4_ERR_NUM The value of this field means the number of error bytes during programming Block8. (RO)

EFUSE_KEY3_FAIL 0: Means no failure and that the data of key3 is reliable 1: Means that programming key3 failed and the number of error bytes is over 6. (RO)

Register 4.102. EFUSE_RD_RS_ERR1_REG (0x01C4)



EFUSE_KEY5_ERR_NUM The value of this field means the number of error bytes during programming Block9. (RO)

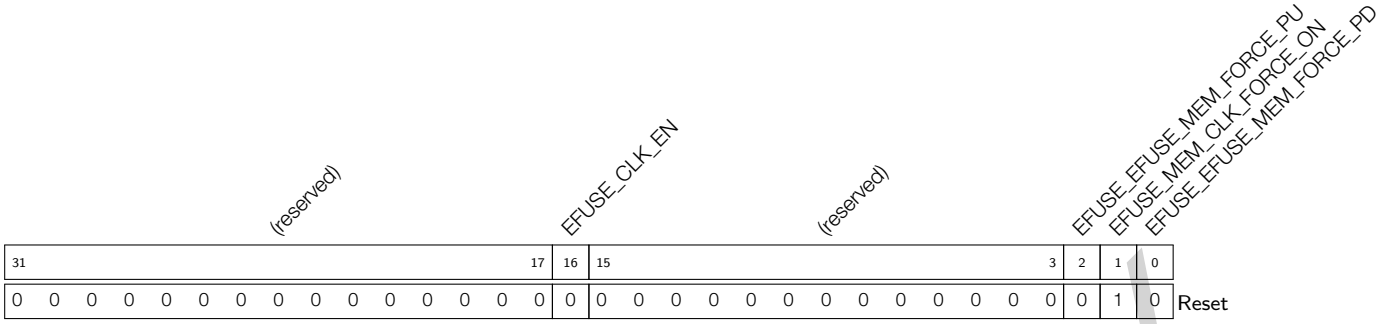
EFUSE_KEY4_FAIL 0: Means no failure and that the data of KEY4 is reliable 1: Means that programming data of KEY4 failed and the number of error bytes is over 6. (RO)

EFUSE_SYS_PART2_ERR_NUM The value of this field means the number of error bytes during programming Block10. (RO)

EFUSE_KEY5_FAIL 0: Means no failure and that the data of KEY5 is reliable 1: Means that programming data of KEY5 failed and the number of error bytes is over 6. (RO)

PRELIMINARY

Register 4.103. EFUSE_CLK_REG (0x01C8)



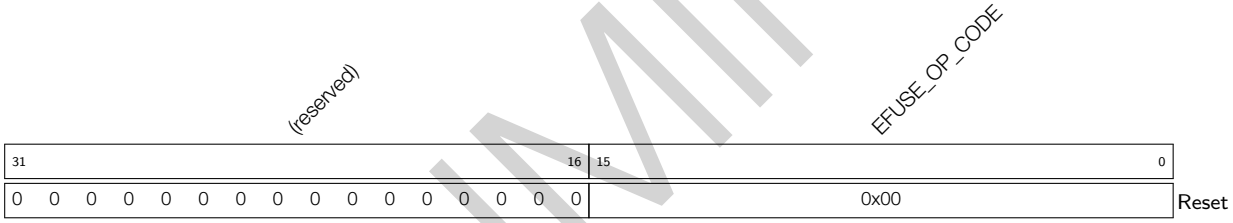
EFUSE_EFUSE_MEM_FORCE_PD This bit be set to force eFuse SRAM into power-saving mode. (R/W)

EFUSE_MEM_CLK_FORCE_ON Set this bit to force on activate clock signal of eFuse SRAM. (R/W)

EFUSE_EFUSE_MEM_FORCE_PU This bit be set to force eFuse SRAM into working mode. (R/W)

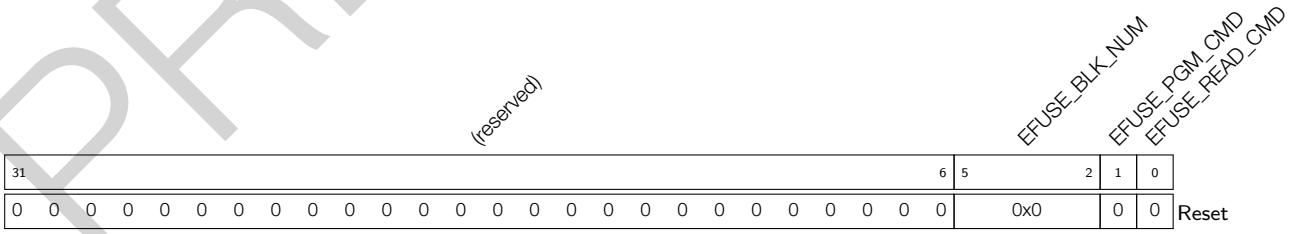
EFUSE_CLK_EN Set this bit and force to enable clock signal of eFuse memory. (R/W)

Register 4.104. EFUSE_CONF_REG (0x01CC)



EFUSE_OP_CODE 0x5A5A: Operate programming command 0x5AA5: Operate read command. (R/W)

Register 4.105. EFUSE_CMD_REG (0x01D4)



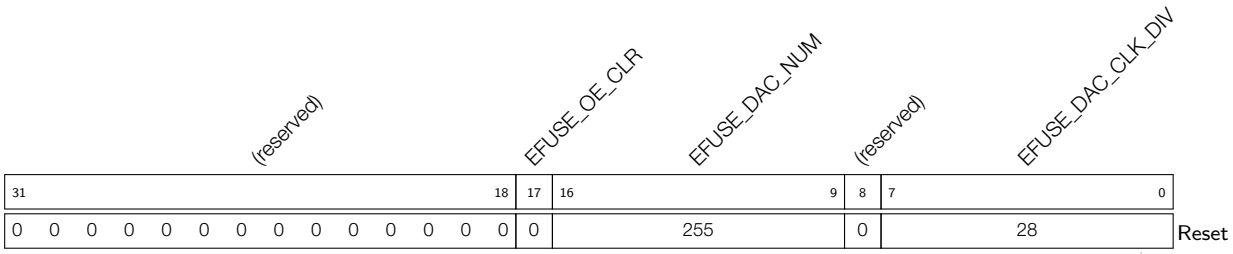
EFUSE_READ_CMD This bit be set to send read command. (R/WS/SC)

EFUSE_PGM_CMD This bit be set to send programming command. (R/WS/SC)

EFUSE_BLK_NUM The index of the block to be programmed. Value 0 ~ 10 corresponds to block number 0 ~ 10, respectively. (R/W)

PRELIMINARY

Register 4.106. EFUSE_DAC_CONF_REG (0x01E8)

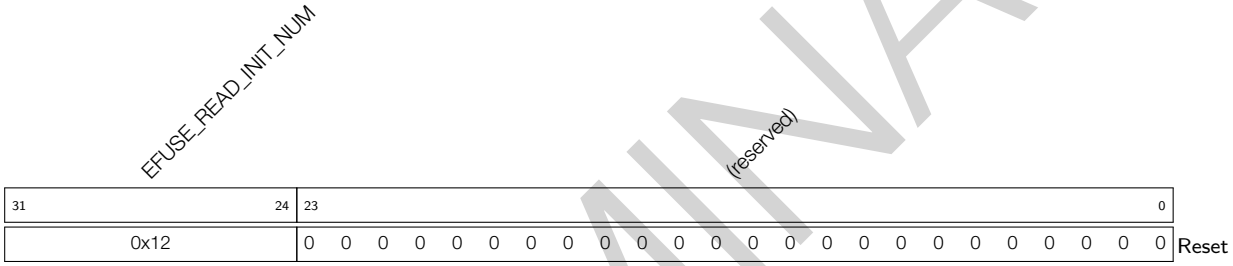


EFUSE_DAC_CLK_DIV Controls the division factor of the clock for the programming voltage. (R/W)

EFUSE_DAC_NUM Controls the rising period of the programming voltage. (R/W)

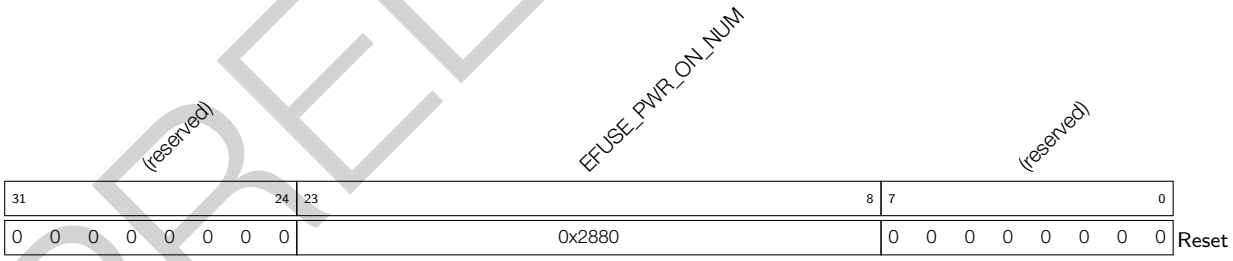
EFUSE_OE_CLR Reduces the power supply of the programming voltage. (R/W)

Register 4.107. EFUSE_RD_TIM_CONF_REG (0x01EC)



EFUSE_READ_INIT_NUM Configures the initial read time of eFuse. (R/W)

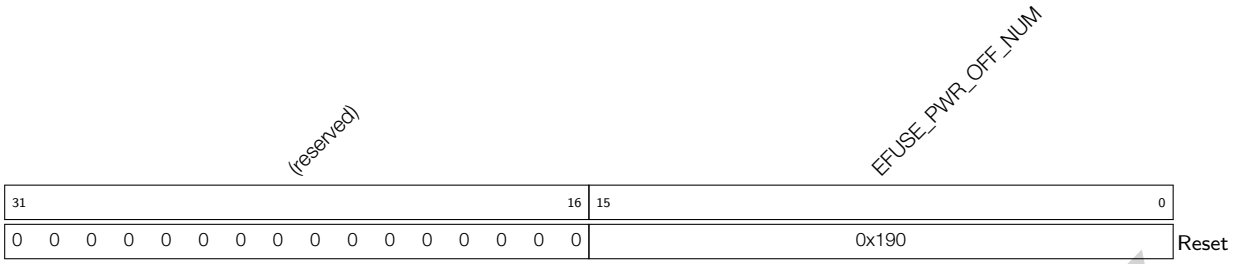
Register 4.108. EFUSE_WR_TIME_CONF1_REG (0x01F4)



EFUSE_PWR_ON_NUM Configures the power up time for VDDQ. (R/W)

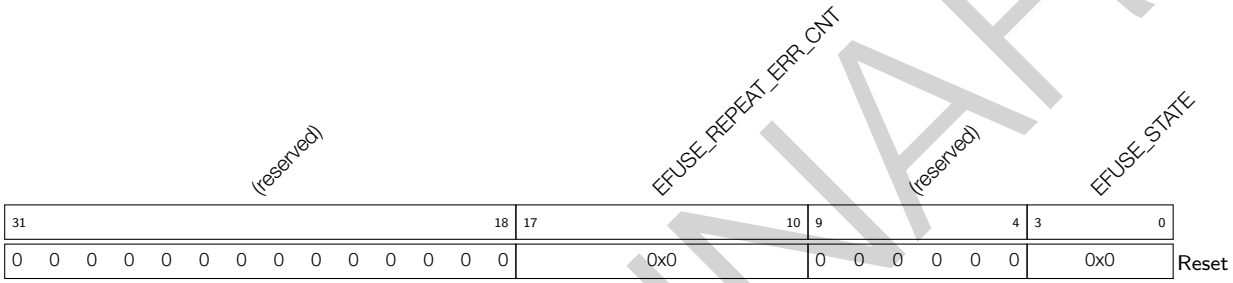
PRELIMINARY

Register 4.109. EFUSE_WR_TIM_CONF2_REG (0x01F8)



EFUSE_PWR_OFF_NUM Configures the power off time for VDDQ. (R/W)

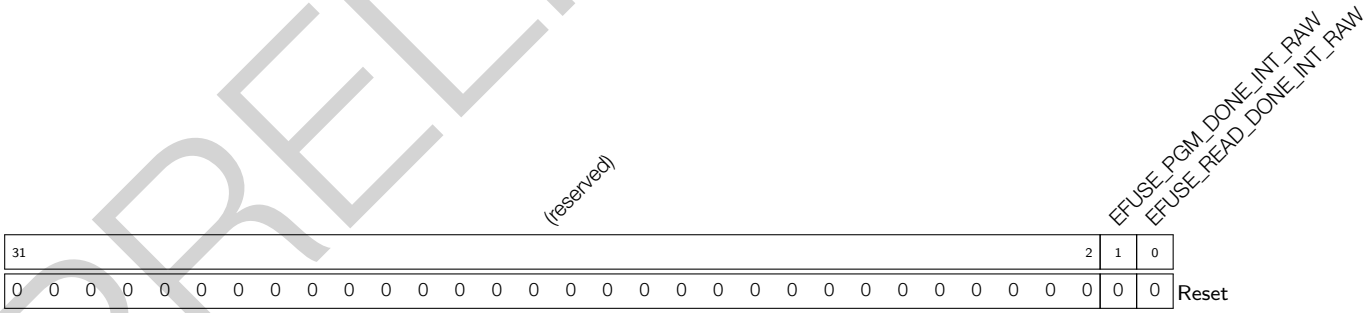
Register 4.110. EFUSE_STATUS_REG (0x01D0)



EFUSE_STATE Indicates the state of the eFuse state machine. (RO)

EFUSE_REPEAT_ERR_CNT Indicates the number of error bits during programming BLOCK0. (RO)

Register 4.111. EFUSE_INT_RAW_REG (0x01D8)

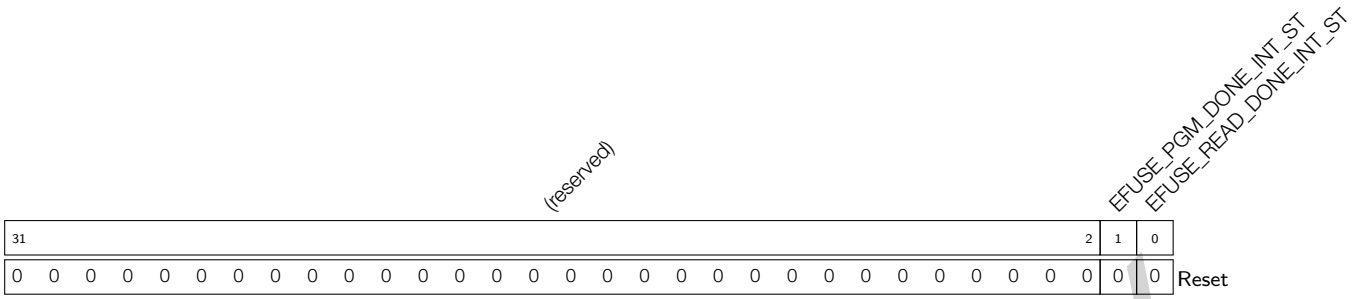


EFUSE_READ_DONE_INT_RAW The raw bit signal for read_done interrupt. (R/WC/SS)

EFUSE_PGM_DONE_INT_RAW The raw bit signal for pgm_done interrupt. (R/WC/SS)

PRELIMINARY

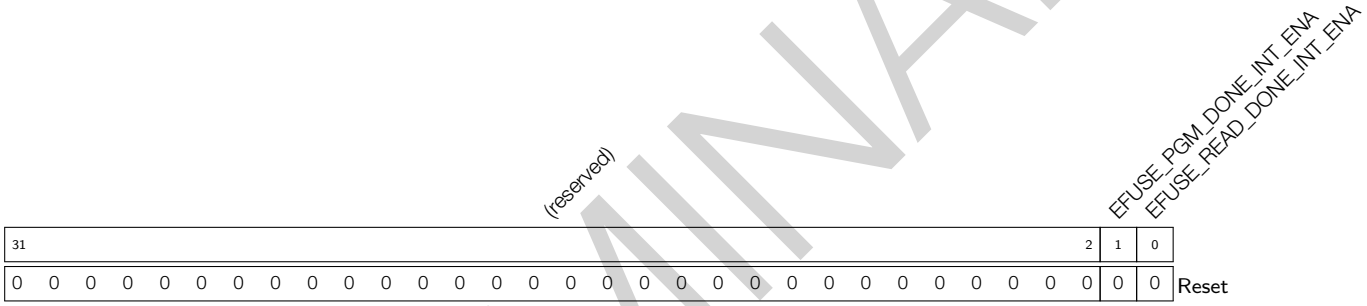
Register 4.112. EFUSE_INT_ST_REG (0x01DC)



EFUSE_READ_DONE_INT_ST The status signal for read_done interrupt. (RO)

EFUSE_PGM_DONE_INT_ST The status signal for pgm_done interrupt. (RO)

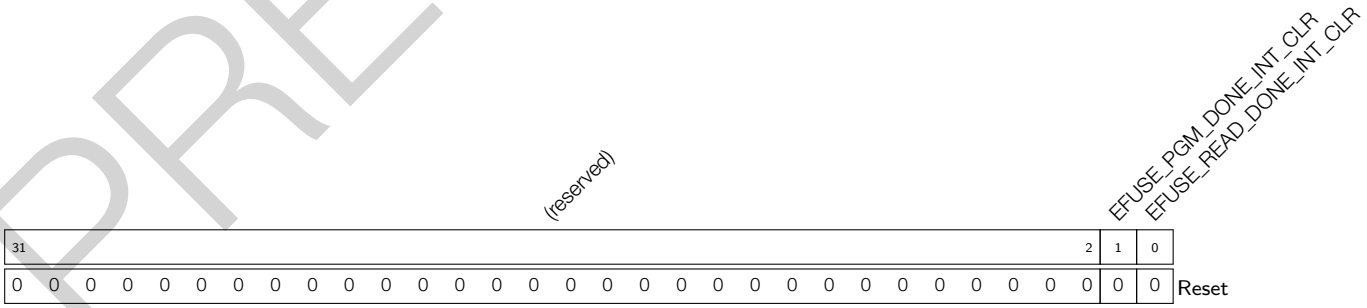
Register 4.113. EFUSE_INT_ENA_REG (0x01E0)



EFUSE_READ_DONE_INT_ENA Set this bit to enable read_done interrupt. (R/W)

EFUSE_PGM_DONE_INT_ENA Set this bit to enable pgm_done interrupt. (R/W)

Register 4.114. EFUSE_INT_CLR_REG (0x01E4)

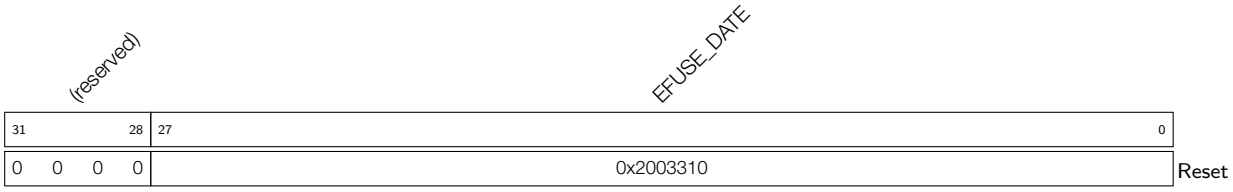


EFUSE_READ_DONE_INT_CLR The clear signal for read_done interrupt. (WO)

EFUSE_PGM_DONE_INT_CLR The clear signal for pgm_done interrupt. (WO)

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Register 4.115. EFUSE_DATE_REG (0x01FC)



EFUSE_DATE Stores eFuse version. (R/W)

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5 IO MUX and GPIO Matrix (GPIO, IO MUX)

5.1 Overview

The ESP32-S3 chip features 45 physical GPIO pins. Each pin can be used as a general-purpose I/O, or be connected to an internal peripheral signal. Through GPIO matrix, IO MUX, and RTC IO MUX, peripheral input signals can be from any GPIO pin, and peripheral output signals can be routed to any GPIO pin. Together these modules provide highly configurable I/O.

Note that the 45 GPIO pins are numbered from 0 ~ 21 and 26 ~ 48. All these pins can be configured either as input or output.

5.2 Features

GPIO Matrix Features

- A full-switching matrix between the peripheral input/output signals and the GPIO pins.
- 175 digital peripheral input signals can be sourced from the input of any GPIO pins.
- The output of any GPIO pins can be from any of the 184 digital peripheral output signals.
- Supports signal synchronization for peripheral inputs based on APB clock bus.
- Provides input signal filter.
- Supports sigma delta modulated output.
- Supports GPIO simple input and output.

IO MUX Features

- Provides one configuration register IO_MUX_GPIO*n*_REG for each GPIO pin. The pin can be configured to
  - perform GPIO function routed by GPIO matrix;
  - or perform direct connection bypassing GPIO matrix.
- Supports some high-speed digital signals (SPI, JTAG, UART) bypassing GPIO matrix for better high-frequency digital performance. In this case, IO MUX is used to connect these pins directly to peripherals.

RTC IO MUX Features

- Controls low power feature of 22 RTC GPIO pins.
- Controls analog functions of 22 RTC GPIO pins.
- Redirects 22 RTC input/output signals to RTC system.

5.3 Architectural Overview

Figure 5-1 shows in details how IO MUX, RTC IO MUX, and GPIO matrix route signals from pins to peripherals, and from peripherals to pins.

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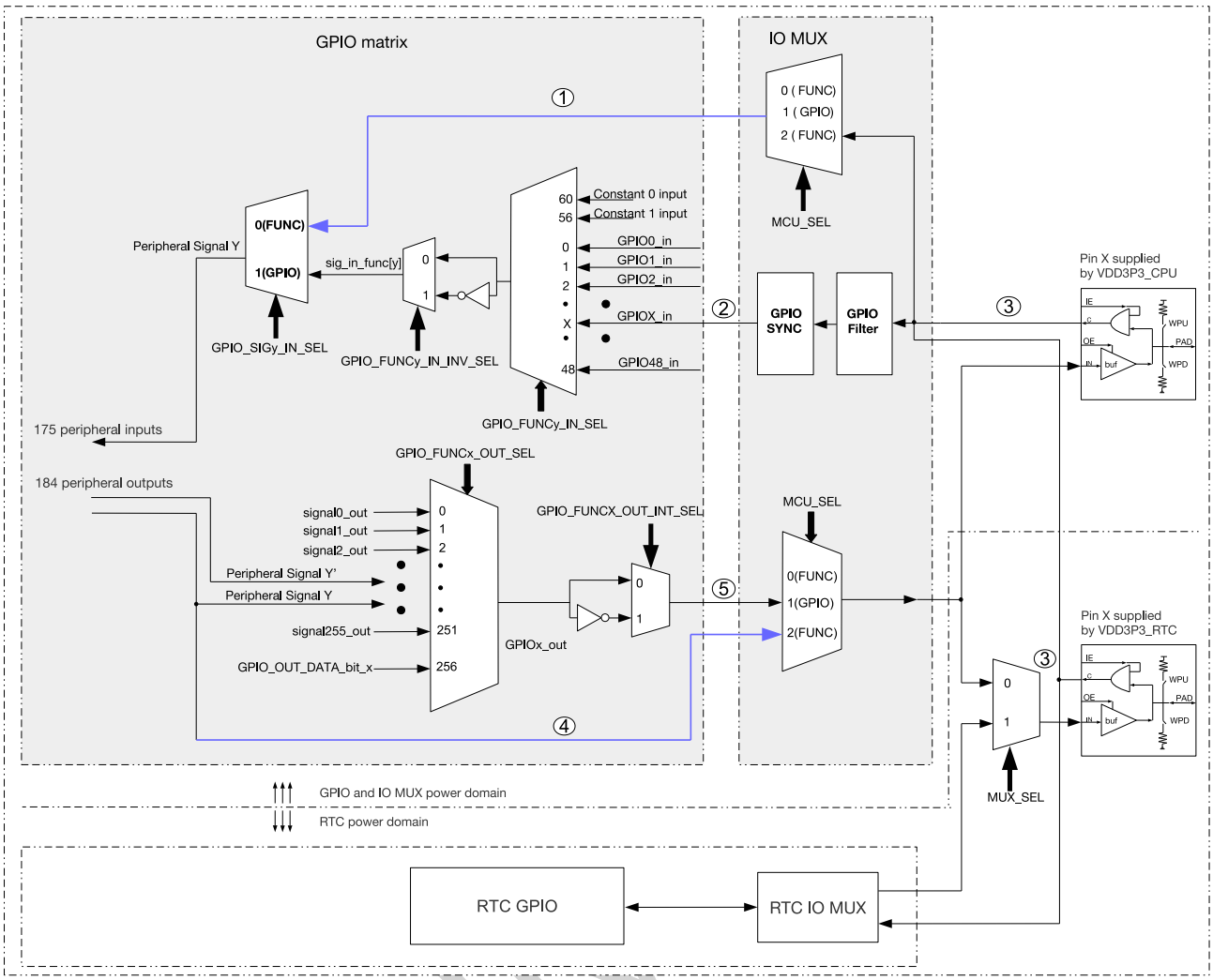


Figure 5-1. Architecture of IO MUX, RTC IO MUX, and GPIO Matrix

1. Only part of peripheral input signals (marked “yes” in column “Direct input through IO MUX” in Table 5-2) can bypass GPIO matrix. The other input signals can only be routed to peripherals via GPIO matrix.
2. There are only 45 inputs from GPIO SYNC to GPIO matrix, since ESP32-S3 provides 45 GPIO pins in total.
3. The pins supplied by VDD3P3_CPU or by VDD3P3_RTC are controlled by the signals: IE, OE, WPU, and WPD.
4. Only part of peripheral outputs (marked “yes” in column “Direct output through IO MUX” in Table 5-2) can be routed to pins bypassing GPIO matrix.
5. There are only 45 outputs (GPIO pin X: 0 ~ 21, 26 ~ 48) from GPIO matrix to IO MUX.

Figure 5-2 shows the internal structure of a pad, which is an electrical interface between the chip logic and the GPIO pin. The structure is applicable to all 45 GPIO pins and can be controlled using IE, OE, WPU, and WPD signals.

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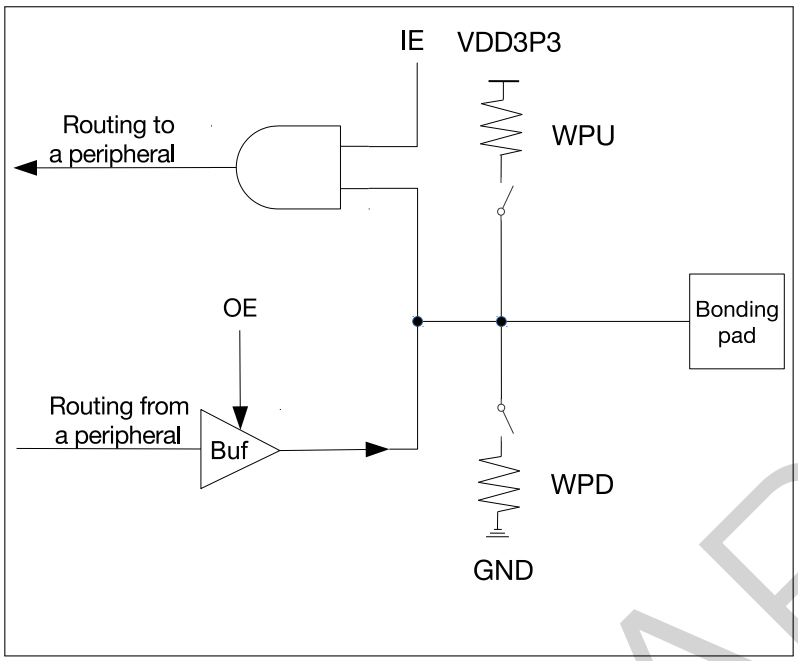


Figure 5-2. Internal Structure of a Pad

Note:

- IE: input enable
- OE: output enable
- WPU: internal weak pull-up
- WPD: internal weak pull-down
- Bonding pad: a terminal point of the chip logic used to make a physical connection from the chip die to GPIO pin in the chip package.

5.4 Peripheral Input via GPIO Matrix

5.4.1 Overview

To receive a peripheral input signal via GPIO matrix, the matrix is configured to source the peripheral input signal from one of the 45 GPIOs (0 ~ 21, 26 ~ 48), see Table 5-2. Meanwhile, register corresponding to the peripheral signal should be set to receive input signal via GPIO matrix.

5.4.2 Signal Synchronization

When signals are directed from pins using the GPIO matrix, the signals will be synchronized to the APB bus clock by the GPIO SYNC hardware, then go to GPIO matrix. This synchronization applies to all GPIO matrix signals but does not apply when using the IO MUX, see Figure 5-1.

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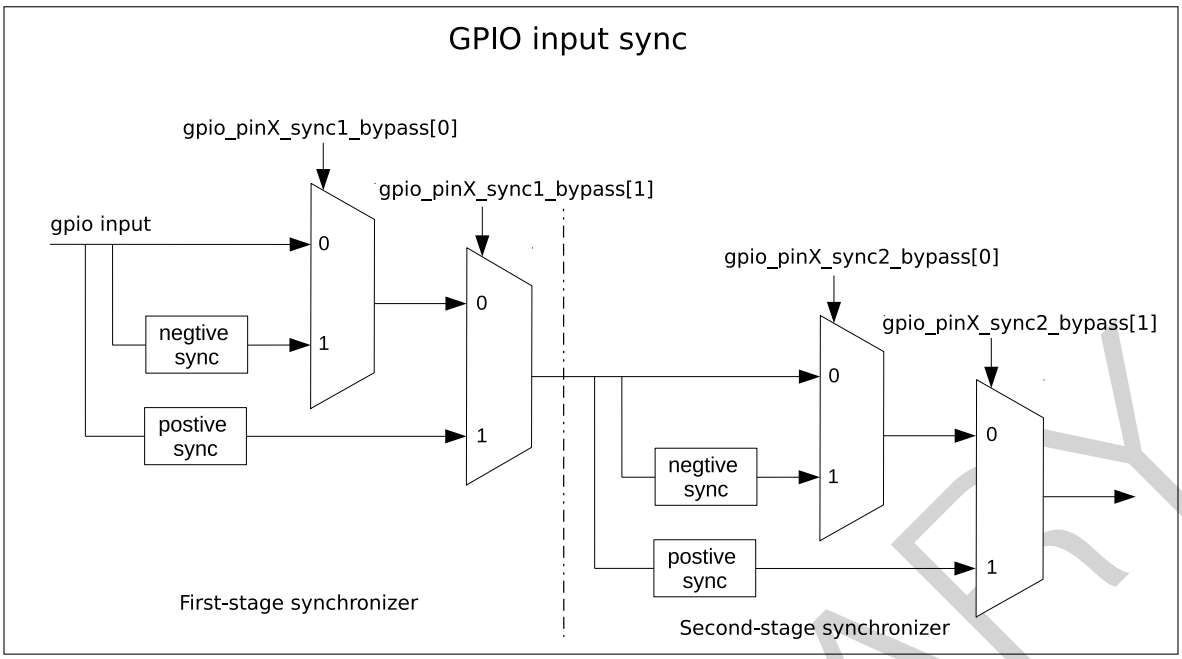


Figure 5-3. GPIO Input Synchronized on APB Clock Rising Edge or on Falling Edge

Figure 5-3 shows the functionality of GPIO SYNC. In the figure, negative sync and positive sync mean GPIO input is synchronized on APB clock falling edge and on APB clock rising edge, respectively.

5.4.3 Functional Description

To read GPIO pin *X*[1] into peripheral signal *Y*, follow the steps below:

1. Configure register GPIO_FUNC*y*_IN_SEL_CFG_REG corresponding to peripheral signal *Y* in GPIO matrix:
   - Set GPIO_SIG*y*_IN_SEL to enable peripheral signal input via GPIO matrix.
   - Set GPIO_FUNC*y*_IN_SEL to the desired GPIO pin, i.e. *X* here.

   Note that some peripheral signals have no valid GPIO_SIG*y*_IN_SEL bit, namely, these peripherals can only receive input signals via GPIO matrix.
2. Optionally enable the filter for pin input signals by setting the register IO_MUX_FILTER_EN. Only the signals with a valid width of more than two APB clock cycles can be sampled, see Figure 5-4.

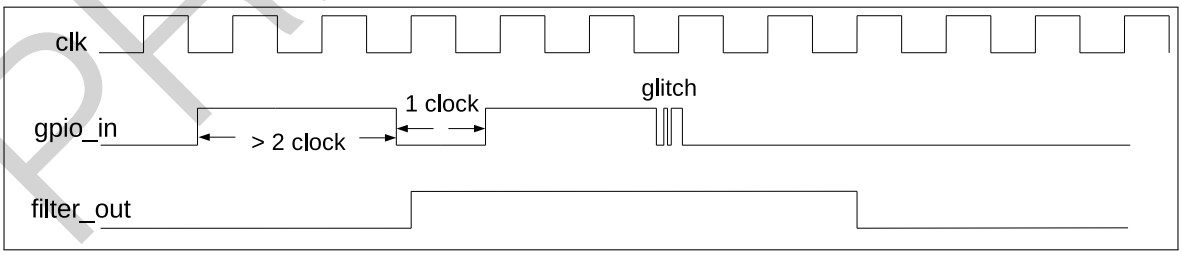


Figure 5-4. Filter Timing of GPIO Input Signals

3. Synchronize GPIO input. To do so, please set GPIO_PIN*x*_REG corresponding to GPIO pin *X* as follows:
   - Set GPIO_PIN*x*_SYNC1_BYPASS to enable input signal synchronized on rising edge or on falling edge in the first clock, see Figure 5-3.

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- Set GPIO_PIN*x*_SYNC2_BYPASS to enable input signal synchronized on rising edge or on falling edge in the second clock, see Figure 5-3.

4. Configure IO MUX register to enable pin input. For this end, please set IO_MUX_*X*_REG corresponding to GPIO pin *x* as follows:
   - Set IO_MUX_FUN_IE to enable input[2].
   - Set or clear IO_MUX_FUN_WPU and IO_MUX_FUN_WPD, as desired, to enable or disable pull-up and pull-down resistors.

For example, to connect RMT channel 0 input signal[3] (rmt_sig_in0, signal index 81) to GPIO40, please follow the steps below. Note that GPIO40 is also named as MTDO pin.

1. Set GPIO_SIG81_IN_SEL in register GPIO_FUNC81_IN_SEL_CFG_REG to enable peripheral signal input via GPIO matrix.
2. Set GPIO_FUNC81_IN_SEL in register GPIO_FUNC81_IN_SEL_CFG_REG to 40, i.e. select GPIO40.
3. Set IO_MUX_FUN_IE in register IO_MUX_GPIO40_REG to enable pin input.

Note:

1. One pin input can be connected to multiple peripheral input signals.
2. The input signal can be inverted by configuring GPIO_FUNC*y*_IN_INV_SEL.
3. It is possible to have a peripheral read a constantly low or constantly high input value without connecting this input to a pin. This can be done by selecting a special GPIO_FUNC*y*_IN_SEL input, instead of a GPIO number:
   - When GPIO_FUNC*y*_IN_SEL is set to 0x3C, input signal is always 0.
   - When GPIO_FUNC*y*_IN_SEL is set to 0x38, input signal is always 1.

5.4.4 Simple GPIO Input

GPIO_IN_REG/GPIO_IN1_REG holds the input values of each GPIO pin. The input value of any GPIO pin can be read at any time without configuring GPIO matrix for a particular peripheral signal. However, it is necessary to enable pin input by setting IO_MUX_FUN_IE in register IO_MUX_*x*_REG corresponding to pin *X*, as described in Section 5.4.2.

5.5 Peripheral Output via GPIO Matrix

5.5.1 Overview

To output a signal from a peripheral via GPIO matrix, the matrix is configured to route peripheral output signals (only signals with a name assigned in the column "Output signal" in Table 5-2) to one of the 45 GPIOs (0 ~ 21, 26 ~ 48).

The output signal is routed from the peripheral into GPIO matrix and then into IO MUX. IO MUX must be configured to set the chosen pin to GPIO function. This enables the output GPIO signal to be connected to the pin.

Note:

There is a range of peripheral output signals (208 ~ 212 in Table 5-2) which are not connected to any peripheral, but to the

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input signals (208 ~ 212) directly. These can be used to input a signal from one GPIO pin and output directly to another GPIO pin.

5.5.2 Functional Description

Some of the 256 output signals (signals with a name assigned in the column "Output signal" in Table 5-2) can be set to go through GPIO matrix into IO MUX and then to a pin. Figure 5-1 illustrates the configuration.

To output peripheral signal *Y* to a particular GPIO pin *X*[1, 2], follow these steps:

1. Configure GPIO_FUNC*x*_OUT_SEL_CFG_REG and GPIO_ENABLE_REG[*x*] corresponding to GPIO pin *X* in GPIO matrix. Recommended operation: use corresponding W1TS (write 1 to set) and W1TC (write 1 to clear) registers to set or clear GPIO_ENABLE_REG.
   - Set the GPIO_FUNC*x*_OUT_SEL field in register GPIO_FUNC*x*_OUT_SEL_CFG_REG to the index of the desired peripheral output signal *Y*.
   - If the signal should always be enabled as an output, set the bit GPIO_FUNC*x*_OEN_SEL in register GPIO_FUNC*x*_OUT_SEL_CFG_REG and the bit in register GPIO_ENABLE/ENABLE1_W1TS_REG, corresponding to GPIO pin *X*. To have the output enable signal decided by internal logic (for example, the SPIQ_oe in column "Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0" in Table 5-2), clear the bit GPIO_FUNC*x*_OEN_SEL instead.
   - Set the corresponding bit in register GPIO_ENABLE/ENABLE1_W1TC_REG to disable the output from the GPIO pin.
2. For an open drain output, set the bit GPIO_PIN*x*_PAD_DRIVER in register GPIO_PIN*x*_REG corresponding to GPIO pin *X*.
3. Configure IO MUX register to enable output via GPIO matrix. Set the IO_MUX_*x*_REG corresponding to GPIO pin *X* as follows:
   - Set the field IO_MUX_MCU_SEL to desired IO MUX function corresponding to GPIO pin *X*. This is Function 1 (GPIO function), numeric value 1, for all pins.
   - Set the field IO_MUX_FUN_DRV to the desired value for output strength (0 ~ 3). The higher the driver strength, the more current can be sourced/sunk from the pin.
     - 0: ~5 mA
     - 1: ~10 mA
     - 2: ~20 mA (default value)
     - 3: ~40 mA
   - If using open drain mode, set/clear IO_MUX_FUN_WPU and IO_MUX_FUN_WPD to enable/disable the internal pull-up/pull-down resistors.

Note:

1. The output signal from a single peripheral can be sent to multiple pins simultaneously.
2. The output signal can be inverted by setting GPIO_FUNC*x*_OUT_INV_SEL.

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5.5.3 Simple GPIO Output

GPIO matrix can also be used for simple GPIO output. This can be done as below:

- Set GPIO matrix GPIO_FUNC*n*_OUT_SEL with a special peripheral index 256 (0x100);
- Set the corresponding bit in GPIO_OUT_REG[31:0] or GPIO_OUT1_REG[21:0] to the desired GPIO output value.

Note:

- GPIO_OUT_REG[21:0] and GPIO_OUT_REG[31:26] correspond to GPIO0 ~ 21 and GPIO26 ~ 31, respectively. GPIO_OUT_REG[25:22] are invalid.
- GPIO_OUT1_REG[16:0] correspond to GPIO32 ~ 48, and GPIO_OUT1_REG[21:17] are invalid.
- Recommended operation: use corresponding W1TS and W1TC registers, such as GPIO_OUT_W1TS/GPIO_OUT_W1TC to set or clear the registers GPIO_OUT_REG/GPIO_OUT1_REG.

5.5.4 Sigma Delta Modulated Output

5.5.4.1 Functional Description

Eight out of the 256 peripheral outputs (index: 93 ~ 100 in Table 5-2) support 1-bit second-order sigma delta modulation. By default output is enabled for these eight channels. This Sigma Delta modulator can also output PDM (pulse density modulation) signal with configurable duty cycle. The transfer function is:

$$H(z) = \mathrm{X(z)z^{-1}} + \mathrm{E(z)(1\text{-}z^{-1})^2}$$

E(z) is quantization error and X(z) is the input.
This modulator supports scaling down of APB_CLK by divider 1 ~ 256:

- Set GPIO_FUNCTION_CLK_EN to enable the modulator clock.
- Configure GPIO_SD*n*_PRESCALE (*n* is 0 ~ 7 for eight channels).

After scaling, the clock cycle is equal to one pulse output cycle from the modulator.

GPIO_SD*n*_IN is a signed number with a range of [-128, 127] and is used to control the duty cycle [1] of PDM output signal.

- GPIO_SD*n*_IN = -128, the duty cycle of the output signal is 0%.
- GPIO_SD*n*_IN = 0, the duty cycle of the output signal is near 50%.
- GPIO_SD*n*_IN = 127, the duty cycle of the output signal is close to 100%.

The formula for calculating PDM signal duty cycle is shown as below:

$$Duty\_Cycle = \frac{GPIO\_SDn\_IN + 128}{256}$$

Note:
For PDM signals, duty cycle refers to the percentage of high level cycles to the whole statistical period (several pulse

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cycles, for example 256 pulse cycles).

5.5.4.2 SDM Configuration

The configuration of SDM is shown below:

- Route one of SDM outputs to a pin via GPIO matrix, see Section 5.5.2.
- Enable the modulator clock by setting GPIO_FUNCTION_CLK_EN.
- Configure the divider value by setting GPIO_SD*n*_PRESCALE.
- Configure the duty cycle of SDM output signal by setting GPIO_SD*n*_IN.

5.6 Direct Input and Output via IO MUX

5.6.1 Overview

Some high-speed signals (SPI and JTAG) can bypass GPIO matrix for better high-frequency digital performance. In this case, IO MUX is used to connect these pins directly to the peripherals.

This option is less flexible than routing signals via GPIO matrix, as the IO MUX register for each GPIO pin can only select from a limited number of functions, but high-frequency digital performance can be improved.

5.6.2 Functional Description

Two registers must be configured in order to bypass GPIO matrix for peripheral input signals:

1. IO_MUX_MCU_SEL for the GPIO pin must be set to the required pin function. For the list of pin functions, please refer to Section 5.12.
2. Clear GPIO_SIG*n*_IN_SEL to route the input directly to the peripheral.

To bypass GPIO matrix for peripheral output signals, IO_MUX_MCU_SEL for the GPIO pin must be set to the required pin function. For the list of pin functions, please refer to Section 5.12.

Note:
Not all signals can be connected to peripheral via IO MUX. Some input/output signals can only be connected to peripheral via GPIO matrix.

5.7 RTC IO MUX for Low Power and Analog Input/Output

5.7.1 Overview

ESP32-S3 provides 22 GPIO pins with low power capabilities (RTC) and analog functions, which are handled by the RTC subsystem of ESP32-S3. IO MUX and GPIO matrix are not used for these functions, rather, RTC IO MUX is used to redirect 22 RTC input/output signals to the RTC subsystem.

When configured as RTC GPIOs, the output pins can still retain the output level value when the chip is in Deep-sleep mode, and the input pins can wake up the chip from Deep-sleep.

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5.7.2 Low Power Capabilities

The pins with RTC functions are controlled by RTC_IO_TOUCH/RTC_PAD*n*_MUX_SEL bit in register RTC_IO_TOUCH/RTC_PAD*n*_REG. By default all bits in these registers are set to 0, routing all input/output signals via IO MUX.

If RTC_IO_TOUCH/RTC_PAD*n*_MUX_SEL is set to 1, then input/output signals to and from that pin is routed to the RTC subsystem. In this mode, RTC_IO_TOUCH/RTC_PAD*n*_REG is used to control RTC low power pins. Note that RTC_IO_TOUCH/RTC_PAD*n*_REG applies the RTC GPIO pin numbering, not the GPIO pin numbering. See Table 5-4 for RTC functions of RTC IO MUX pins.

5.7.3 Analog Functions

When the pin is used for analog purpose, make sure this pin is left floating by configuring the register RTC_IO_TOUCH/RTC_PAD*n*_REG. By such way, external analog signal is connected to internal analog signal via GPIO pin. The configuration is as follows:

- Set RTC_IO_TOUCH/RTC_PAD*n*_MUX_SEL, to select RTC IO MUX to route input and output signals.
- Clear RTC_IO_TOUCH/RTC_PAD*n*_FUN_IE, RTC_IO_TOUCH/RTC_PAD*n*_FUN_RUE, and RTC_IO_TOUCH/RTC_PAD*n*_FUN_RDE, to set this pin floating.
- Configure RTC_IO_TOUCH/RTC_PAD*n*_FUN_SEL to 0, to enable analog function 0.
- Write 1 to RTC_GPIO_ENABLE_W1TC, to clear output enable.

See Table 5-5 for analog functions of RTC IO MUX pins.

5.8 Pin Functions in Light-sleep

Pins may provide different functions when ESP32-S3 is in Light-sleep mode. If IO_MUX_SLP_SEL in register IO_MUX_*n*_REG for a GPIO pin is set to 1, a different set of bits will be used to control the pin when the chip is in Light-sleep mode.

Table 5-1. Bits Used to Control IO MUX Functions in Light-sleep Mode

IO MUX Functions	Normal Execution OR IO_MUX_SLP_SEL = 0	Light-sleep Mode AND IO_MUX_SLP_SEL = 1
Output Drive Strength	IO_MUX_FUN_DRV	IO_MUX_FUN_DRV
Pull-up Resistor	IO_MUX_FUN_WPU	IO_MUX_MCU_WPU
Pull-down Resistor	IO_MUX_FUN_WPD	IO_MUX_MCU_WPD
Output Enable	OEN_SEL from GPIO matrix *	IO_MUX_MCU_OE

Note:
If IO_MUX_SLP_SEL is set to 0, pin functions remain the same in both normal execution and Light-sleep mode. Please refer to Section 5.5.2 for how to enable output in normal execution.

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5.9 Pin Hold Feature

Each GPIO pin (including the RTC pins) has an individual hold function controlled by an RTC register. When the pin is set to hold, the state is latched at that moment and will not change no matter how the internal signals change or how the IO MUX/GPIO configuration is modified. Users can use the hold function for the pins to retain the pin state through a core reset and system reset triggered by watchdog time-out or Deep-sleep events.

Note:

- For digital pins, to maintain pin input/output status in Deep-sleep mode, users can set RTC_CNTL_DG_PAD_FORCE_UNHOLD to 0 before powering down. For RTC pins, the input and output values are controlled by the corresponding bits of register RTC_CNTL_PAD_HOLD_REG, and users can set it to 1 to hold the value or set it to 0 to unhold the value.
- To disable the hold function after the chip is woken up, users can set RTC_CNTL_DG_PAD_FORCE_UNHOLD to 1. To maintain the hold function of the pin, users can set the corresponding bit in register RTC_CNTL_PAD_HOLD_REG to 1.

5.10 Power Supply and Management of GPIO Pins

5.10.1 Power Supply of GPIO Pins

For more information on the power supply for GPIO pins, please refer to Pin Definition in *ESP32-S3 Datasheet*.

5.10.2 Power Supply Management

Each ESP32-S3 pin is connected to one of the three different power domains.

- VDD3P3_RTC: the input power supply for both RTC and CPU
- VDD3P3_CPU: the input power supply for CPU
- VDD_SPI: configurable input/output power supply

VDD_SPI can be configured to use an internal LDO. The LDO input and output both are 1.8 V. If the LDO is not enabled, VDD_SPI is connected directly to the same power supply as VDD3P3_RTC.

The VDD_SPI configuration is determined by the value of strapping pin GPIO45, or can be overriden by eFuse and/or register settings. See *ESP32-S3 Datasheet* sections Power Scheme and Strapping Pins for more details.

Note that GPIO33 ~ GPIO37 can be powered either by VDD_SPI or VDD3P3_CPU.

5.11 Peripheral Signals via GPIO Matrix

Table 5-2 shows the peripheral input/output signals via GPIO matrix.

Please pay attention to the configuration of the bit GPIO_FUNC*n*_OEN_SEL:

- GPIO_FUNC*n*_OEN_SEL = 1: the output enable is controlled by the corresponding bit *n* of GPIO_ENABLE_REG:
  - GPIO_ENABLE_REG = 0: output is disabled;

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  - GPIO_ENABLE_REG = 1: output is enabled;

- GPIO_FUNC*n*_OEN_SEL = 0: use the output enable signal from peripheral, for example SPIQ_oe in the column “Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0” of Table 5-2. Note that the signals such as SPIQ_oe can be 1 (1’d1) or 0 (1’d0), depending on the configuration of corresponding peripherals. If it’s 1’d1 in the “Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0”, it indicates that once the register GPIO_FUNC*n*_OEN_SEL is cleared, the output signal is always enabled by default.

Note:

Signals are numbered consecutively, but not all signals are valid.

- Only the signals with a name assigned in the column ”Input signal” in Table 5-2 are valid input signals.
- Only the signals with a name assigned in the column ”Output signal” in Table 5-2 are valid output signals.

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Table 5-2. Peripheral Signals via GPIO Matrix

Signal No.	Input Signal	Default value	Direct Input via IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0	Direct Output via IO MUX
0	SPIQ_in	0	yes	SPIQ_out	SPIQ_oe	yes
1	SPID_in	0	yes	SPID_out	SPID_oe	yes
2	SPIHD_in	0	yes	SPIHD_out	SPIHD_oe	yes
3	SPIWP_in	0	yes	SPIWP_out	SPIWP_oe	yes
4	-	-	-	SPICLK_out_mux	SPICLK_oe	yes
5	-	-	-	SPICS0_out	SPICS0_oe	yes
6	-	-	-	SPICS1_out	SPICS1_oe	yes
7	SPID4_in	0	yes	SPID4_out	SPID4_oe	yes
8	SPID5_in	0	yes	SPID5_out	SPID5_oe	yes
9	SPID6_in	0	yes	SPID6_out	SPID6_oe	yes
10	SPID7_in	0	yes	SPID7_out	SPID7_oe	yes
11	SPIDQS_in	0	yes	SPIDQS_out	SPIDQS_oe	yes
12	U0RXD_in	0	yes	U0TXD_out	1'd1	yes
13	U0CTS_in	0	yes	U0RTS_out	1'd1	yes
14	U0DSR_in	0	no	U0DTR_out	1'd1	no
15	U1RXD_in	0	yes	U1TXD_out	1'd1	yes
16	U1CTS_in	0	yes	U1RTS_out	1'd1	yes
17	U1DSR_in	0	no	U1DTR_out	1'd1	no
18	U2RXD_in	0	no	U2TXD_out	1'd1	no
19	U2CTS_in	0	no	U2RTS_out	1'd1	no
20	U2DSR_in	0	no	U2DTR_out	1'd1	no
21	I2S1_MCLK_in	0	no	I2S1_MCLK_out	1'd1	no
22	I2S0O_BCK_in	0	no	I2S0O_BCK_out	1'd1	no
23	I2S0_MCLK_in	0	no	I2S0_MCLK_out	1'd1	no
24	I2S0O_WS_in	0	no	I2S0O_WS_out	1'd1	no

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Signal No.	Input Signal	Default value	Direct Input via IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0	Direct Output via IO MUX
25	I2S0I_SD_in	0	no	I2S0O_SD_out	1'd1	no
26	I2S0I_BCK_in	0	no	I2S0I_BCK_out	1'd1	no
27	I2S0I_WS_in	0	no	I2S0I_WS_out	1'd1	no
28	I2S1O_BCK_in	0	no	I2S1O_BCK_out	1'd1	no
29	I2S1O_WS_in	0	no	I2S1O_WS_out	1'd1	no
30	I2S1I_SD_in	0	no	I2S1O_SD_out	1'd1	no
31	I2S1I_BCK_in	0	no	I2S1I_BCK_out	1'd1	no
32	I2S1I_WS_in	0	no	I2S1I_WS_out	1'd1	no
33	pcnt_sig_ch0_in0	0	no	-	1'd1	no
34	pcnt_sig_ch1_in0	0	no	-	1'd1	no
35	pcnt_ctrl_ch0_in0	0	no	-	1'd1	-
36	pcnt_ctrl_ch1_in0	0	no	-	1'd1	-
37	pcnt_sig_ch0_in1	0	no	-	1'd1	-
38	pcnt_sig_ch1_in1	0	no	-	1'd1	-
39	pcnt_ctrl_ch0_in1	0	no	-	1'd1	-
40	pcnt_ctrl_ch1_in1	0	no	-	1'd1	-
41	pcnt_sig_ch0_in2	0	no	-	1'd1	-
42	pcnt_sig_ch1_in2	0	no	-	1'd1	-
43	pcnt_ctrl_ch0_in2	0	no	-	1'd1	-
44	pcnt_ctrl_ch1_in2	0	no	-	1'd1	-
45	pcnt_sig_ch0_in3	0	no	-	1'd1	-
46	pcnt_sig_ch1_in3	0	no	-	1'd1	-
47	pcnt_ctrl_ch0_in3	0	no	-	1'd1	-
48	pcnt_ctrl_ch1_in3	0	no	-	1'd1	-
49	-	-	-	-	1'd1	-
50	-	-	-	-	1'd1	-
51	I2S0I_SD1_in	0	no	-	1'd1	-

PRELIMINARY

Signal No.	Input Signal	Default value	Direct Input via IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0	Direct Output via IO MUX
52	I2S0I_SD2_in	0	no	-	1'd1	-
53	I2S0I_SD3_in	0	no	-	1'd1	-
54	Core1_gpio_in7	0	no	Core1_gpio_out7	1'd1	no
55	-	-	-	-	1'd1	-
56	-	-	-	-	1'd1	-
57	-	-	-	-	1'd1	-
58	usb_otg_iddig_in	0	no	-	1'd1	-
59	usb_otg_avalid_in	0	no	-	1'd1	-
60	usb_srp_bvalid_in	0	no	usb_otg_idpullup	1'd1	no
61	usb_otg_vbusvalid_in	0	no	usb_otg_dppulldown	1'd1	no
62	usb_srp_sessend_in	0	no	usb_otg_dmpulldown	1'd1	no
63	-	-	-	usb_otg_drvvbus	1'd1	no
64	-	-	-	usb_srp_chrgvbus	1'd1	no
65	-	-	-	usb_srp_dischrgvbus	1'd1	no
66	SPI3_CLK_in	0	no	SPI3_CLK_out_mux	SPI3_CLK_oe	no
67	SPI3_Q_in	0	no	SPI3_Q_out	SPI3_Q_oe	no
68	SPI3_D_in	0	no	SPI3_D_out	SPI3_D_oe	no
69	SPI3_HD_in	0	no	SPI3_HD_out	SPI3_HD_oe	no
70	SPI3_WP_in	0	no	SPI3_WP_out	SPI3_WP_oe	no
71	SPI3_CS0_in	0	no	SPI3_CS0_out	SPI3_CS0_oe	no
72	-	-	-	SPI3_CS1_out	SPI3_CS1_oe	no
73	ext_adc_start	0	no	ledc_ls_sig_out0	1'd1	no
74	-	-	-	ledc_ls_sig_out1	1'd1	no
75	-	-	-	ledc_ls_sig_out2	1'd1	no
76	-	-	-	ledc_ls_sig_out3	1'd1	no
77	-	-	-	ledc_ls_sig_out4	1'd1	no
78	-	-	-	ledc_ls_sig_out5	1'd1	no

PRELIMINARY

Signal No.	Input Signal	Default value	Direct Input via IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0	Direct Output via IO MUX
79	-	-	-	ledc_ls_sig_out6	1'd1	no
80	-	-	-	ledc_ls_sig_out7	1'd1	no
81	rmt_sig_in0	0	no	rmt_sig_out0	1'd1	no
82	rmt_sig_in1	0	no	rmt_sig_out1	1'd1	no
83	rmt_sig_in2	0	no	rmt_sig_out2	1'd1	no
84	rmt_sig_in3	0	no	rmt_sig_out3	1'd1	no
85	-	-	-	-	1'd1	-
86	-	-	-	-	1'd1	-
87	-	-	-	-	1'd1	-
88	-	-	-	-	1'd1	-
89	I2CEXT0_SCL_in	1	no	I2CEXT0_SCL_out	I2CEXT0_SCL_oe	no
90	I2CEXT0_SDA_in	1	no	I2CEXT0_SDA_out	I2CEXT0_SDA_oe	no
91	I2CEXT1_SCL_in	1	no	I2CEXT1_SCL_out	I2CEXT1_SCL_oe	no
92	I2CEXT1_SDA_in	1	no	I2CEXT1_SDA_out	I2CEXT1_SDA_oe	no
93	-	-	-	gpio_sd0_out	1'd1	no
94	-	-	-	gpio_sd1_out	1'd1	no
95	-	-	-	gpio_sd2_out	1'd1	no
96	-	-	-	gpio_sd3_out	1'd1	no
97	-	-	-	gpio_sd4_out	1'd1	no
98	-	-	-	gpio_sd5_out	1'd1	no
99	-	-	-	gpio_sd6_out	1'd1	no
100	-	-	-	gpio_sd7_out	1'd1	no
101	FSPICLK_in	0	yes	FSPICLK_out_mux	FSPICLK_oe	yes
102	FSPIQ_in	0	yes	FSPIQ_out	FSPIQ_oe	yes
103	FSPID_in	0	yes	FSPID_out	FSPID_oe	yes
104	FSPIHD_in	0	yes	FSPIHD_out	FSPIHD_oe	yes
105	FSPIWP_in	0	yes	FSPIWP_out	FSPIWP_oe	yes

PRELIMINARY

Signal No.	Input Signal	Default value	Direct Input via IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0	Direct Output via IO MUX
106	FSPIIO4_in	0	yes	FSPIIO4_out	FSPIIO4_oe	yes
107	FSPIIO5_in	0	yes	FSPIIO5_out	FSPIIO5_oe	yes
108	FSPIIO6_in	0	yes	FSPIIO6_out	FSPIIO6_oe	yes
109	FSPIIO7_in	0	yes	FSPIIO7_out	FSPIIO7_oe	yes
110	FSPICS0_in	0	yes	FSPICS0_out	FSPICS0_oe	yes
111	-	-	-	FSPICS1_out	FSPICS1_oe	no
112	-	-	-	FSPICS2_out	FSPICS2_oe	no
113	-	-	-	FSPICS3_out	FSPICS3_oe	no
114	-	-	-	FSPICS4_out	FSPICS4_oe	no
115	-	-	-	FSPICS5_out	FSPICS5_oe	no
116	twai_rx	1	no	twai_tx	1'd1	no
117	-	-	-	twai_bus_off_on	1'd1	no
118	-	-	-	twai_clkout	1'd1	no
119	-	-	-	SUBSPICLK_out_mux	SUBSPICLK_oe	no
120	SUBSPIQ_in	0	yes	SUBSPIQ_out	SUBSPIQ_oe	yes
121	SUBSPID_in	0	yes	SUBSPID_out	SUBSPID_oe	yes
122	SUBSPIHD_in	0	yes	SUBSPIHD_out	SUBSPIHD_oe	yes
123	SUBSPIWP_in	0	yes	SUBSPIWP_out	SUBSPIWP_oe	yes
124	-	-	-	SUBSPICS0_out	SUBSPICS0_oe	yes
125	-	-	-	SUBSPICS1_out	SUBSPICS1_oe	yes
126	-	-	-	FSPIDQS_out	FSPIDQS_oe	yes
127	-	-	-	SPI3_CS2_out	SPI3_CS2_oe	no
128	-	-	-	I2S0O_SD1_out	1'd1	no
129	Core1_gpio_in0	0	no	Core1_gpio_out0	1'd1	no
130	Core1_gpio_in1	0	no	Core1_gpio_out1	1'd1	no
131	Core1_gpio_in2	0	no	Core1_gpio_out2	1'd1	no
132	-	-	-	LCD_CS	1'd1	no

PRELIMINARY

Signal No.	Input Signal	Default value	Direct Input via IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0	Direct Output via IO MUX
133	CAM_DATA_in0	0	no	LCD_DATA_out0	1'd1	no
134	CAM_DATA_in1	0	no	LCD_DATA_out1	1'd1	no
135	CAM_DATA_in2	0	no	LCD_DATA_out2	1'd1	no
136	CAM_DATA_in3	0	no	LCD_DATA_out3	1'd1	no
137	CAM_DATA_in4	0	no	LCD_DATA_out4	1'd1	no
138	CAM_DATA_in5	0	no	LCD_DATA_out5	1'd1	no
139	CAM_DATA_in6	0	no	LCD_DATA_out6	1'd1	no
140	CAM_DATA_in7	0	no	LCD_DATA_out7	1'd1	no
141	CAM_DATA_in8	0	no	LCD_DATA_out8	1'd1	no
142	CAM_DATA_in9	0	no	LCD_DATA_out9	1'd1	no
143	CAM_DATA_in10	0	no	LCD_DATA_out10	1'd1	no
144	CAM_DATA_in11	0	no	LCD_DATA_out11	1'd1	no
145	CAM_DATA_in12	0	no	LCD_DATA_out12	1'd1	no
146	CAM_DATA_in13	0	no	LCD_DATA_out13	1'd1	no
147	CAM_DATA_in14	0	no	LCD_DATA_out14	1'd1	no
148	CAM_DATA_in15	0	no	LCD_DATA_out15	1'd1	no
149	CAM_PCLK	0	no	CAM_CLK	1'd1	no
150	CAM_H_ENABLE	0	no	LCD_H_ENABLE	1'd1	no
151	CAM_H_SYNC	0	no	LCD_H_SYNC	1'd1	no
152	CAM_V_SYNC	0	no	LCD_V_SYNC	1'd1	no
153	-	-	-	LCD_DC	1'd1	no
154	-	-	-	LCD_PCLK	1'd1	no
155	SUBSPID4_in	0	yes	SUBSPID4_out	SUBSPID4_oe	no
156	SUBSPID5_in	0	yes	SUBSPID5_out	SUBSPID5_oe	no
157	SUBSPID6_in	0	yes	SUBSPID6_out	SUBSPID6_oe	no
158	SUBSPID7_in	0	yes	SUBSPID7_out	SUBSPID7_oe	no
159	SUBSPIDQS_in	0	yes	SUBSPIDQS_out	SUBSPIDQS_oe	no

PRELIMINARY

Signal No.	Input Signal	Default value	Direct Input via IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0	Direct Output via IO MUX
160	pwm0_sync0_in	0	no	pwm0_out0a	1'd1	no
161	pwm0_sync1_in	0	no	pwm0_out0b	1'd1	no
162	pwm0_sync2_in	0	no	pwm0_out1a	1'd1	no
163	pwm0_f0_in	0	no	pwm0_out1b	1'd1	no
164	pwm0_f1_in	0	no	pwm0_out2a	1'd1	no
165	pwm0_f2_in	0	no	pwm0_out2b	1'd1	no
166	pwm0_cap0_in	0	no	pwm1_out0a	1'd1	no
167	pwm0_cap1_in	0	no	pwm1_out0b	1'd1	no
168	pwm0_cap2_in	0	no	pwm1_out1a	1'd1	no
169	pwm1_sync0_in	0	no	pwm1_out1b	1'd1	no
170	pwm1_sync1_in	0	no	pwm1_out2a	1'd1	no
171	pwm1_sync2_in	0	no	pwm1_out2b	1'd1	no
172	pwm1_f0_in	0	no	sdhost_cclk_out_1	1'd1	no
173	pwm1_f1_in	0	no	sdhost_cclk_out_2	1'd1	no
174	pwm1_f2_in	0	no	sdhost_rst_n_1	1'd1	no
175	pwm1_cap0_in	0	no	sdhost_rst_n_2	1'd1	no
176	pwm1_cap1_in	0	no	sdhost_ccmd_od_pullup_en_n	1'd1	no
177	pwm1_cap2_in	0	no	sdio_tohost_int_out	1'd1	no
178	sdhost_ccmd_in_1	1	no	sdhost_ccmd_out_1	sdhost_ccmd_out_en_1	no
179	sdhost_ccmd_in_2	1	no	sdhost_ccmd_out_2	sdhost_ccmd_out_en_2	no
180	sdhost_cdata_in_10	1	no	sdhost_cdata_out_10	sdhost_cdata_out_en_10	no
181	sdhost_cdata_in_11	1	no	sdhost_cdata_out_11	sdhost_cdata_out_en_11	no
182	sdhost_cdata_in_12	1	no	sdhost_cdata_out_12	sdhost_cdata_out_en_12	no
183	sdhost_cdata_in_13	1	no	sdhost_cdata_out_13	sdhost_cdata_out_en_13	no
184	sdhost_cdata_in_14	1	no	sdhost_cdata_out_14	sdhost_cdata_out_en_14	no
185	sdhost_cdata_in_15	1	no	sdhost_cdata_out_15	sdhost_cdata_out_en_15	no

PRELIMINARY

Signal No.	Input Signal	Default value	Direct Input via IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0	Direct Output via IO MUX
186	sdhost_cdata_in_16	1	no	sdhost_cdata_out_16	sdhost_cdata_out_en_16	no
187	sdhost_cdata_in_17	1	no	sdhost_cdata_out_17	sdhost_cdata_out_en_17	no
188	-	-	-	-	1'd1	-
189	-	-	-	-	1'd1	-
190	-	-	-	-	1'd1	-
191	-	-	-	-	1'd1	-
192	sdhost_data_strobe_1	0	no	-	1'd1	-
193	sdhost_data_strobe_2	0	no	-	1'd1	-
194	sdhost_card_detect_n_1	0	no	-	1'd1	-
195	sdhost_card_detect_n_2	0	no	-	1'd1	-
196	sdhost_card_write_prt_1	0	no	-	1'd1	-
197	sdhost_card_write_prt_2	0	no	-	1'd1	-
198	sdhost_card_int_n_1	0	no	-	1'd1	-
199	sdhost_card_int_n_2	0	no	-	1'd1	-
200	-	-	-	-	1'd1	no
201	-	-	-	-	1'd1	no
202	-	-	-	-	1'd1	no
203	-	-	-	-	1'd1	no
204	-	-	-	-	1'd1	no
205	-	-	-	-	1'd1	no
206	-	-	-	-	1'd1	no
207	-	-	-	-	1'd1	no
208	sig_in_func_208	0	no	sig_in_func208	1'd1	no
209	sig_in_func_209	0	no	sig_in_func209	1'd1	no
210	sig_in_func_210	0	no	sig_in_func210	1'd1	no
211	sig_in_func_211	0	no	sig_in_func211	1'd1	no
212	sig_in_func_212	0	no	sig_in_func212	1'd1	no

PRELIMINARY

Signal No.	Input Signal	Default value	Direct Input via IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0	Direct Output via IO MUX
213	sdhost_cdata_in_20	1	no	sdhost_cdata_out_20	sdhost_cdata_out_en_20	no
214	sdhost_cdata_in_21	1	no	sdhost_cdata_out_21	sdhost_cdata_out_en_21	no
215	sdhost_cdata_in_22	1	no	sdhost_cdata_out_22	sdhost_cdata_out_en_22	no
216	sdhost_cdata_in_23	1	no	sdhost_cdata_out_23	sdhost_cdata_out_en_23	no
217	sdhost_cdata_in_24	1	no	sdhost_cdata_out_24	sdhost_cdata_out_en_24	no
218	sdhost_cdata_in_25	1	no	sdhost_cdata_out_25	sdhost_cdata_out_en_25	no
219	sdhost_cdata_in_26	1	no	sdhost_cdata_out_26	sdhost_cdata_out_en_26	no
220	sdhost_cdata_in_27	1	no	sdhost_cdata_out_27	sdhost_cdata_out_en_27	no
221	pro_alonegpio_in0	0	no	pro_alonegpio_out0	1'd1	no
222	pro_alonegpio_in1	0	no	pro_alonegpio_out1	1'd1	no
223	pro_alonegpio_in2	0	no	pro_alonegpio_out2	1'd1	no
224	pro_alonegpio_in3	0	no	pro_alonegpio_out3	1'd1	no
225	pro_alonegpio_in4	0	no	pro_alonegpio_out4	1'd1	no
226	pro_alonegpio_in5	0	no	pro_alonegpio_out5	1'd1	no
227	pro_alonegpio_in6	0	no	pro_alonegpio_out6	1'd1	no
228	pro_alonegpio_in7	0	no	pro_alonegpio_out7	1'd1	no
229	-	-	-	-	1'd1	-
230	-	-	-	-	1'd1	-
231	-	-	-	-	1'd1	-
232	-	-	-	-	1'd1	-
233	-	-	-	-	1'd1	-
234	-	-	-	-	1'd1	-
235	-	-	-	-	1'd1	-
236	-	-	-	-	1'd1	-
237	-	-	-	-	1'd1	-
238	-	-	-	-	1'd1	-
239	-	-	-	-	1'd1	-

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Signal No.	Input Signal	Default value	Direct Input via IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0	Direct Output via IO MUX
240	-	-	-	-	1'd1	-
241	-	-	-	-	1'd1	-
242	-	-	-	-	1'd1	-
243	-	-	-	-	1'd1	-
244	-	-	-	-	1'd1	-
245	-	-	-	-	1'd1	-
246	-	-	-	-	1'd1	-
247	-	-	-	-	1'd1	-
248	-	-	-	-	1'd1	-
249	-	-	-	-	1'd1	-
250	-	-	-	-	1'd1	-
251	usb_jtag_tdo_bridge	0	no	usb_jtag_trst	1'd1	no
252	Core1_gpio_in3	0	no	Core1_gpio_out3	1'd1	no
253	Core1_gpio_in4	0	no	Core1_gpio_out4	1'd1	no
254	Core1_gpio_in5	0	no	Core1_gpio_out5	1'd1	no
255	Core1_gpio_in6	0	no	Core1_gpio_out6	1'd1	no

PRELIMINARY

5.12 IO MUX Function List

Table 5-3 shows the IO MUX functions of each GPIO pin.

Table 5-3. IO MUX Pin Functions

GPIO	Pin Name	Function 0	Function 1	Function 2	Function 3	Function 4	DRV	RST	Notes
0	GPIO0	GPIO0	GPIO0	-	-	-	2	3	R
1	GPIO1	GPIO1	GPIO1	-	-	-	2	1	R
2	GPIO2	GPIO2	GPIO2	-	-	-	2	1	R
3	GPIO3	GPIO3	GPIO3	-	-	-	2	1	R
4	GPIO4	GPIO4	GPIO4	-	-	-	2	0	R
5	GPIO5	GPIO5	GPIO5	-	-	-	2	0	R
6	GPIO6	GPIO6	GPIO6	-	-	-	2	0	R
7	GPIO7	GPIO7	GPIO7	-	-	-	2	0	R
8	GPIO8	GPIO8	GPIO8	-	SUBSPICS1	-	2	0	R
9	GPIO9	GPIO9	GPIO9	-	SUBSPIHD	FSPIHD	2	1	R
10	GPIO10	GPIO10	GPIO10	FSPIIO4	SUBSPICS0	FSPICS0	2	1	R
11	GPIO11	GPIO11	GPIO11	FSPIIO5	SUBSPID	FSPID	2	1	R
12	GPIO12	GPIO12	GPIO12	FSPIIO6	SUBSPICLK	FSPICLK	2	1	R
13	GPIO13	GPIO13	GPIO13	FSPIIO7	SUBSPIQ	FSPIQ	2	1	R
14	GPIO14	GPIO14	GPIO14	FSPIDQS	SUBSPIWP	FSPIWP	2	1	R
15	XTAL_32K_P	GPIO15	GPIO15	U0RTS	-	-	2	0	R
16	XTAL_32K_N	GPIO16	GPIO16	U0CTS	-	-	2	0	R
17	GPIO17	GPIO17	GPIO17	U1TXD	-	-	2	1	R
18	GPIO18	GPIO18	GPIO18	U1RXD	CLK_OUT3	-	2	1	R
19	GPIO19	GPIO19	GPIO19	U1RTS	CLK_OUT2	-	3	0	R
20	GPIO20	GPIO20	GPIO20	U1CTS	CLK_OUT1	-	3	0	R
21	GPIO21	GPIO21	GPIO21	-	-	-	2	0	R
26	SPICS1	SPICS1	GPIO26	-	-	-	2	3	-
27	SPIHD	SPIHD	GPIO27	-	-	-	2	3	-
28	SPIWP	SPIWP	GPIO28	-	-	-	2	3	-
29	SPICS0	SPICS0	GPIO29	-	-	-	2	3	-
30	SPICLK	SPICLK	GPIO30	-	-	-	2	3	-
31	SPIQ	SPIQ	GPIO31	-	-	-	2	3	-
32	SPID	SPID	GPIO32	-	-	-	2	3	-
33	GPIO33	GPIO33	GPIO33	FSPIHD	SUBSPIHD	SPIIO4	2	1	-
34	GPIO34	GPIO34	GPIO34	FSPICS0	SUBSPICS0	SPIIO5	2	1	-
35	GPIO35	GPIO35	GPIO35	FSPID	SUBSPID	SPIIO6	2	1	-
36	GPIO36	GPIO36	GPIO36	FSPICLK	SUBSPICLK	SPIIO7	2	1	-
37	GPIO37	GPIO37	GPIO37	FSPIQ	SUBSPIQ	SPIDQS	2	1	-
38	GPIO38	GPIO38	GPIO38	FSPIWP	SUBSPIWP	-	2	1	-
39	MTCK	MTCK	GPIO39	CLK_OUT3	SUBSPICS1	-	2	1*	-
40	MTDO	MTDO	GPIO40	CLK_OUT2	-	-	2	1	-
41	MTDI	MTDI	GPIO41	CLK_OUT1	-	-	2	1	-
42	MTMS	MTMS	GPIO42	-	-	-	2	1	-

PRELIMINARY

GPIO	Pin Name	Function 0	Function 1	Function 2	Function 3	Function 4	DRV	RST	Notes
43	U0TXD	U0TXD	GPIO43	CLK_OUT1	-	-	2	4	-
44	U0RXD	U0RXD	GPIO44	CLK_OUT2	-	-	2	3	-
45	GPIO45	GPIO45	GPIO45	-	-	-	2	2	-
46	GPIO46	GPIO46	GPIO46	-	-	-	2	2	-
47	SPICLK_P	SPICLK_DIFF	GPIO47	SUBSPICLK_P_DIFF	-	-	2	1	-
48	SPICLK_N	SPICLK_DIFF	GPIO48	SUBSPICLK_N_DIFF	-	-	2	1	-

Drive Strength

"DRV" column shows the drive strength of each pin after reset:

- **0** - Drive current = ~5 mA
- **1** - Drive current = ~10 mA
- **2** - Drive current = ~20 mA
- **3** - Drive current = ~40 mA

Reset Configurations

"RST" column shows the default configuration of each pin after reset:

- **0** - IE = 0 (input disabled)
- **1** - IE = 1 (input enabled)
- **2** - IE = 1, WPD = 1 (input enabled, pull-down resistor enabled)
- **3** - IE = 1, WPU = 1 (input enabled, pull-up resistor enabled)
- **4** - OE = 1, WPU = 1 (output enabled, pull-up resistor enabled)
- **1*** - If EFUSE_DIS_JTAG = 1, the pin MTCK is left floating after reset, i.e. IE = 1. If EFUSE_DIS_JTAG = 0, the pin MTCK is connected to internal pull-up resistor, i.e. IE = 1, WPU = 1.

Note:

- **R** - Pin has RTC/analog functions via RTC IO MUX.

Please refer to Appendix A – ESP32-S3 Pin Lists in *ESP32-S3 Datasheet* for more details.

5.13 RTC IO MUX Pin List

Table 5-4 shows the RTC pins, their corresponding GPIO pins and RTC functions.

Table 5-4. RTC Functions of RTC IO MUX Pins

RTC GPIO Num	GPIO Num	Pin Name	RTC Function			
			0	1	2	3
0	0	GPIO0	RTC_GPIO0	-	-	sar_i2c_scl_0[a]
1	1	GPIO1	RTC_GPIO1	-	-	sar_i2c_sda_0[a]
2	2	GPIO2	RTC_GPIO2	-	-	sar_i2c_scl_1[a]
3	3	GPIO3	RTC_GPIO3	-	-	sar_i2c_sda_1[a]

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Table 5-4 – cont'd from previous page

RTC GPIO Num	GPIO Num	Pin Name	RTC Function			
			0	1	2	3
4	4	GPIO4	RTC_GPIO4	-	-	-
5	5	GPIO5	RTC_GPIO5	-	-	-
6	6	GPIO6	RTC_GPIO6	-	-	-
7	7	GPIO7	RTC_GPIO7	-	-	-
8	8	GPIO8	RTC_GPIO8	-	-	-
9	9	GPIO9	RTC_GPIO9	-	-	-
10	10	GPIO10	RTC_GPIO10	-	-	-
11	11	GPIO11	RTC_GPIO11	-	-	-
12	12	GPIO12	RTC_GPIO12	-	-	-
13	13	GPIO13	RTC_GPIO13	-	-	-
14	14	GPIO14	RTC_GPIO14	-	-	-
15	15	XTAL_32K_P	RTC_GPIO15	-	-	-
16	16	XTAL_32K_N	RTC_GPIO16	-	-	-
17	17	GPIO17	RTC_GPIO17	-	-	-
18	18	GPIO18	RTC_GPIO18	-	-	-
19	19	GPIO19	RTC_GPIO19	-	-	-
20	20	GPIO20	RTC_GPIO20	-	-	-
21	21	GPIO21	RTC_GPIO21	-	-	-

[a] For more information on the configuration of sar_i2c_xx, see Section RTC I2C Controller in Chapter 1 *ULP Coprocessor (ULP-FSM, ULP-RISC-V)*.

Table 5-5 shows the RTC pins, their corresponding GPIO pins and analog functions.

Table 5-5. Analog Functions of RTC IO MUX Pins

RTC GPIO Num	GPIO Num	Pin Name	Analog Function	
			0	1
0	0	GPIO0	-	-
1	1	GPIO1	TOUCH1	ADC1_CH0
2	2	GPIO2	TOUCH2	ADC1_CH1
3	3	GPIO3	TOUCH3	ADC1_CH2
4	4	GPIO4	TOUCH4	ADC1_CH3
5	5	GPIO5	TOUCH5	ADC1_CH4
6	6	GPIO6	TOUCH6	ADC1_CH5
7	7	GPIO7	TOUCH7	ADC1_CH6
8	8	GPIO8	TOUCH8	ADC1_CH7
9	9	GPIO9	TOUCH9	ADC1_CH8
10	10	GPIO10	TOUCH10	ADC1_CH9
11	11	GPIO11	TOUCH11	ADC2_CH0
12	12	GPIO12	TOUCH12	ADC2_CH1
13	13	GPIO13	TOUCH13	ADC2_CH2
14	14	GPIO14	TOUCH14	ADC2_CH3

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RTC GPIO Num	GPIO Num	Pin Name	Analog Function	
			0	1
15	15	XTAL_32K_P	XTAL_32K_P	ADC2_CH4
16	16	XTAL_32K_N	XTAL_32K_N	ADC2_CH5
17	17	GPIO17	-	ADC2_CH6
18	18	GPIO18	-	ADC2_CH7
19	19	GPIO19	USB_D-	ADC2_CH8
20	20	GPIO20	USB_D+	ADC2_CH9
21	21	GPIO21	-	-

5.14 Register Summary

5.14.1 GPIO Matrix Register Summary

The addresses in this section are relative to the GPIO base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
GPIO Configuration Registers			
GPIO_BT_SELECT_REG	GPIO bit select register	0x0000	R/W
GPIO_OUT_REG	GPIO0 ~ 31 output register	0x0004	R/W
GPIO_OUT_W1TS_REG	GPIO0 ~ 31 output bit set register	0x0008	WO
GPIO_OUT_W1TC_REG	GPIO0 ~ 31 output bit clear register	0x000C	WO
GPIO_OUT1_REG	GPIO32 ~ 48 output register	0x0010	R/W
GPIO_OUT1_W1TS_REG	GPIO32 ~ 48 output bit set register	0x0014	WO
GPIO_OUT1_W1TC_REG	GPIO32 ~ 48 output bit clear register	0x0018	WO
GPIO_SDIO_SELECT_REG	GPIO SDIO selection register	0x001C	R/W
GPIO_ENABLE_REG	GPIO0 ~ 31 output enable register	0x0020	R/W
GPIO_ENABLE_W1TS_REG	GPIO0 ~ 31 output enable bit set register	0x0024	WO
GPIO_ENABLE_W1TC_REG	GPIO0 ~ 31 output enable bit clear register	0x0028	WO
GPIO_ENABLE1_REG	GPIO32 ~ 48 output enable register	0x002C	R/W
GPIO_ENABLE1_W1TS_REG	GPIO32 ~ 48 output enable bit set register	0x0030	WO
GPIO_ENABLE1_W1TC_REG	GPIO32 ~ 48 output enable bit clear register	0x0034	WO
GPIO_STRAP_REG	Strapping pin value register	0x0038	RO
GPIO_IN_REG	GPIO0 ~ 31 input register	0x003C	RO
GPIO_IN1_REG	GPIO32 ~ 48 input register	0x0040	RO
GPIO_PIN0_REG	Configuration for GPIO pin 0	0x0074	R/W
GPIO_PIN1_REG	Configuration for GPIO pin 1	0x0078	R/W
GPIO_PIN2_REG	Configuration for GPIO pin 2	0x007C	R/W
...	...	...	...
GPIO_PIN46_REG	Configuration for GPIO pin 46	0x012C	R/W
GPIO_PIN47_REG	Configuration for GPIO pin 47	0x0130	R/W
GPIO_PIN48_REG	Configuration for GPIO pin 48	0x0134	R/W
GPIO_FUNC0_IN_SEL_CFG_REG	Peripheral function 0 input selection register	0x0154	R/W
GPIO_FUNC1_IN_SEL_CFG_REG	Peripheral function 1 input selection register	0x0158	R/W

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Name	Description	Address	Access
GPIO_FUNC2_IN_SEL_CFG_REG	Peripheral function 2 input selection register	0x015C	R/W
...	...	...	...
GPIO_FUNC253_IN_SEL_CFG_REG	Peripheral function 253 input selection register	0x0548	R/W
GPIO_FUNC254_IN_SEL_CFG_REG	Peripheral function 254 input selection register	0x054C	R/W
GPIO_FUNC255_IN_SEL_CFG_REG	Peripheral function 255 input selection register	0x0550	R/W
GPIO_FUNC0_OUT_SEL_CFG_REG	Peripheral output selection for GPIO0	0x0554	R/W
GPIO_FUNC1_OUT_SEL_CFG_REG	Peripheral output selection for GPIO1	0x0558	R/W
GPIO_FUNC2_OUT_SEL_CFG_REG	Peripheral output selection for GPIO2	0x055C	R/W
...	...	...	...
GPIO_FUNC47_OUT_SEL_CFG_REG	Peripheral output selection for GPIO47	0x0610	R/W
GPIO_FUNC48_OUT_SEL_CFG_REG	Peripheral output selection for GPIO47	0x0614	R/W
GPIO_CLOCK_GATE_REG	GPIO clock gating register	0x062C	R/W
Interrupt Status Registers			
GPIO_STATUS_REG	GPIO0 ~ 31 interrupt status register	0x0044	R/W
GPIO_STATUS1_REG	GPIO32 ~ 48 interrupt status register	0x0050	R/W
GPIO_CPU_INT_REG	GPIO0 ~ 31 CPU interrupt status register	0x005C	RO
GPIO_CPU_NMI_INT_REG	GPIO0 ~ 31 CPU non-maskable interrupt status register	0x0060	RO
GPIO_CPU_INT1_REG	GPIO32 ~ 48 CPU interrupt status register	0x0068	RO
GPIO_CPU_NMI_INT1_REG	GPIO32 ~ 48 CPU non-maskable interrupt status register	0x006C	RO
Interrupt Configuration Registers			
GPIO_STATUS_W1TS_REG	GPIO0 ~ 31 interrupt status bit set register	0x0048	WO
GPIO_STATUS_W1TC_REG	GPIO0 ~ 31 interrupt status bit clear register	0x004C	WO
GPIO_STATUS1_W1TS_REG	GPIO32 ~ 48 interrupt status bit set register	0x0054	WO
GPIO_STATUS1_W1TC_REG	GPIO32 ~ 48 interrupt status bit clear register	0x0058	WO
GPIO Interrupt Source Registers			
GPIO_STATUS_NEXT_REG	GPIO0 ~ 31 interrupt source register	0x014C	RO
GPIO_STATUS_NEXT1_REG	GPIO32 ~ 48 interrupt source register	0x0150	RO
Version Register			
GPIO_DATE_REG	Version control register	0x06FC	R/W

5.14.2 IO MUX Register Summary

The addresses in this section are relative to the IO MUX base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
IO_MUX_PIN_CTRL_REG	Clock output configuration register	0x0000	R/W
IO_MUX_GPIO0_REG	Configuration register for pin GPIO0	0x0004	R/W
IO_MUX_GPIO1_REG	Configuration register for pin GPIO1	0x0008	R/W
IO_MUX_GPIO2_REG	Configuration register for pin GPIO2	0x000C	R/W
IO_MUX_GPIO3_REG	Configuration register for pin GPIO3	0x0010	R/W
IO_MUX_GPIO4_REG	Configuration register for pin GPIO4	0x0014	R/W

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Name	Description	Address	Access
IO_MUX_GPIO5_REG	Configuration register for pin GPIO5	0x0018	R/W
IO_MUX_GPIO6_REG	Configuration register for pin GPIO6	0x001C	R/W
IO_MUX_GPIO7_REG	Configuration register for pin GPIO7	0x0020	R/W
IO_MUX_GPIO8_REG	Configuration register for pin GPIO8	0x0024	R/W
IO_MUX_GPIO9_REG	Configuration register for pin GPIO9	0x0028	R/W
IO_MUX_GPIO10_REG	Configuration register for pin GPIO10	0x002C	R/W
IO_MUX_GPIO11_REG	Configuration register for pin GPIO11	0x0030	R/W
IO_MUX_GPIO12_REG	Configuration register for pin GPIO12	0x0034	R/W
IO_MUX_GPIO13_REG	Configuration register for pin GPIO13	0x0038	R/W
IO_MUX_GPIO14_REG	Configuration register for pin GPIO14	0x003C	R/W
IO_MUX_GPIO15_REG	Configuration register for pad XTAL_32K_P	0x0040	R/W
IO_MUX_GPIO16_REG	Configuration register for pad XTAL_32K_N	0x0044	R/W
IO_MUX_GPIO17_REG	Configuration register for pad DAC_1	0x0048	R/W
IO_MUX_GPIO18_REG	Configuration register for pad DAC_2	0x004C	R/W
IO_MUX_GPIO19_REG	Configuration register for pin GPIO19	0x0050	R/W
IO_MUX_GPIO20_REG	Configuration register for pin GPIO20	0x0054	R/W
IO_MUX_GPIO21_REG	Configuration register for pin GPIO21	0x0058	R/W
IO_MUX_GPIO26_REG	Configuration register for pad SPICS1	0x006C	R/W
IO_MUX_GPIO27_REG	Configuration register for pad SPIHD	0x0070	R/W
IO_MUX_GPIO28_REG	Configuration register for pad SPIWP	0x0074	R/W
IO_MUX_GPIO29_REG	Configuration register for pad SPICS0	0x0078	R/W
IO_MUX_GPIO30_REG	Configuration register for pad SPICLK	0x007C	R/W
IO_MUX_GPIO31_REG	Configuration register for pad SPIQ	0x0080	R/W
IO_MUX_GPIO32_REG	Configuration register for pad SPID	0x0084	R/W
IO_MUX_GPIO33_REG	Configuration register for pin GPIO33	0x0088	R/W
IO_MUX_GPIO34_REG	Configuration register for pin GPIO34	0x008C	R/W
IO_MUX_GPIO35_REG	Configuration register for pin GPIO35	0x0090	R/W
IO_MUX_GPIO36_REG	Configuration register for pin GPIO36	0x0094	R/W
IO_MUX_GPIO37_REG	Configuration register for pin GPIO37	0x0098	R/W
IO_MUX_GPIO38_REG	Configuration register for pin GPIO38	0x009C	R/W
IO_MUX_GPIO39_REG	Configuration register for pad MTCK	0x00A0	R/W
IO_MUX_GPIO40_REG	Configuration register for pad MTDO	0x00A4	R/W
IO_MUX_GPIO41_REG	Configuration register for pad MTDI	0x00A8	R/W
IO_MUX_GPIO42_REG	Configuration register for pad MTMS	0x00AC	R/W
IO_MUX_GPIO43_REG	Configuration register for pad U0TXD	0x00B0	R/W
IO_MUX_GPIO44_REG	Configuration register for pad U0RXD	0x00B4	R/W
IO_MUX_GPIO45_REG	Configuration register for pin GPIO45	0x00B8	R/W
IO_MUX_GPIO46_REG	Configuration register for pin GPIO46	0x00BC	R/W
IO_MUX_GPIO47_REG	Configuration register for pin GPIO47	0x00C0	R/W
IO_MUX_GPIO48_REG	Configuration register for pin GPIO48	0x00C4	R/W

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5.14.3 SDM Output Register Summary

The addresses in this section are relative to (GPIO base address provided in Table 3-3 in Chapter 3 *System and Memory* + 0x0F00).

Name	Description	Address	Access
Configuration Registers			
GPIO_SIGMADELTA0_REG	Duty Cycle Configure Register of SDM0	0x0000	R/W
GPIO_SIGMADELTA1_REG	Duty Cycle Configure Register of SDM1	0x0004	R/W
GPIO_SIGMADELTA2_REG	Duty Cycle Configure Register of SDM2	0x0008	R/W
GPIO_SIGMADELTA3_REG	Duty Cycle Configure Register of SDM3	0x000C	R/W
GPIO_SIGMADELTA4_REG	Duty Cycle Configure Register of SDM4	0x0010	R/W
GPIO_SIGMADELTA5_REG	Duty Cycle Configure Register of SDM5	0x0014	R/W
GPIO_SIGMADELTA6_REG	Duty Cycle Configure Register of SDM6	0x0018	R/W
GPIO_SIGMADELTA7_REG	Duty Cycle Configure Register of SDM7	0x001C	R/W
GPIO_SIGMADELTA_CG_REG	Clock Gating Configure Register	0x0020	R/W
GPIO_SIGMADELTA_MISC_REG	MISC Register	0x0024	R/W
GPIO_SIGMADELTA_VERSION_REG	Version Control Register	0x0028	R/W

5.14.4 RTC IO MUX Register Summary

The addresses in this section are relative to (Low-Power Management base address provided in Table 3-3 in Chapter 3 *System and Memory* + 0x0400).

Name	Description	Address	Access
GPIO configuration/data registers			
RTC_GPIO_OUT_REG	RTC GPIO output register	0x0000	R/W
RTC_GPIO_OUT_W1TS_REG	RTC GPIO output bit set register	0x0004	WO
RTC_GPIO_OUT_W1TC_REG	RTC GPIO output bit clear register	0x0008	WO
RTC_GPIO_ENABLE_REG	RTC GPIO output enable register	0x000C	R/W
RTC_GPIO_ENABLE_W1TS_REG	RTC GPIO output enable bit set register	0x0010	WO
RTC_GPIO_ENABLE_W1TC_REG	RTC GPIO output enable bit clear register	0x0014	WO
RTC_GPIO_STATUS_REG	RTC GPIO interrupt status register	0x0018	R/W
RTC_GPIO_STATUS_W1TS_REG	RTC GPIO interrupt status bit set register	0x001C	WO
RTC_GPIO_STATUS_W1TC_REG	RTC GPIO interrupt status bit clear register	0x0020	WO
RTC_GPIO_IN_REG	RTC GPIO input register	0x0024	RO
RTC_GPIO_PIN0_REG	RTC configuration for pin 0	0x0028	R/W
RTC_GPIO_PIN1_REG	RTC configuration for pin 1	0x002C	R/W
RTC_GPIO_PIN2_REG	RTC configuration for pin 2	0x0030	R/W
RTC_GPIO_PIN3_REG	RTC configuration for pin 3	0x0034	R/W
RTC_GPIO_PIN4_REG	RTC configuration for pin 4	0x0038	R/W
RTC_GPIO_PIN5_REG	RTC configuration for pin 5	0x003C	R/W
RTC_GPIO_PIN6_REG	RTC configuration for pin 6	0x0040	R/W
RTC_GPIO_PIN7_REG	RTC configuration for pin 7	0x0044	R/W
RTC_GPIO_PIN8_REG	RTC configuration for pin 8	0x0048	R/W
RTC_GPIO_PIN9_REG	RTC configuration for pin 9	0x004C	R/W

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Name	Description	Address	Access
RTC_GPIO_PIN10_REG	RTC configuration for pin 10	0x0050	R/W
RTC_GPIO_PIN11_REG	RTC configuration for pin 11	0x0054	R/W
RTC_GPIO_PIN12_REG	RTC configuration for pin 12	0x0058	R/W
RTC_GPIO_PIN13_REG	RTC configuration for pin 13	0x005C	R/W
RTC_GPIO_PIN14_REG	RTC configuration for pin 14	0x0060	R/W
RTC_GPIO_PIN15_REG	RTC configuration for pin 15	0x0064	R/W
RTC_GPIO_PIN16_REG	RTC configuration for pin 16	0x0068	R/W
RTC_GPIO_PIN17_REG	RTC configuration for pin 17	0x006C	R/W
RTC_GPIO_PIN18_REG	RTC configuration for pin 18	0x0070	R/W
RTC_GPIO_PIN19_REG	RTC configuration for pin 19	0x0074	R/W
RTC_GPIO_PIN20_REG	RTC configuration for pin 20	0x0078	R/W
RTC_GPIO_PIN21_REG	RTC configuration for pin 21	0x007C	R/W
GPIO RTC function configuration registers			
RTC_IO_TOUCH_PAD0_REG	Touch pin 0 configuration register	0x0084	R/W
RTC_IO_TOUCH_PAD1_REG	Touch pin 1 configuration register	0x0088	R/W
RTC_IO_TOUCH_PAD2_REG	Touch pin 2 configuration register	0x008C	R/W
RTC_IO_TOUCH_PAD3_REG	Touch pin 3 configuration register	0x0090	R/W
RTC_IO_TOUCH_PAD4_REG	Touch pin 4 configuration register	0x0094	R/W
RTC_IO_TOUCH_PAD5_REG	Touch pin 5 configuration register	0x0098	R/W
RTC_IO_TOUCH_PAD6_REG	Touch pin 6 configuration register	0x009C	R/W
RTC_IO_TOUCH_PAD7_REG	Touch pin 7 configuration register	0x00A0	R/W
RTC_IO_TOUCH_PAD8_REG	Touch pin 8 configuration register	0x00A4	R/W
RTC_IO_TOUCH_PAD9_REG	Touch pin 9 configuration register	0x00A8	R/W
RTC_IO_TOUCH_PAD10_REG	Touch pin 10 configuration register	0x00AC	R/W
RTC_IO_TOUCH_PAD11_REG	Touch pin 11 configuration register	0x00B0	R/W
RTC_IO_TOUCH_PAD12_REG	Touch pin 12 configuration register	0x00B4	R/W
RTC_IO_TOUCH_PAD13_REG	Touch pin 13 configuration register	0x00B8	R/W
RTC_IO_TOUCH_PAD14_REG	Touch pin 14 configuration register	0x00BC	R/W
RTC_IO_XTAL_32P_PAD_REG	32 kHz crystal P-pin configuration register	0x00C0	R/W
RTC_IO_XTAL_32N_PAD_REG	32 kHz crystal N-pin configuration register	0x00C4	R/W
RTC_IO_RTC_PAD17_REG	RTC pin 17 configuration register	0x00C8	R/W
RTC_IO_RTC_PAD18_REG	RTC pin 18 configuration register	0x00CC	R/W
RTC_IO_RTC_PAD19_REG	RTC pin 19 configuration register	0x00D0	R/W
RTC_IO_RTC_PAD20_REG	RTC pin 20 configuration register	0x00D4	R/W
RTC_IO_RTC_PAD21_REG	RTC pin 21 configuration register	0x00D8	R/W
RTC_IO_XTL_EXT_CTR_REG	Crystal power down enable GPIO source	0x00E0	R/W
RTC_IO_SAR_I2C_IO_REG	RTC I2C pin selection	0x00E4	R/W
Version Register			
RTC_IO_DATE_REG	Version control register	0x01FC	R/W

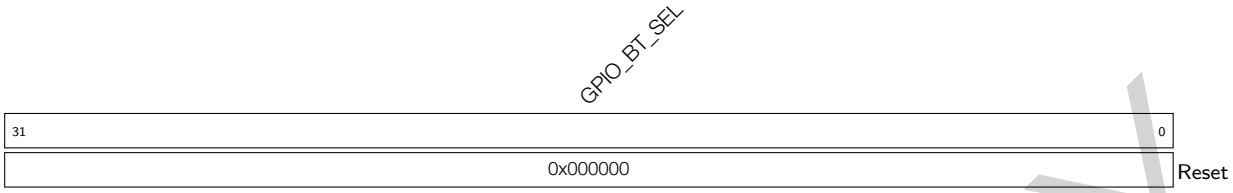
5.15 Registers

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5.15.1 GPIO Matrix Registers

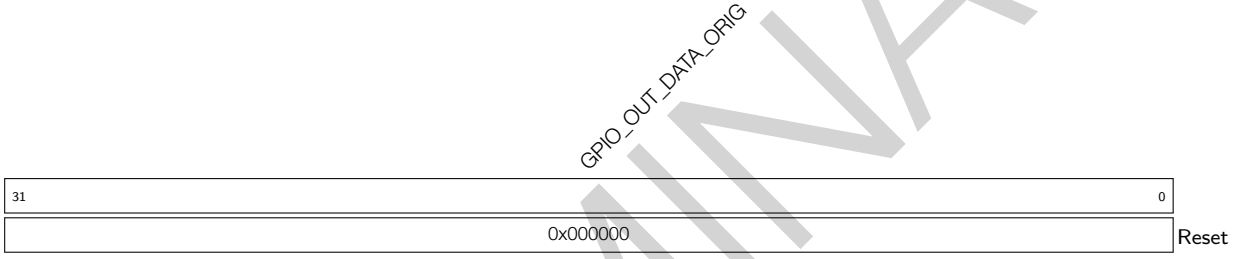
The addresses in this section are relative to the GPIO base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 5.1. GPIO_BT_SELECT_REG (0x0000)



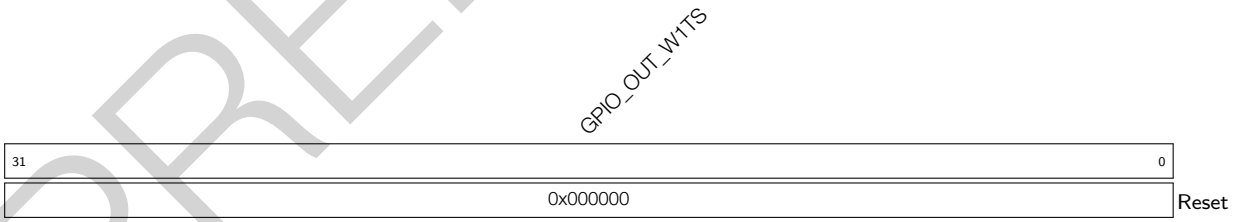
GPIO_BT_SEL Reserved (R/W)

Register 5.2. GPIO_OUT_REG (0x0004)



GPIO_OUT_DATA_ORIG GPIO0 ~ 21 and GPIO26 ~ 31 output values in simple GPIO output mode. The values of bit0 ~ bit21 correspond to the output values of GPIO0 ~ 21, and bit26 ~ bit31 to GPIO26 ~ 31. Bit22 ~ bit25 are invalid. (R/W)

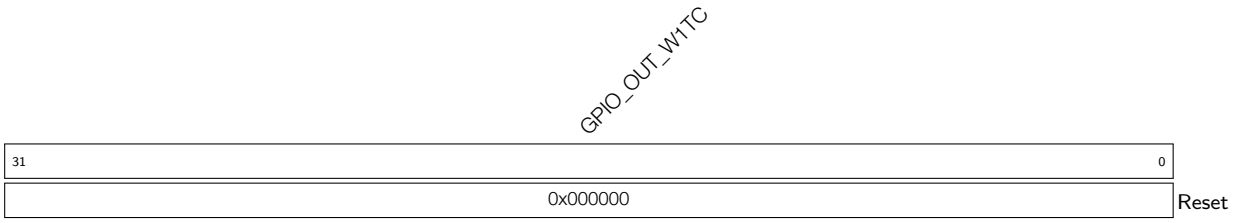
Register 5.3. GPIO_OUT_W1TS_REG (0x0008)



GPIO_OUT_W1TS GPIO0 ~ 31 output set register. If the value 1 is written to a bit here, the corresponding bit in GPIO_OUT_REG will be set to 1. Recommended operation: use this register to set GPIO_OUT_REG. (WO)

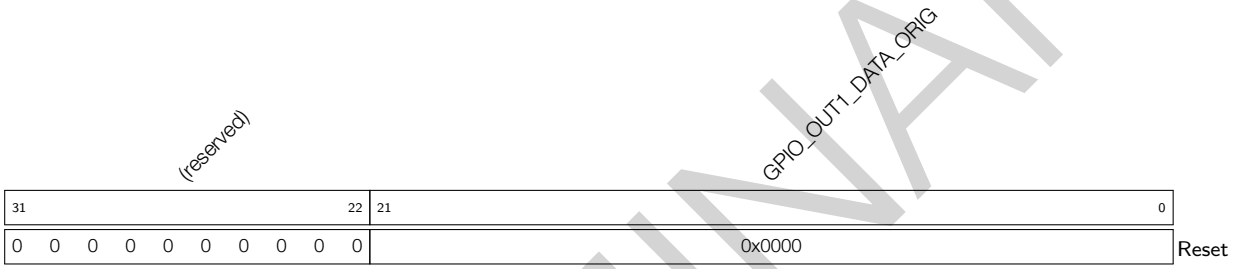
PRELIMINARY

Register 5.4. GPIO_OUT_W1TC_REG (0x000C)



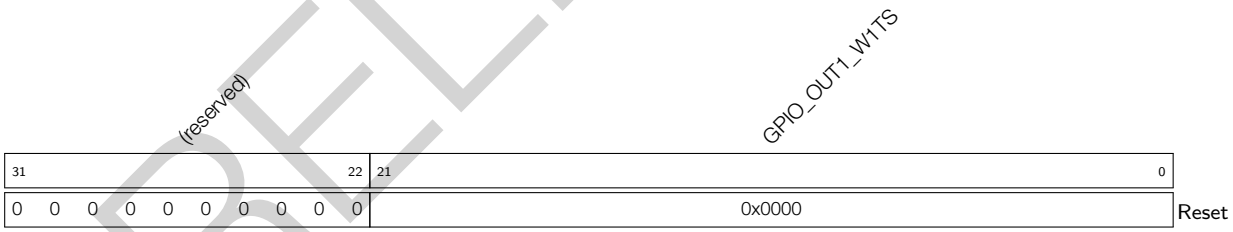
GPIO_OUT_W1TC GPIO0 ~ 31 output clear register. If the value 1 is written to a bit here, the corresponding bit in GPIO_OUT_REG will be cleared. Recommended operation: use this register to clear GPIO_OUT_REG. (WO)

Register 5.5. GPIO_OUT1_REG (0x0010)



GPIO_OUT1_DATA_ORIG GPIO32 ~ 48 output value in simple GPIO output mode. The values of bit0 ~ bit16 correspond to GPIO32 ~ GPIO48. Bit17 ~ bit21 are invalid. (R/W)

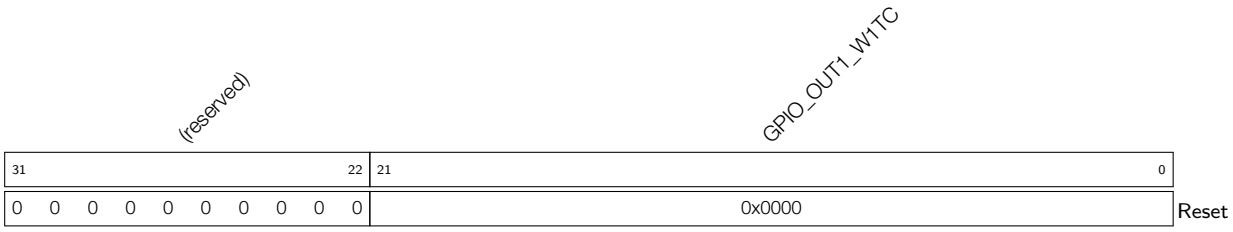
Register 5.6. GPIO_OUT1_W1TS_REG (0x0014)



GPIO_OUT1_W1TS GPIO32 ~ 48 output value set register. If the value 1 is written to a bit here, the corresponding bit in GPIO_OUT1_REG will be set to 1. Recommended operation: use this register to set GPIO_OUT1_REG. (WO)

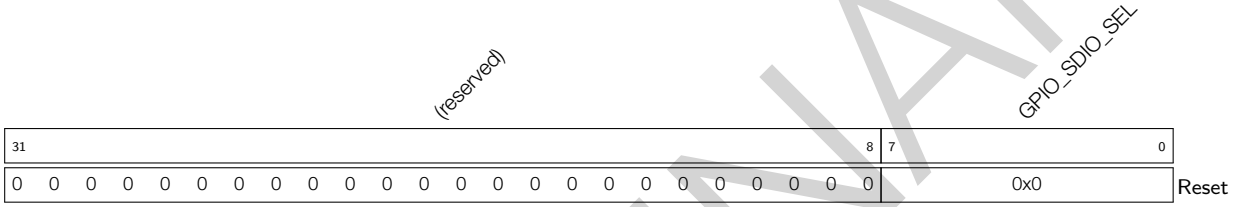
PRELIMINARY

Register 5.7. GPIO_OUT1_W1TC_REG (0x0018)



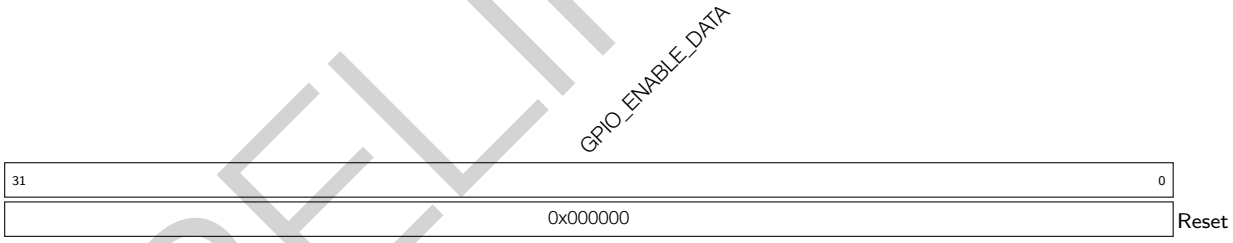
GPIO_OUT1_W1TC GPIO32 ~ 48 output value clear register. If the value 1 is written to a bit here, the corresponding bit in GPIO_OUT1_REG will be cleared. Recommended operation: use this register to clear GPIO_OUT1_REG. (WO)

Register 5.8. GPIO_SDIO_SELECT_REG (0x001C)



GPIO_SDIO_SEL Reserved (R/W)

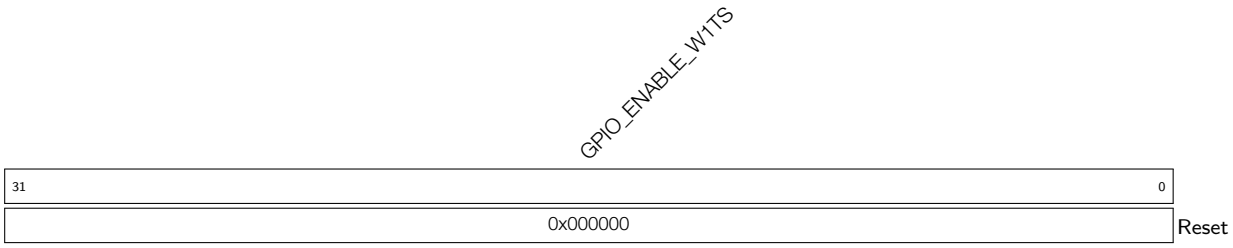
Register 5.9. GPIO_ENABLE_REG (0x0020)



GPIO_ENABLE_DATA GPIO0~31 output enable register. (R/W)

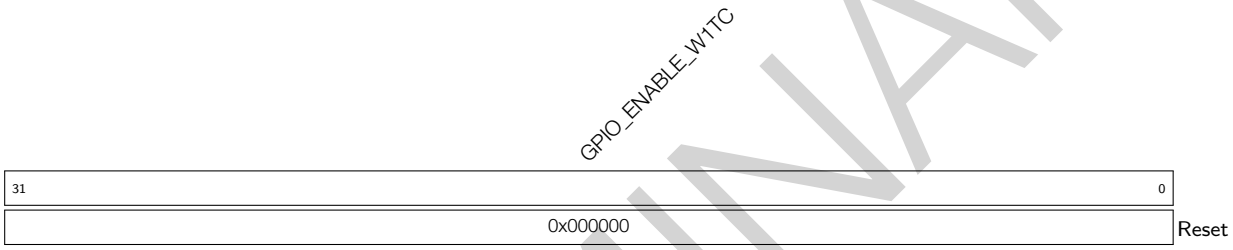
PRELIMINARY

Register 5.10. GPIO_ENABLE_W1TS_REG (0x0024)



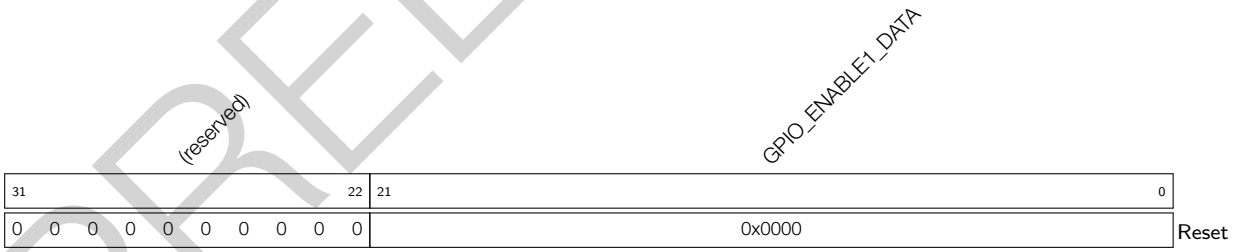
GPIO_ENABLE_W1TS GPIO0 ~ 31 output enable set register. If the value 1 is written to a bit here, the corresponding bit in GPIO_ENABLE_REG will be set to 1. Recommended operation: use this register to set GPIO_ENABLE_REG. (WO)

Register 5.11. GPIO_ENABLE_W1TC_REG (0x0028)



GPIO_ENABLE_W1TC GPIO0 ~ 31 output enable clear register. If the value 1 is written to a bit here, the corresponding bit in GPIO_ENABLE_REG will be cleared. Recommended operation: use this register to clear GPIO_ENABLE_REG. (WO)

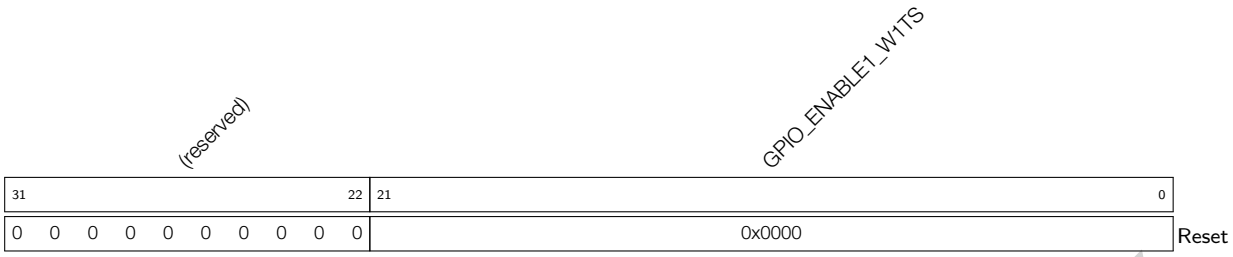
Register 5.12. GPIO_ENABLE1_REG (0x002C)



GPIO_ENABLE1_DATA GPIO32 ~ 48 output enable register. (R/W)

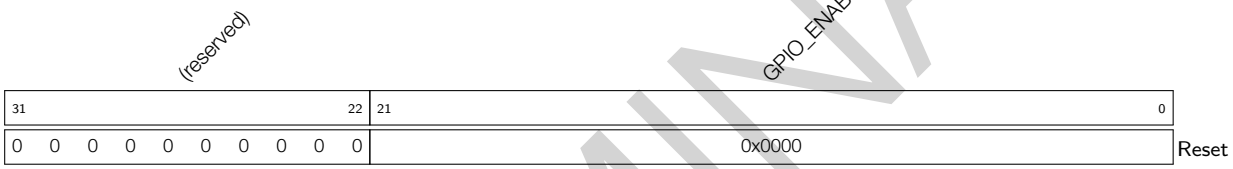
PRELIMINARY

Register 5.13. GPIO_ENABLE1_W1TS_REG (0x0030)



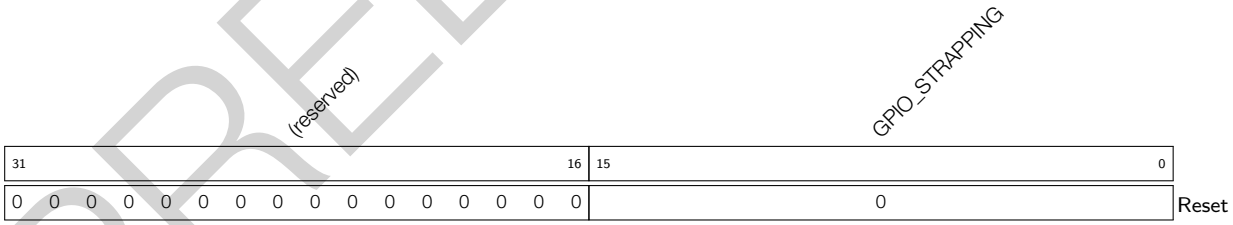
GPIO_ENABLE1_W1TS GPIO32 ~ 48 output enable set register. If the value 1 is written to a bit here, the corresponding bit in GPIO_ENABLE1_REG will be set to 1. Recommended operation: use this register to set GPIO_ENABLE1_REG. (WO)

Register 5.14. GPIO_ENABLE1_W1TC_REG (0x0034)



GPIO_ENABLE1_W1TC GPIO32 ~ 48 output enable clear register. If the value 1 is written to a bit here, the corresponding bit in GPIO_ENABLE1_REG will be cleared. Recommended operation: use this register to clear GPIO_ENABLE1_REG. (WO)

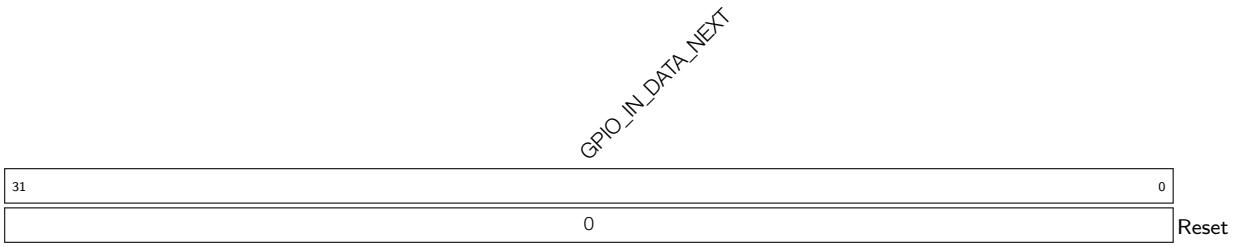
Register 5.15. GPIO_STRAP_REG (0x0038)



GPIO_STRAPPING GPIO strapping values: bit5 ~ bit2 correspond to stripping pins GPIO3, GPIO45, GPIO0, and GPIO46 respectively. (RO)

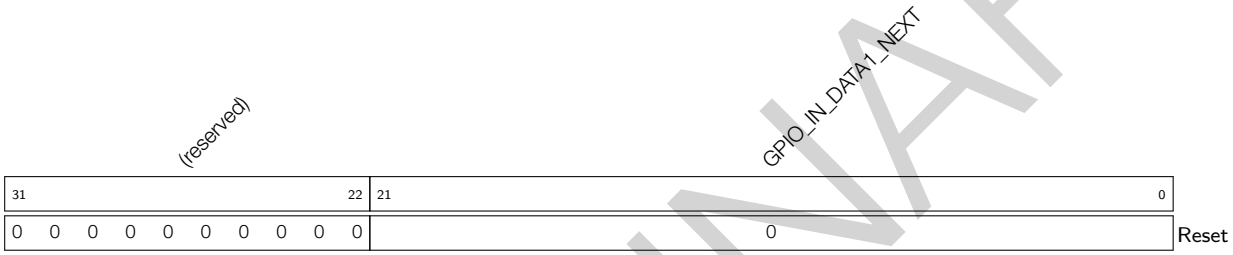
PRELIMINARY

Register 5.16. GPIO_IN_REG (0x003C)



GPIO_IN_DATA_NEXT GPIO0 ~ 31 input value. Each bit represents a pin input value, 1 for high level and 0 for low level. (RO)

Register 5.17. GPIO_IN1_REG (0x0040)



GPIO_IN_DATA1_NEXT GPIO32 ~ 48 input value. Each bit represents a pin input value. (RO)

PRELIMINARY

Register 5.18. GPIO_PIN*n*_REG (*n*: 0-48) (0x0074+0x4n*)**



GPIO_PIN*n*_SYNC2_BYPASS For the second stage synchronization, GPIO input data can be synchronized on either edge of the APB clock. 0: no synchronization; 1: synchronized on falling edge; 2 and 3: synchronized on rising edge. (R/W)

GPIO_PIN*n*_PAD_DRIVER Pin driver selection. 0: normal output; 1: open drain output. (R/W)

GPIO_PIN*n*_SYNC1_BYPASS For the first stage synchronization, GPIO input data can be synchronized on either edge of the APB clock. 0: no synchronization; 1: synchronized on falling edge; 2 and 3: synchronized on rising edge. (R/W)

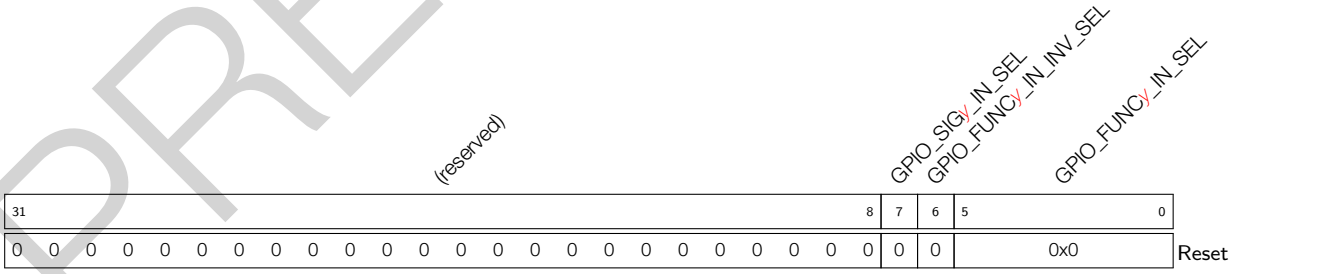
GPIO_PIN*n*_INT_TYPE Interrupt type selection. 0: GPIO interrupt disabled; 1: rising edge trigger; 2: falling edge trigger; 3: any edge trigger; 4: low level trigger; 5: high level trigger. (R/W)

GPIO_PIN*n*_WAKEUP_ENABLE GPIO wake-up enable bit, only wakes up the CPU from Light-sleep. (R/W)

GPIO_PIN*n*_CONFIG Reserved (R/W)

GPIO_PIN*n*_INT_ENA Interrupt enable bits. bit13: CPU interrupt enabled; bit14: CPU non-maskable interrupt enabled. (R/W)

Register 5.19. GPIO_FUNC*y*_IN_SEL_CFG_REG (*y*: 0-255) (0x0154+0x4y*)**



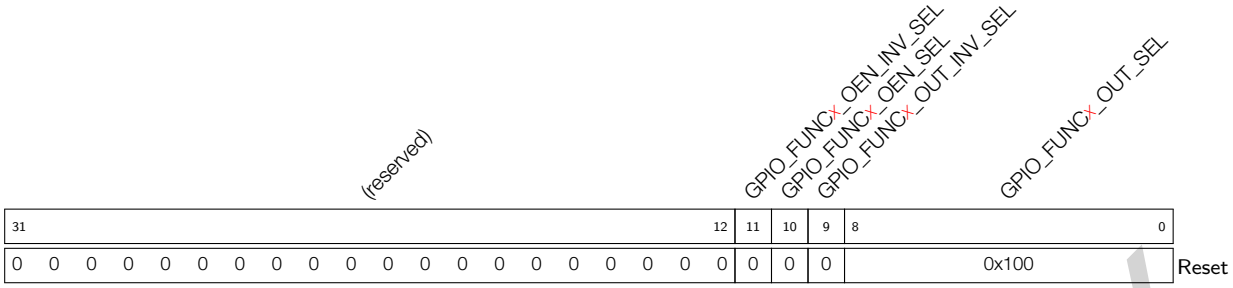
GPIO_FUNC*y*_IN_SEL Selection control for peripheral input signal *Y*, selects a pin from the 48 GPIO matrix pins to connect this input signal. Or selects 0x38 for a constantly high input or 0x3C for a constantly low input. (R/W)

GPIO_FUNC*y*_IN_INV_SEL 1: Invert the input value; 0: Do not invert the input value. (R/W)

GPIO_SIG*y*_IN_SEL Bypass GPIO matrix. 1: route signals via GPIO matrix, 0: connect signals directly to peripheral configured in IO MUX. (R/W)

PRELIMINARY

Register 5.20. GPIO_FUNC*x*_OUT_SEL_CFG_REG (*x*: 0-48) (0x0554+0x4x*)**



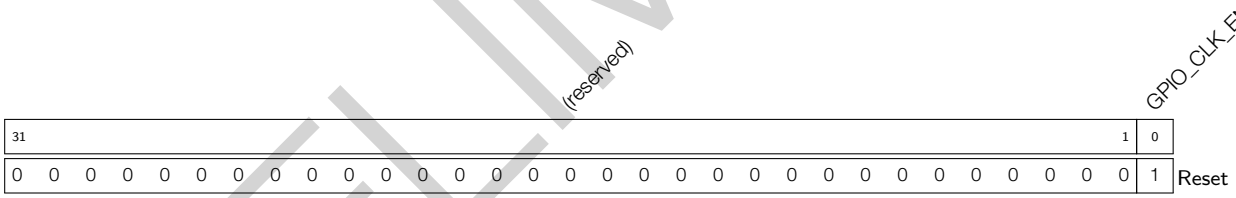
GPIO_FUNC*x*_OUT_SEL Selection control for GPIO output *X*. If a value *Y* (0<=Y<256) is written to this field, the peripheral output signal *Y* will be connected to GPIO output *X*. If a value 256 is written to this field, bit *X* of GPIO_OUT_REG/GPIO_OUT1_REG and GPIO_ENABLE_REG/GPIO_ENABLE1_REG will be selected as the output value and output enable. (R/W)

GPIO_FUNC*x*_OUT_INV_SEL 0: Do not invert the output value; 1: Invert the output value. (R/W)

GPIO_FUNC*x*_OEN_SEL 0: Use output enable signal from peripheral; 1: Force the output enable signal to be sourced from GPIO_ENABLE_REG[*x*]. (R/W)

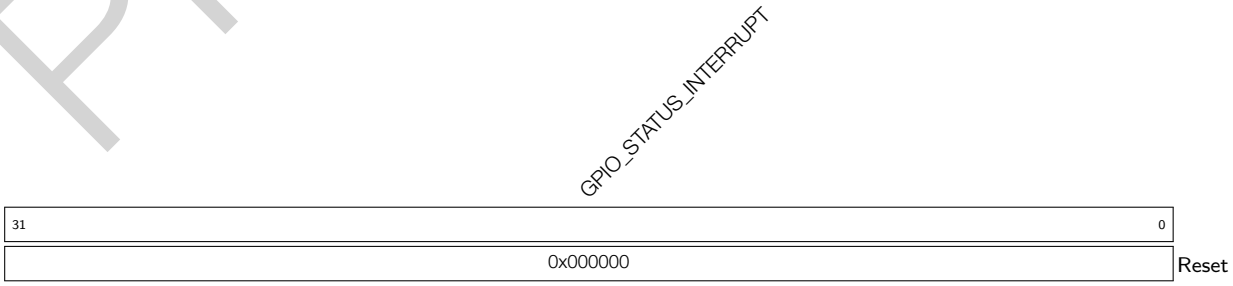
GPIO_FUNC*n*_OEN_INV_SEL 0: Do not invert the output enable signal; 1: Invert the output enable signal. (R/W)

Register 5.21. GPIO_CLOCK_GATE_REG (0x062C)



GPIO_CLK_EN Clock gating enable bit. If set to 1, the clock is free running. (R/W)

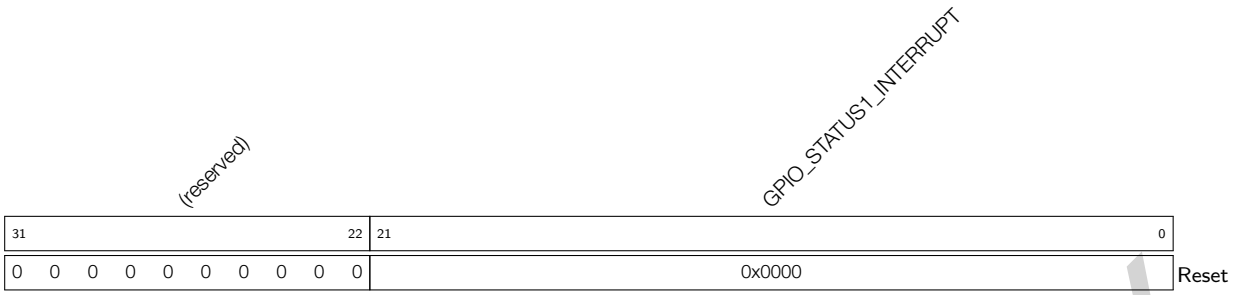
Register 5.22. GPIO_STATUS_REG (0x0044)



GPIO_STATUS_INTERRUPT GPIO0 ~ 31 interrupt status register. (R/W)

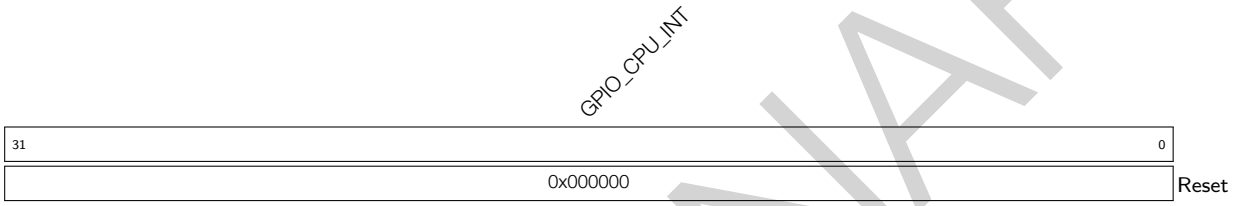
PRELIMINARY

Register 5.23. GPIO_STATUS1_REG (0x0050)



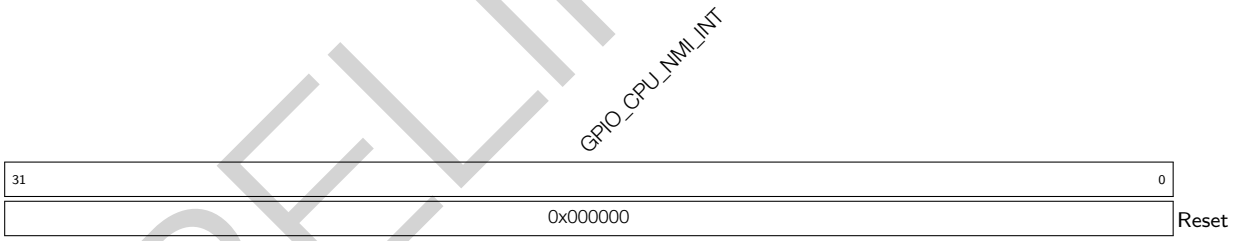
GPIO_STATUS1_INTERRUPT GPIO32 ~ 48 interrupt status register. (R/W)

Register 5.24. GPIO_CPU_INT_REG (0x005C)



GPIO_CPU_INT GPIO0 ~ 31 CPU interrupt status. This interrupt status is corresponding to the bit in GPIO_STATUS_REG when assert (high) enable signal (bit13 of GPIO_PIN*n*_REG). (RO)

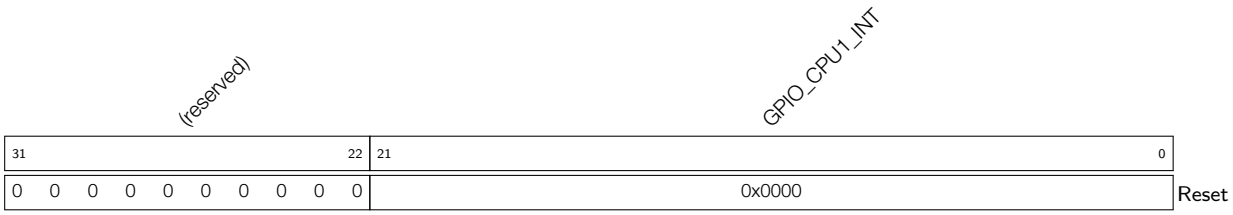
Register 5.25. GPIO_CPU_NMI_INT_REG (0x0060)



GPIO_CPU_NMI_INT GPIO0 ~ 31 CPU non-maskable interrupt status. This interrupt status is corresponding to the bit in GPIO_STATUS_REG when assert (high) enable signal (bit 14 of GPIO_PIN*n*_REG). (RO)

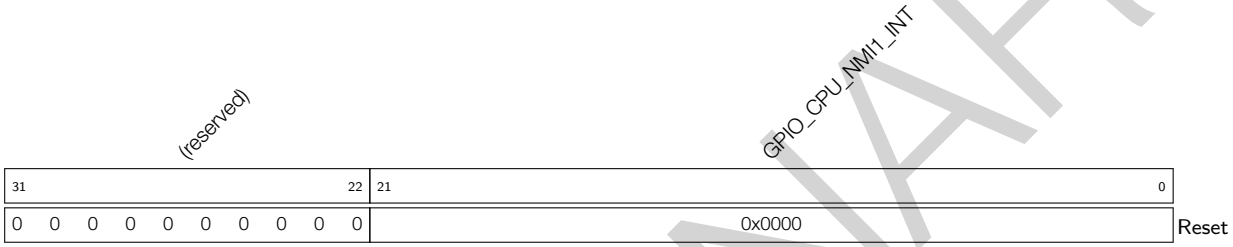
PRELIMINARY

Register 5.26. GPIO_CPU_INT1_REG (0x0068)



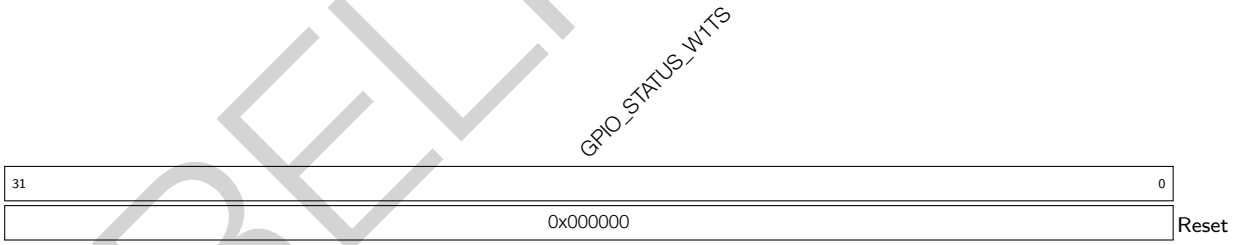
GPIO_CPU1_INT GPIO32 ~ 48 CPU interrupt status. This interrupt status is corresponding to the bit in GPIO_STATUS1_REG when assert (high) enable signal (bit 13 of GPIO_PIN*n*_REG). (RO)

Register 5.27. GPIO_CPU_NMI_INT1_REG (0x006C)



GPIO_CPU_NMI1_INT GPIO32 ~ 48 CPU non-maskable interrupt status. This interrupt status is corresponding to bit in GPIO_STATUS1_REG when assert (high) enable signal (bit 14 of GPIO_PIN*n*_REG). (RO)

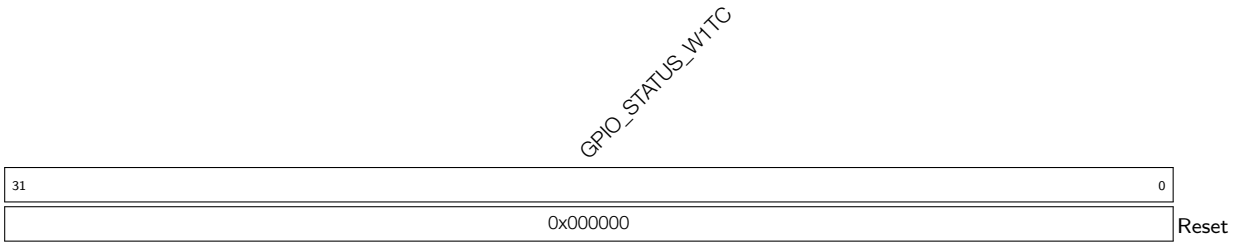
Register 5.28. GPIO_STATUS_W1TS_REG (0x0048)



GPIO_STATUS_W1TS GPIO0 ~ 31 interrupt status set register. If the value 1 is written to a bit here, the corresponding bit in GPIO_STATUS_INTERRUPT will be set to 1. Recommended operation: use this register to set GPIO_STATUS_INTERRUPT. (WO)

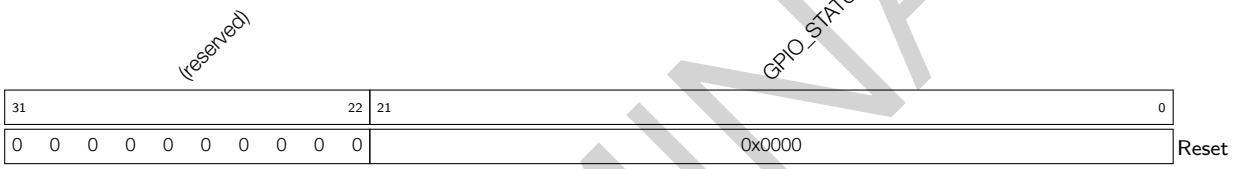
PRELIMINARY

Register 5.29. GPIO_STATUS_W1TC_REG (0x004C)



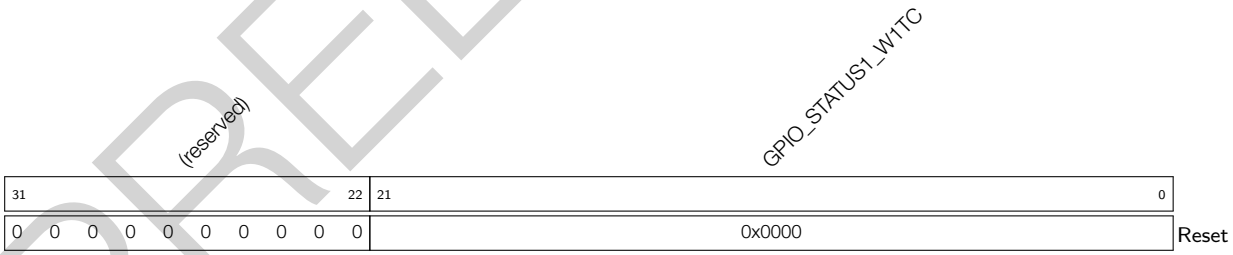
GPIO_STATUS_W1TC GPIO0 ~ 31 interrupt status clear register. If the value 1 is written to a bit here, the corresponding bit in GPIO_STATUS_INTERRUPT will be cleared. Recommended operation: use this register to clear GPIO_STATUS_INTERRUPT. (WO)

Register 5.30. GPIO_STATUS1_W1TS_REG (0x0054)



GPIO_STATUS1_W1TS GPIO32 ~ 48 interrupt status set register. If the value 1 is written to a bit here, the corresponding bit in GPIO_STATUS1_REG will be set to 1. Recommended operation: use this register to set GPIO_STATUS1_REG. (WO)

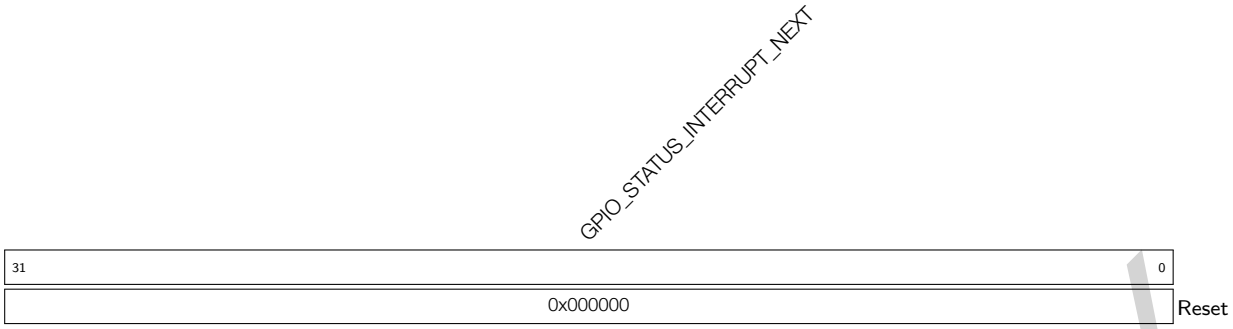
Register 5.31. GPIO_STATUS1_W1TC_REG (0x0058)



GPIO_STATUS1_W1TC GPIO32 ~ 48 interrupt status clear register. If the value 1 is written to a bit here, the corresponding bit in GPIO_STATUS1_REG will be cleared. Recommended operation: use this register to clear GPIO_STATUS1_REG. (WO)

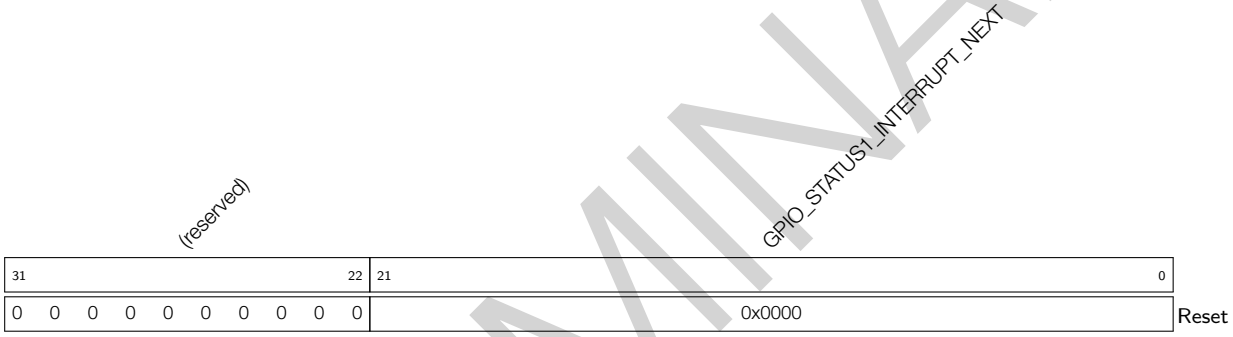
PRELIMINARY

Register 5.32. GPIO_STATUS_NEXT_REG (0x014C)



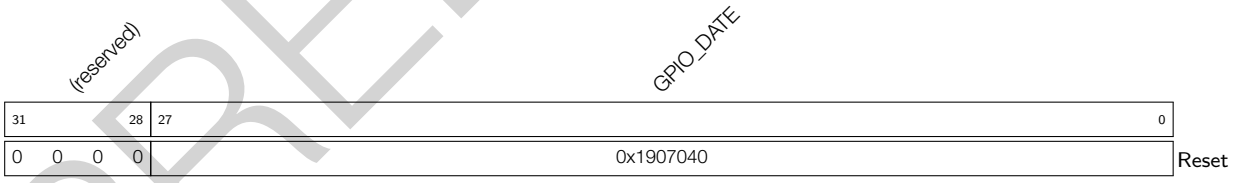
GPIO_STATUS_INTERRUPT_NEXT Interrupt source signal of GPIO0 ~ 31, could be rising edge interrupt, falling edge interrupt, level sensitive interrupt and any edge interrupt. (RO)

Register 5.33. GPIO_STATUS_NEXT1_REG (0x0150)



GPIO_STATUS1_INTERRUPT_NEXT Interrupt source signal of GPIO32 ~ 48. (RO)

Register 5.34. GPIO_DATE_REG (0x06FC)



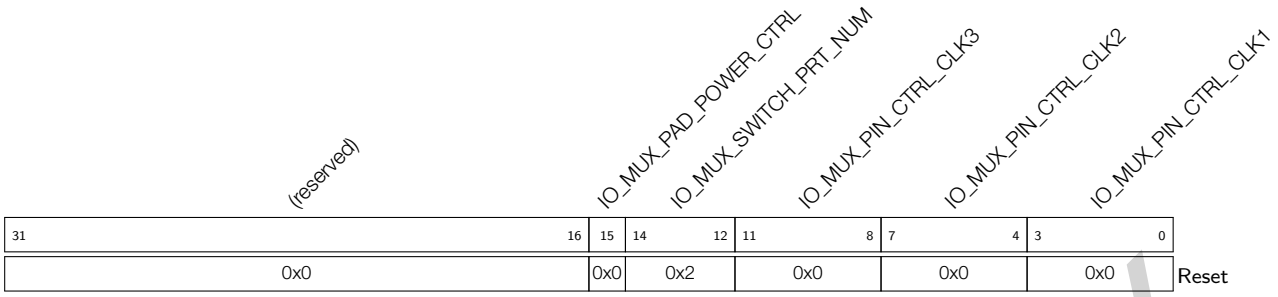
GPIO_DATE Version control register (R/W)

5.15.2 IO MUX Registers

The addresses in this section are relative to the IO MUX base address provided in Table 3-3 in Chapter 3 *System and Memory*.

PRELIMINARY

Register 5.35. IO_MUX_PIN_CTRL_REG (0x0000)



IO_MUX_PIN_CTRL_CLK*x* If you want to output clock for I2S0 to: (R/W)

CLK_OUT1 then set IO_MUX_PIN_CTRL_CLK1 = 0x0

CLK_OUT2 then set IO_MUX_PIN_CTRL_CLK2 = 0x0;

CLK_OUT3 then set IO_MUX_PIN_CTRL_CLK3 = 0x0.

If you want to output clock for I2S1 to: (R/W)

CLK_OUT1 then set IO_MUX_PIN_CTRL_CLK1 = 0xF

CLK_OUT2 then set IO_MUX_PIN_CTRL_CLK2 = 0xF;

CLK_OUT3 then set IO_MUX_PIN_CTRL_CLK3 = 0xF.

Note:

Only the above mentioned combinations of clock source and clock output pins are possible.

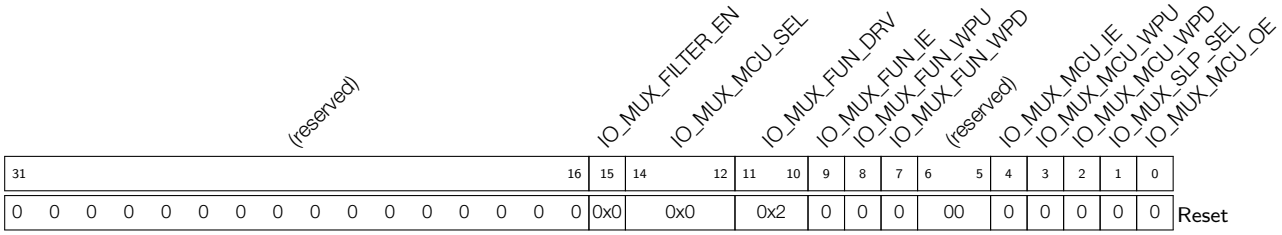
The CLK_OUT1 ~ 3 can be found in IO_MUX Pin Function List.

IO_MUX_SWITCH_PRT_NUM GPIO pin power switch delay, delay unit is one APB clock. (R/W)

IO_MUX_PAD_POWER_CTRL Select power voltage for GPIO33 ~ 37. 1: select VDD_SPI 1.8 V; 0: select VDD3P3_CPU 3.3 V. (R/W)

PRELIMINARY

Register 5.36. IO_MUX_*n*_REG (*n*: GPIO0-GPIO21, GPIO26-GPIO48) (0x0010+4n*)**



IO_MUX_MCU_OE Output enable of the pin in sleep mode. 1: Output enabled; 0: Output disabled. (R/W)

IO_MUX_SLP_SEL Sleep mode selection of this pin. Set to 1 to put the pin in sleep mode. (R/W)

IO_MUX_MCU_WPD Pull-down enable of the pin during sleep mode. 1: Internal pull-down enabled; 0: Internal pull-down disabled. (R/W)

IO_MUX_MCU_WPU Pull-up enable of the pin during sleep mode. 1: Internal pull-up enabled; 0: Internal pull-up disabled.

IO_MUX_MCU_IE Input enable of the pin during sleep mode. 1: Input enabled; 0: Input disabled. (R/W)

IO_MUX_FUN_WPD Pull-down enable of the pin. 1: Pull-down enabled; 0: Pull-down disabled. (R/W)

IO_MUX_FUN_WPU Pull-up enable of the pin. 1: Internal pull-up enabled; 0: Internal pull-up disabled. (R/W)

IO_MUX_FUN_IE Input enable of the pin. 1: Input enabled; 0: Input disabled. (R/W)

IO_MUX_FUN_DRV Select the drive strength of the pin. 0: ~5 mA: 1: ~10 mA: 2: ~20 mA; 3: ~40 mA. (R/W)

IO_MUX_MCU_SEL Select IO MUX function for this signal. 0: Select Function 0; 1: Select Function 1, etc. (R/W)

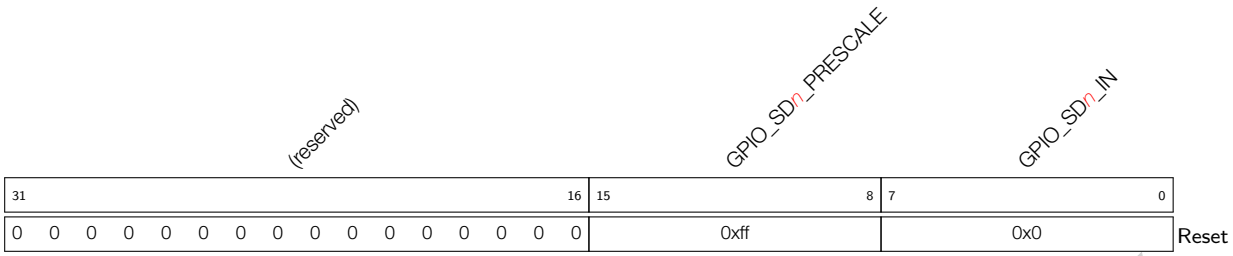
IO_MUX_FILTER_EN Enable filter for pin input signals. 1: Filter enabled; 2: Filter disabled. (R/W)

5.15.3 SDM Output Registers

The addresses in this section are relative to (GPIO base address provided in Table 3-3 in Chapter 3 *System and Memory* + 0x0F00).

PRELIMINARY

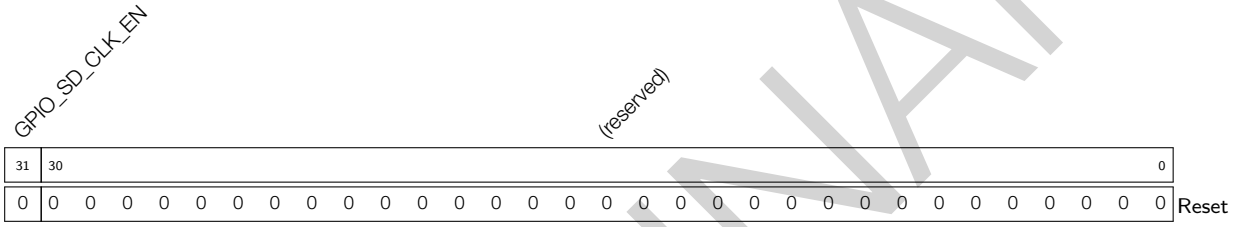
Register 5.37. GPIO_SIGMADELTA*n*_REG (*n*: 0-7) (0x0000+4n*)**



GPIO_SD*n*_IN This field is used to configure the duty cycle of sigma delta modulation output. (R/W)

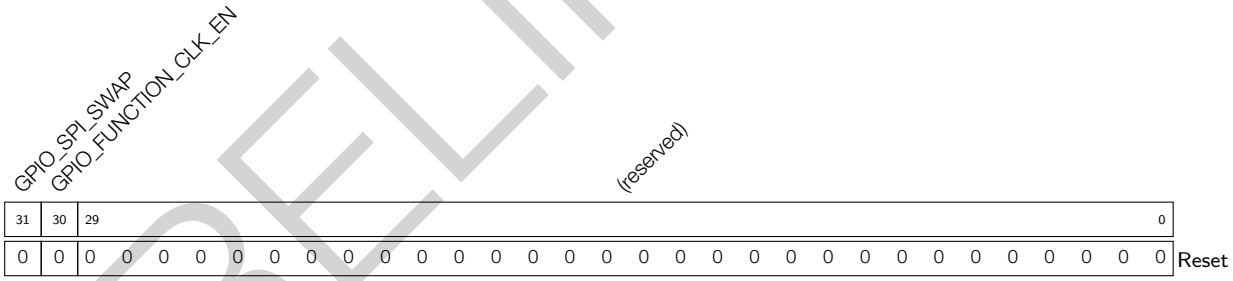
GPIO_SD*n*_PRESCALE This field is used to set a divider value to divide APB clock. (R/W)

Register 5.38. GPIO_SIGMADELTA_CG_REG (0x0020)



GPIO_SD_CLK_EN Clock enable bit of configuration registers for sigma delta modulation. (R/W)

Register 5.39. GPIO_SIGMADELTA_MISC_REG (0x0024)

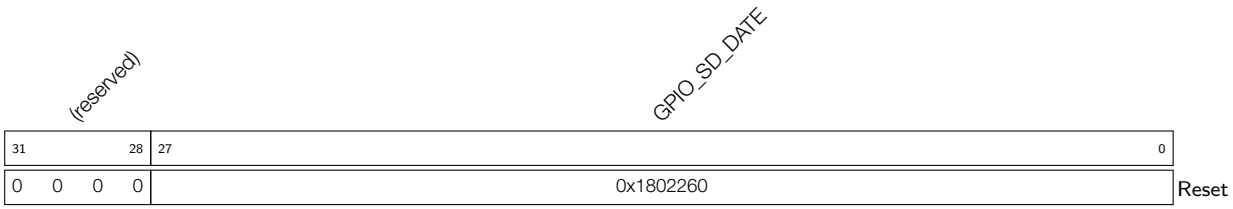


GPIO_FUNCTION_CLK_EN Clock enable bit of sigma delta modulation. (R/W)

GPIO_SPI_SWAP Reserved. (R/W)

PRELIMINARY

Register 5.40. GPIOSD_SIGMADELTA_VERSION_REG (0x0028)

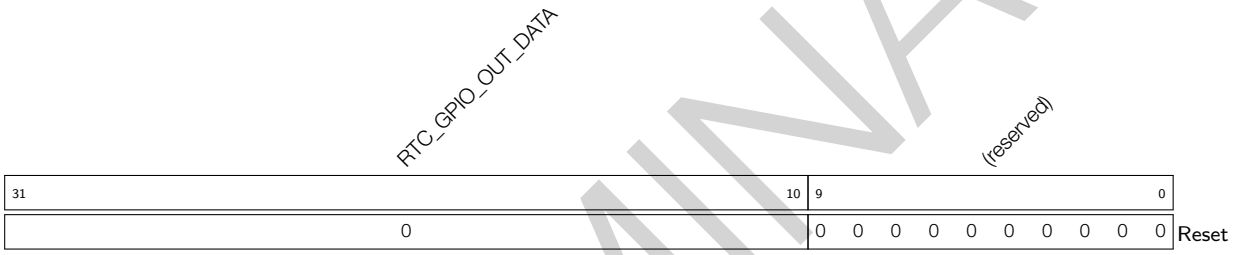


GPIO_SD_DATE Version control register. (R/W)

5.15.4 RTC IO MUX Registers

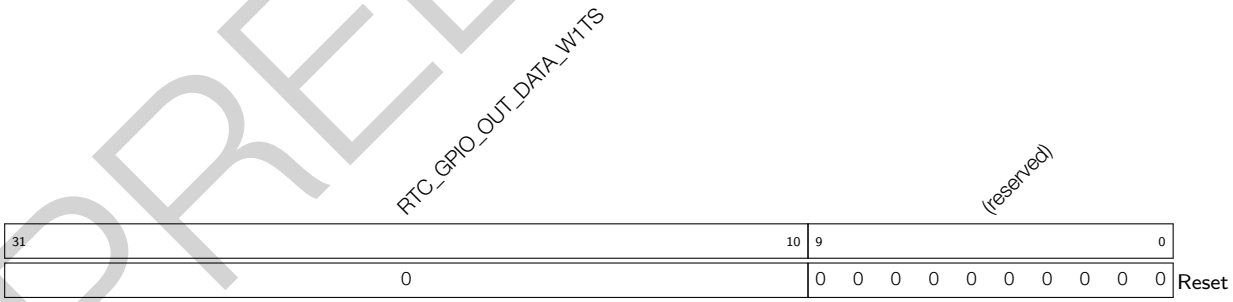
The addresses in this section are relative to (Low-Power Management base address provided in Table 3-3 in Chapter 3 *System and Memory* + 0x0400).

Register 5.41. RTC_GPIO_OUT_REG (0x0000)



RTC_GPIO_OUT_DATA GPIO0 ~ 21 output register. Bit10 corresponds to GPIO0, bit11 corresponds to GPIO1, etc. (R/W)

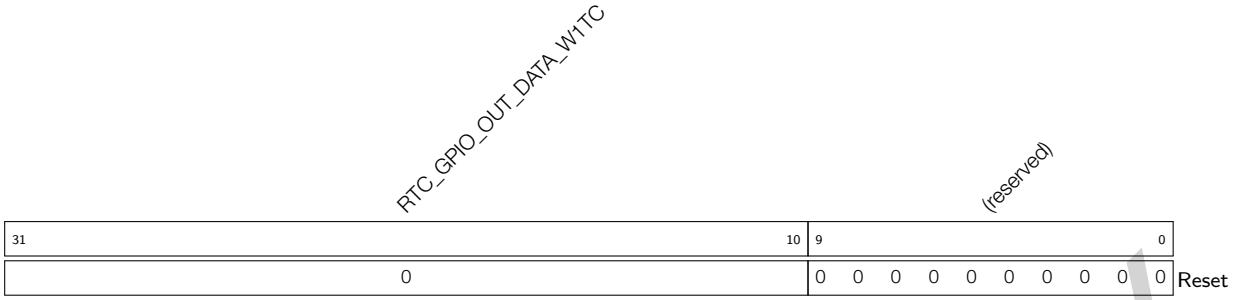
Register 5.42. RTC_GPIO_OUT_W1TS_REG (0x0004)



RTC_GPIO_OUT_DATA_W1TS GPIO0 ~ 21 output set register. If the value 1 is written to a bit here, the corresponding bit in RTC_GPIO_OUT_REG will be set to 1. Recommended operation: use this register to set RTC_GPIO_OUT_REG. (WO)

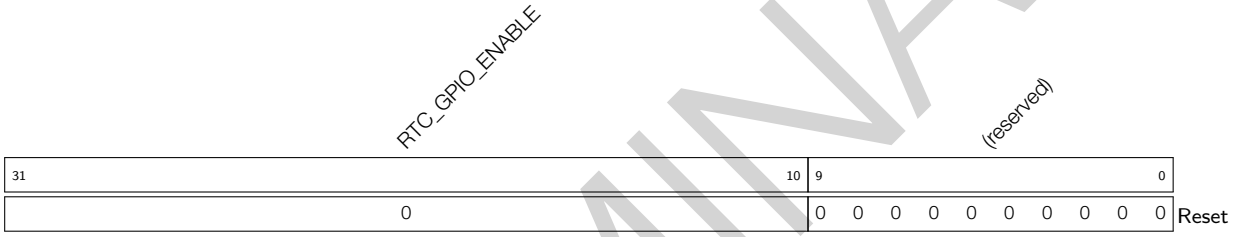
PRELIMINARY

Register 5.43. RTC_GPIO_OUT_W1TC_REG (0x0008)



RTC_GPIO_OUT_DATA_W1TC GPIO0 ~ 21 output clear register. If the value 1 is written to a bit here, the corresponding bit in RTC_GPIO_OUT_REG will be cleared. Recommended operation: use this register to clear RTC_GPIO_OUT_REG. (WO)

Register 5.44. RTC_GPIO_ENABLE_REG (0x000C)



RTC_GPIO_ENABLE GPIO0 ~ 21 output enable. Bit10 corresponds to GPIO0, bit11 corresponds to GPIO1, etc. If the bit is set to 1, it means this GPIO pin is output. (R/W)

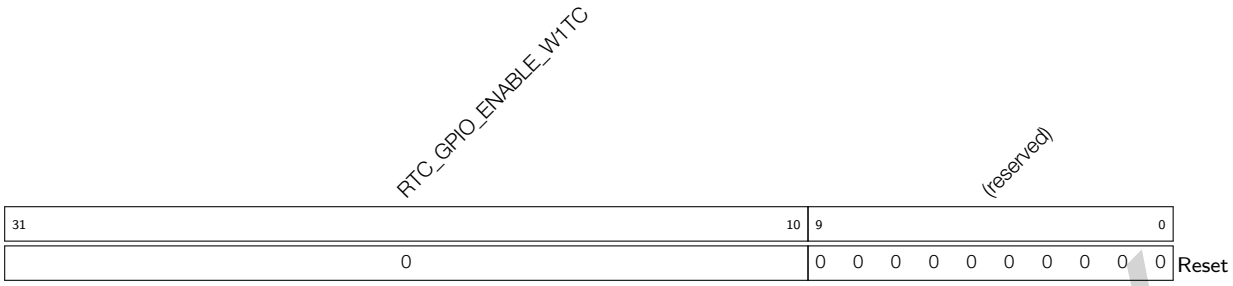
Register 5.45. RTC_GPIO_ENABLE_W1TS_REG (0x0010)



RTC_GPIO_ENABLE_W1TS GPIO0 ~ 21 output enable set register. If the value 1 is written to a bit here, the corresponding bit in RTC_GPIO_ENABLE_REG will be set to 1. Recommended operation: use this register to set RTC_GPIO_ENABLE_REG. (WO)

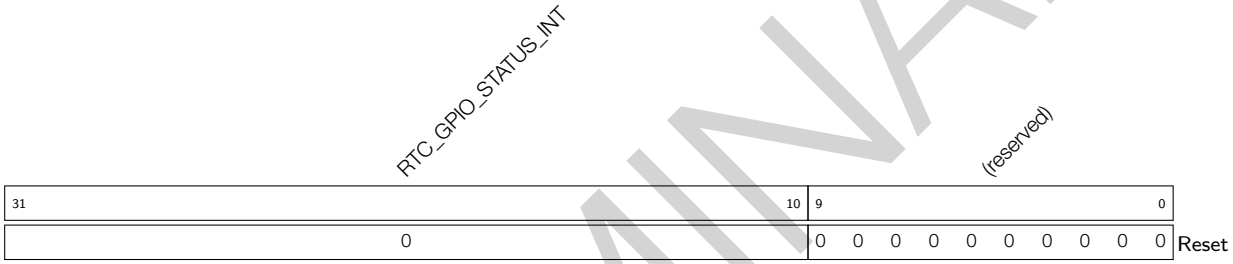
PRELIMINARY

Register 5.46. RTC_GPIO_ENABLE_W1TC_REG (0x0014)



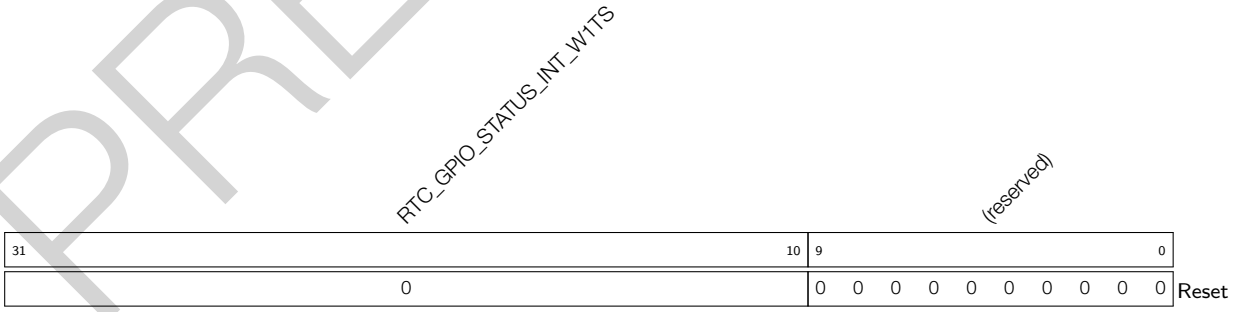
RTC_GPIO_ENABLE_W1TC GPIO0 ~ 21 output enable clear register. If the value 1 is written to a bit here, the corresponding bit in RTC_GPIO_ENABLE_REG will be cleared. Recommended operation: use this register to clear RTC_GPIO_ENABLE_REG. (WO)

Register 5.47. RTC_GPIO_STATUS_REG (0x0018)



RTC_GPIO_STATUS_INT GPIO0 ~ 21 interrupt status register. Bit10 corresponds to GPIO0, bit11 corresponds to GPIO1, etc. This register should be used together with RTC_GPIO_PIN*n*_INT_TYPE in RTC_GPIO_PIN*n*_REG. 0: no interrupt; 1: corresponding interrupt. (R/W)

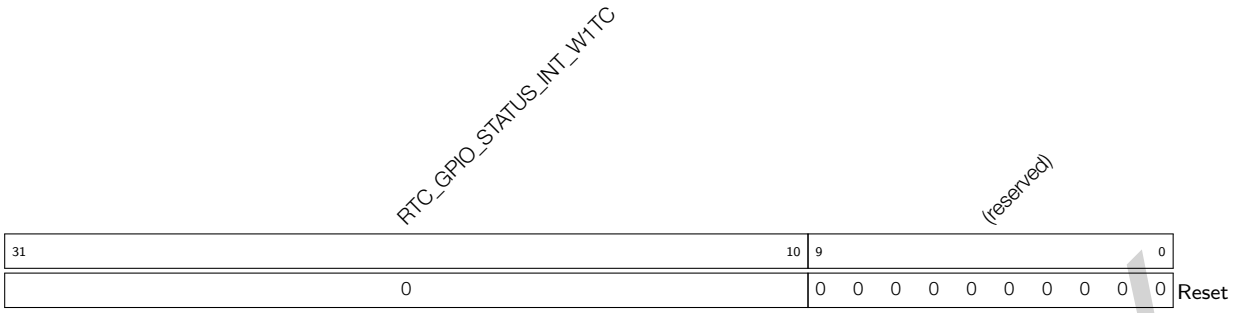
Register 5.48. RTC_GPIO_STATUS_W1TS_REG (0x001C)



RTC_GPIO_STATUS_INT_W1TS GPIO0 ~ 21 interrupt set register. If the value 1 is written to a bit here, the corresponding bit in RTC_GPIO_STATUS_INT will be set to 1. Recommended operation: use this register to set RTC_GPIO_STATUS_INT. (WO)

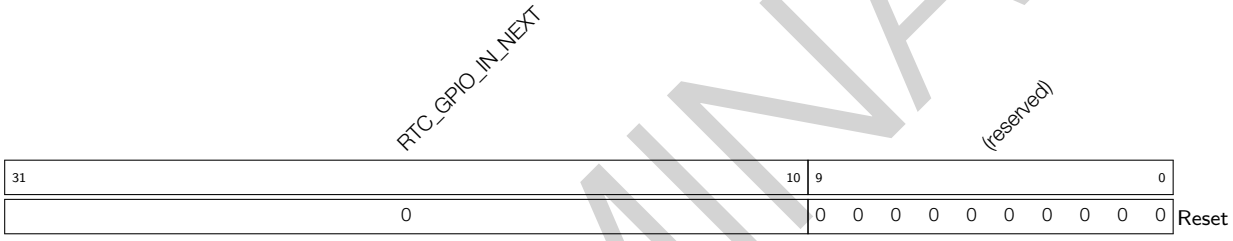
PRELIMINARY

Register 5.49. RTC_GPIO_STATUS_W1TC_REG (0x0020)



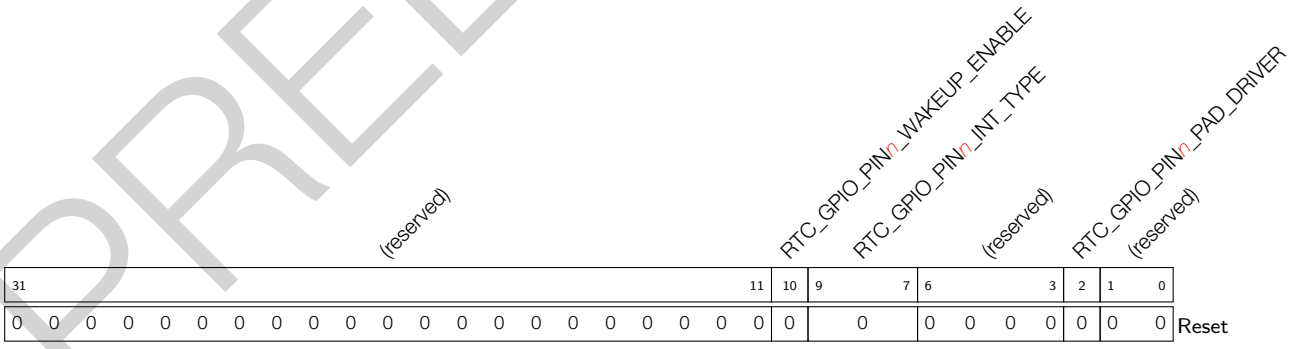
RTC_GPIO_STATUS_INT_W1TC GPIO0 ~ 21 interrupt clear register. If the value 1 is written to a bit here, the corresponding bit in RTC_GPIO_STATUS_INT will be cleared. Recommended operation: use this register to clear RTC_GPIO_STATUS_INT. (WO)

Register 5.50. RTC_GPIO_IN_REG (0x0024)



RTC_GPIO_IN_NEXT GPIO0 ~ 21 input value. Bit10 corresponds to GPIO0, bit11 corresponds to GPIO1, etc. Each bit represents a pin input value, 1 for high level, and 0 for low level. (RO)

Register 5.51. RTC_GPIO_PIN*n*_REG (*n*: 0-21) (0x0028+0x4n*)**



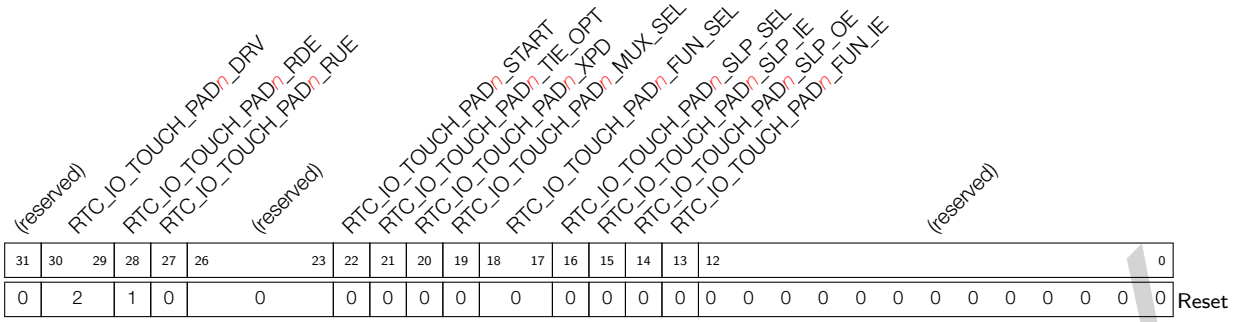
RTC_GPIO_PIN*n*_PAD_DRIVER Pin driver selection. 0: normal output; 1: open drain. (R/W)

RTC_GPIO_PIN*n*_INT_TYPE GPIO interrupt type selection. 0: GPIO interrupt disabled; 1: rising edge trigger; 2: falling edge trigger; 3: any edge trigger; 4: low level trigger; 5: high level trigger. (R/W)

RTC_GPIO_PIN*n*_WAKEUP_ENABLE GPIO wake-up enable. This will only wake up the chip from Light-sleep. (R/W)

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Register 5.52. RTC_IO_TOUCH_PADn_REG (n: 0-14) (0x0084+0x4*n)



RTC_IO_TOUCH_PADn_FUN_IE Input enable in normal execution. (R/W)

RTC_IO_TOUCH_PADn_SLP_OE Output enable in sleep mode. (R/W)

RTC_IO_TOUCH_PADn_SLP_IE Input enable in sleep mode. (R/W)

RTC_IO_TOUCH_PADn_SLP_SEL 0: no sleep mode; 1: enable sleep mode. (R/W)

RTC_IO_TOUCH_PADn_FUN_SEL Function selection. (R/W)

RTC_IO_TOUCH_PADn_MUX_SEL Connect the RTC pin input or digital pin input. 0 is available, i.e. select digital pin input. (R/W)

RTC_IO_TOUCH_PADn_XPD Touch sensor power on. (R/W)

RTC_IO_TOUCH_PADn_TIE_OPT The tie option of touch sensor. 0: tie low; 1: tie high. (R/W)

RTC_IO_TOUCH_PADn_START Start touch sensor. (R/W)

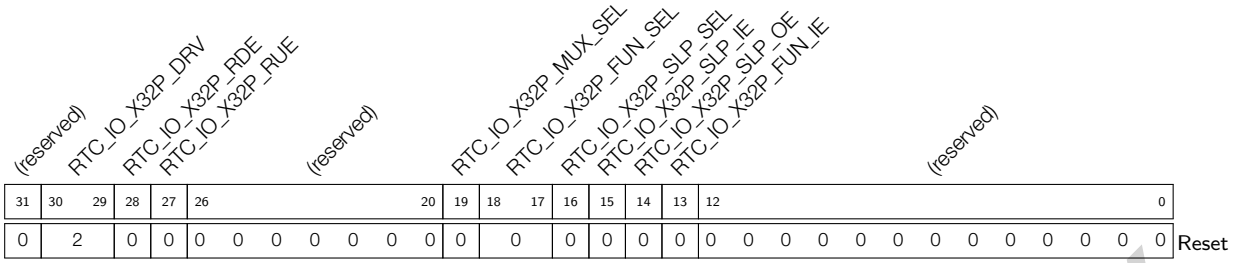
RTC_IO_TOUCH_PADn_RUE Pull-up enable of the pin. 1: internal pull-up enabled; 0: internal pull-up disabled. (R/W)

RTC_IO_TOUCH_PADn_RDE Pull-down enable of the pin. 1: internal pull-down enabled, 0: internal pull-down disabled. (R/W)

RTC_IO_TOUCH_PADn_DRV Select the drive strength of the pin. 0: ~5 mA: 1: ~10 mA: 2: ~20 mA; 3: ~40 mA. (R/W)

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Register 5.53. RTC_IO_XTAL_32P_PAD_REG (0x00C0)



RTC_IO_X32P_FUN_IE Input enable in normal execution. (R/W)

RTC_IO_X32P_SLP_OE Output enable in sleep mode. (R/W)

RTC_IO_X32P_SLP_IE Input enable in sleep mode. (R/W)

RTC_IO_X32P_SLP_SEL 1: enable sleep mode; 0: no sleep mode. (R/W)

RTC_IO_X32P_FUN_SEL Function selection. (R/W)

RTC_IO_X32P_MUX_SEL 1: use RTC GPIO; 0: use digital GPIO. (R/W)

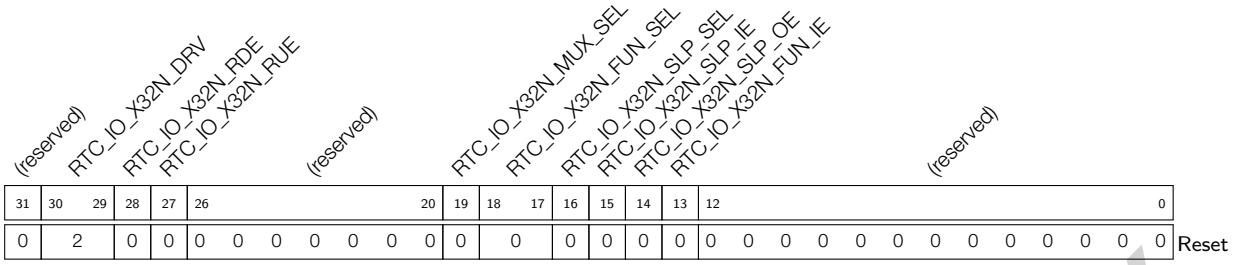
RTC_IO_X32P_RUE Pull-up enable of the pin. 1: internal pull-up enabled; 0: internal pull-up disabled. (R/W)

RTC_IO_X32P_RDE Pull-down enable of the pin. 1: internal pull-down enabled, 0: internal pull-down disabled. (R/W)

RTC_IO_X32P_DRV Select the drive strength of the pin. 0: ~5 mA: 1: ~10 mA: 2: ~20 mA; 3: ~40 mA. (R/W)

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Register 5.54. RTC_IO_XTAL_32N_PAD_REG (0x00C4)



RTC_IO_X32N_FUN_IE Input enable in normal execution. (R/W)

RTC_IO_X32N_SLP_OE Output enable in sleep mode. (R/W)

RTC_IO_X32N_SLP_IE Input enable in sleep mode. (R/W)

RTC_IO_X32N_SLP_SEL 1: enable sleep mode; 0: no sleep mode. (R/W)

RTC_IO_X32N_FUN_SEL Function selection. (R/W)

RTC_IO_X32N_MUX_SEL 1: use RTC GPIO; 0: use digital GPIO. (R/W)

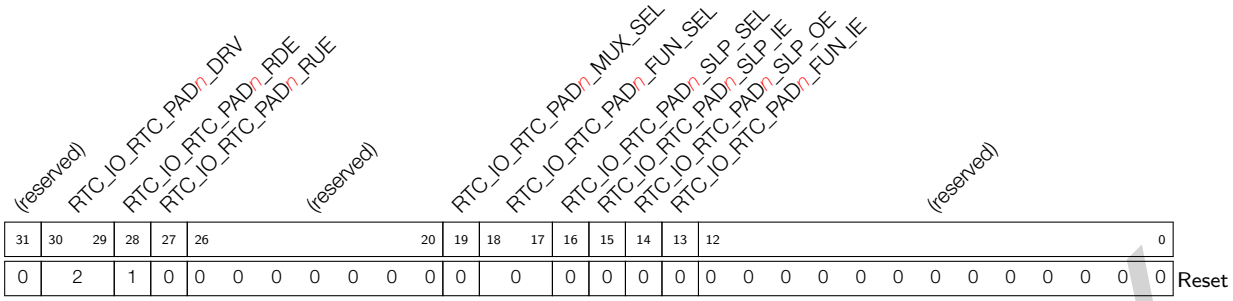
RTC_IO_X32N_RUE Pull-up enable of the pin. 1: internal pull-up enabled; 0: internal pull-up disabled. (R/W)

RTC_IO_X32N_RDE Pull-down enable of the pin. 1: internal pull-down enabled, 0: internal pull-down disabled. (R/W)

RTC_IO_X32N_DRV Select the drive strength of the pin. 0: ~5 mA: 1: ~10 mA: 2: ~20 mA; 3: ~40 mA. (R/W)

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Register 5.55. RTC_IO_RTC_PADn_REG (n: 17-21) (0x00C8, 0x00CC, 0x00D0, 0x00D4, 0x00D8)



RTC_IO_RTC_PADn_FUN_IE Input enable in normal execution. (R/W)

RTC_IO_RTC_PADn_SLP_OE Output enable in sleep mode. (R/W)

RTC_IO_RTC_PADn_SLP_IE Input enable in sleep mode. (R/W)

RTC_IO_RTC_PADn_SLP_SEL 1: enable sleep mode; 0: no sleep mode. (R/W)

RTC_IO_RTC_PADn_FUN_SEL Function selection. (R/W)

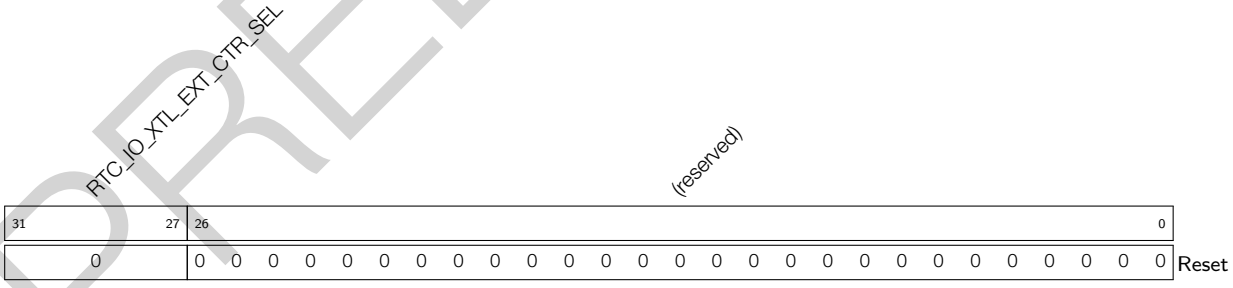
RTC_IO_RTC_PADn_MUX_SEL 1: use RTC GPIO; 0: use digital GPIO. (R/W)

RTC_IO_RTC_PADn_RUE Pull-up enable of the pin. 1: internal pull-up enabled; 0: internal pull-up disabled. (R/W)

RTC_IO_RTC_PADn_RDE Pull-down enable of the pin. 1: internal pull-down enabled, 0: internal pull-down disabled. (R/W)

RTC_IO_RTC_PADn_DRV Select the drive strength of the pin. 0: ~5 mA: 1: ~10 mA: 2: ~20 mA; 3: ~40 mA. (R/W)

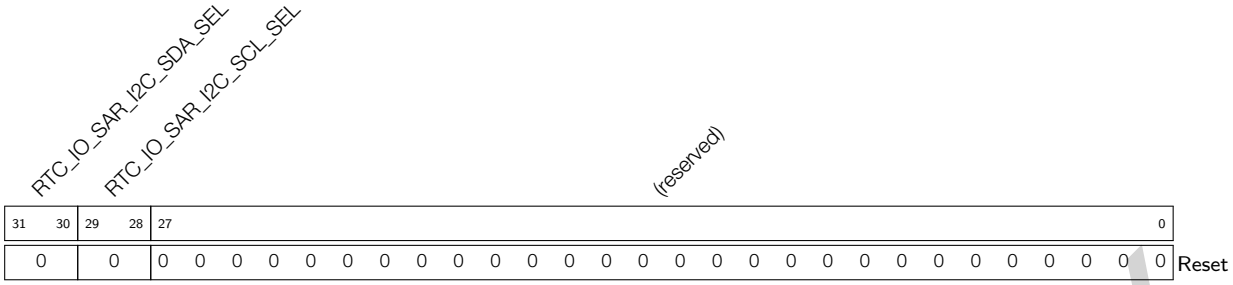
Register 5.56. RTC_IO_XTL_EXT_CTR_REG (0x00E0)



RTC_IO_XTL_EXT_CTR_SEL Select the external crystal power down enable source to get into sleep mode. 0: select GPIO0; 1: select GPIO1, etc. The input value on this pin XOR RTC_CNTL_EXT_XTL_CONF_REG[30] is the crystal power down enable signal. (R/W)

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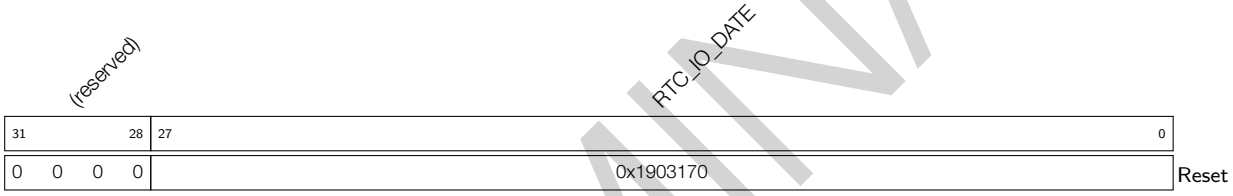
Register 5.57. RTC_IO_SAR_I2C_IO_REG (0x00E4)



RTC_IO_SAR_I2C_SCL_SEL Selects a pin the RTC I2C SCL signal connects to. 0: use RTC GPIO0; 1: use RTC GPIO2. (R/W)

RTC_IO_SAR_I2C_SDA_SEL Selects a pin the RTC I2C SDA signal connects to. 0: use RTC GPIO1; 1: use RTC GPIO3. (R/W)

Register 5.58. RTC_IO_DATE_REG (0x01FC)



RTC_IO_DATE Version control register (R/W)

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6 Reset and Clock

6.1 Reset

6.1.1 Overview

ESP32-S3 provides four reset levels, namely CPU Reset, Core Reset, System Reset, and Chip Reset.

All reset levels mentioned above (except Chip Reset) maintain the data stored in internal memory. Figure 6-1 shows the affected subsystems of the four reset levels.

6.1.2 Architectural Overview

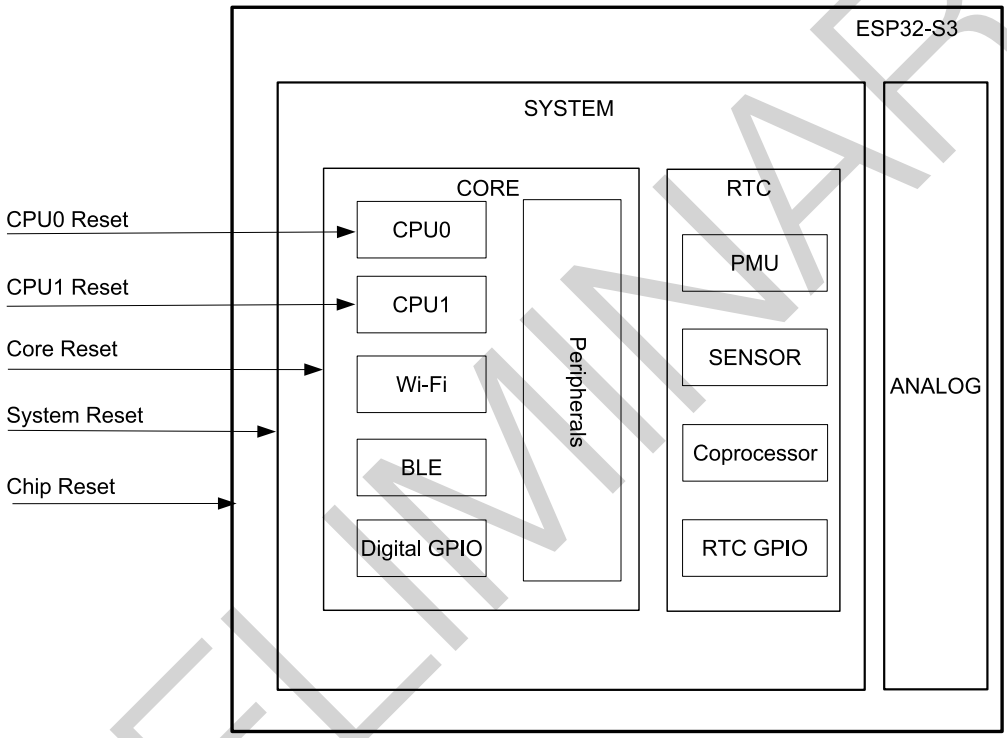


Figure 6-1. Reset Levels

6.1.3 Features

- Support four reset levels:
  - CPU Reset: only resets CPU*x* core. CPU*x* can be CPU0 or CPU1 here. Once such reset is released, programs will be executed from CPU*x* reset vector. Each CPU core has its own reset logic.
  - Core Reset: resets the whole digital system except RTC, including CPU0, CPU1, peripherals, Wi-Fi, Bluetooth® LE (BLE), and digital GPIOs.
  - System Reset: resets the whole digital system, including RTC.
  - Chip Reset: resets the whole chip.
- Support software reset and hardware reset:
  - Software reset is triggered by CPU*x* configuring its corresponding registers.

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– Hardware reset is directly triggered by the circuit.

Note:
If CPU Reset is from CPU0, the sensitive registers will be reset, too.

6.1.4 Functional Description

CPU0 and CPU1 will be reset immediately when any of the reset above occurs. After the reset is released, CPU0 and CPU1 can read from the registers RTC_CNTL_RESET_CAUSE_PROCPU and RTC_CNTL_RESET_CAUSE_APPCPU to get the reset source, respectively. The reset sources recorded in the two registers are shared by the two CPUs, except the CPU reset sources, i.e. each CPU has its own CPU reset sources.

Table 6-1 lists the reset sources and the types of reset they trigger.

Table 6-1. Reset Sources

Code	Source	Reset Type	Comments
0x01	Chip reset[1]	Chip Reset	-
0x0F	Brown-out system reset	Chip Reset or System Reset	Triggered by brown-out detector[2]
0x10	RWDT system reset	System Reset	See Chapter 11 *Watchdog Timers (WDT)*
0x12	Super Watchdog reset	System Reset	See Chapter 11 *Watchdog Timers (WDT)*
0x13	GLITCH reset	System Reset	See Chapter 22 *Clock Glitch Detection*
0x03	Software system reset	Core Reset	Triggered by configuring RTC_CNTL_SW_SYS_RST
0x05	Deep-sleep reset	Core Reset	See Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*
0x07	MWDT0 core reset	Core Reset	See Chapter 11 *Watchdog Timers (WDT)*
0x08	MWDT1 core reset	Core Reset	See Chapter 11 *Watchdog Timers (WDT)*
0x09	RWDT core reset	Core Reset	See Chapter 11 *Watchdog Timers (WDT)*
0x14	eFuse reset	Core Reset	Triggered by eFuse CRC error
0x15	USB (UART) reset	Core Reset	Triggered when external USB host sends a specific command to the Serial interface of USB-Serial-JTAG. See 29 *USB Serial/JTAG Controller (USB_SERIAL_JTAG)*
0x16	USB (JTAG) reset	Core Reset	Triggered when external USB host sends a specific command to the JTAG interface of USB-Serial-JTAG. See 29 *USB Serial/JTAG Controller (USB_SERIAL_JTAG)*
0x0B	MWDT0 CPU*x* reset	CPU Reset	See Chapter 11 *Watchdog Timers (WDT)*
0x0C	Software CPU*x* reset	CPU Reset	Triggered by configuring RTC_CNTL_SW_PRO(APP)CPU_RST
0x0D	RWDT CPU*x* reset	CPU Reset	See Chapter 11 *Watchdog Timers (WDT)*
0x11	MWDT1 CPU*x* reset	CPU Reset	See Chapter 11 *Watchdog Timers (WDT)*

[1] Chip Reset can be triggered by the following three sources:
- Triggered by chip power-on;
- Triggered by brown-out detector;
- Triggered by Super Watchdog (SWD).

[2] Once brown-out status is detected, the detector will trigger System Reset or Chip Reset, depending on register configuration. For more information, please see Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*.

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6.2 Clock

6.2.1 Overview

ESP32-S3 clocks are mainly sourced from oscillator (OSC), RC, and PLL circuit, and then processed by the dividers/selectors, which allows most functional modules to select their working clock according to their power consumption and performance requirements. Figure 6-2 shows the system clock structure.

6.2.2 Architectural Overview

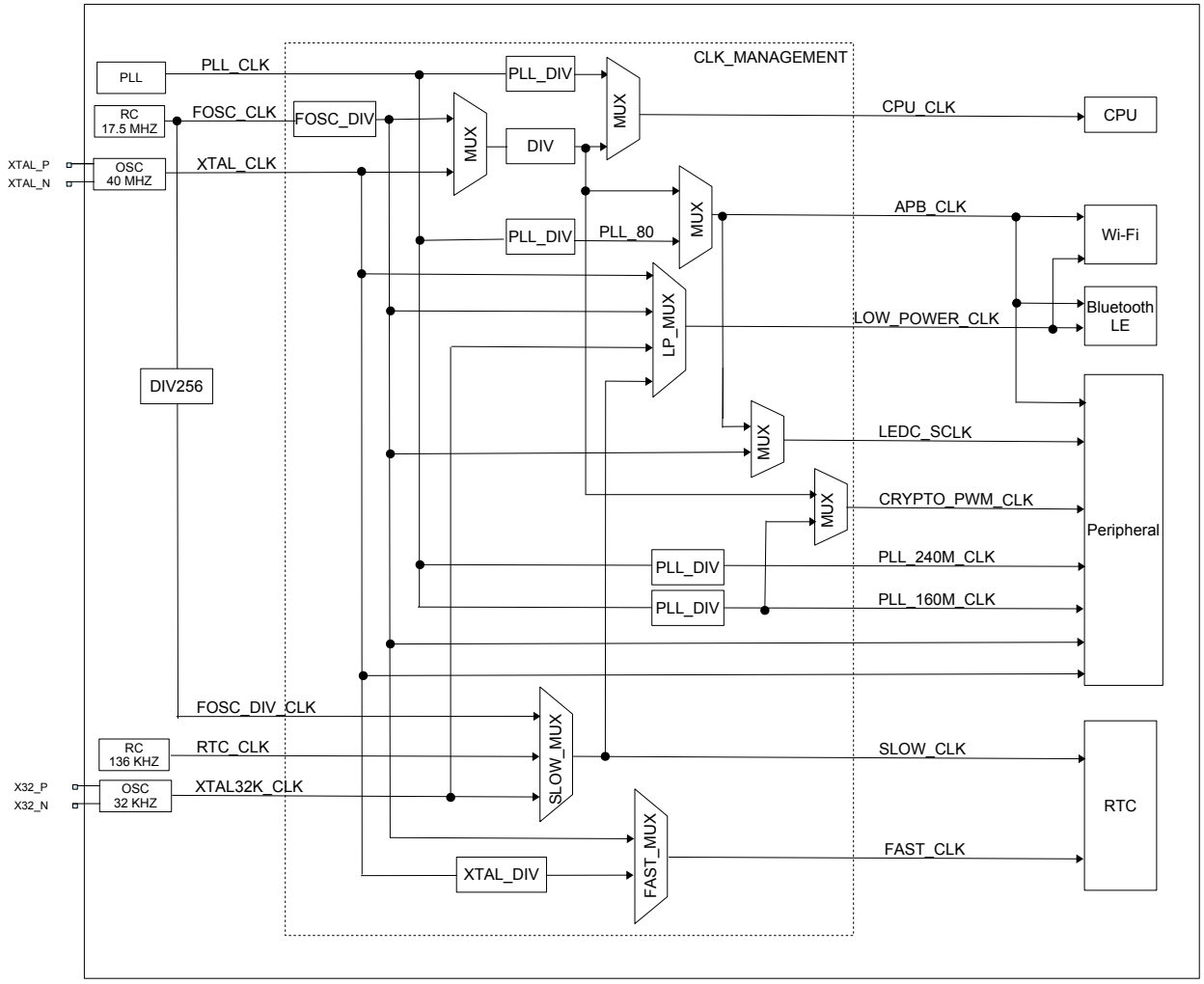


Figure 6-2. Clock Structure

6.2.3 Features

ESP32-S3 clocks can be classified in two types depending on their frequencies:

- High speed clocks for devices working at a higher frequency, such as CPU and digital peripherals
  - PLL_CLK (320 MHz or 480 MHz): internal PLL clock
  - XTAL_CLK (40 MHz): external crystal clock
- Slow speed clocks for low-power devices, such as RTC module and low-power peripherals

- XTAL32K_CLK (32 kHz): external crystal clock
- FOSC_CLK (17.5 MHz by default): internal fast RC oscillator clock with adjustable frequency
- FOSC_DIV_CLK: internal fast RC oscillator clock derived from FOSC_CLK divided by 256
- RTC_CLK (136 kHz by default): internal low RC oscillator clock with adjustable frequency

6.2.4 Functional Description

6.2.4.1 CPU Clock

As Figure 6-2 shows, CPU_CLK is the master clock for CPU*x* and it can be as high as 240 MHz when CPU*x* works in high performance mode. Alternatively, CPU*x* can run at lower frequencies, such as at 2 MHz, to lower power consumption.

Users can set PLL_CLK, FOSC_CLK or XTAL_CLK as CPU_CLK clock source by configuring register SYSTEM_SOC_CLK_SEL, see Table 6-2 and Table 6-3. By default, the CPU clock is sourced from XTAL_CLK with a divider of 2, i.e. the CPU clock is 20 MHz.

Table 6-2. CPU Clock Source

SYSTEM_SOC_CLK_SEL Value	CPU Clock Source
0	XTAL_CLK
1	PLL_CLK
2	FOSC_CLK

Table 6-3. CPU Clock Frequency

CPU Clock Source	SEL_0*	SEL_1*	SEL_2*	CPU Clock Frequency
XTAL_CLK	0	-	-	CPU_CLK = XTAL_CLK/(SYSTEM_PRE_DIV_CNT + 1) SYSTEM_PRE_DIV_CNT ranges from 0 ~ 1023. Default is 1
PLL_CLK (480 MHz)	1	1	0	CPU_CLK = PLL_CLK/6 CPU_CLK frequency is 80 MHz
PLL_CLK (480 MHz)	1	1	1	CPU_CLK = PLL_CLK/3 CPU_CLK frequency is 160 MHz
PLL_CLK (480 MHz)	1	1	2	CPU_CLK = PLL_CLK/2 CPU_CLK frequency is 240 MHz
PLL_CLK (320 MHz)	1	0	0	CPU_CLK = PLL_CLK/4 CPU_CLK frequency is 80 MHz
PLL_CLK (320 MHz)	1	0	1	CPU_CLK = PLL_CLK/2 CPU_CLK frequency is 160 MHz
FOSC_CLK	2	-	-	CPU_CLK = FOSC_CLK/(SYSTEM_PRE_DIV_CNT + 1) SYSTEM_PRE_DIV_CNT ranges from 0 ~ 1023. Default is 1

* The value of register SYSTEM_SOC_CLK_SEL.

* The value of register SYSTEM_PLL_FREQ_SEL.

* The value of register SYSTEM_CPUPERIOD_SEL.

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6.2.4.2 Peripheral Clocks

Peripheral clocks include APB_CLK, CRYPTO_PWM_CLK, PLL_160M_CLK, PLL_240M_CLK, LEDC_CLK, XTAL_CLK, and FOSC_CLK. Table 6-4 shows which clock can be used by each peripheral.

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Table 6-4. Peripheral Clocks

Peripheral	XTAL_CLK	APB_CLK	PLL_160M_CLK	PLL_240M_CLK	FOSC_CLK	CRYPTO_PWM_CLK	LEDC_CLK
TIMG	Y	Y					
I2S	Y		Y	Y			
UHCI		Y					
UART	Y	Y			Y		
RMT	Y	Y			Y		
PWM						Y	
I2C	Y				Y		
SPI	Y	Y					
PCNT		Y					
eFuse Controller		Y					
SARADC		Y		Y			
USB		Y					
CRYPTO						Y	
TWAI Controller		Y					
SDIO HOST	Y		Y				
LEDC	Y	Y			Y		Y
LCD_CAM	Y		Y	Y			
SYS_TIMER	Y	Y					

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APB_CLK

APB_CLK frequency is determined by the clock source of CPU_CLK as shown in Table 6-5.

Table 6-5. APB_CLK Fequency

CPU_CLK Source	APB_CLK Frequency
PLL_CLK	80 MHz
XTAL_CLK	CPU_CLK
FOSC_CLK	CPU_CLK

CRYPTO_PWM_CLK

The frequency of CRYPTO_PWM_CLK is determined by the CPU_CLK source, as shown in Table 6-6.

Table 6-6. CRYPTO_PWM_CLK Frequency

CPU_CLK Source	CRYPTO_PWM_CLK Frequency
PLL_CLK	160 MHz
XTAL_CLK	CPU_CLK
FOSC_CLK	CPU_CLK

PLL_160M_CLK

PLL_160M_CLK is divided from PLL_CLK according to current PLL frequency.

PLL_240M_CLK

PLL_240M_CLK is divided from PLL_CLK according to current PLL frequency.

LEDC_CLK

LEDC module uses FOSC_CLK as clock source when APB_CLK is disabled. In other words, when the system is in low-power mode, most peripherals will be halted (APB_CLK is turned off), but LEDC can work normally via FOSC_CLK.

6.2.4.3 Wi-Fi and Bluetooth LE Clock

Wi-Fi and Bluetooth LE can work only when CPU_CLK uses PLL_CLK as its clock source. Suspending PLL_CLK requires that Wi-Fi and Bluetooth LE has entered low-power mode first.

LOW_POWER_CLK uses XTAL32K_CLK, XTAL_CLK, FOSC_CLK or SLOW_CLK (the low clock selected by RTC) as its clock source for Wi-Fi and Bluetooth LE in low-power mode.

6.2.4.4 RTC Clock

The clock sources for SLOW_CLK and FAST_CLK are low-frequency clocks. RTC module can operate when most other clocks are stopped.

SLOW_CLK is derived from RTC_CLK, XTAL32K_CLK or FOSC_DIV_CLK and used to clock Power Management module. FAST_CLK is used to clock On-chip Sensor module. It can be sourced from a divided XTAL_CLK or from FOSC_CLK.

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7 Chip Boot Control

7.1 Overview

ESP32-S3 has four strapping pins:

- GPIO0
- GPIO3
- GPIO45
- GPIO46

These strapping pins are used to control the following functions during chip power-on or hardware reset:

- control chip boot mode
- enable or disable ROM messages printing
- control the voltage of VDD_SPI
- control the source of JTAG signals

During power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset (see Chapter 6 *Reset and Clock*), hardware captures samples and stores the voltage level of strapping pins as strapping bit of "0" or "1" in latches, and holds these bits until the chip is powered down or shut down. Software can read the latch status (strapping value) from the register GPIO_STRAPPING.

By default, GPIO0, GPIO45, and GPIO46 are connected to the chip's internal pull-up/pull-down resistors. If these pins are not connected or connected to an external high-impedance circuit, the internal weak pull-up/pull-down determines the default input level of these strapping pins (see Table 7-1).

Table 7-1. Default Configuration of Strapping Pins

Strapping Pin	Default Configuration
GPIO0	Pull-up
GPIO3	N/A
GPIO45	Pull-down
GPIO46	Pull-down

To change the strapping bit values, users can apply external pull-down/pull-up resistors, or use host MCU GPIOs to control the voltage level of these pins when powering on ESP32-S3. After the reset is released, the strapping pins work as normal-function pins.

Note:
The following section provides description of the chip functions and the pattern of the strapping pins values to invoke each function. Only documented patterns should be used. If some pattern is not documented, it may trigger unexpected behavior.

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7.2 Boot Mode Control

GPIO0 and GPIO46 control the boot mode after the reset is released.

Table 7-2. Boot Mode Control

Boot Mode	GPIO0	GPIO46
SPI Boot	1	x
Download Boot	0	0

Table 7-2 shows the strapping pin values of GPIO0 and GPIO46, and the associated boot modes. "x" means that this value is ignored. The ESP32-S3 chip only supports the two boot modes listed above. The strapping combination of GPIO0 = 0 and GPIO46 = 1 is not supported and will trigger unexpected behavior.

In SPI Boot mode, the CPU boots the system by reading the program stored in SPI flash. SPI Boot mode can be further classified as follows:

- Normal Flash Boot: supports Security Boot and programs run in RAM.
- Direct Boot: does not support Security Boot and programs run directly in flash. To enable this mode, make sure that the first two words of the bin file downloading to flash (address: 0x42000000) are 0xaedb041d.

In Download Boot mode, users can download code to flash using UART0 or USB interface. It is also possible to load a program into SRAM and execute it in this mode.

The following eFuses control boot mode behaviors:

- EFUSE_DIS_FORCE_DOWNLOAD

  If this eFuse is 0 (default), software can force switch the chip from SPI Boot mode to Download Boot mode by setting register RTC_CNTL_FORCE_DOWNLOAD_BOOT and triggering a CPU reset. If this eFuse is 1, RTC_CNTL_FORCE_DOWNLOAD_BOOT is disabled.

- EFUSE_DIS_DOWNLOAD_MODE

  If this eFuse is 1, Download Boot mode is disabled.

- EFUSE_ENABLE_SECURITY_DOWNLOAD

  If this eFuse is 1, Download Boot mode only allows reading, writing, and erasing plaintext flash and does not support any SRAM or register operations. Ignore this eFuse if Download Boot mode is disabled.

USB Serial/JTAG Controller can also force the chip into Download Boot mode from SPI Boot mode, as well as force the chip into SPI Boot mode from Download Boot mode. For detailed information, please refer to Chapter 29 *USB Serial/JTAG Controller (USB_SERIAL_JTAG)*.

7.3 ROM Messages Printing Control

During the boot process, ROM messages are printed to both UART0 and USB Serial/JTAG controller by default. The printing to UART0 or USB Serial/JTAG controller can be disabled in various boot modes or configuration.

Printing to UART0 is controlled as described in the table below.

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Table 7-3. Control of ROM Messages Printing to UART0

Boot Mode	Register[1]	eFuse[2]	GPIO46	ROM Messages Printing to UART0
Download Boot Mode	x[3]	x	x	Printing is enabled during boot.
SPI Boot Mode	0	0	x	Printing is enabled during boot.
		1	0	Printing is enabled during boot.
			1	Printing is disabled during boot.
		2	0	Printing is disabled during boot.
			1	Printing is enabled during boot.
		3	x	Printing is disabled during boot.
	1	x	x	Printing is disabled during boot.

[1] Register: RTC_CNTL_STORE4_REG[0].

[2] eFuse: EFUSE_UART_PRINT_CONTROL.

[3] x: the value is ignored.

Printing to USB Serail/JTAG controller is controlled as described in the table below.

Table 7-4. Control of ROM Messages Printing to USB Serail/JTAG controller

Boot Mode	Register[1]	eFuse_1[2]	eFuse_2[3]	eFuse_3[4]	ROM Messages Printing to USB Serial/JTAG controller
Download Boot Mode	x[5]	0	0	0	Printing is enabled during boot.
		Others			Printing is disabled during boot.
SPI Boot Mode	0	1	1	x	Printing is enabled during boot.
		00/10/01		0	Printing is enabled during boot.
		00/10/01		1	Printing is disabled during boot.
	1	x	x	x	Printing is disabled during boot.

[1] Register: RTC_CNTL_STORE4_REG[0].

[2] eFuse_1: EFUSE_DIS_USB_SERIAL_JTAG.

[3] eFuse_2: In Download Boot mode, eFuse_2 is EFUSE_DIS_USB_SERIAL_JTAG_DOWNLOAD_MODE; In SPI Boot mode, eFuse_2 is EFUSE_DIS_USB_OTG.

[4] eFuse_3: In Download Boot mode, eFuse_3 is EFUSE_DIS_DOWNLOAD_MODE; In SPI Boot mode, eFuse_3 is EFUSE_DIS_USB_PRINT.

[5] x: the value is ignored.

Note:

The value of RTC_CNTL_STORE4_REG[0] can be read and written any number of times, whereas eFuse can only be burned once. Therefore, RTC_CNTL_STORE4_REG[0] can be used to temporarily disable ROM messages printing, while eFuse can be used to permanently disable ROM messages printing.

7.4 VDD_SPI Voltage Control

GPIO45 is used to select the VDD_SPI power supply voltage at reset:

- GPIO45 = 0, VDD_SPI pin is powered directly from VDD3P3_RTC via resistor R_{SPI}. Typically this voltage is

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3.3 V. For more information, see Figure: ESP32-S3 Power Scheme in ESP32-S3 Datasheet.

- GPIO45 = 1, VDD_SPI pin is powered from internal 1.8 V LDO.

This functionality can be overridden by setting eFuse bit EFUSE_VDD_SPI_FORCE to 1, in which case the EFUSE_
VDD_SPI_TIEH determines the VDD_SPI voltage:

- EFUSE_VDD_SPI_TIEH = 0, VDD_SPI connects to 1.8 V LDO.
- EFUSE_VDD_SPI_TIEH = 1, VDD_SPI connects to VDD3P3_RTC.

7.5 JTAG Signal Source Control

GPIO3 controls the source of JTAG signals during the early boot process. This GPIO is used together with EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_STRAP_JTAG_SEL, see Table 7-5.

Table 7-5. JTAG Signal Source Control

eFuse 1[a]	eFuse 2[b]	eFuse 3[c]	GPIO3	Signal Source
0	0	0	x	JTAG signals come from USB Serial/JTAG Controller. The value of GPIO3 is ignored.
		1	0	JTAG signals come from corresponding pins[d]
			1	JTAG signals come from USB Serial/JTAG Controller.
0	1	x	x	JTAG signals come from corresponding pins[d]. The values of EFUSE_STRAP_JTAG_SEL and GPIO3 are ignored.
1	0	x	x	JTAG signals come from USB Serial/JTAG Controller. The values of EFUSE_STRAP_JTAG_SEL and GPIO3 are ignored.
1	1	x	x	JTAG is disabled. The values of EFUSE_STRAP_JTAG_SEL and GPIO3 are ignored.

[a] eFuse 1: EFUSE_DIS_PAD_JTAG
[b] eFuse 2: EFUSE_DIS_USB_JTAG
[c] eFuse 3: EFUSE_STRAP_JTAG_SEL
[d] JTAG pins: MTDI, MTCK, MTMS, and MTDO.

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8 Interrupt Matrix (INTERRUPT)

8.1 Overview

The interrupt matrix embedded in ESP32-S3 independently allocates peripheral interrupt sources to the two CPUs' peripheral interrupts, to timely inform CPU0 or CPU1 to process the interrupts once the interrupt signals are generated.

Peripheral interrupt sources must be routed to CPU0/CPU1 peripheral interrupts via this interrupt matrix due to the following considerations:

- ESP32-S3 has 99 peripheral interrupt sources. To map them to 32 CPU0 interrupts or 32 CPU1 interrupts, this matrix is needed.
- Through this matrix, one peripheral interrupt source can be mapped to multiple CPU0 interrupts or CPU1 interrupts according to application requirements.

8.2 Features

- Accept 99 peripheral interrupt sources as input
- Generate 26 peripheral interrupts to CPU0 and 26 peripheral interrupts to CPU1 as output. Note that the remaining six CPU0 interrupts and six CPU1 interrupts are internal interrupts.
- Support to disable CPU non-maskable interrupt (NMI) sources
- Support to query current interrupt status of peripheral interrupt sources

Figure 8-1 shows the structure of the interrupt matrix.

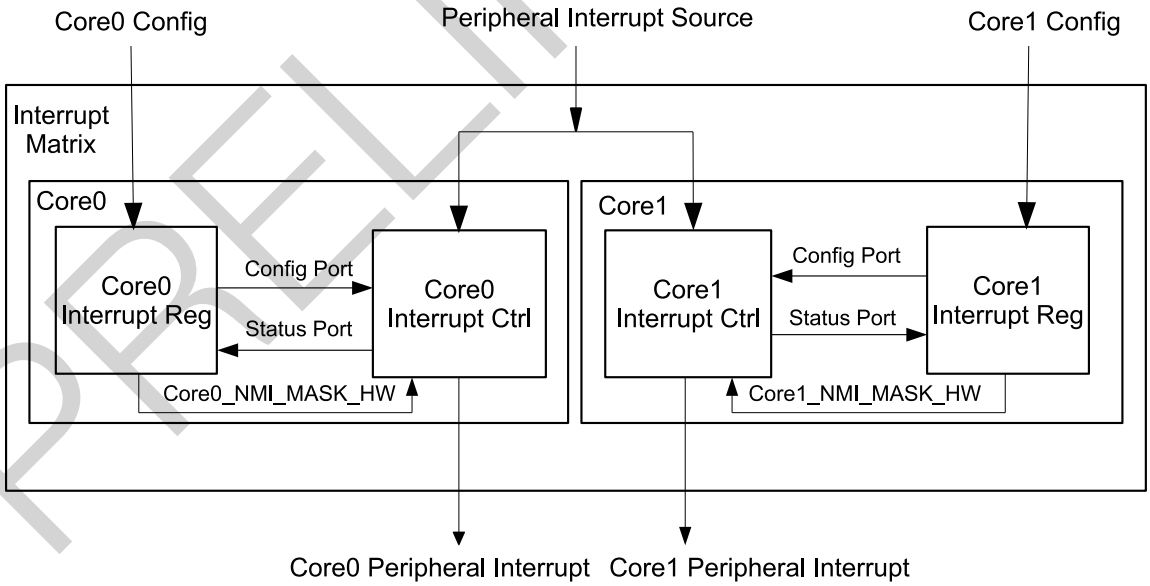


Figure 8-1. Interrupt Matrix Structure

All the interrupts generated by the peripheral interrupt sources can be handled by CPU0 or CPU1. Users can configure CPU0 interrupt registers ("Core0 Interrupt Reg" module in Figure 8-1) to allocate peripheral interrupt sources to CPU0, or configure CPU1 interrupt registers ("Core1 Interrupt Reg" module in Figure 8-1) to allocate

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peripheral interrupt sources to CPU1. Peripheral interrupt sources can be allocated both to CPU0 and CPU1 simultaneously, if so, CPU0 and CPU1 will accept the interrupts.

8.3 Functional Description

8.3.1 Peripheral Interrupt Sources

ESP32-S3 has 99 peripheral interrupt sources in total. For the peripheral interrupt sources and their configuration/status registers, please refer to Table 8-1.

- Column “No.”: the peripheral interrupt source number, can be 0 ~ 98
- Column “Source”: all peripheral interrupt sources available
- Column “Configuration Register”: the registers used for routing the peripheral interrupt sources to CPU0/CPU1 peripheral interrupts
- Column “Status Register”: the registers used for indicating the interrupt status of peripheral interrupt sources
  - Column “Status Register - Bit”: the bit position in status registers
  - Column “Status Register - Name”: the name of status registers

The register in column “Configuration Register” and the bit in column “Bit” correspond to the peripheral interrupt source in column “Source”. For example, the configuration register for interrupt source MAC_INTR is INTERRUPT_CORE*x*_MAC_INTR_MAP_REG, and its status bit in INTERRUPT_CORE*x*_INTR_STATUS_0_REG is bit0.

Note that CORE*x* in the table can be CORE0 (CPU0) or CORE1 (CPU1).

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Table 8-1. CPU Peripheral Interrupt Configuration/Status Registers and Peripheral Interrupt Sources

No.	Source	Configuration Register	Status Register	
			Bit	Name
0	MAC_INTR	INTERRUPT_COREx_MAC_INTR_MAP_REG	0	INTERRUPT_COREx_INTR_STATUS_0_REG
1	MAC_NMI	INTERRUPT_COREx_MAC_NMI_MAP_REG	1	
2	PWR_INTR	INTERRUPT_COREx_PWR_INTR_MAP_REG	2	
3	BB_INT	INTERRUPT_COREx_BB_INT_MAP_REG	3	
4	BT_MAC_INT	INTERRUPT_COREx_BT_MAC_INT_MAP_REG	4	
5	BT_BB_INT	INTERRUPT_COREx_BT_BB_INT_MAP_REG	5	
6	BT_BB_NMI	INTERRUPT_COREx_BT_BB_NMI_MAP_REG	6	
7	RWBT_IRQ	INTERRUPT_COREx_RWBT_IRQ_MAP_REG	7	
8	RWBLE_IRQ	INTERRUPT_COREx_RWBLE_IRQ_MAP_REG	8	
9	RWBT_NMI	INTERRUPT_COREx_RWBT_NMI_MAP_REG	9	
10	RWBLE_NMI	INTERRUPT_COREx_RWBLE_NMI_MAP_REG	10	
11	I2C_MST_INT	INTERRUPT_COREx_I2C_MST_INT_MAP_REG	11	
12	reserved	reserved	12	
13	reserved	reserved	13	
14	UHCI0_INTR	INTERRUPT_COREx_UHCI0_INTR_MAP_REG	14	
15	reserved	reserved	15	
16	GPIO_INTERRUPT_CPU	INTERRUPT_COREx_GPIO_INTERRUPT_CPU_MAP_REG	16	
17	GPIO_INTERRUPT_CPU_NMI	INTERRUPT_COREx_GPIO_INTERRUPT_CPU_NMI_MAP_REG	17	
18	reserved	reserved	18	
19	reserved	reserved	19	
20	SPI_INTR_1	INTERRUPT_COREx_SPI_INTR_1_MAP_REG	20	
21	SPI_INTR_2	INTERRUPT_COREx_SPI_INTR_2_MAP_REG	21	
22	SPI_INTR_3	INTERRUPT_COREx_SPI_INTR_3_MAP_REG	22	
23	reserved	reserved	23	
24	LCD_CAM_INT	INTERRUPT_COREx_LCD_CAM_INT_MAP_REG	24	
25	I2S0_INT	INTERRUPT_COREx_I2S0_INT_MAP_REG	25	
26	I2S1_INT	INTERRUPT_COREx_I2S1_INT_MAP_REG	26	
27	UART_INTR	INTERRUPT_COREx_UART_INTR_MAP_REG	27	
28	UART1_INTR	INTERRUPT_COREx_UART1_INTR_MAP_REG	28	
29	UART2_INTR	INTERRUPT_COREx_UART2_INTR_MAP_REG	29	
30	SDIO_HOST_INTERRUPT	INTERRUPT_COREx_SDIO_HOST_INTERRUPT_MAP_REG	30	
31	PWM0_INTR	INTERRUPT_COREx_PWM0_INTR_MAP_REG	31	
32	PWM1_INTR	INTERRUPT_COREx_PWM1_INTR_MAP_REG	0	INTERRUPT_COREx_INTR_STATUS_1_REG
33	reserved	reserved	1	
34	reserved	reserved	2	

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No.	Source	Configuration Register	Status Register	
			Bit	Name
35	LEDC_INT	INTERRUPT_COREx_LEDC_INT_MAP_REG	3	
36	EFUSE_INT	INTERRUPT_COREx_EFUSE_INT_MAP_REG	4	
37	CAN_INT	INTERRUPT_COREx_CAN_INT_MAP_REG	5	
38	USB_INTR	INTERRUPT_COREx_USB_INTR_MAP_REG	6	
39	RTC_CORE_INTR	INTERRUPT_COREx_RTC_CORE_INTR_MAP_REG	7	
40	RMT_INTR	INTERRUPT_COREx_RMT_INTR_MAP_REG	8	
41	PCNT_INTR	INTERRUPT_COREx_PCNT_INTR_MAP_REG	9	
42	I2C_EXT0_INTR	INTERRUPT_COREx_I2C_EXT0_INTR_MAP_REG	10	
43	I2C_EXT1_INTR	INTERRUPT_COREx_I2C_EXT1_INTR_MAP_REG	11	
44	reserved	reserved	12	
45	reserved	reserved	13	
46	reserved	reserved	14	
47	reserved	reserved	15	
48	reserved	reserved	16	
49	reserved	reserved	17	
50	TG_T0_INT	INTERRUPT_COREx_TG_T0_INT_MAP_REG	18	
51	TG_T1_INT	INTERRUPT_COREx_TG_T1_INT_MAP_REG	19	INTERRUPT_COREx_INTR_STATUS_1_REG
52	TG_WDT_INT	INTERRUPT_COREx_TG_WDT_INT_MAP_REG	20	
53	TG1_T0_INT	INTERRUPT_COREx_TG1_T0_INT_MAP_REG	21	
54	TG1_T1_INT	INTERRUPT_COREx_TG1_T1_INT_MAP_REG	22	
55	TG1_WDT_INT	INTERRUPT_COREx_TG1_WDT_INT_MAP_REG	23	
56	CACHE_IA_INT	INTERRUPT_COREx_CACHE_IA_INT_MAP_REG	24	
57	SYSTIMER_TARGET0_INT	INTERRUPT_COREx_SYSTIMER_TARGET0_INT_MAP_REG	25	
58	SYSTIMER_TARGET1_INT	INTERRUPT_COREx_SYSTIMER_TARGET1_INT_MAP_REG	26	
59	SYSTIMER_TARGET2_INT	INTERRUPT_COREx_SYSTIMER_TARGET2_INT_MAP_REG	27	
60	SPI_MEM_REJECT_INTR	INTERRUPT_COREx_SPI_MEM_REJECT_INTR_MAP_REG	28	
61	DCACHE_PRELOAD_INT	INTERRUPT_COREx_DCACHE_PRELOAD_INT_MAP_REG	29	
62	ICACHE_PRELOAD_INT	INTERRUPT_COREx_ICACHE_PRELOAD_INT_MAP_REG	30	
63	DCACHE_SYNC_INT	INTERRUPT_COREx_DCACHE_SYNC_INT_MAP_REG	31	
64	ICACHE_SYNC_INT	INTERRUPT_COREx_ICACHE_SYNC_INT_MAP_REG	0	
65	APB_ADC_INT	INTERRUPT_COREX_APB_ADC_INT_MAP_REG	1	
66	DMA_IN_CH0_INT	INTERRUPT_COREX_DMA_IN_CH0_INT_MAP_REG	2	
67	DMA_IN_CH1_INT	INTERRUPT_COREx_DMA_IN_CH1_INT_MAP_REG	3	
68	DMA_IN_CH2_INT	INTERRUPT_COREx_DMA_IN_CH2_INT_MAP_REG	4	INTERRUPT_COREx_INTR_STATUS_2_REG
69	DMA_IN_CH3_INT	INTERRUPT_COREx_DMA_IN_CH3_INT_MAP_REG	5	
70	DMA_IN_CH4_INT	INTERRUPT_COREx_DMA_IN_CH4_INT_MAP_REG	6	
71	DMA_OUT_CH0_INT	INTERRUPT_COREX_DMA_OUT_CH0_INT_MAP_REG	7	

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No.	Source	Configuration Register	Status Register	
			Bit	Name
72	DMA_OUT_CH1_INT	INTERRUPT_COREx_DMA_OUT_CH1_INT_MAP_REG	8	
73	DMA_OUT_CH2_INT	INTERRUPT_COREx_DMA_OUT_CH2_INT_MAP_REG	9	
74	DMA_OUT_CH3_INT	INTERRUPT_COREx_DMA_OUT_CH3_INT_MAP_REG	10	
75	DMA_OUT_CH4_INT	INTERRUPT_COREx_DMA_OUT_CH4_INT_MAP_REG	11	
76	RSA_INTR	INTERRUPT_COREx_RSA_INTR_MAP_REG	12	
77	AES_INTR	INTERRUPT_COREx_AES_INTR_MAP_REG	13	
78	SHA_INTR	INTERRUPT_COREx_SHA_INTR_MAP_REG	14	
79	CPU_INTR_FROM_CPU_0	INTERRUPT_COREx_CPU_INTR_FROM_CPU_0_MAP_REG	15	
80	CPU_INTR_FROM_CPU_1	INTERRUPT_COREx_CPU_INTR_FROM_CPU_1_MAP_REG	16	
81	CPU_INTR_FROM_CPU_2	INTERRUPT_COREx_CPU_INTR_FROM_CPU_2_MAP_REG	17	
82	CPU_INTR_FROM_CPU_3	INTERRUPT_COREx_CPU_INTR_FROM_CPU_3_MAP_REG	18	
83	ASSIST_DEBUG_INTR	INTERRUPT_COREx_ASSIST_DEBUG_INTR_MAP_REG	19	INTERRUPT_COREx_INTR_STATUS_2_REG
84	DMA_APB_PMS_MONITOR_VIOLATE_INTR	INTERRUPT_COREx_DMA_APB_PMS_MONITOR_VIOLATE_INTR_MAP_REG	20	
85	CORE_0_IRAM0_PMS_MONITOR_VIOLATE_INTR	INTERRUPT_COREx_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	21	
86	CORE_0_DRAM0_PMS_MONITOR_VIOLATE_INTR	INTERRUPT_COREx_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	22	
87	CORE_0_PIF_PMS_MONITOR_VIOLATE_INTR	INTERRUPT_COREx_CORE_0_PIF_PMS_MONITOR_VIOLATE_INTR_MAP_REG	23	
88	CORE_0_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR	INTERRUPT_COREx_CORE_0_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR_MAP_REG	24	
89	CORE_1_IRAM0_PMS_MONITOR_VIOLATE_INTR	INTERRUPT_COREx_CORE_1_IRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	25	
90	CORE_1_DRAM0_PMS_MONITOR_VIOLATE_INTR	INTERRUPT_COREx_CORE_1_DRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	26	
91	CORE_1_PIF_PMS_MONITOR_VIOLATE_INTR	INTERRUPT_COREx_CORE_1_PIF_PMS_MONITOR_VIOLATE_INTR_MAP_REG	27	
92	CORE_1_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR	INTERRUPT_COREx_CORE_1_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR_MAP_REG	28	
93	BACKUP_PMS_VIOLATE_INT	INTERRUPT_COREx_BACKUP_PMS_VIOLATE_INTR_MAP_REG	29	
94	CACHE_CORE0_ACS_INT	INTERRUPT_COREx_CACHE_CORE0_ACS_INT_MAP_REG	30	
95	CACHE_CORE1_ACS_INT	INTERRUPT_COREx_CACHE_CORE1_ACS_INT_MAP_REG	31	
96	USB_DEVICE_INT	INTERRUPT_COREx_USB_DEVICE_INT_MAP_REG	0	
97	PERI_BACKUP_INT	INTERRUPT_COREx_PERI_BACKUP_INT_MAP_REG	1	INTERRUPT_COREx_INTR_STATUS_3_REG
98	DMA_EXTMEM_REJECT_INT	INTERRUPT_COREx_DMA_EXTMEM_REJECT_INT_MAP_REG	2	

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8.3.2 CPU Interrupts

Each CPU has 32 interrupts, numbered from 0 ~ 31, including 26 peripheral interrupts and six internal interrupts.

- Peripheral interrupts: triggered by peripheral interrupt sources, include the following types:
  - Level-triggered interrupts: triggered by a high level signal. The interrupt sources should hold the level till the CPU*x* handles the interrupts.
  - Edge-triggered interrupts: triggered on a rising edge. CPU*x* responds to this kind of interrupts immediately.
  - NMI interrupt: once triggered, the NMI interrupt can not be masked by software using the CPU*x* internal registers. World Controller provides a way to mask this kind of interrupt. For more information, see Chapter 14 *World Controller*.
- Internal interrupts: generated inside CPU*x*, include the following types:
  - Timer interrupts: triggered by internal timers and are used to generate periodic interrupts.
  - Software interrupts: triggered when software writes to special registers.
  - Profiling interrupt: triggered for performance monitoring and analysis.

Level-triggered and edge-triggered both describe the ways of CPU*x* to accept interrupt signals. For level-triggered interrupts, the level of interrupt signal should be kept till the CPU handles the interrupt, otherwise the interrupt may be lost. For edge-triggered interrupts, when a rising edge is detected, this edge will be recorded by CPU*x*, which then allows the interrupt signal to be released.

Interrupt matrix routes the peripheral interrupt sources to any of the CPU*x* peripheral interrupts. By such way, CPU*x* can receive the interrupt signals from peripheral interrupt sources. Table 8-2 lists all the interrupts and their types as well as priorities.

ESP32-S3 supports the above-mentioned 32 interrupts at six levels as shown in the table below. A higher level corresponds to a higher priority. NMI has the highest interrupt priority and once triggered, the CPU*x* must handle such interrupt. Nested interrupts are also supported, i.e. low-level interrupts can be stopped by high-level interrupts.

Table 8-2. CPU Interrupts

No.	Category	Type	Priority
0	Peripheral	Level-triggered	1
1	Peripheral	Level-triggered	1
2	Peripheral	Level-triggered	1
3	Peripheral	Level-triggered	1
4	Peripheral	Level-triggered	1
5	Peripheral	Level-triggered	1
6	Internal	Timer.0	1
7	Internal	Software	1
8	Peripheral	Level-triggered	1
9	Peripheral	Level-triggered	1
10	Peripheral	Level-triggered	1

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No.	Category	Type	Priority
11	Internal	Profiling	3
12	Peripheral	Level-triggered	1
13	Peripheral	Level-triggered	1
14	Peripheral	NMI	NMI
15	Internal	Timer.1	3
16	Internal	Timer.2	5
17	Peripheral	Level-triggered	1
18	Peripheral	Level-triggered	1
19	Peripheral	Level-triggered	2
20	Peripheral	Level-triggered	2
21	Peripheral	Level-triggered	2
22	Peripheral	Level-triggered	3
23	Peripheral	Level-triggered	3
24	Peripheral	Level-triggered	4
25	Peripheral	Level-triggered	4
26	Peripheral	Level-triggered	5
27	Peripheral	Level-triggered	3
28	Peripheral	Level-triggered	4
29	Internal	Software	3
30	Peripheral	Level-triggered	4
31	Peripheral	Level-triggered	5

8.3.3 Allocate Peripheral Interrupt Source to CPU*x* Interrupt

In this section, the following terms are used to describe the operation of the interrupt matrix.

- Source_*Y*: stands for a peripheral interrupt source, wherein, *Y* means the number of this interrupt source in Table 8-1.
- INTERRUPT_CORE*x*_SOURCE_*Y*_MAP_REG: stands for a configuration register for the peripheral interrupt source (Source_*Y*) of CPU*x*.
- Interrupt_P: stands for the CPU*x* peripheral interrupt numbered as Num_P. The value of Num_P can be 0 ~ 5, 8 ~ 10, 12 ~ 14, 17 ~ 28, and 30 ~ 31. See Table 8-2.
- Interrupt_I: stands for the CPU*x* internal interrupt numbered as Num_I. The value of Num_I can be 6, 7, 11, 15, 16, and 29. See Table 8-2.

8.3.3.1 Allocate one peripheral interrupt source (Source_*Y*) to CPU*x*

Setting the corresponding configuration register INTERRUPT_CORE*x*_SOURCE_*Y*_MAP_REG of Source_*Y* to Num

_P allocates this interrupt source to Interrupt_P. Num_P here can be any value from 0 ~ 5, 8 ~ 10, 12 ~ 14, 17 ~ 28, and 30 ~ 31. Note that one CPU*x* interrupt can be shared by multiple peripherals.

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8.3.3.2 Allocate multiple peripheral interrupt sources (Source_Y*n*) to CPU*x*

Setting the corresponding configuration register INTERRUPT_CORE*x*_SOURCE_Y*n*_MAP_REG of each interrupt source to the same Num_P allocates multiple sources to the same Interrupt_P. Any of these sources can trigger CPU*x* Interrupt_P. When an interrupt signal is generated, CPU*x* checks the interrupt status registers to figure out which peripheral the signal comes from.

8.3.3.3 Disable CPU*x* peripheral interrupt source (Source_*Y*)

Setting the corresponding configuration register INTERRUPT_CORE*x*_SOURCE_*Y*_MAP_REG of the source to any Num_I disables this interrupt Source_*Y*. The choice of Num_I (6, 7, 11, 15, 16, 29) does not matter, as none of peripheral interrupt sources allocated to Num_I is connected to the CPU*x*. Therefore this functionality can be used to disable peripheral interrupt sources.

8.3.4 Disable CPU*x* NMI Interrupt

All CPU*x* interrupts, except for NMI interrupt (No.14 in Table 8-2), can be masked and enabled by software using CPU special register (INTENABLE). NMI interrupt can not be masked by the way above, but ESP32-S3 provides two ways to mask NMI interrupt:

- Disconnect peripheral interrupt sources from NMI interrupt, i.e. the sources routed to NMI interrupt before are now routed to other interrupts. By such way, the previous NMI interrupt is maskable.
- Connect peripheral interrupt sources with NMI interrupt, but use World Controller module to mask NMI interrupt. For more information, see Chapter Chapter 14 *World Controller*.

8.3.5 Query Current Interrupt Status of Peripheral Interrupt Source

Users can query current interrupt status of a CPU*x* peripheral interrupt source by reading the bit value in INTERRUPT_CORE*x*_INTR_STATUS_*n*_REG (read only). For the mapping between INTERRUPT_CORE*x*_INTR_STATUS_*n*_REG and peripheral interrupt sources, please refer to Table 8-1.

8.4 Register Summary

The addresses in this section are relative to the Interrupt Matrix base address provided in Table 3-3 in Chapter 3 *System and Memory*.

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8.4.1 CPU0 Interrupt Register Summary

Name	Description	Address	Access
Configuration Registers			
INTERRUPT_CORE0_MAC_INTR_MAP_REG	MAC interrupt configuration register	0x0000	R/W
INTERRUPT_CORE0_MAC_NMI_MAP_REG	MAC_NMI interrupt configuration register	0x0004	R/W
INTERRUPT_CORE0_PWR_INTR_MAP_REG	PWR interrupt configuration register	0x0008	R/W
INTERRUPT_CORE0_BB_INT_MAP_REG	BB interrupt configuration register	0x000C	R/W
INTERRUPT_CORE0_BT_MAC_INT_MAP_REG	BB_MAC interrupt configuration register	0x0010	R/W
INTERRUPT_CORE0_BT_BB_INT_MAP_REG	BT_BB interrupt configuration register	0x0014	R/W
INTERRUPT_CORE0_BT_BB_NMI_MAP_REG	BT_BB_NMI interrupt configuration register	0x0018	R/W
INTERRUPT_CORE0_RWBT_IRQ_MAP_REG	RWBT_IRQ interrupt configuration register	0x001C	R/W
INTERRUPT_CORE0_RWBLE_IRQ_MAP_REG	RWBLE_IRQ interrupt configuration register	0x0020	R/W
INTERRUPT_CORE0_RWBT_NMI_MAP_REG	RWBT_NMI interrupt configuration register	0x0024	R/W
INTERRUPT_CORE0_RWBLE_NMI_MAP_REG	RWBLE_NMI interrupt configuration register	0x0028	R/W
INTERRUPT_CORE0_I2C_MST_INT_MAP_REG	I2C_MST interrupt configuration register	0x002C	R/W
INTERRUPT_CORE0_UHCI0_INTR_MAP_REG	UHCI0 interrupt configuration register	0x0038	R/W
INTERRUPT_CORE0_GPIO_INTERRUPT_CPU_MAP_REG	GPIO_INTERRUPT_CPU interrupt configuration register	0x0040	R/W
INTERRUPT_CORE0_GPIO_INTERRUPT_CPU_NMI_MAP_REG	GPIO_INTERRUPT_CPU_NMI interrupt configuration register	0x0044	R/W
INTERRUPT_CORE0_SPI_INTR_1_MAP_REG	SPI_INTR_1 interrupt configuration register	0x0050	R/W
INTERRUPT_CORE0_SPI_INTR_2_MAP_REG	SPI_INTR_2 interrupt configuration register	0x0054	R/W
INTERRUPT_CORE0_SPI_INTR_3_MAP_REG	SPI_INTR_3 interrupt configuration register	0x0058	R/W
INTERRUPT_CORE0_LCD_CAM_INT_MAP_REG	LCD_CAM interrupt configuration register	0x0060	R/W
INTERRUPT_CORE0_I2S0_INT_MAP_REG	I2S0 interrupt configuration register	0x0064	R/W
INTERRUPT_CORE0_I2S1_INT_MAP_REG	I2S1 interrupt configuration register	0x0068	R/W
INTERRUPT_CORE0_UART_INTR_MAP_REG	UART interrupt configuration register	0x006C	R/W
INTERRUPT_CORE0_UART1_INTR_MAP_REG	UART1 interrupt configuration register	0x0070	R/W
INTERRUPT_CORE0_UART2_INTR_MAP_REG	UART2 interrupt configuration register	0x0074	R/W
INTERRUPT_CORE0_SDIO_HOST_INTERRUPT_MAP_REG	SDIO_HOST interrupt configuration register	0x0078	R/W
INTERRUPT_CORE0_PWM0_INTR_MAP_REG	PWM0 interrupt configuration register	0x007C	R/W

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Name	Description	Address	Access
INTERRUPT_CORE0_PWM1_INTR_MAP_REG	PWM1 interrupt configuration register	0x0080	R/W
INTERRUPT_CORE0_LEDC_INT_MAP_REG	LEDC interrupt configuration register	0x008C	R/W
INTERRUPT_CORE0_EFUSE_INT_MAP_REG	EFUSE interrupt configuration register	0x0090	R/W
INTERRUPT_CORE0_CAN_INT_MAP_REG	CAN interrupt configuration register	0x0094	R/W
INTERRUPT_CORE0_USB_INTR_MAP_REG	USB interrupt configuration register	0x0098	R/W
INTERRUPT_CORE0_RTC_CORE_INTR_MAP_REG	RTC_CORE interrupt configuration register	0x009C	R/W
INTERRUPT_CORE0_RMT_INTR_MAP_REG	RMT interrupt configuration register	0x00A0	R/W
INTERRUPT_CORE0_PCNT_INTR_MAP_REG	PCNT interrupt configuration register	0x00A4	R/W
INTERRUPT_CORE0_I2C_EXT0_INTR_MAP_REG	I2C_EXT0 interrupt configuration register	0x00A8	R/W
INTERRUPT_CORE0_I2C_EXT1_INTR_MAP_REG	I2C_EXT1 interrupt configuration register	0x00AC	R/W
INTERRUPT_CORE0_TG_T0_INT_MAP_REG	TG_T0 interrupt configuration register	0x00C8	R/W
INTERRUPT_CORE0_TG_T1_INT_MAP_REG	TG_T1 interrupt configuration register	0x00CC	R/W
INTERRUPT_CORE0_TG_WDT_INT_MAP_REG	TG_WDT interrupt configuration register	0x00D0	R/W
INTERRUPT_CORE0_TG1_T0_INT_MAP_REG	TG1_T0 interrupt configuration register	0x00D4	R/W
INTERRUPT_CORE0_TG1_T1_INT_MAP_REG	TG1_T1 interrupt configuration register	0x00D8	R/W
INTERRUPT_CORE0_TG1_WDT_INT_MAP_REG	TG1_WDT interrupt configuration register	0x00DC	R/W
INTERRUPT_CORE0_CACHE_IA_INT_MAP_REG	CACHE_IA interrupt configuration register	0x00E0	R/W
INTERRUPT_CORE0_SYSTIMER_TARGET0_INT_MAP_REG	SYSTIMER_TARGET0 interrupt configuration register	0x00E4	R/W
INTERRUPT_CORE0_SYSTIMER_TARGET1_INT_MAP_REG	SYSTIMER_TARGET1 interrupt configuration register	0x00E8	R/W
INTERRUPT_CORE0_SYSTIMER_TARGET2_INT_MAP_REG	SYSTIMER_TARGET2 interrupt configuration register	0x00EC	R/W
INTERRUPT_CORE0_SPI_MEM_REJECT_INTR_MAP_REG	SPI_MEM_REJECT interrupt configuration register	0x00F0	R/W
INTERRUPT_CORE0_DCACHE_PRELOAD_INT_MAP_REG	DCACHE_PRELAOD interrupt configuration register	0x00F4	R/W
INTERRUPT_CORE0_ICACHE_PRELOAD_INT_MAP_REG	ICACHE_PRELOAD interrupt configuration register	0x00F8	R/W
INTERRUPT_CORE0_DCACHE_SYNC_INT_MAP_REG	DCACHE_SYNC interrupt configuration register	0x00FC	R/W
INTERRUPT_CORE0_ICACHE_SYNC_INT_MAP_REG	ICACHE_SYNC interrupt configuration register	0x0100	R/W
INTERRUPT_CORE0_APB_ADC_INT_MAP_REG	APB_ADC interrupt configuration register	0x0104	R/W
INTERRUPT_CORE0_DMA_IN_CH0_INT_MAP_REG	DMA_IN_CH0 interrupt configuration register	0x0108	R/W
INTERRUPT_CORE0_DMA_IN_CH1_INT_MAP_REG	DMA_IN_CH1 interrupt configuration register	0x010C	R/W
INTERRUPT_CORE0_DMA_IN_CH2_INT_MAP_REG	DMA_IN_CH2 interrupt configuration register	0x0110	R/W

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Name	Description	Address	Access
INTERRUPT_CORE0_DMA_IN_CH3_INT_MAP_REG	DMA_IN_CH3 interrupt configuration register	0x0114	R/W
INTERRUPT_CORE0_DMA_IN_CH4_INT_MAP_REG	DMA_IN_CH4 interrupt configuration register	0x0118	R/W
INTERRUPT_CORE0_DMA_OUT_CH0_INT_MAP_REG	DMA_OUT_CH0 interrupt configuration register	0x011C	R/W
INTERRUPT_CORE0_DMA_OUT_CH1_INT_MAP_REG	DMA_OUT_CH1 interrupt configuration register	0x0120	R/W
INTERRUPT_CORE0_DMA_OUT_CH2_INT_MAP_REG	DMA_OUT_CH2 interrupt configuration register	0x0124	R/W
INTERRUPT_CORE0_DMA_OUT_CH3_INT_MAP_REG	DMA_OUT_CH3 interrupt configuration register	0x0128	R/W
INTERRUPT_CORE0_DMA_OUT_CH4_INT_MAP_REG	DMA_OUT_CH4 interrupt configuration register	0x012C	R/W
INTERRUPT_CORE0_RSA_INT_MAP_REG	RSA interrupt configuration register	0x0130	R/W
INTERRUPT_CORE0_AES_INT_MAP_REG	AES interrupt configuration register	0x0134	R/W
INTERRUPT_CORE0_SHA_INT_MAP_REG	SHA interrupt configuration register	0x0138	R/W
INTERRUPT_CORE0_CPU_INTR_FROM_CPU_0_MAP_REG	CPU_INTR_FROM_CPU_0 interrupt configuration register	0x013C	R/W
INTERRUPT_CORE0_CPU_INTR_FROM_CPU_1_MAP_REG	CPU_INTR_FROM_CPU_1 interrupt configuration register	0x0140	R/W
INTERRUPT_CORE0_CPU_INTR_FROM_CPU_2_MAP_REG	CPU_INTR_FROM_CPU_2 interrupt configuration register	0x0144	R/W
INTERRUPT_CORE0_CPU_INTR_FROM_CPU_3_MAP_REG	CPU_INTR_FROM_CPU_3 interrupt configuration register	0x0148	R/W
INTERRUPT_CORE0_ASSIST_DEBUG_INTR_MAP_REG	ASSIST_DEBUG interrupt configuration register	0x014C	R/W
INTERRUPT_CORE0_DMA_APBPERI_PMS_MONITOR_VIOLATE_INTR_MAP_REG	dma_pms_monitor_violatile interrupt configuration register	0x0150	R/W
INTERRUPT_CORE0_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core0_IRam0_pms_monitor_violatile interrupt configuration register	0x0154	R/W
INTERRUPT_CORE0_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core0_DRam0_pms_monitor_violatile interrupt configuration register	0x0158	R/W
INTERRUPT_CORE0_CORE_0_PIF_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core0_PIF_pms_monitor_violatile interrupt configuration register	0x015C	R/W
INTERRUPT_CORE0_CORE_0_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR_MAP_REG	core0_PIF_pms_monitor_violatile_size interrupt configuration register	0x0160	R/W
INTERRUPT_CORE0_CORE_1_IRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core1_IRam0_pms_monitor_violatile interrupt configuration register	0x0164	R/W
INTERRUPT_CORE0_CORE_1_DRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core1_DRam0_pms_monitor_violatile interrupt configuration register	0x0168	R/W

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Name	Description	Address	Access
INTERRUPT_CORE0_CORE_1_PIF_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core1_PIF_pms_monitor_violatile interrupt configuration register	0x016C	R/W
INTERRUPT_CORE0_CORE_1_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR_MAP_REG	core1_PIF_pms_monitor_violatile_size interrupt configuration register	0x0170	R/W
INTERRUPT_CORE0_BACKUP_PMS_VIOLATE_INTR_MAP_REG	BACKUP_PMS_MONITOR_VIOLATILE interrupt configuration register	0x0174	R/W
INTERRUPT_CORE0_CACHE_CORE0_ACS_INT_MAP_REG	CACHE_CORE0_ACS interrupt configuration register	0x0178	R/W
INTERRUPT_CORE0_CACHE_CORE1_ACS_INT_MAP_REG	CACHE_CORE1_ACS interrupt configuration register	0x017C	R/W
INTERRUPT_CORE0_USB_DEVICE_INT_MAP_REG	USB_DEVICE interrupt configuration register	0x0180	R/W
INTERRUPT_CORE0_PERI_BACKUP_INT_MAP_REG	PERI_BACKUP interrupt configuration register	0x0184	R/W
INTERRUPT_CORE0_DMA_EXTMEM_REJECT_INT_MAP_REG	DMA_EXTMEM_REJECT interrupt configuration register	0x0188	R/W
Status Registers			
INTERRUPT_CORE0_INTR_STATUS_0_REG	Interrupt status register	0x018C	RO
INTERRUPT_CORE0_INTR_STATUS_1_REG	Interrupt status register	0x0190	RO
INTERRUPT_CORE0_INTR_STATUS_2_REG	Interrupt status register	0x0194	RO
INTERRUPT_CORE0_INTR_STATUS_3_REG	Interrupt status register	0x0198	RO
Clock Register			
INTERRUPT_CORE0_CLOCK_GATE_REG	Clock gate register	0x019C	R/W
Version Register			
INTERRUPT_CORE0_DATE_REG	Version control register	0x07FC	R/W

8.4.2 CPU1 Interrupt Register Summary

Name	Description	Address	Access
Configuration Registers			
INTERRUPT_CORE1_MAC_INTR_MAP_REG	MAC interrupt configuration register	0x0800	R/W
INTERRUPT_CORE1_MAC_NMI_MAP_REG	MAC_NMI interrupt configuration register	0x0804	R/W
INTERRUPT_CORE1_PWR_INTR_MAP_REG	PWR interrupt configuration register	0x0808	R/W
INTERRUPT_CORE1_BB_INT_MAP_REG	BB interrupt configuration register	0x080C	R/W

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Name	Description	Address	Access
INTERRUPT_CORE1_BT_MAC_INT_MAP_REG	BB_MAC interrupt configuration register	0x0810	R/W
INTERRUPT_CORE1_BT_BB_INT_MAP_REG	BT_BB interrupt configuration register	0x0814	R/W
INTERRUPT_CORE1_BT_BB_NMI_MAP_REG	BT_BB_NMI interrupt configuration register	0x0818	R/W
INTERRUPT_CORE1_RWBT_IRQ_MAP_REG	RWBT_IRQ interrupt configuration register	0x081C	R/W
INTERRUPT_CORE1_RWBLE_IRQ_MAP_REG	RWBLE_IRQ interrupt configuration register	0x0820	R/W
INTERRUPT_CORE1_RWBT_NMI_MAP_REG	RWBT_NMI interrupt configuration register	0x0824	R/W
INTERRUPT_CORE1_RWBLE_NMI_MAP_REG	RWBLE_NMI interrupt configuration register	0x0828	R/W
INTERRUPT_CORE1_I2C_MST_INT_MAP_REG	I2C_MST interrupt configuration register	0x082C	R/W
INTERRUPT_CORE1_UHCI0_INTR_MAP_REG	UHCI0 interrupt configuration register	0x0838	R/W
INTERRUPT_CORE1_GPIO_INTERRUPT_CPU_MAP_REG	GPIO_INTERRUPT_CPU interrupt configuration register	0x0840	R/W
INTERRUPT_CORE1_GPIO_INTERRUPT_CPU_NMI_MAP_REG	GPIO_INTERRUPT_CPU_NMI Interrupt configuration register	0x0844	R/W
INTERRUPT_CORE1_SPI_INTR_1_MAP_REG	SPI_INTR_1 interrupt configuration register	0x0850	R/W
INTERRUPT_CORE1_SPI_INTR_2_MAP_REG	SPI_INTR_2 interrupt configuration register	0x0854	R/W
INTERRUPT_CORE1_SPI_INTR_3_MAP_REG	SPI_INTR_3 interrupt configuration register	0x0858	R/W
INTERRUPT_CORE1_LCD_CAM_INT_MAP_REG	LCD_CAM interrupt configuration register	0x0860	R/W
INTERRUPT_CORE1_I2S0_INT_MAP_REG	I2S0 interrupt configuration register	0x0864	R/W
INTERRUPT_CORE1_I2S1_INT_MAP_REG	I2S1 interrupt configuration register	0x0868	R/W
INTERRUPT_CORE1_UART_INTR_MAP_REG	UART interrupt configuration register	0x086C	R/W
INTERRUPT_CORE1_UART1_INTR_MAP_REG	UART1 interrupt configuration register	0x0870	R/W
INTERRUPT_CORE1_UART2_INTR_MAP_REG	UART2 interrupt configuration register	0x0874	R/W
INTERRUPT_CORE1_SDIO_HOST_INTERRUPT_MAP_REG	SDIO_HOST interrupt configuration register	0x0878	R/W
INTERRUPT_CORE1_PWM0_INTR_MAP_REG	PWM0 interrupt configuration register	0x087C	R/W
INTERRUPT_CORE1_PWM1_INTR_MAP_REG	PWM1 interrupt configuration register	0x0880	R/W
INTERRUPT_CORE1_LEDC_INT_MAP_REG	LEDC interrupt configuration register	0x088C	R/W
INTERRUPT_CORE1_EFUSE_INT_MAP_REG	EFUSE interrupt configuration register	0x0890	R/W
INTERRUPT_CORE1_CAN_INT_MAP_REG	CAN interrupt configuration register	0x0894	R/W
INTERRUPT_CORE1_USB_INTR_MAP_REG	USB interrupt configuration register	0x0898	R/W
INTERRUPT_CORE1_RTC_CORE_INTR_MAP_REG	RTC_CORE interrupt configuration register	0x089C	R/W
INTERRUPT_CORE1_RMT_INTR_MAP_REG	RMT interrupt configuration register	0x08A0	R/W

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Name	Description	Address	Access
INTERRUPT_CORE1_PCNT_INTR_MAP_REG	PCNT interrupt configuration register	0x08A4	R/W
INTERRUPT_CORE1_I2C_EXT0_INTR_MAP_REG	I2C_EXT0 interrupt configuration register	0x08A8	R/W
INTERRUPT_CORE1_I2C_EXT1_INTR_MAP_REG	I2C_EXT1 interrupt configuration register	0x08AC	R/W
INTERRUPT_CORE1_TG_T1_INT_MAP_REG	TG_T1 interrupt configuration register	0x08CC	R/W
INTERRUPT_CORE1_TG_WDT_INT_MAP_REG	TG_WDT interrupt configuration register	0x08D0	R/W
INTERRUPT_CORE1_TG1_T0_INT_MAP_REG	TG1_T0 interrupt configuration register	0x08D4	R/W
INTERRUPT_CORE1_TG1_T1_INT_MAP_REG	TG1_T1 interrupt configuration register	0x08D8	R/W
INTERRUPT_CORE1_TG1_WDT_INT_MAP_REG	TG1_WDT interrupt configuration register	0x08DC	R/W
INTERRUPT_CORE1_CACHE_IA_INT_MAP_REG	CACHE_IA interrupt configuration register	0x08E0	R/W
INTERRUPT_CORE1_SYSTIMER_TARGET0_INT_MAP_REG	SYSTIMER_TARGET0 interrupt configuration register	0x08E4	R/W
INTERRUPT_CORE1_SYSTIMER_TARGET1_INT_MAP_REG	SYSTIMER_TARGET1 interrupt configuration register	0x08E8	R/W
INTERRUPT_CORE1_SYSTIMER_TARGET2_INT_MAP_REG	SYSTIMER_TARGET2 interrupt configuration register	0x08EC	R/W
INTERRUPT_CORE1_SPI_MEM_REJECT_INTR_MAP_REG	SPI_MEM_REJECT interrupt configuration register	0x08F0	R/W
INTERRUPT_CORE1_DCACHE_PRELOAD_INT_MAP_REG	DCACHE_PRELAOD interrupt configuration register	0x08F4	R/W
INTERRUPT_CORE1_ICACHE_PRELOAD_INT_MAP_REG	ICACHE_PRELOAD interrupt configuration register	0x08F8	R/W
INTERRUPT_CORE1_DCACHE_SYNC_INT_MAP_REG	DCACHE_SYNC interrupt configuration register	0x08FC	R/W
INTERRUPT_CORE1_ICACHE_SYNC_INT_MAP_REG	ICACHE_SYNC interrupt configuration register	0x0900	R/W
INTERRUPT_CORE1_APB_ADC_INT_MAP_REG	APB_ADC interrupt configuration register	0x0904	R/W
INTERRUPT_CORE1_DMA_IN_CH0_INT_MAP_REG	DMA_IN_CH0 interrupt configuration register	0x0908	R/W
INTERRUPT_CORE1_DMA_IN_CH1_INT_MAP_REG	DMA_IN_CH1 interrupt configuration register	0x090C	R/W
INTERRUPT_CORE1_DMA_IN_CH2_INT_MAP_REG	DMA_IN_CH2 interrupt configuration register	0x0910	R/W
INTERRUPT_CORE1_DMA_IN_CH3_INT_MAP_REG	DMA_IN_CH3 interrupt configuration register	0x0914	R/W
INTERRUPT_CORE1_DMA_IN_CH4_INT_MAP_REG	DMA_IN_CH4 interrupt configuration register	0x0918	R/W
INTERRUPT_CORE1_DMA_OUT_CH0_INT_MAP_REG	DMA_OUT_CH0 interrupt configuration register	0x091C	R/W
INTERRUPT_CORE1_DMA_OUT_CH1_INT_MAP_REG	DMA_OUT_CH1 interrupt configuration register	0x0920	R/W
INTERRUPT_CORE1_DMA_OUT_CH2_INT_MAP_REG	DMA_OUT_CH2 interrupt configuration register	0x0924	R/W
INTERRUPT_CORE1_DMA_OUT_CH3_INT_MAP_REG	DMA_OUT_CH3 interrupt configuration register	0x0928	R/W
INTERRUPT_CORE1_DMA_OUT_CH4_INT_MAP_REG	DMA_OUT_CH4 interrupt configuration register	0x092C	R/W
INTERRUPT_CORE1_RSA_INT_MAP_REG	RSA interrupt configuration register	0x0930	R/W

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Name	Description	Address	Access
INTERRUPT_CORE1_AES_INT_MAP_REG	AES interrupt configuration register	0x0934	R/W
INTERRUPT_CORE1_SHA_INT_MAP_REG	SHA interrupt configuration register	0x0938	R/W
INTERRUPT_CORE1_CPU_INTR_FROM_CPU_0_MAP_REG	CPU_INTR_FROM_CPU_0 interrupt configuration register	0x093C	R/W
INTERRUPT_CORE1_CPU_INTR_FROM_CPU_1_MAP_REG	CPU_INTR_FROM_CPU_1 interrupt configuration register	0x0940	R/W
INTERRUPT_CORE1_CPU_INTR_FROM_CPU_2_MAP_REG	CPU_INTR_FROM_CPU_2 interrupt configuration register	0x0944	R/W
INTERRUPT_CORE1_CPU_INTR_FROM_CPU_3_MAP_REG	CPU_INTR_FROM_CPU_3 interrupt configuration register	0x0948	R/W
INTERRUPT_CORE1_ASSIST_DEBUG_INTR_MAP_REG	ASSIST_DEBUG interrupt configuration register	0x094C	R/W
INTERRUPT_CORE1_DMA_APBPERI_PMS_MONITOR_VIOLATE_INTR_MAP_REG	dma_pms_monitor_violatile interrupt configuration register	0x0950	R/W
INTERRUPT_CORE1_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core0_IRam0_pms_monitor_violatile interrupt configuration register	0x0954	R/W
INTERRUPT_CORE1_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core0_DRam0_pms_monitor_violatile interrupt configuration register	0x0958	R/W
INTERRUPT_CORE1_CORE_0_PIF_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core0_PIF_pms_monitor_violatile interrupt configuration register	0x095C	R/W
INTERRUPT_CORE1_CORE_0_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR_MAP_REG	core0_PIF_pms_monitor_violatile_size interrupt configuration register	0x0960	R/W
INTERRUPT_CORE1_CORE_1_IRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core1_IRam0_pms_monitor_violatile interrupt configuration register	0x0964	R/W
INTERRUPT_CORE1_CORE_1_DRAM0_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core1_DRam0_pms_monitor_violatile interrupt configuration register	0x0968	R/W
INTERRUPT_CORE1_CORE_1_PIF_PMS_MONITOR_VIOLATE_INTR_MAP_REG	core1_PIF_pms_monitor_violatile interrupt configuration register	0x096C	R/W
INTERRUPT_CORE1_CORE_1_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR_MAP_REG	core1_PIF_pms_monitor_violatile_size interrupt configuration register	0x0970	R/W
INTERRUPT_CORE1_BACKUP_PMS_VIOLATE_INTR_MAP_REG	BACKUP_PMS_MONITOR_VIOLATILE interrupt configuration register	0x0974	R/W
INTERRUPT_CORE1_CACHE_CORE0_ACS_INT_MAP_REG	CACHE_CORE0_ACS interrupt configuration register REG	0x0978	R/W
INTERRUPT_CORE1_CACHE_CORE1_ACS_INT_MAP_REG	CACHE_CORE1_ACS interrupt configuration register REG	0x097C	R/W

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Name	Description	Address	Access
INTERRUPT_CORE1_USB_DEVICE_INT_MAP_REG	USB_DEVICE interrupt configuration register	0x0980	R/W
INTERRUPT_CORE1_PERI_BACKUP_INT_MAP_REG	PERI_BACKUP interrupt configuration register	0x0984	R/W
INTERRUPT_CORE1_DMA_EXTMEM_REJECT_INT_MAP_REG	DMA_EXTMEM_REJECT interrupt configuration register	0x0988	R/W
Status Registers			
INTERRUPT_CORE1_INTR_STATUS_0_REG	Interrupt status register	0x098C	RO
INTERRUPT_CORE1_INTR_STATUS_1_REG	Interrupt status register	0x0990	RO
INTERRUPT_CORE1_INTR_STATUS_2_REG	Interrupt status register	0x0994	RO
INTERRUPT_CORE1_INTR_STATUS_3_REG	Interrupt status register	0x0998	RO
Clock Register			
INTERRUPT_CORE1_CLOCK_GATE_REG	Clock gate register	0x099C	R/W
Version Register			
INTERRUPT_CORE1_DATE_REG	Version control register	0x0FFC	R/W

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8.5 Registers

8.5.1 CPU0 Interrupt Registers

Register 8.1. INTERRUPT_CORE0_*MAC_INTR*_MAP_REG (0x0000)

Register 8.2. INTERRUPT_CORE0_*MAC_NMI*_MAP_REG (0x0004)

Register 8.3. INTERRUPT_CORE0_*PWR_INTR*_MAP_REG (0x0008)

Register 8.4. INTERRUPT_CORE0_*BB_INT*_MAP_REG (0x000C)

Register 8.5. INTERRUPT_CORE0_*BT_MAC_INT*_MAP_REG (0x0010)

Register 8.6. INTERRUPT_CORE0_*BT_BB_INT*_MAP_REG (0x0014)

Register 8.7. INTERRUPT_CORE0_*BT_BB_NMI*_MAP_REG (0x0018)

Register 8.8. INTERRUPT_CORE0_*RWBT_IRQ*_MAP_REG (0x001C)

Register 8.9. INTERRUPT_CORE0_*RWBLE_IRQ*_MAP_REG (0x0020)

Register 8.10. INTERRUPT_CORE0_*RWBT_NMI*_MAP_REG (0x0024)

Register 8.11. INTERRUPT_CORE0_*RWBLE_NMI*_MAP_REG (0x0028)

Register 8.12. INTERRUPT_CORE0_*I2C_MST_INT*_MAP_REG (0x002C)

Register 8.13. INTERRUPT_CORE0_*UHCI0_INTR*_MAP_REG (0x0038)

Register 8.14. INTERRUPT_CORE0_*GPIO_INTERRUPT_CPU*_MAP_REG (0x0040)

Register 8.15. INTERRUPT_CORE0_*GPIO_INTERRUPT_CPU_NMI*_MAP_REG (0x0044)

Register 8.16. INTERRUPT_CORE0_*SPI_INTR_1*_MAP_REG (0x0050)

Register 8.17. INTERRUPT_CORE0_*SPI_INTR_2*_MAP_REG (0x0054)

Register 8.18. INTERRUPT_CORE0_*SPI_INTR_3*_MAP_REG (0x0058)

Register 8.19. INTERRUPT_CORE0_*LCD_CAM_INT*_MAP_REG (0x0060)

Register 8.20. INTERRUPT_CORE0_*I2S0_INT*_MAP_REG (0x0064)

Register 8.21. INTERRUPT_CORE0_*I2S1_INT*_MAP_REG (0x0068)

Register 8.22. INTERRUPT_CORE0_*UART_INTR*_MAP_REG (0x006C)

Register 8.23. INTERRUPT_CORE0_*UART1_INTR*_MAP_REG (0x0070)

Register 8.24. INTERRUPT_CORE0_*UART2_INTR*_MAP_REG (0x0074)

Register 8.25. INTERRUPT_CORE0_*SDIO_HOST_INTERRUPT*_MAP_REG (0x0078)

Register 8.26. INTERRUPT_CORE0_*PWM0_INTR*_MAP_REG (0x007C)

Register 8.27. INTERRUPT_CORE0_*PWM1_INTR*_MAP_REG (0x0080)

Register 8.28. INTERRUPT_CORE0_*LEDC_INT*_MAP_REG (0x008C)

Register 8.29. INTERRUPT_CORE0_*EFUSE_INT*_MAP_REG (0x0090)

Register 8.30. INTERRUPT_CORE0_*CAN_INT*_MAP_REG (0x0094)

Register 8.31. INTERRUPT_CORE0_*USB_INTR*_MAP_REG (0x0098)

Register 8.32. INTERRUPT_CORE0_*RTC_CORE_INTR*_MAP_REG (0x009C)

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Register 8.33. INTERRUPT_CORE0_*RMT_INTR*_MAP_REG (0x00A0)

Register 8.34. INTERRUPT_CORE0_*PCNT_INTR*_MAP_REG (0x00A4)

Register 8.35. INTERRUPT_CORE0_*I2C_EXT0_INTR*_MAP_REG (0x00A8)

Register 8.36. INTERRUPT_CORE0_*I2C_EXT1_INTR*_MAP_REG (0x00AC)

Register 8.37. INTERRUPT_CORE0_*TG_T0_INT*_MAP_REG (0x00C8)

Register 8.38. INTERRUPT_CORE0_*TG_T1_INT*_MAP_REG (0x00CC)

Register 8.39. INTERRUPT_CORE0_*TG_WDT_INT*_MAP_REG (0x00D0)

Register 8.40. INTERRUPT_CORE0_*TG1_T0_INT*_MAP_REG (0x00D4)

Register 8.41. INTERRUPT_CORE0_*TG1_T1_INT*_MAP_REG (0x00D8)

Register 8.42. INTERRUPT_CORE0_*TG1_WDT_INT*_MAP_REG (0x00DC)

Register 8.43. INTERRUPT_CORE0_*CACHE_IA_INT*_MAP_REG (0x00E0)

Register 8.44. INTERRUPT_CORE0_*SYSTIMER_TARGET0_INT*_MAP_REG (0x00E4)

Register 8.45. INTERRUPT_CORE0_*SYSTIMER_TARGET1_INT*_MAP_REG (0x00E8)

Register 8.46. INTERRUPT_CORE0_*SYSTIMER_TARGET2_INT*_MAP_REG (0x00EC)

Register 8.47. INTERRUPT_CORE0_*SPI_MEM_REJECT_INTR*_MAP_REG (0x00F0)

Register 8.48. INTERRUPT_CORE0_*DCACHE_PRELOAD_INT*_MAP_REG (0x00F4)

Register 8.49. INTERRUPT_CORE0_*ICACHE_PRELOAD_INT*_MAP_REG (0x00F8)

Register 8.50. INTERRUPT_CORE0_*DCACHE_SYNC_INT*_MAP_REG (0x00FC)

Register 8.51. INTERRUPT_CORE0_*ICACHE_SYNC_INT*_MAP_REG (0x0100)

Register 8.52. INTERRUPT_CORE0_*APB_ADC_INT*_MAP_REG (0x0104)

Register 8.53. INTERRUPT_CORE0_*DMA_IN_CH0_INT*_MAP_REG (0x0108)

Register 8.54. INTERRUPT_CORE0_*DMA_IN_CH1_INT*_MAP_REG (0x010C)

Register 8.55. INTERRUPT_CORE0_*DMA_IN_CH2_INT*_MAP_REG (0x0110)

Register 8.56. INTERRUPT_CORE0_*DMA_IN_CH3_INT*_MAP_REG (0x0114)

Register 8.57. INTERRUPT_CORE0_*DMA_IN_CH4_INT*_MAP_REG (0x0118)

Register 8.58. INTERRUPT_CORE0_*DMA_OUT_CH0_INT*_MAP_REG (0x011C)

Register 8.59. INTERRUPT_CORE0_*DMA_OUT_CH1_INT*_MAP_REG (0x0120)

Register 8.60. INTERRUPT_CORE0_*DMA_OUT_CH2_INT*_MAP_REG (0x0124)

Register 8.61. INTERRUPT_CORE0_*DMA_OUT_CH3_INT*_MAP_REG (0x0128)

Register 8.62. INTERRUPT_CORE0_*DMA_OUT_CH4_INT*_MAP_REG (0x012C)

Register 8.63. INTERRUPT_CORE0_*RSA_INT*_MAP_REG (0x0130)

Register 8.64. INTERRUPT_CORE0_*AES_INT*_MAP_REG (0x0134)

Register 8.65. INTERRUPT_CORE0_*SHA_INT*_MAP_REG (0x0138)

Register 8.66. INTERRUPT_CORE0_*CPU_INTR_FROM_CPU_0*_MAP_REG (0x013C)

Register 8.67. INTERRUPT_CORE0_*CPU_INTR_FROM_CPU_1*_MAP_REG (0x0140)

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Register 8.68. INTERRUPT_CORE0_*CPU_INTR_FROM_CPU_2*_MAP_REG (0x0144)

Register 8.69. INTERRUPT_CORE0_*CPU_INTR_FROM_CPU_3*_MAP_REG (0x0148)

Register 8.70. INTERRUPT_CORE0_*ASSIST_DEBUG_INTR*_MAP_REG (0x014C)

Register 8.71. INTERRUPT_CORE0_*DMA_APBPERI_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x0150)

Register 8.72. INTERRUPT_CORE0_*CORE_0_IRAM0_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x0154)

Register 8.73. INTERRUPT_CORE0_*CORE_0_DRAM0_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x0158)

Register 8.74. INTERRUPT_CORE0_*CORE_0_PIF_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x015C)

Register 8.75. INTERRUPT_CORE0_*CORE_0_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR*_MAP_REG (0x0160)

Register 8.76. INTERRUPT_CORE0_*CORE_1_IRAM0_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x0164)

Register 8.77. INTERRUPT_CORE0_*CORE_1_DRAM0_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x0168)

Register 8.78. INTERRUPT_CORE0_*CORE_1_PIF_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x016C)

Register 8.79. INTERRUPT_CORE0_*CORE_1_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR*_MAP_REG (0x0170)

Register 8.80. INTERRUPT_CORE0_*BACKUP_PMS_VIOLATE_INTR*_MAP_REG (0x0174)

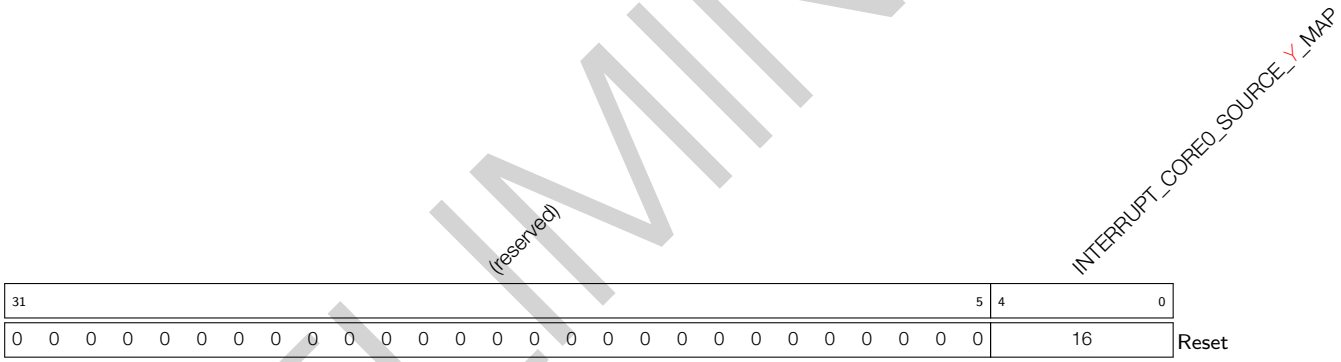
Register 8.81. INTERRUPT_CORE0_*CACHE_CORE0_ACS_INT*_MAP_REG (0x0178)

Register 8.82. INTERRUPT_CORE0_*CACHE_CORE1_ACS_INT*_MAP_REG (0x017C)

Register 8.83. INTERRUPT_CORE0_*USB_DEVICE_INT*_MAP_REG (0x0180)

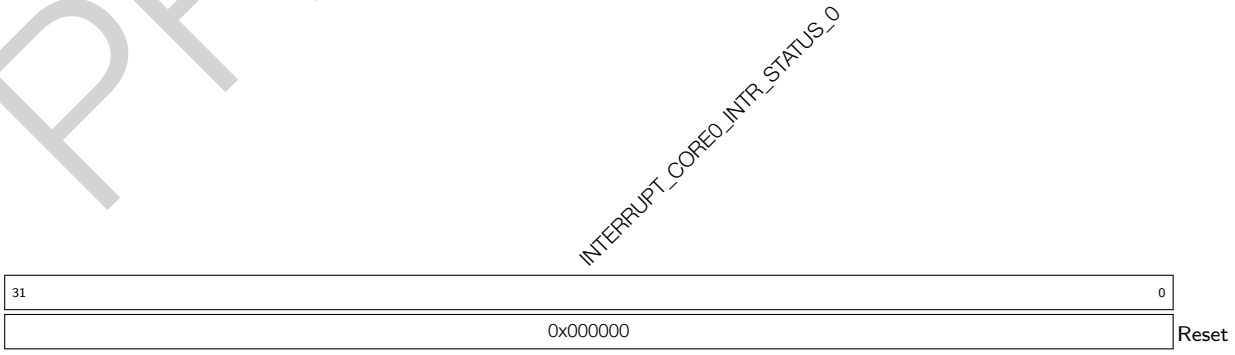
Register 8.84. INTERRUPT_CORE0_*PERI_BACKUP_INT*_MAP_REG (0x0184)

Register 8.85. INTERRUPT_CORE0_*DMA_EXTMEM_REJECT_INT*_MAP_REG (0x0188)



INTERRUPT_CORE0_SOURCE_*Y*_MAP Map interrupt signal of Source_*Y* to one of CPU0 external interrupt, can be configured as 0 ~ 5, 8 ~ 10, 12 ~ 14, 17 ~ 28, 30 ~ 31. The remaining values are invalid. For Source_*Y*, see Table 8-1. (R/W)

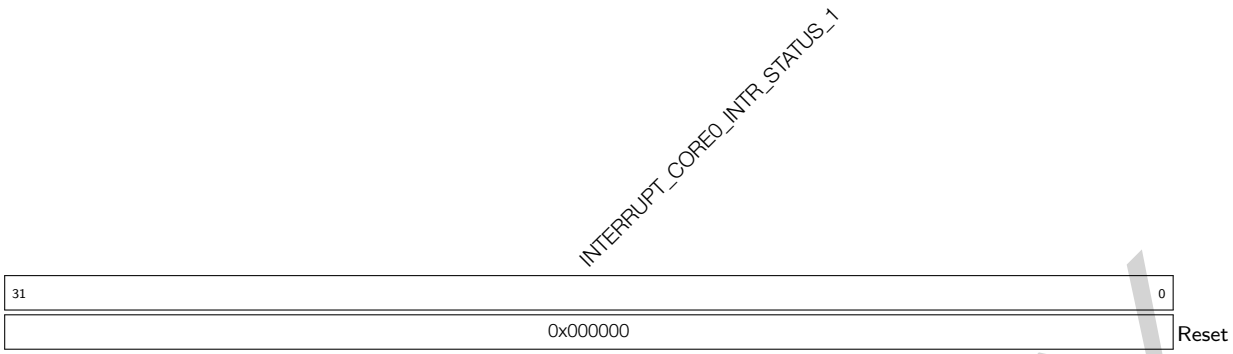
Register 8.86. INTERRUPT_CORE0_INTR_STATUS_0_REG (0x018C)



INTERRUPT_CORE0_INTR_STATUS_0 This register stores the status of the first 32 interrupt sources. (RO)

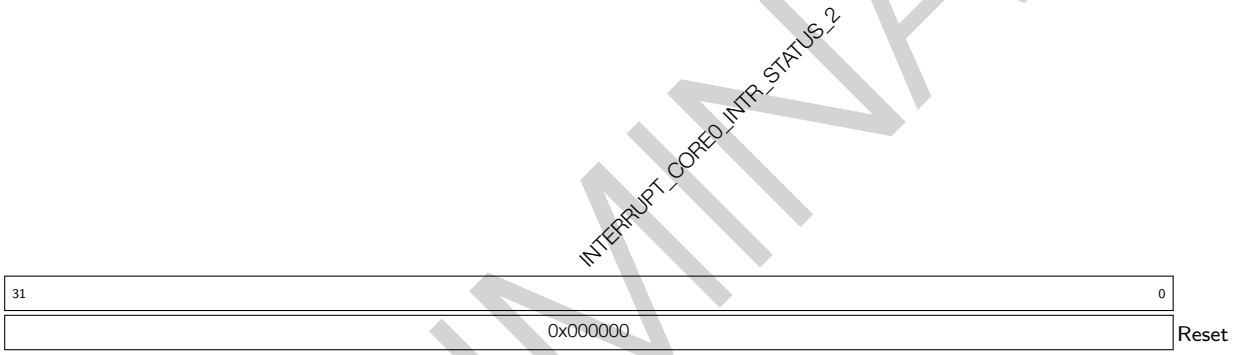
PRELIMINARY

Register 8.87. INTERRUPT_CORE0_INTR_STATUS_1_REG (0x0190)



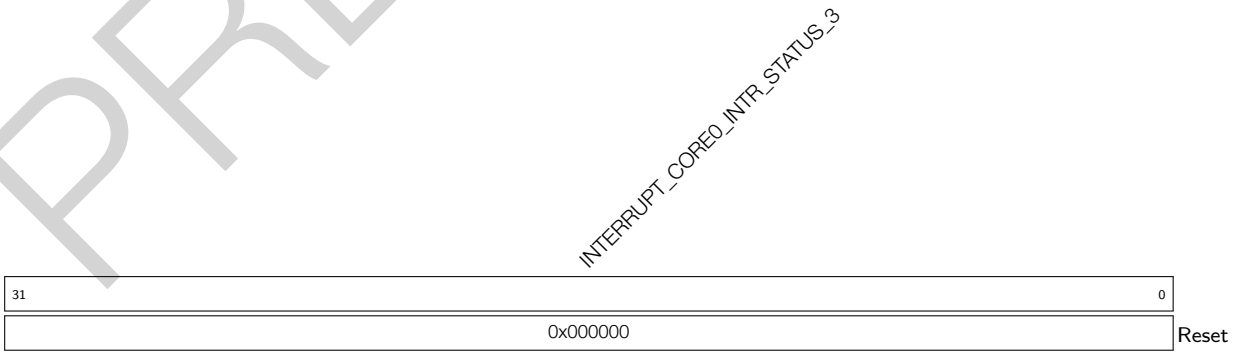
INTERRUPT_CORE0_INTR_STATUS_1 This register stores the status of the second 32 interrupt sources. (RO)

Register 8.88. INTERRUPT_CORE0_INTR_STATUS_2_REG (0x0194)



INTERRUPT_CORE0_INTR_STATUS_2 This register stores the status of the third 32 interrupt sources. (RO)

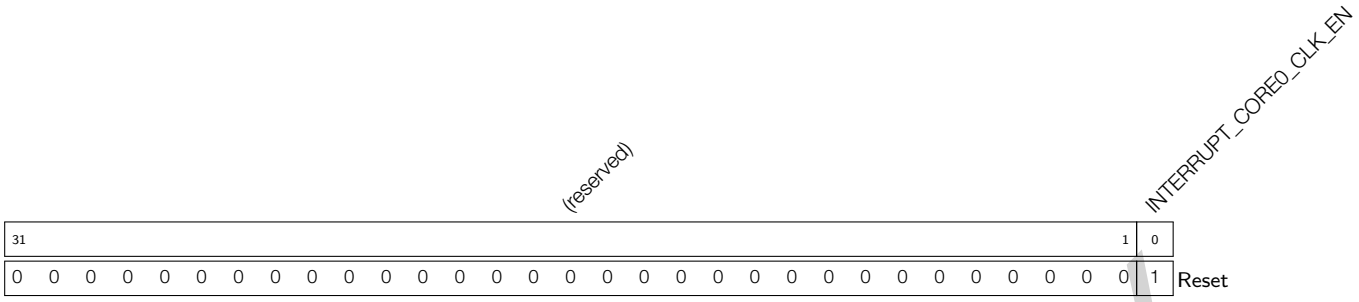
Register 8.89. INTERRUPT_CORE0_INTR_STATUS_3_REG (0x0198)



INTERRUPT_CORE0_INTR_STATUS_3 This register stores the status of the last 3 interrupt sources. (RO)

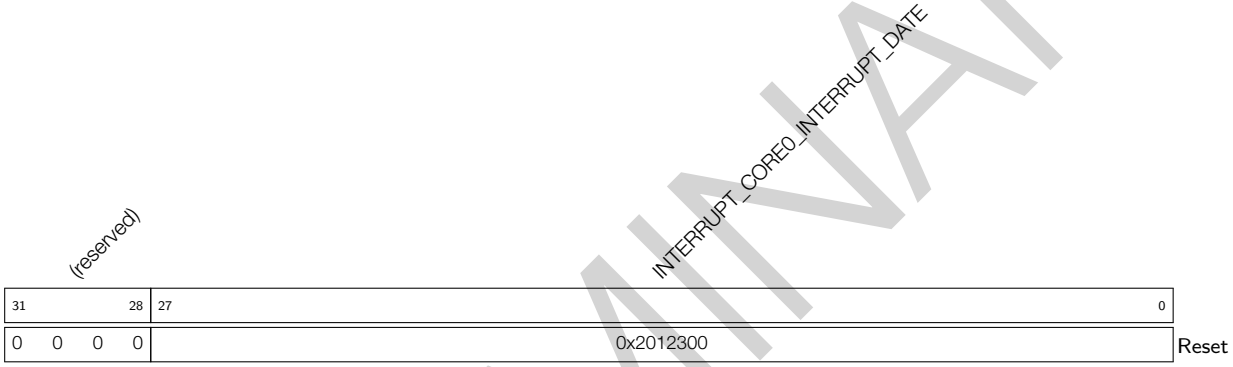
PRELIMINARY

Register 8.90. INTERRUPT_CORE0_CLOCK_GATE_REG (0x019C)



INTERRUPT_CORE0_CLK_EN This register is used to control clock-gating of interrupt matrix. (R/W)

Register 8.91. INTERRUPT_CORE0_DATE_REG (0x07FC)



INTERRUPT_CORE0_INTERRUPT_DATE Version control register (R/W)

8.5.2 CPU1 Interrupt Registers

Register 8.92. INTERRUPT_CORE1_*MAC_INTR*_MAP_REG (0x0800)

Register 8.93. INTERRUPT_CORE1_*MAC_NMI*_MAP_REG (0x0804)

Register 8.94. INTERRUPT_CORE1_*PWR_INTR*_MAP_REG (0x0808)

Register 8.95. INTERRUPT_CORE1_*BB_INT*_MAP_REG (0x080C)

Register 8.96. INTERRUPT_CORE1_*BT_MAC_INT*_MAP_REG (0x0810)

Register 8.97. INTERRUPT_CORE1_*BT_BB_INT*_MAP_REG (0x0814)

Register 8.98. INTERRUPT_CORE1_*BT_BB_NMI*_MAP_REG (0x0818)

Register 8.99. INTERRUPT_CORE1_*RWBT_IRQ*_MAP_REG (0x081C)

Register 8.100. INTERRUPT_CORE1_*RWBLE_IRQ*_MAP_REG (0x0820)

Register 8.101. INTERRUPT_CORE1_*RWBT_NMI*_MAP_REG (0x0824)

Register 8.102. INTERRUPT_CORE1_*RWBLE_NMI*_MAP_REG (0x0828)

Register 8.103. INTERRUPT_CORE1_*I2C_MST_INT*_MAP_REG (0x082C)

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Register 8.104. INTERRUPT_CORE1_*UHCI0_INTR*_MAP_REG (0x0838)

Register 8.105. INTERRUPT_CORE1_*GPIO_INTERRUPT_CPU*_MAP_REG (0x0840)

Register 8.106. INTERRUPT_CORE1_*GPIO_INTERRUPT_CPU_NMI*_MAP_REG (0x0844)

Register 8.107. INTERRUPT_CORE1_*SPI_INTR_1*_MAP_REG (0x0850)

Register 8.108. INTERRUPT_CORE1_*SPI_INTR_2*_MAP_REG (0x0854)

Register 8.109. INTERRUPT_CORE1_*SPI_INTR_3*_MAP_REG (0x0858)

Register 8.110. INTERRUPT_CORE1_*LCD_CAM_INT*_MAP_REG (0x0860)

Register 8.111. INTERRUPT_CORE1_*I2S0_INT*_MAP_REG (0x0864)

Register 8.112. INTERRUPT_CORE1_*I2S1_INT*_MAP_REG (0x0868)

Register 8.113. INTERRUPT_CORE1_*UART_INTR*_MAP_REG (0x086C)

Register 8.114. INTERRUPT_CORE1_*UART1_INTR*_MAP_REG (0x0870)

Register 8.115. INTERRUPT_CORE1_*UART2_INTR*_MAP_REG (0x0874)

Register 8.116. INTERRUPT_CORE1_*SDIO_HOST_INTERRUPT*_MAP_REG (0x0878)

Register 8.117. INTERRUPT_CORE1_*PWM0_INTR*_MAP_REG (0x087C)

Register 8.118. INTERRUPT_CORE1_*PWM1_INTR*_MAP_REG (0x0880)

Register 8.119. INTERRUPT_CORE1_*LEDC_INT*_MAP_REG (0x088C)

Register 8.120. INTERRUPT_CORE1_*EFUSE_INT*_MAP_REG (0x0890)

Register 8.121. INTERRUPT_CORE1_*CAN_INT*_MAP_REG (0x0894)

Register 8.122. INTERRUPT_CORE1_*USB_INTR*_MAP_REG (0x0898)

Register 8.123. INTERRUPT_CORE1_*RTC_CORE_INTR*_MAP_REG (0x089C)

Register 8.124. INTERRUPT_CORE1_*RMT_INTR*_MAP_REG (0x08A0)

Register 8.125. INTERRUPT_CORE1_*PCNT_INTR*_MAP_REG (0x08A4)

Register 8.126. INTERRUPT_CORE1_*I2C_EXT0_INTR*_MAP_REG (0x08A8)

Register 8.127. INTERRUPT_CORE1_*I2C_EXT1_INTR*_MAP_REG (0x08AC)

Register 8.128. INTERRUPT_CORE1_*TG_T0_INT*_MAP_REG (0x08C8)

Register 8.129. INTERRUPT_CORE1_*TG_T1_INT*_MAP_REG (0x08CC)

Register 8.130. INTERRUPT_CORE1_*TG_WDT_INT*_MAP_REG (0x08D0)

Register 8.131. INTERRUPT_CORE1_*TG1_T0_INT*_MAP_REG (0x08D4)

Register 8.132. INTERRUPT_CORE1_*TG1_T1_INT*_MAP_REG (0x08D8)

Register 8.133. INTERRUPT_CORE1_*TG1_WDT_INT*_MAP_REG (0x08DC)

Register 8.134. INTERRUPT_CORE1_*CACHE_IA_INT*_MAP_REG (0x08E0)

Register 8.135. INTERRUPT_CORE1_*SYSTIMER_TARGET0_INT*_MAP_REG (0x08E4)

Register 8.136. INTERRUPT_CORE1_*SYSTIMER_TARGET1_INT*_MAP_REG (0x08E8)

Register 8.137. INTERRUPT_CORE1_*SYSTIMER_TARGET2_INT*_MAP_REG (0x08EC)

Register 8.138. INTERRUPT_CORE1_*SPI_MEM_REJECT_INTR*_MAP_REG (0x08F0)

PRELIMINARY

Register 8.139. INTERRUPT_CORE1_*DCACHE_PRELOAD_INT*_MAP_REG (0x08F4)
Register 8.140. INTERRUPT_CORE1_*ICACHE_PRELOAD_INT*_MAP_REG (0x08F8)
Register 8.141. INTERRUPT_CORE1_*DCACHE_SYNC_INT*_MAP_REG (0x08FC)
Register 8.142. INTERRUPT_CORE1_*ICACHE_SYNC_INT*_MAP_REG (0x0900)
Register 8.143. INTERRUPT_CORE1_*APB_ADC_INT*_MAP_REG (0x0904)
Register 8.144. INTERRUPT_CORE1_*DMA_IN_CH0_INT*_MAP_REG (0x0908)
Register 8.145. INTERRUPT_CORE1_*DMA_IN_CH1_INT*_MAP_REG (0x090C)
Register 8.146. INTERRUPT_CORE1_*DMA_IN_CH2_INT*_MAP_REG (0x0910)
Register 8.147. INTERRUPT_CORE1_*DMA_IN_CH3_INT*_MAP_REG (0x0914)
Register 8.148. INTERRUPT_CORE1_*DMA_IN_CH4_INT*_MAP_REG (0x0918)
Register 8.149. INTERRUPT_CORE1_*DMA_OUT_CH0_INT*_MAP_REG (0x091C)
Register 8.150. INTERRUPT_CORE1_*DMA_OUT_CH1_INT*_MAP_REG (0x0920)
Register 8.151. INTERRUPT_CORE1_*DMA_OUT_CH2_INT*_MAP_REG (0x0924)
Register 8.152. INTERRUPT_CORE1_*DMA_OUT_CH3_INT*_MAP_REG (0x0928)
Register 8.153. INTERRUPT_CORE1_*DMA_OUT_CH4_INT*_MAP_REG (0x092C)
Register 8.154. INTERRUPT_CORE1_*RSA_INT*_MAP_REG (0x0930)
Register 8.155. INTERRUPT_CORE1_*AES_INT*_MAP_REG (0x0934)
Register 8.156. INTERRUPT_CORE1_*SHA_INT*_MAP_REG (0x0938)
Register 8.157. INTERRUPT_CORE1_*CPU_INTR_FROM_CPU_0*_MAP_REG (0x093C)
Register 8.158. INTERRUPT_CORE1_*CPU_INTR_FROM_CPU_1*_MAP_REG (0x0940)
Register 8.159. INTERRUPT_CORE1_*CPU_INTR_FROM_CPU_2*_MAP_REG (0x0944)
Register 8.160. INTERRUPT_CORE1_*CPU_INTR_FROM_CPU_3*_MAP_REG (0x0948)
Register 8.161. INTERRUPT_CORE1_*ASSIST_DEBUG_INTR*_MAP_REG (0x094C)
Register 8.162. INTERRUPT_CORE1_*DMA_APBPERI_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x0950)
Register 8.163. INTERRUPT_CORE1_*CORE_0_IRAM0_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x0954)
Register 8.164. INTERRUPT_CORE1_*CORE_0_DRAM0_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x0958)
Register 8.165. INTERRUPT_CORE1_*CORE_0_PIF_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x095C)
Register 8.166. INTERRUPT_CORE1_*CORE_0_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR*_MAP_REG (0x0960)
Register 8.167. INTERRUPT_CORE1_*CORE_1_IRAM0_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x0964)
Register 8.168. INTERRUPT_CORE1_*CORE_1_DRAM0_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x0968)
Register 8.169. INTERRUPT_CORE1_*CORE_1_PIF_PMS_MONITOR_VIOLATE_INTR*_MAP_REG (0x096C)
Register 8.170. INTERRUPT_CORE1_*CORE_1_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR*_MAP_REG (0x0970)
Register 8.171. INTERRUPT_CORE1_*BACKUP_PMS_VIOLATE_INTR*_MAP_REG (0x0974)
Register 8.172. INTERRUPT_CORE1_*CACHE_CORE0_ACS_INT*_MAP_REG (0x0978)

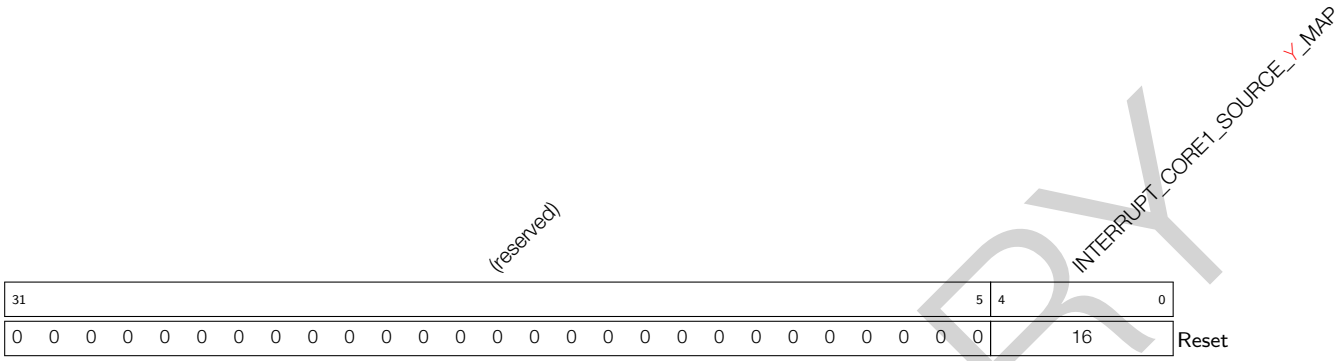
PRELIMINARY

Register 8.173. INTERRUPT_CORE1_*CACHE_CORE1_ACS_INT*_MAP_REG (0x097C)

Register 8.174. INTERRUPT_CORE1_*USB_DEVICE_INT*_MAP_REG (0x0980)

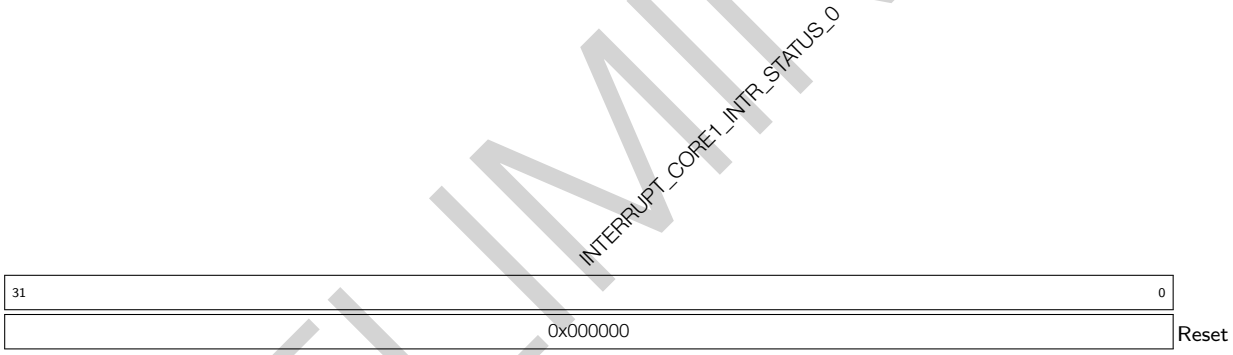
Register 8.175. INTERRUPT_CORE1_*PERI_BACKUP_INT*_MAP_REG (0x0984)

Register 8.176. INTERRUPT_CORE1_*DMA_EXTMEM_REJECT_INT*_MAP_REG (0x0988)



INTERRUPT_CORE1_SOURCE_*Y*_MAP Map interrupt signal of Source_*Y* to one of CPU1 external interrupt, can be configured as 0 ~ 5, 8 ~ 10, 12 ~ 14, 17 ~ 28, 30 ~ 31. The remaining values are invalid. For Source_*Y*, see Table 8-1. (R/W)

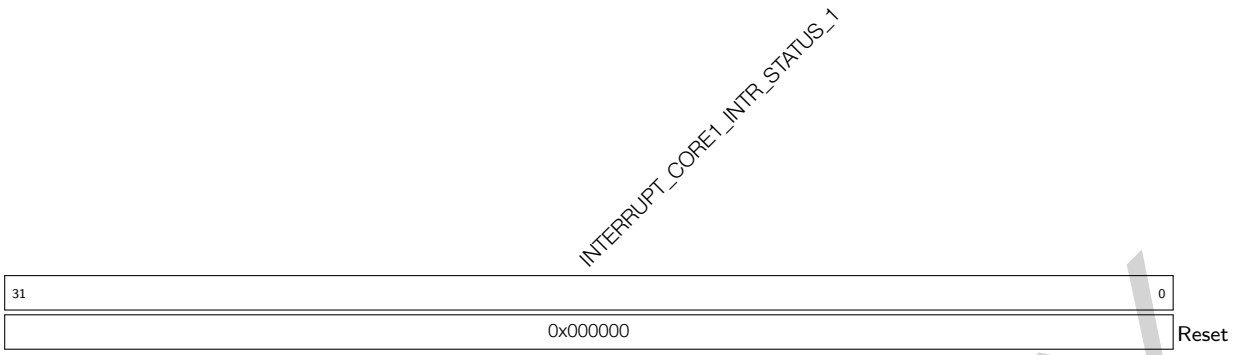
Register 8.177. INTERRUPT_CORE1_INTR_STATUS_0_REG (0x098C)



INTERRUPT_CORE1_INTR_STATUS_0 This register stores the status of the first 32 interrupt sources. (RO)

PRELIMINARY

Register 8.178. INTERRUPT_CORE1_INTR_STATUS_1_REG (0x0990)



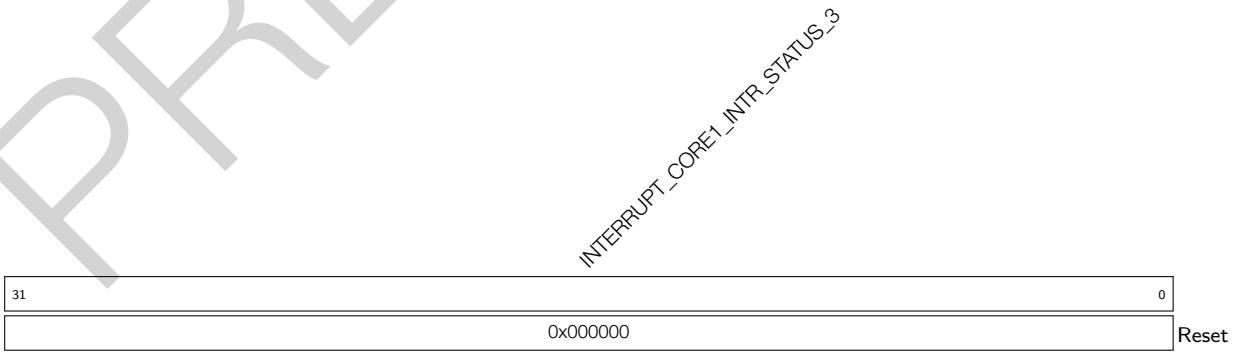
INTERRUPT_CORE1_INTR_STATUS_1 This register stores the status of the second 32 interrupt sources. (RO)

Register 8.179. INTERRUPT_CORE1_INTR_STATUS_2_REG (0x0994)



INTERRUPT_CORE1_INTR_STATUS_2 This register stores the status of the third 32 interrupt sources. (RO)

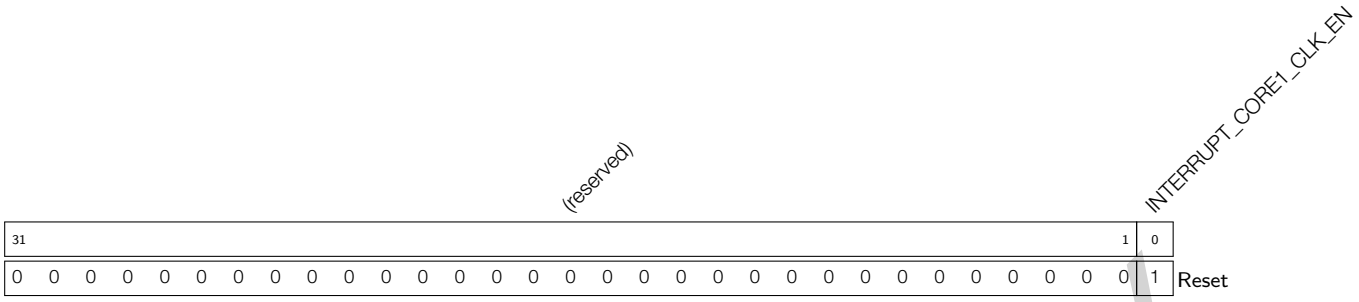
Register 8.180. INTERRUPT_CORE1_INTR_STATUS_3_REG (0x0998)



INTERRUPT_CORE1_INTR_STATUS_3 This register stores the status of the last 3 interrupt sources. (RO)

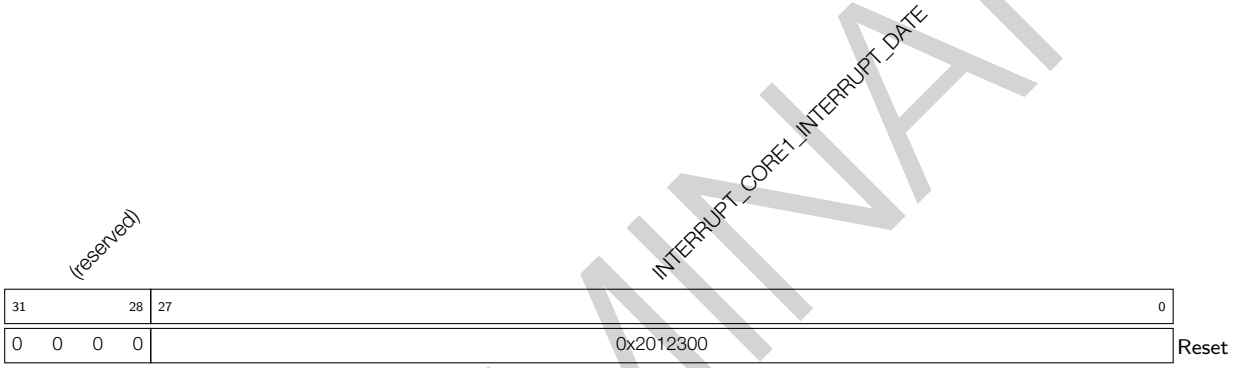
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Register 8.181. INTERRUPT_CORE1_CLOCK_GATE_REG (0x099C)



INTERRUPT_CORE1_CLK_EN This register is used to control clock-gating of interrupt matrix. (R/W)

Register 8.182. INTERRUPT_CORE1_DATE_REG (0x0FFC)



INTERRUPT_CORE1_INTERRUPT_DATE Version control register. (R/W)

PRELIMINARY

9 System Timer (SYSTIMER)

9.1 Overview

ESP32-S3 provides a 52-bit timer, which can be used to generate tick interrupts for operating system, or be used as a general timer to generate periodic interrupts or one-time interrupts. With the help of RTC timer, system timer can account for the period of the ESP32-S3 being in Light-sleep or Deep-sleep.

The timer consists of two counters UNIT0 and UNIT1. The counter values can be monitored by three comparators COMP0, COMP1 and COMP2. See the timer block diagram on Figure 9-1.

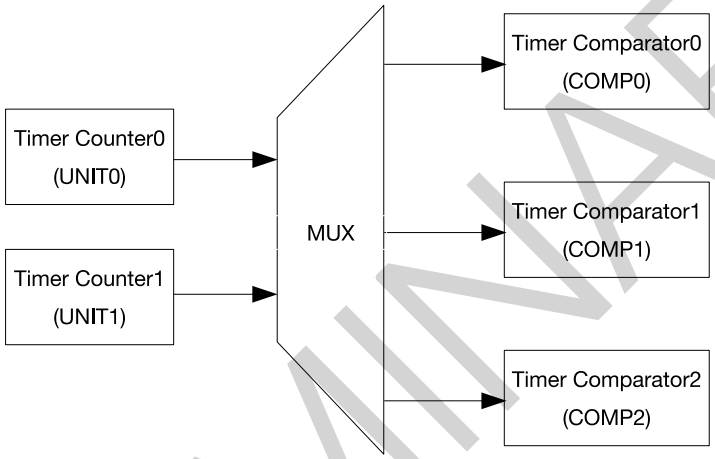


Figure 9-1. System Timer Structure

9.2 Features

- Consist of two 52-bit counters and three 52-bit comparators
- Software accessing registers is clocked by APB_CLK
- Use CNT_CLK for counting, with an average frequency of 16 MHz in two counting cycles
- Use 40 MHz XTAL_CLK as the clock source of CNT_CLK
- Support for 52-bit alarm values (t) and 26-bit alarm periods (δt)
- Provide two modes to generate alarms:
  - Target mode: only a one-time alarm is generated based on the alarm value (t)
  - Period mode: periodic alarms are generated based on the alarm period (δt)
- Three comparators can generate three independent interrupts based on configured alarm value (t) or alarm period (δt)
- Load back sleep time recorded by RTC timer via software after Deep-sleep or Light-sleep
- Can be configured to stall or continue running when CPU stalls or enters on-chip-debugging mode

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9.3 Clock Source Selection

The counters and comparators are driven using XTAL_CLK. After scaled by a fractional divider, a $f_{XTAL\_CLK}/3$ clock is generated in one count cycle and a $f_{XTAL\_CLK}/2$ clock in another count cycle. The average clock frequency is $f_{XTAL\_CLK}/2.5$, which is 16 MHz, i.e. the CNT_CLK in Figure 9-2. The timer counting is incremented by 1/16 μs on each CNT_CLK cycle.

Software operation such as configuring registers is clocked by APB_CLK. For more information about APB_CLK, see Chapter 6 *Reset and Clock*.

The following two bits of system registers are also used to control the system timer:

- SYSTEM_SYSTIMER_CLK_EN in register SYSTEM_PERIP_CLK_EN0_REG: enable APB_CLK signal to system timer.
- SYSTEM_SYSTIMER_RST in register SYSTEM_PERIP_RST_EN0_REG: reset system timer.

Note that if the timer is reset, its registers will be restored to their default values. For more information, please refer to Table Peripheral Clock Gating and Reset in Chapter 15 *System Registers*.

9.4 Functional Description

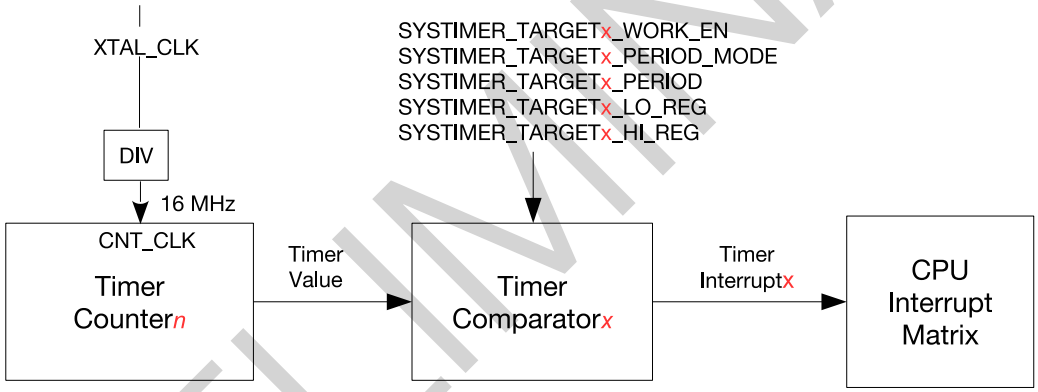


Figure 9-2. System Timer Alarms

Figure 9-2 shows the procedure to generate alarm/interrupt in system timer. In this process, one timer counter and one timer comparator are used. An alarm interrupt will be generated accordingly based on the comparison result in comparator.

9.4.1 Counter

The system timer has two 52-bit timer counters, shown as UNIT*n* (*n* = 0 or 1). Their counting clock source is a 16 MHz clock, i.e. CNT_CLK. Whether UNIT*n* works or not is controlled by three bits in register SYSTIMER_CONF_REG:

- SYSTIMER_TIMER_UNIT*n*_WORK_EN: set this bit to enable the counter UNIT*n* in system timer.
- SYSTIMER_TIMER_UNIT*n*_CORE0_STALL_EN: if this bit is set, the counter UNIT*n* stops counting when CPU0 is stalled. The counter continues its counting after the CPU0 resumes.
- SYSTIMER_TIMER_UNIT*n*_CORE1_STALL_EN: if this bit is set, the counter UNIT*n* stops counting when CPU1 is stalled. The counter continues its counting after the CPU1 resumes.

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The configuration of the three bits to control the counter UNIT*n* is shown below, assuming that CPU0 and CPU1 both are stalled.

Table 9-1. UNIT*n* Configuration Bits

SYSTIMER_TIMER_UNIT*n*_WORK_EN	SYSTIMER_TIMER_UNIT*n*_CORE0_STALL_EN	SYSTIMER_TIMER_UNIT*n*_CORE1_STALL_EN	Counter UNIT*n*
0	x*	x	Not at work
1	x	1	Stop counting, but will continue its counting after CPU1 resumes.
1	1	x	Stop counting, but will continue its counting after CPU0 resumes.
1	0	0	Keep counting

* x: Don't-care.

When the counter UNIT*n* is at work, the count value is incremented on each counting cycle. When the counter UNIT*n* is stopped or stalled, the count value stops increasing and keeps unchanged.

The low 32 bits and high 20 bits of initial count value are loaded from SYSTIMER_TIMER_UNIT*n*_LOAD_LO and SYSTIMER_TIMER_UNIT*n*_LOAD_HI. Writing 1 to the bit SYSTIMER_TIMER_UNIT*n*_LOAD will trigger a reload event, and the current count value will be changed immediately. If UNIT*n* is at work, the counter will continue to count up from the new reloaded value.

Writing 1 to SYSTIMER_TIMER_UNIT*n*_UPDATE will trigger an update event. The low 32 bits and high 20 bits of current count value will be locked into SYSTIMER_TIMER_UNIT*n*_VALUE_LO and SYSTIMER_TIMER_UNIT*n*_VALUE_HI, and then SYSTIMER_TIMER_UNIT*n*_VALUE_VALID is asserted. Before the next update event, the values of SYSTIMER_TIMER_UNIT*n*_VALUE_LO and SYSTIMER_TIMER_UNIT*n*_VALUE_HI remain unchanged.

9.4.2 Comparator and Alarm

The system timer has three 52-bit comparators, shown as COMP*x* (*x* = 0, 1, or 2). The comparators can generate independent interrupts based on different alarm values (t) or alarm periods (δt).

Configure SYSTIMER_TARGET*x*_PERIOD_MODE to choose from the two alarm modes for each COMP*x*:

- 1: select period mode
- 0: select target mode

In period mode, the alarm period (δt) is provided by the register SYSTIMER_TARGET*x*_PERIOD. Assuming that current count value is t1, when it reaches (t1 + δt), an alarm interrupt will be generated. Another alarm interrupt also will be generated when the counter value reaches (t1 + 2*δt). By such way, periodic alarms are generated.

In target mode, the low 32 bits and high 20 bits of the alarm value (t) are provided by SYSTIMER_TIMER_TARGET*x*_LO and SYSTIMER_TIMER_TARGET*x*_HI. Assuming that current count value is t2 (t2 <= t), an alarm interrupt will be generated when the count value reaches the alarm value (t). Unlike in period mode, only one alarm interrupt is generated in target mode.

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SYSTIMER_TARGET*x*_TIMER_UNIT_SEL is used to choose the count value from which timer counter to be compared for alarm:

- 1: use the count value from UNIT*1*
- 0: use the count value from UNIT*0*

Finally, set SYSTIMER_TARGET*x*_WORK_EN and COMP*x* starts to compare the count value with the alarm value (t) in target mode or with the alarm period (t1 + n*δt) in period mode.

An alarm is generated when the count value equals to the alarm value (t) in target mode or to the start value(t1) + n*alarm period δt (n = 1,2,3...) in period mode. But if the alarm value (t) set in registers is less than current count value, i.e. the target has already passed, or current count value is larger than the real target value within a range (0 ~ 2^{51} -1), an alarm interrupt also is generated immediately. The relationship between current count value t_c, the alarm value t_t and alarm trigger point is shown below. No matter in target mode or period mode, the low 32 bits and high 20 bits of the real target value can always be read from SYSTIMER_TARGET*x*_LO_RO and SYSTIMER_TARGET*x*_HI_RO.

Table 9-2. Trigger Point

Relationship Between t_c and t_t	Trigger Point
t_c- t_t <= 0	t_c = t_t, an alarm is triggered.
0 <= t_c - t_t < 2^{51} - 1 (t_c < 2^{51} and t_t < 2^{51}, or t_c >= 2^{51} and t_t >= 2^{51})	An alarm is triggered immediately.
t_c - t_t >= 2^{51} - 1	t_c overflows after counting to its maximum value 52'hfffffffffffff, and then starts counting up from 0. When its value reaches t_t, an alarm is triggered.

9.4.3 Synchronization Operation

The clock APB_CLK is used in software operation, while timer counters and comparators are working on CNT_CLK. Synchronization is needed for some configuration registers. A complete synchronization action takes two steps:

1. Software writes suitable values to configuration fields, see the first column in Table 9-3.
2. Software writes 1 to corresponding bits to start synchronization, see the second column in Table 9-3.

Table 9-3. Synchronization Operation

Configuration Fields	Synchronization Enable Bit
SYSTIMER_TIMER_UNIT*n*_LOAD_LO SYSTIMER_TIMER_UNIT*n*_LOAD_HI	SYSTIMER_TIMER_UNIT*n*_LOAD
SYSTIMER_TARGET*x*_PERIOD SYSTIMER_TIMER_TARGET*x*_HI SYSTIMER_TIMER_TARGET*x*_LO	SYSTIMER_TIMER_COMP*x*_LOAD

PRELIMINARY

9.4.4 Interrupt

Each comparator has one level-triggered alarm interrupt, named as SYSTIMER_TARGET*x*_INT. Interrupt signal is asserted high when the comparator starts to alarm. Until the interrupt is cleared by software, it remains high. To enable interrupts, set the bit SYSTIMER_TARGET*x*_INT_ENA.

9.5 Programming Procedure

9.5.1 Read Current Count Value

1. Set SYSTIMER_TIMER_UNIT*n*_UPDATE to update the current count value into SYSTIMER_TIMER_UNIT*n*_VALUE_HI and SYSTIMER_TIMER_UNIT*n*_VALUE_LO.
2. Poll the reading of SYSTIMER_TIMER_UNIT*n*_VALUE_VALID, till it's 1, which means user now can read the count values from SYSTIMER_TIMER_UNIT*n*_VALUE_HI and SYSTIMER_TIMER_UNIT*n*_VALUE_LO.
3. Read the low 32 bits and high 20 bits from SYSTIMER_TIMER_UNIT*n*_VALUE_LO and SYSTIMER_TIMER_UNIT*n*_VALUE_HI.

9.5.2 Configure One-Time Alarm in Target Mode

1. Set SYSTIMER_TARGET*x*_TIMER_UNIT_SEL to select the counter (UNIT*0* or UNIT*1*) used for COMP*x*.
2. Read current count value, see Section 9.5.1. This value will be used to calculate the alarm value (t) in Step 4.
3. Clear SYSTIMER_TARGET*x*_PERIOD_MODE to enable target mode.
4. Set an alarm value (t), and fill its low 32 bits to SYSTIMER_TIMER_TARGET*x*_LO, and the high 20 bits to SYSTIMER_TIMER_TARGET*x*_HI.
5. Set SYSTIMER_TIMER_COMP*x*_LOAD to synchronize the alarm value to COMP*x*, i.e. load the alarm value (t) to the COMP*x*.
6. Set SYSTIMER_TARGET*x*_WORK_EN to enable the selected COMP*x*. COMP*x* starts comparing the count value with the alarm value (t).
7. Set SYSTIMER_TARGET*x*_INT_ENA to enable timer interrupt. When Unit*n* counts to the alarm value (t), a SYSTIMER_TARGET*x*_INT interrupt is triggered.

9.5.3 Configure Periodic Alarms in Period Mode

1. Set SYSTIMER_TARGET*x*_TIMER_UNIT_SEL to select the counter (UNIT*0* or UNIT*1*) used for COMP*x*.
2. Set a alarm period (δt), and fill it to SYSTIMER_TARGET*x*_PERIOD.
3. Set SYSTIMER_TIMER_COMP*x*_LOAD to synchronize the alarm period (δt) to COMP*x*. , i.e. load the alarm period (δt) to COMP*x*.
4. Set SYSTIMER_TARGET*x*_PERIOD_MODE to configure COMP*x* into period mode.
5. Set SYSTIMER_TARGET*x*_WORK_EN to enable the selected COMP*x*. COMP*x* starts comparing the count value with the sum of start value + n*δt (n = 1, 2, 3...).
6. Set SYSTIMER_TARGET*x*_INT_ENA to enable timer interrupt. A SYSTIMER_TARGET*x*_INT interrupt is triggered when Unit*n* counts to start value + n*δt (n = 1, 2, 3...) set in step 2.

PRELIMINARY

9.5.4 Update After Deep-sleep and Light-sleep

1. Configure RTC timer before the chip goes to Deep-sleep or Light-sleep, to record the exact sleep time. For more information, see Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*.
2. Read the sleep time from RTC timer when the chip is woken up from Deep-sleep or Light-sleep.
3. Read current count value of system timer, see Section 9.5.1.
4. Convert the time value recorded by RTC timer from the clock cycles based on RTC_SLOW_CLK to that based on 16 MHz CNT_CLK. For example, if the frequency of RTC_SLOW_CLK is 32 KHz, the recorded RTC timer value should be converted by multiplying by 500.
5. Add the converted RTC value to current count value of system timer:
   - Fill the new value into SYSTIMER_TIMER_UNIT*n*_LOAD_LO (low 32 bits) and SYSTIMER_TIMER_UNIT*n*_LOAD_HI (high 20 bits).
   - Set SYSTIMER_TIMER_UNIT*n*_LOAD to load new timer value into system timer. By such way, the system timer is updated.

9.6 Register Summary

The addresses in this section are relative to system timer base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
Clock Control Register			
SYSTIMER_CONF_REG	Configure system timer clock	0x0000	R/W
UNIT*0* Control and Configuration Registers			
SYSTIMER_UNIT0_OP_REG	Read UNIT0 value to registers	0x0004	varies
SYSTIMER_UNIT0_LOAD_HI_REG	High 20 bits to be loaded to UNIT0	0x000C	R/W
SYSTIMER_UNIT0_LOAD_LO_REG	Low 32 bits to be loaded to UNIT0	0x0010	R/W
SYSTIMER_UNIT0_VALUE_HI_REG	UNIT0 value, high 20 bits	0x0040	RO
SYSTIMER_UNIT0_VALUE_LO_REG	UNIT0 value, low 32 bits	0x0044	RO
SYSTIMER_UNIT0_LOAD_REG	UNIT0 synchronization register	0x005C	WT
UNIT*1* Control and Configuration Registers			
SYSTIMER_UNIT1_OP_REG	Read UNIT1 value to registers	0x0008	varies
SYSTIMER_UNIT1_LOAD_HI_REG	High 20 bits to be loaded to UNIT1	0x0014	R/W
SYSTIMER_UNIT1_LOAD_LO_REG	Low 32 bits to be loaded to UNIT1	0x0018	R/W
SYSTIMER_UNIT1_VALUE_HI_REG	UNIT1 value, high 20 bits	0x0048	RO
SYSTIMER_UNIT1_VALUE_LO_REG	UNIT1 value, low 32 bits	0x004C	RO
SYSTIMER_UNIT1_LOAD_REG	UNIT1 synchronization register	0x0060	WT
Comparator*0* Control and Configuration Registers			
SYSTIMER_TARGET0_HI_REG	Alarm value to be loaded to COMP0, high 20 bits	0x001C	R/W
SYSTIMER_TARGET0_LO_REG	Alarm value to be loaded to COMP0, low 32 bits	0x0020	R/W
SYSTIMER_TARGET0_CONF_REG	Configure COMP0 alarm mode	0x0034	R/W
SYSTIMER_COMP0_LOAD_REG	COMP0 synchronization register	0x0050	WT
Comparator*1* Control and Configuration Registers			
SYSTIMER_TARGET1_HI_REG	Alarm value to be loaded to COMP1, high 20 bits	0x0024	R/W

PRELIMINARY

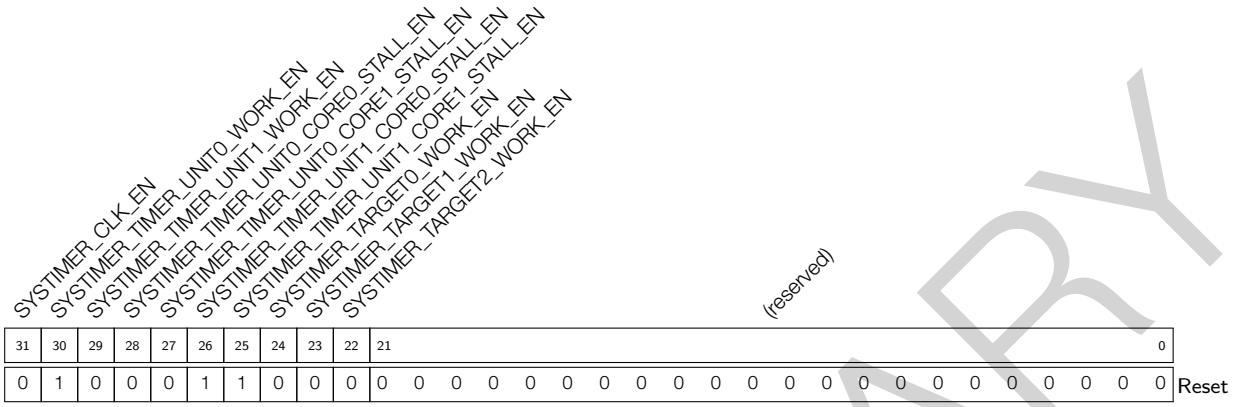
Name	Description	Address	Access
SYSTIMER_TARGET1_LO_REG	Alarm value to be loaded to COMP1, low 32 bits	0x0028	R/W
SYSTIMER_TARGET1_CONF_REG	Configure COMP1 alarm mode	0x0038	R/W
SYSTIMER_COMP1_LOAD_REG	COMP1 synchronization register	0x0054	WT
Comparator*2* Control and Configuration Registers			
SYSTIMER_TARGET2_HI_REG	Alarm value to be loaded to COMP2, high 20 bits	0x002C	R/W
SYSTIMER_TARGET2_LO_REG	Alarm value to be loaded to COMP2, low 32 bits	0x0030	R/W
SYSTIMER_TARGET2_CONF_REG	Configure COMP2 alarm mode	0x003C	R/W
SYSTIMER_COMP2_LOAD_REG	COMP2 synchronization register	0x0058	WT
Interrupt Registers			
SYSTIMER_INT_ENA_REG	Interrupt enable register of system timer	0x0064	R/W
SYSTIMER_INT_RAW_REG	Interrupt raw register of system timer	0x0068	R/WTC/SS
SYSTIMER_INT_CLR_REG	Interrupt clear register of system timer	0x006C	WT
SYSTIMER_INT_ST_REG	Interrupt status register of system timer	0x0070	RO
COMP*0* Status Registers			
SYSTIMER_REAL_TARGET0_LO_REG	Actual target value of COMP0, low 32 bits	0x0074	RO
SYSTIMER_REAL_TARGET0_HI_REG	Actual target value of COMP0, high 20 bits	0x0078	RO
COMP*1* Status Registers			
SYSTIMER_REAL_TARGET1_LO_REG	Actual target value of COMP1, low 32 bits	0x007C	RO
SYSTIMER_REAL_TARGET1_HI_REG	Actual target value of COMP1, high 20 bits	0x0080	RO
COMP*2* Status Registers			
SYSTIMER_REAL_TARGET2_LO_REG	Actual target value of COMP2, low 32 bits	0x0084	RO
SYSTIMER_REAL_TARGET2_HI_REG	Actual target value of COMP2, high 20 bits	0x0088	RO
Version Register			
SYSTIMER_DATE_REG	Version control register	0x00FC	R/W

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9.7 Registers

The addresses in this section are relative to system timer base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 9.1. SYSTIMER_CONF_REG (0x0000)



SYSTIMER_TARGET2_WORK_EN COMP2 work enable bit. (R/W)

SYSTIMER_TARGET1_WORK_EN COMP1 work enable bit. (R/W)

SYSTIMER_TARGET0_WORK_EN COMP0 work enable bit. (R/W)

SYSTIMER_TIMER_UNIT1_CORE1_STALL_EN UNIT1 is stalled when CPU1 stalled. (R/W)

SYSTIMER_TIMER_UNIT1_CORE0_STALL_EN UNIT1 is stalled when CPU0 stalled. (R/W)

SYSTIMER_TIMER_UNIT0_CORE1_STALL_EN UNIT0 is stalled when CPU1 stalled. (R/W)

SYSTIMER_TIMER_UNIT0_CORE0_STALL_EN UNIT0 is stalled when CPU0 stalled. (R/W)

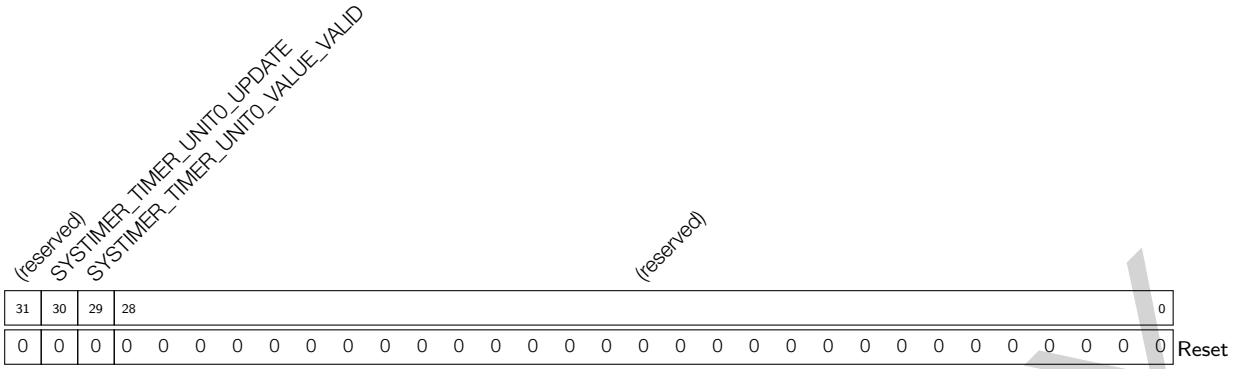
SYSTIMER_TIMER_UNIT1_WORK_EN UNIT1 work enable bit. (R/W)

SYSTIMER_TIMER_UNIT0_WORK_EN UNIT0 work enable bit. (R/W)

SYSTIMER_CLK_EN Register clock gating. 1: Register clock is always enabled for read and write operations. 0: Only enable needed clock for register read or write operations. (R/W)

PRELIMINARY

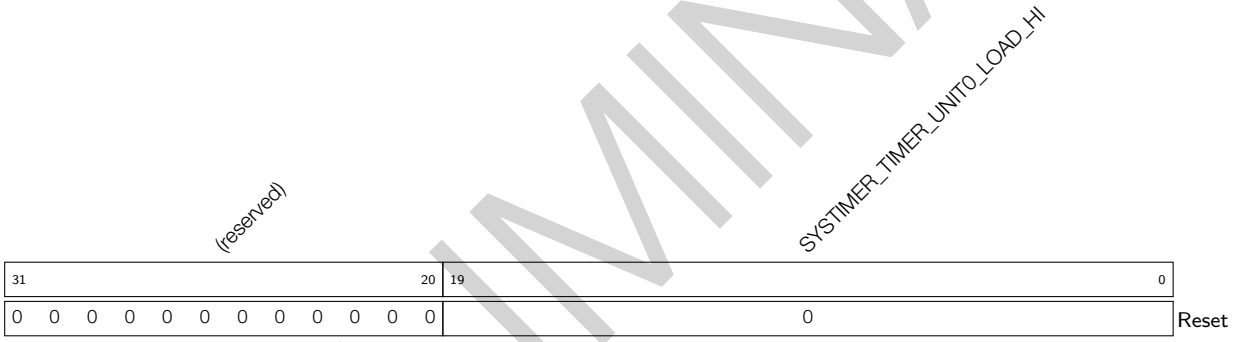
Register 9.2. SYSTIMER_UNIT0_OP_REG (0x0004)



SYSTIMER_TIMER_UNIT0_VALUE_VALID UNIT0 value is synchronized and valid. (R/SS/WTC)

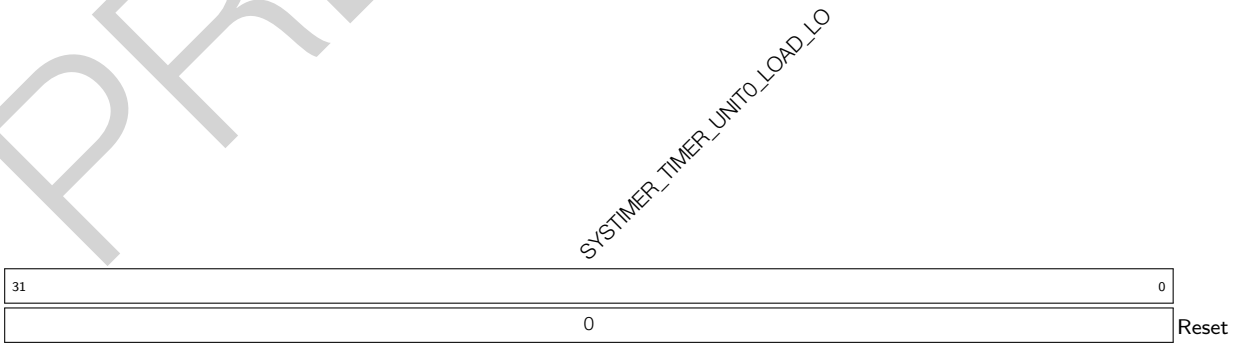
SYSTIMER_TIMER_UNIT0_UPDATE Update timer UNIT0, i.e. read the UNIT0 count value to SYSTIMER_TIMER_UNIT0_VALUE_HI and SYSTIMER_TIMER_UNIT0_VALUE_LO. (WT)

Register 9.3. SYSTIMER_UNIT0_LOAD_HI_REG (0x000C)



SYSTIMER_TIMER_UNIT0_LOAD_HI The value to be loaded to UNIT0, high 20 bits. (R/W)

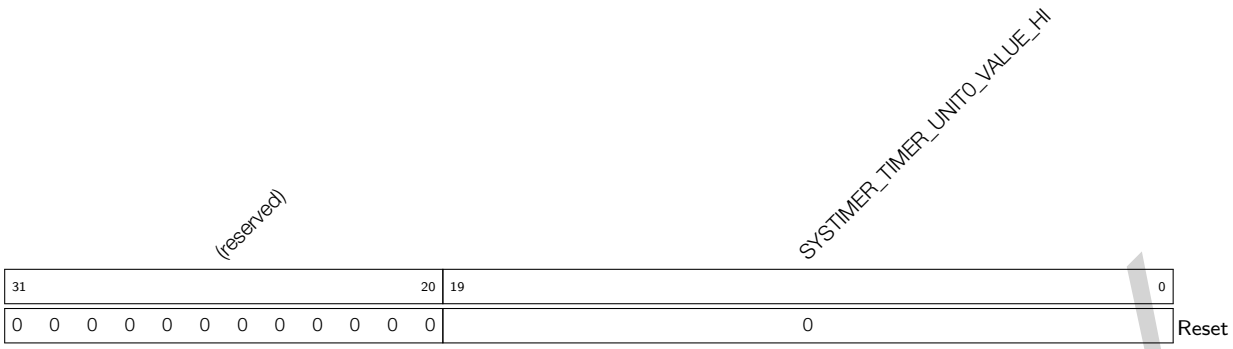
Register 9.4. SYSTIMER_UNIT0_LOAD_LO_REG (0x0010)



SYSTIMER_TIMER_UNIT0_LOAD_LO The value to be loaded to UNIT0, low 32 bits. (R/W)

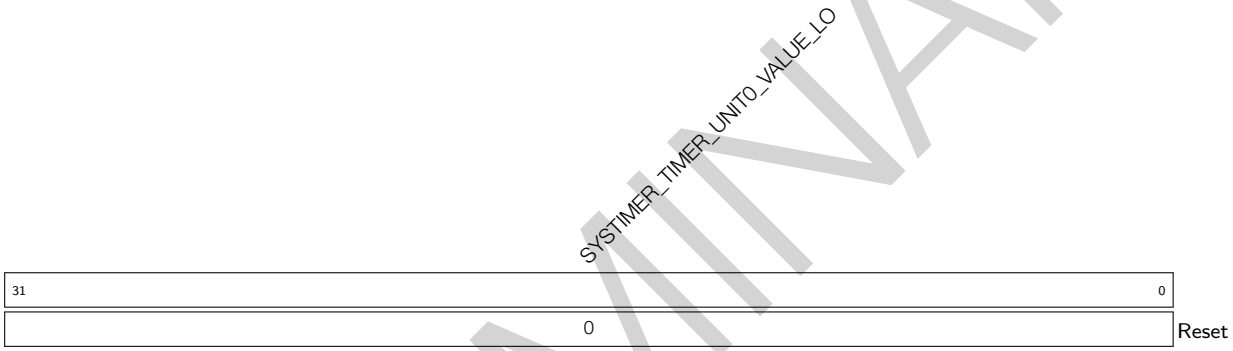
PRELIMINARY

Register 9.5. SYSTIMER_UNIT0_VALUE_HI_REG (0x0040)



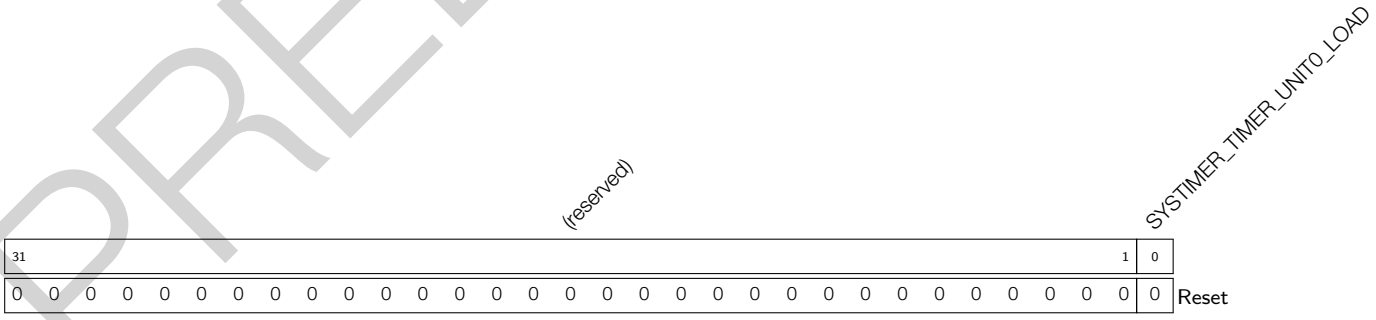
SYSTIMER_TIMER_UNIT0_VALUE_HI UNIT0 read value, high 20 bits. (RO)

Register 9.6. SYSTIMER_UNIT0_VALUE_LO_REG (0x0044)



SYSTIMER_TIMER_UNIT0_VALUE_LO UNIT0 read value, low 32 bits. (RO)

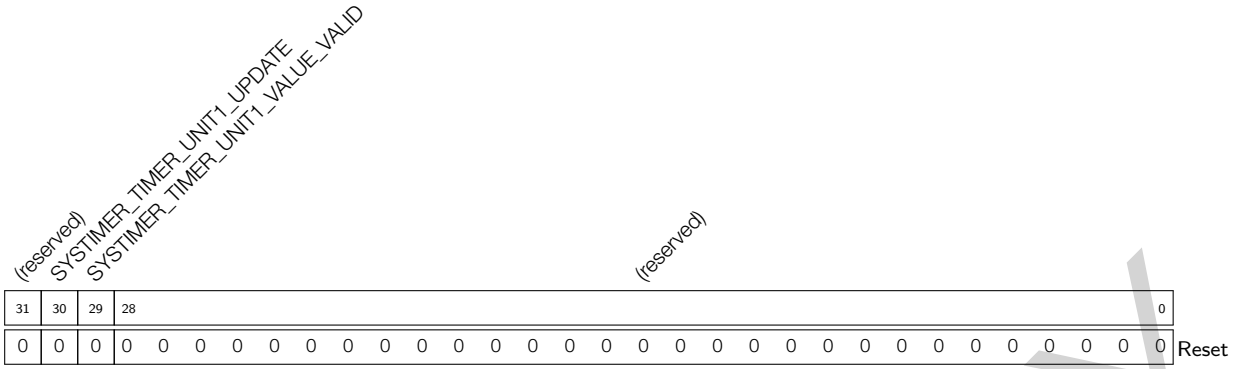
Register 9.7. SYSTIMER_UNIT0_LOAD_REG (0x005C)



SYSTIMER_TIMER_UNIT0_LOAD UNIT0 synchronization enable signal. Set this bit to reload the values of SYSTIMER_TIMER_UNIT0_LOAD_HI and SYSTIMER_TIMER_UNIT0_LOAD_LO to UNIT0. (WT)

PRELIMINARY

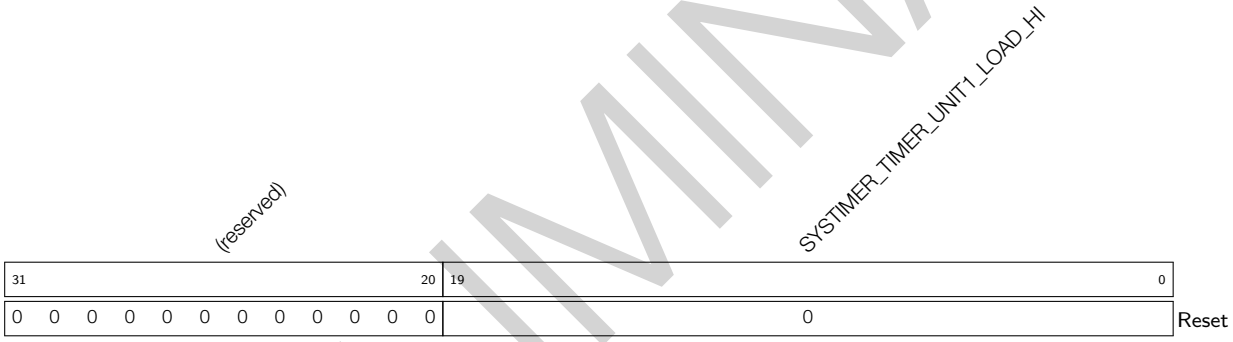
Register 9.8. SYSTIMER_UNIT1_OP_REG (0x0008)



SYSTIMER_TIMER_UNIT1_VALUE_VALID UNIT1 value is synchronized and valid. (R/SS/WTC)

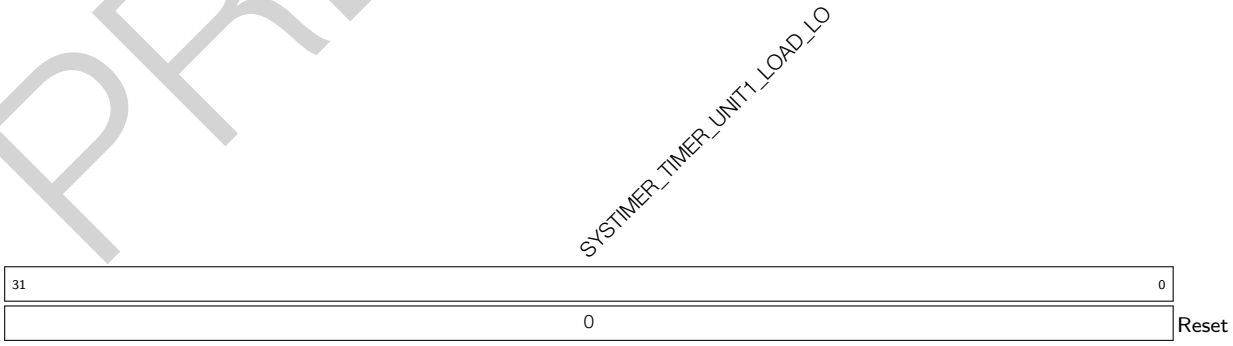
SYSTIMER_TIMER_UNIT1_UPDATE Update timer UNIT1, i.e. read the UNIT1 count value to SYSTIMER_TIMER_UNIT1_VALUE_HI and SYSTIMER_TIMER_UNIT1_VALUE_LO. (WT)

Register 9.9. SYSTIMER_UNIT1_LOAD_HI_REG (0x0014)



SYSTIMER_TIMER_UNIT1_LOAD_HI The value to be loaded to UNIT1, high 20 bits. (R/W)

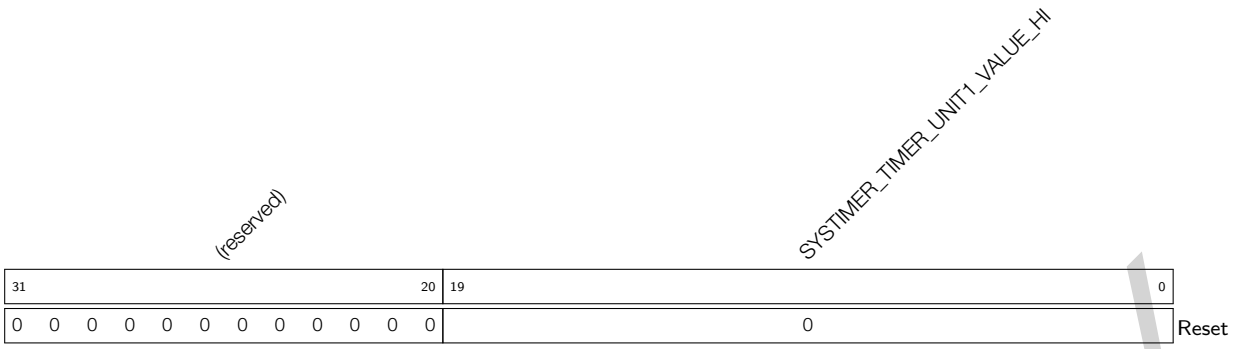
Register 9.10. SYSTIMER_UNIT1_LOAD_LO_REG (0x0018)



SYSTIMER_TIMER_UNIT1_LOAD_LO The value to be loaded to UNIT1, low 32 bits. (R/W)

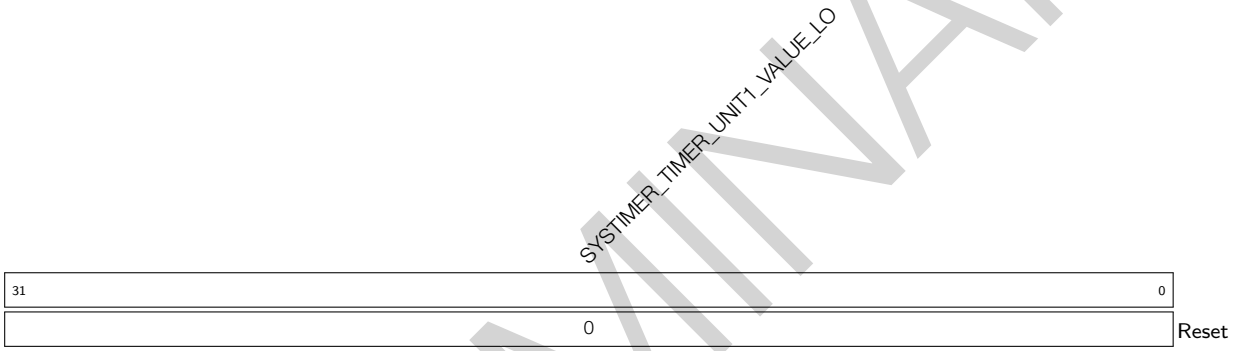
PRELIMINARY

Register 9.11. SYSTIMER_UNIT1_VALUE_HI_REG (0x0048)



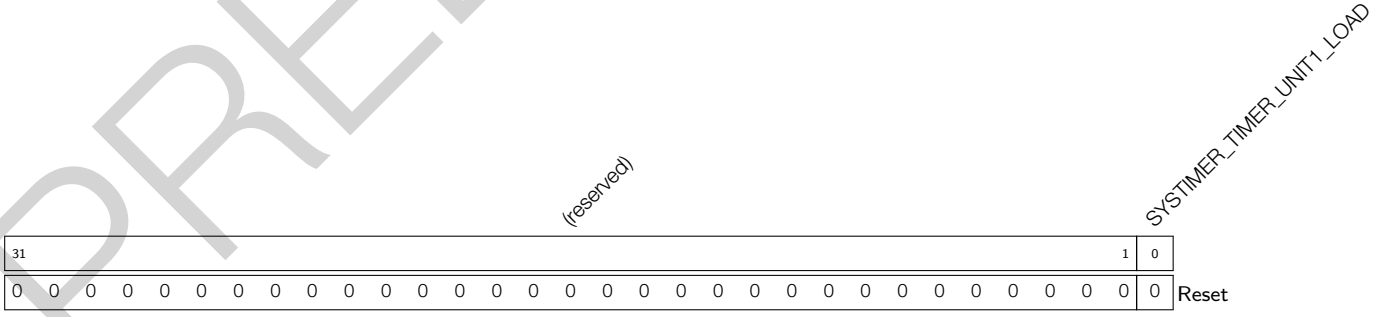
SYSTIMER_TIMER_UNIT1_VALUE_HI UNIT1 read value, high 20 bits. (RO)

Register 9.12. SYSTIMER_UNIT1_VALUE_LO_REG (0x004C)



SYSTIMER_TIMER_UNIT1_VALUE_LO UNIT1 read value, low 32 bits. (RO)

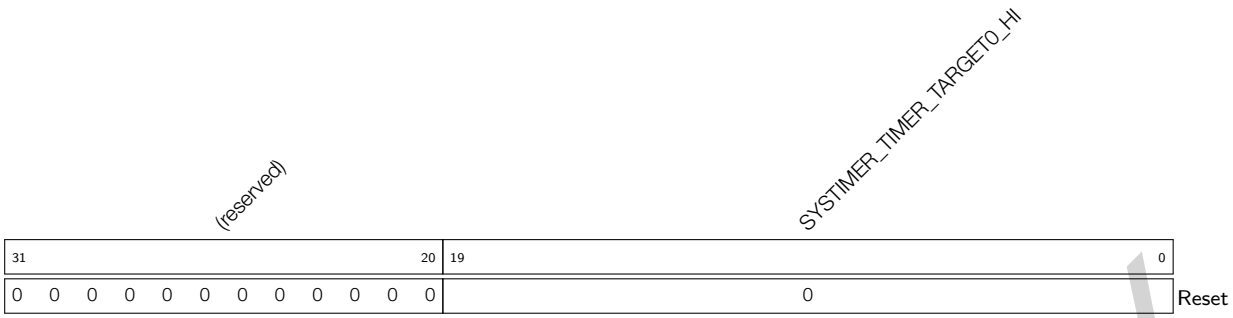
Register 9.13. SYSTIMER_UNIT1_LOAD_REG (0x0060)



SYSTIMER_TIMER_UNIT1_LOAD UNIT1 synchronization enable signal. Set this bit to reload the values of SYSTIMER_TIMER_UNIT1_LOAD_HI and SYSTIMER_TIMER_UNIT1_LOAD_LO to UNIT1. (WT)

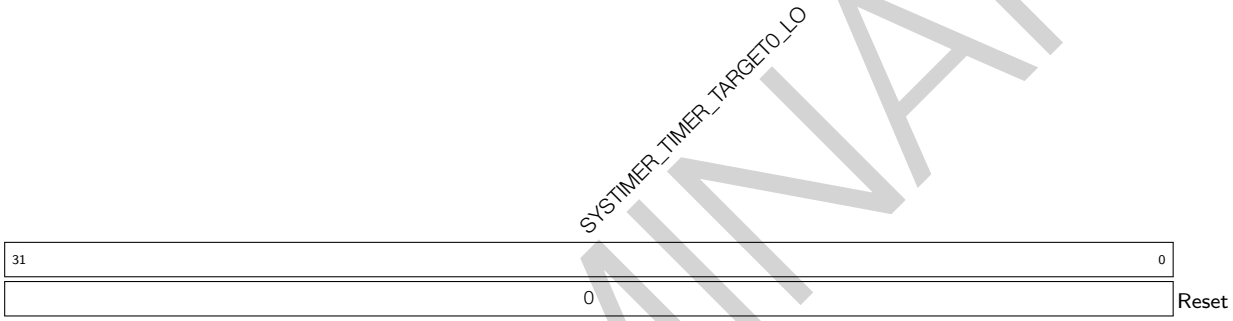
PRELIMINARY

Register 9.14. SYSTIMER_TARGET0_HI_REG (0x001C)



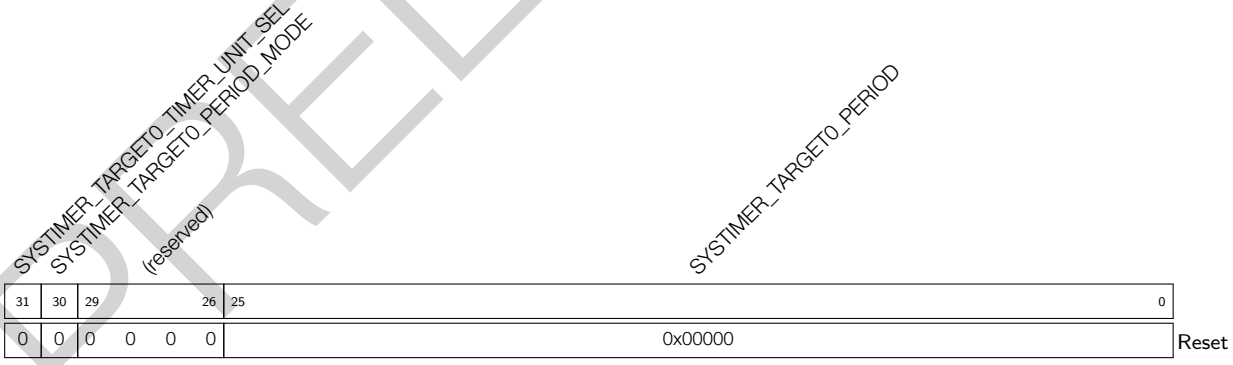
SYSTIMER_TIMER_TARGET0_HI The alarm value to be loaded to COMP0, high 20 bits. (R/W)

Register 9.15. SYSTIMER_TARGET0_LO_REG (0x0020)



SYSTIMER_TIMER_TARGET0_LO The alarm value to be loaded to COMP0, low 32 bits. (R/W)

Register 9.16. SYSTIMER_TARGET0_CONF_REG (0x0034)



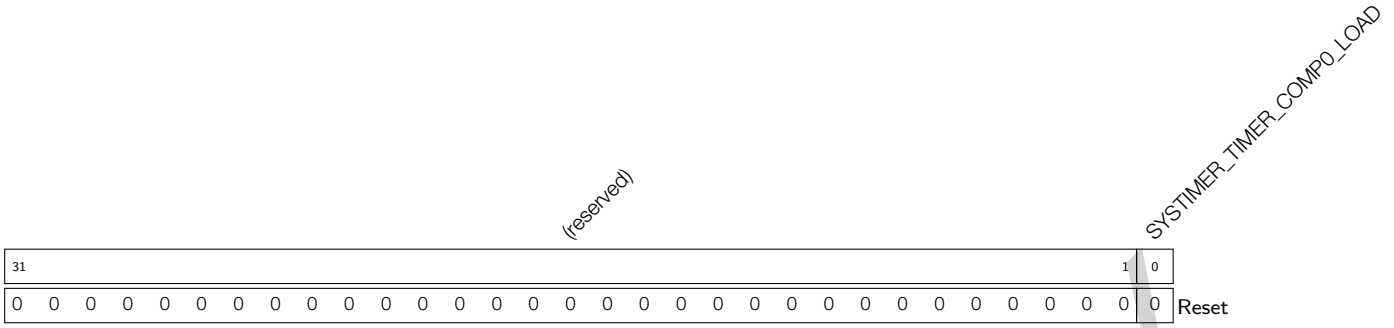
SYSTIMER_TARGET0_PERIOD COMP0 alarm period. (R/W)

SYSTIMER_TARGET0_PERIOD_MODE Set COMP0 to period mode. (R/W)

SYSTIMER_TARGET0_TIMER_UNIT_SEL Select which counter unit to compare for COMP0. (R/W)

PRELIMINARY

Register 9.17. SYSTIMER_COMP0_LOAD_REG (0x0050)



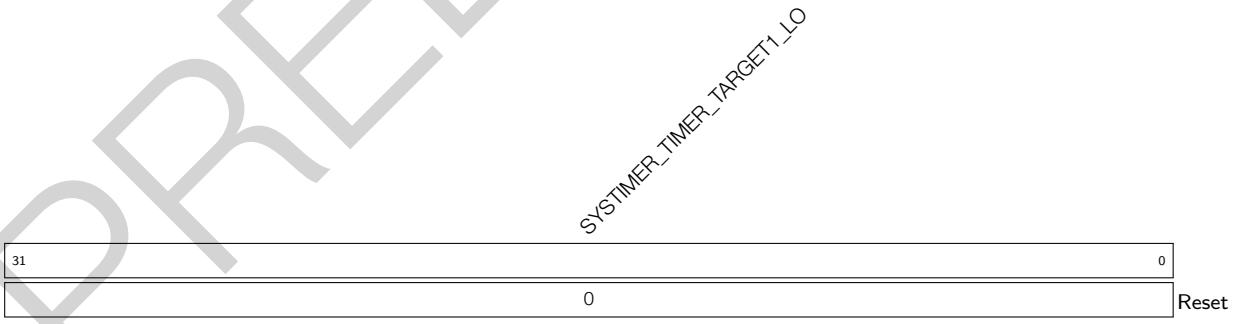
SYSTIMER_TIMER_COMP0_LOAD COMP0 synchronization enable signal. Set this bit to reload the alarm value/period to COMP0. (WT)

Register 9.18. SYSTIMER_TARGET1_HI_REG (0x0024)



SYSTIMER_TIMER_TARGET1_HI The alarm value to be loaded to COMP1, high 20 bits. (R/W)

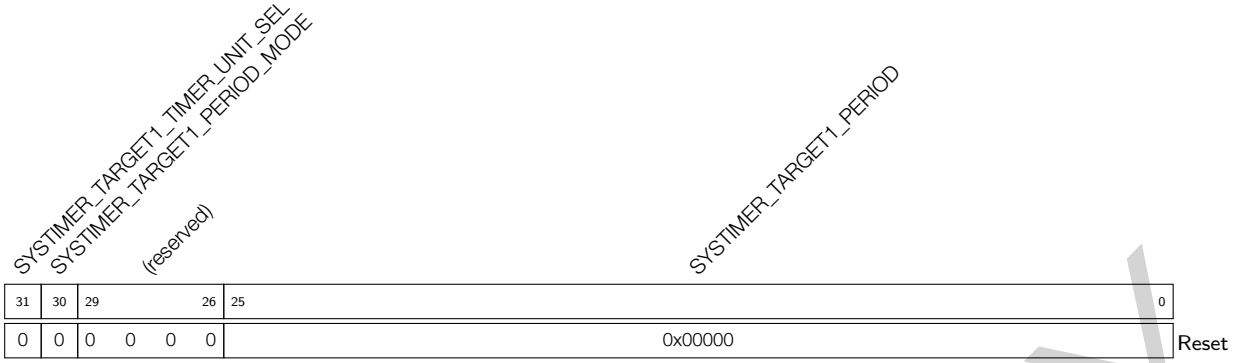
Register 9.19. SYSTIMER_TARGET1_LO_REG (0x0028)



SYSTIMER_TIMER_TARGET1_LO The alarm value to be loaded to COMP1, low 32 bits. (R/W)

PRELIMINARY

Register 9.20. SYSTIMER_TARGET1_CONF_REG (0x0038)

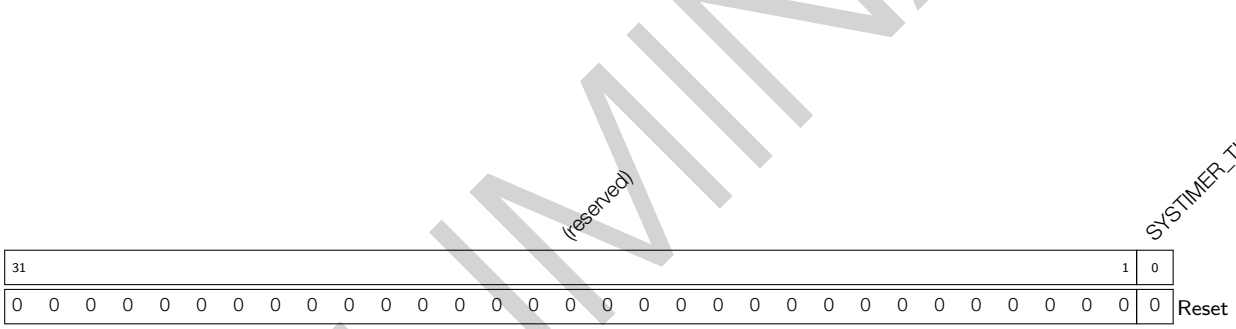


SYSTIMER_TARGET1_PERIOD COMP1 alarm period. (R/W)

SYSTIMER_TARGET1_PERIOD_MODE Set COMP1 to period mode. (R/W)

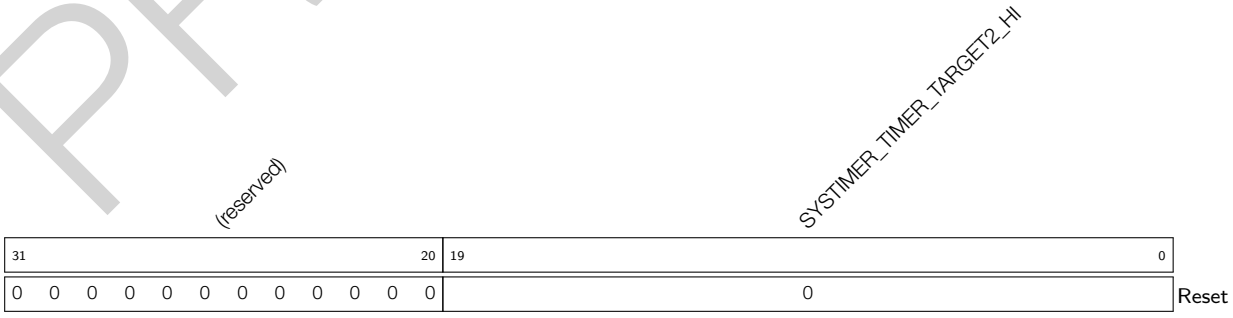
SYSTIMER_TARGET1_TIMER_UNIT_SEL Select which counter unit to compare for COMP1. (R/W)

Register 9.21. SYSTIMER_COMP1_LOAD_REG (0x0054)



SYSTIMER_TIMER_COMP1_LOAD COMP1 synchronization enable signal. Set this bit to reload the alarm value/period to COMP1. (WT)

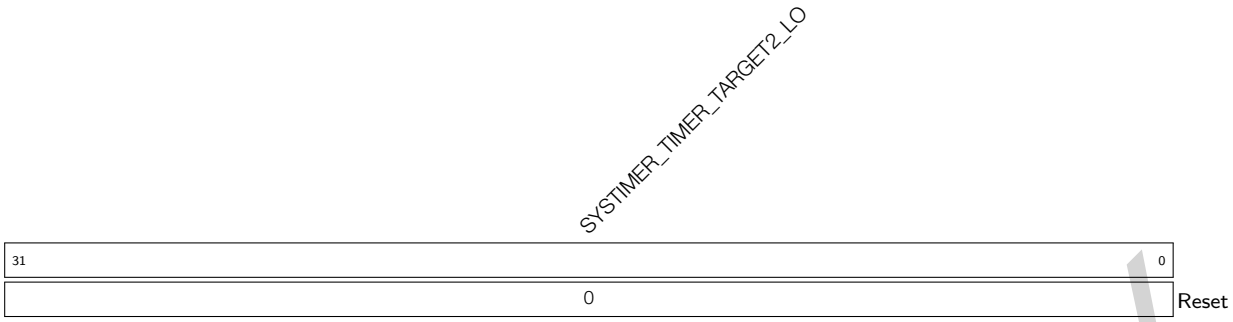
Register 9.22. SYSTIMER_TARGET2_HI_REG (0x002C)



SYSTIMER_TIMER_TARGET2_HI The alarm value to be loaded to COMP2, high 20 bits. (R/W)

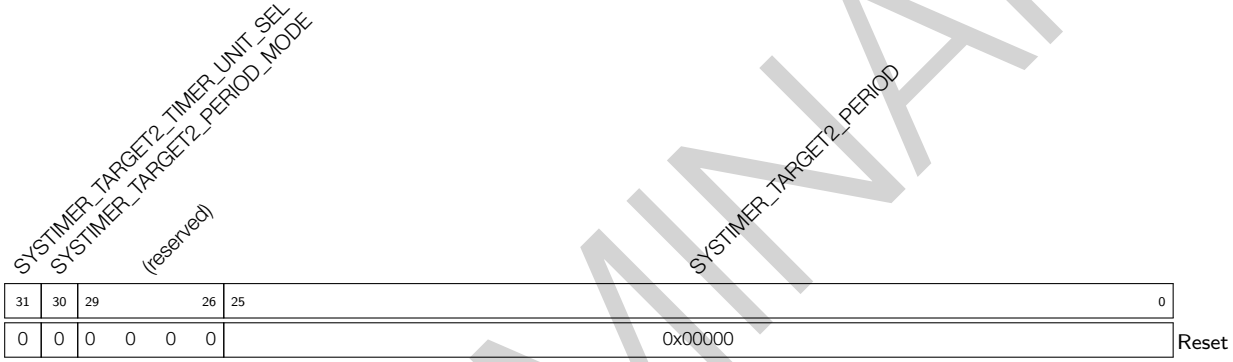
PRELIMINARY

Register 9.23. SYSTIMER_TARGET2_LO_REG (0x0030)



SYSTIMER_TIMER_TARGET2_LO The alarm value to be loaded to COMP2, low 32 bits. (R/W)

Register 9.24. SYSTIMER_TARGET2_CONF_REG (0x003C)

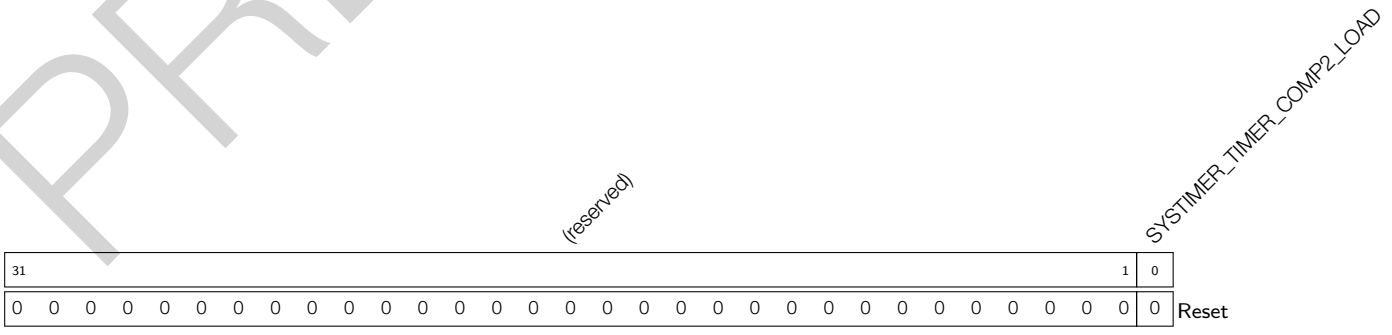


SYSTIMER_TARGET2_PERIOD COMP2 alarm period. (R/W)

SYSTIMER_TARGET2_PERIOD_MODE Set COMP2 to period mode. (R/W)

SYSTIMER_TARGET2_TIMER_UNIT_SEL Select which counter unit to compare for COMP2. (R/W)

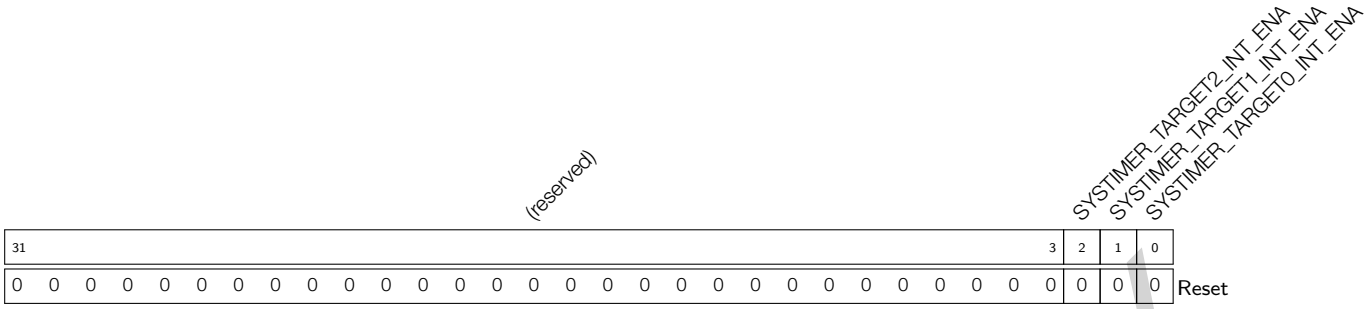
Register 9.25. SYSTIMER_COMP2_LOAD_REG (0x0058)



SYSTIMER_TIMER_COMP2_LOAD COMP2 synchronization enable signal. Set this bit to reload the alarm value/period to COMP2. (WT)

PRELIMINARY

Register 9.26. SYSTIMER_INT_ENA_REG (0x0064)

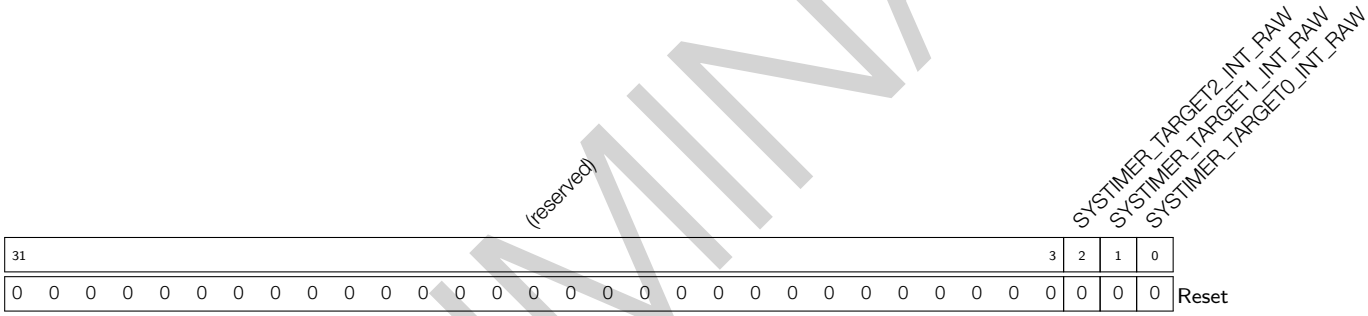


SYSTIMER_TARGET0_INT_ENA SYSTIMER_TARGET0_INT enable bit. (R/W)

SYSTIMER_TARGET1_INT_ENA SYSTIMER_TARGET1_INT enable bit. (R/W)

SYSTIMER_TARGET2_INT_ENA SYSTIMER_TARGET2_INT enable bit. (R/W)

Register 9.27. SYSTIMER_INT_RAW_REG (0x0068)



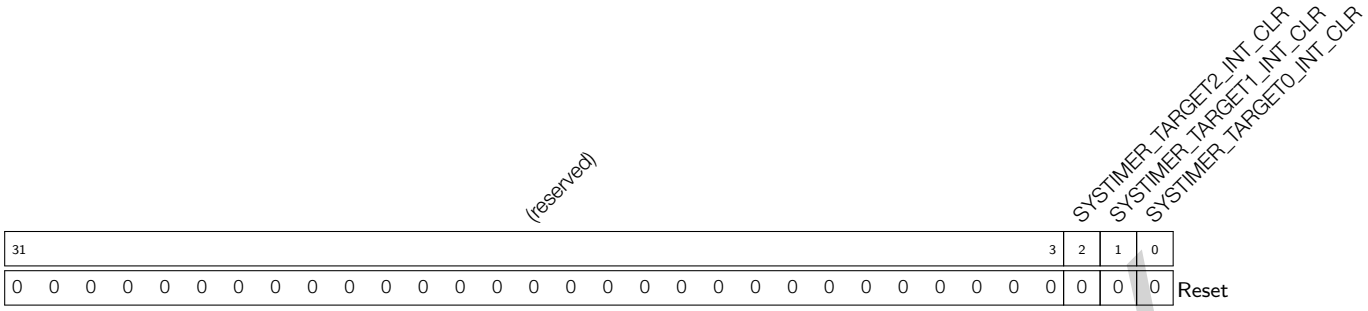
SYSTIMER_TARGET0_INT_RAW SYSTIMER_TARGET0_INT raw bit. (R/WTC/SS)

SYSTIMER_TARGET1_INT_RAW SYSTIMER_TARGET1_INT raw bit. (R/WTC/SS)

SYSTIMER_TARGET2_INT_RAW SYSTIMER_TARGET2_INT raw bit. (R/WTC/SS)

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Register 9.28. SYSTIMER_INT_CLR_REG (0x006C)

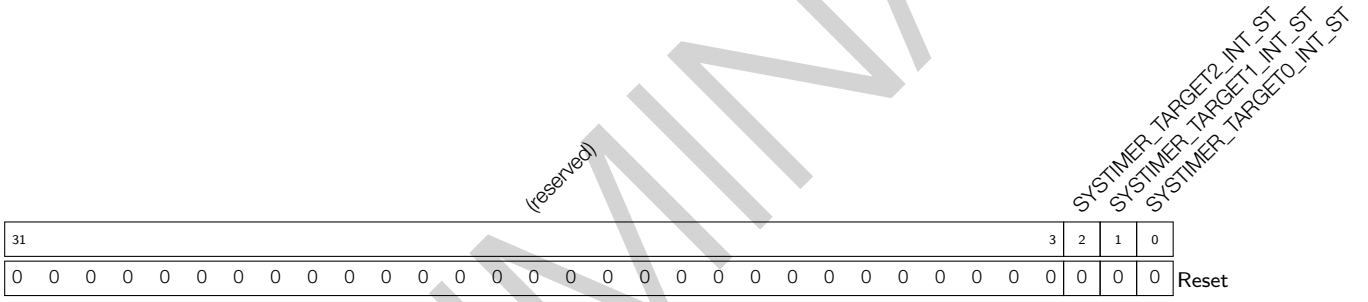


SYSTIMER_TARGET0_INT_CLR SYSTIMER_TARGET0_INT clear bit. (WT)

SYSTIMER_TARGET1_INT_CLR SYSTIMER_TARGET1_INT clear bit. (WT)

SYSTIMER_TARGET2_INT_CLR SYSTIMER_TARGET2_INT clear bit. (WT)

Register 9.29. SYSTIMER_INT_ST_REG (0x0070)

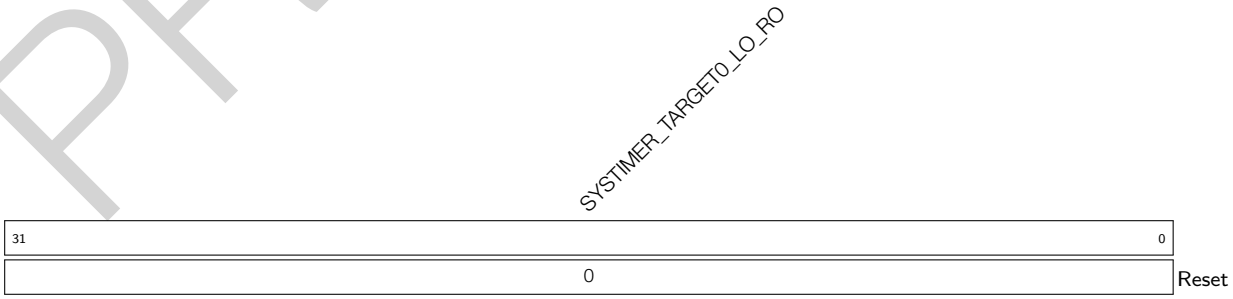


SYSTIMER_TARGET0_INT_ST SYSTIMER_TARGET0_INT status bit. (RO)

SYSTIMER_TARGET1_INT_ST SYSTIMER_TARGET1_INT status bit. (RO)

SYSTIMER_TARGET2_INT_ST SYSTIMER_TARGET2_INT status bit. (RO)

Register 9.30. SYSTIMER_REAL_TARGET0_LO_REG (0x0074)



SYSTIMER_TARGET0_LO_RO Actual target value of COMP0, low 32 bits. (RO)

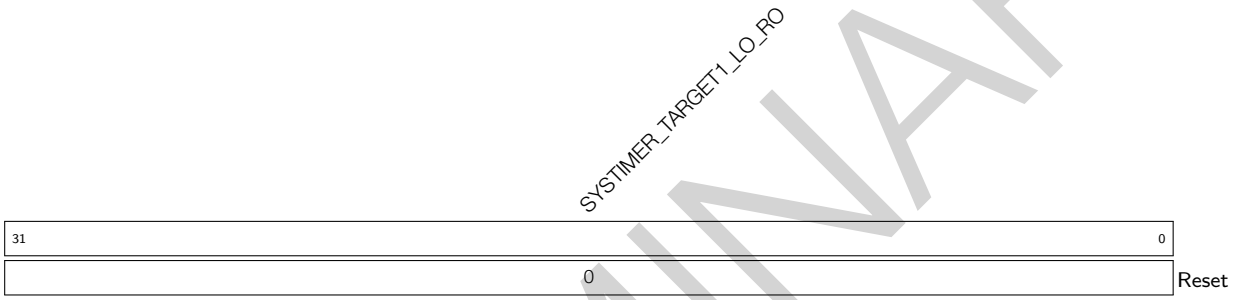
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Register 9.31. SYSTIMER_REAL_TARGET0_HI_REG (0x0078)



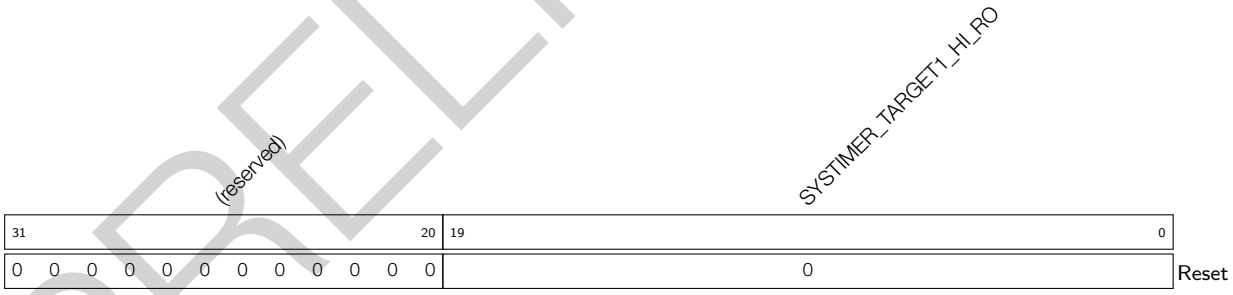
SYSTIMER_TARGET0_HI_RO Actual target value of COMP0, high 20 bits. (RO)

Register 9.32. SYSTIMER_REAL_TARGET1_LO_REG (0x007C)



SYSTIMER_TARGET1_LO_RO Actual target value of COMP1, low 32 bits. (RO)

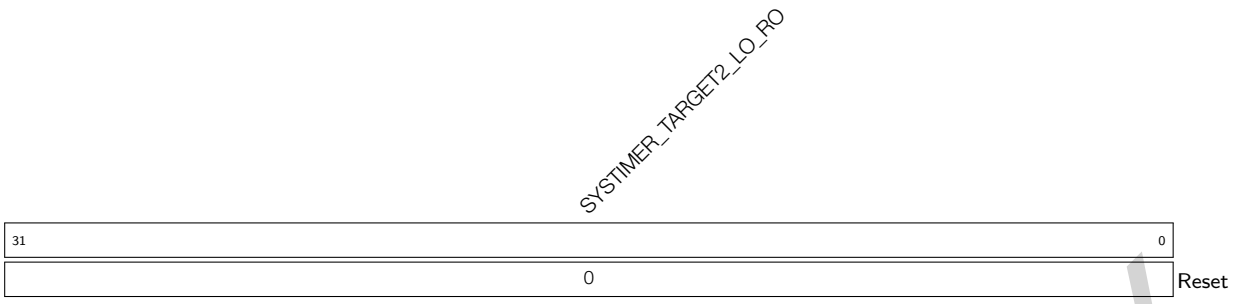
Register 9.33. SYSTIMER_REAL_TARGET1_HI_REG (0x0080)



SYSTIMER_TARGET1_HI_RO Actual target value of COMP1, high 20 bits. (RO)

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Register 9.34. SYSTIMER_REAL_TARGET2_LO_REG (0x0084)



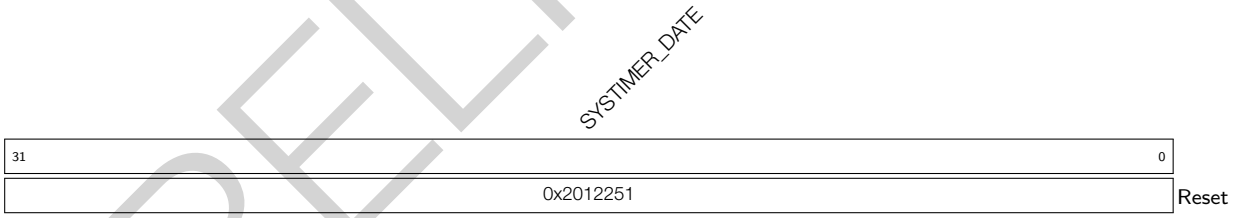
SYSTIMER_TARGET2_LO_RO Actual target value of COMP2, low 32 bits. (RO)

Register 9.35. SYSTIMER_REAL_TARGET2_HI_REG (0x0088)



SYSTIMER_TARGET2_HI_RO Actual target value of COMP2, high 20 bits. (RO)

Register 9.36. SYSTIMER_DATE_REG (0x00FC)



SYSTIMER_DATE Version control register. (R/W)

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10 Timer Group (TIMG)

10.1 Overview

General purpose timers can be used to precisely time an interval, trigger an interrupt after a particular interval (periodically and aperiodically), or act as a hardware clock. As shown in Figure 10-1, the ESP32-S3 chip contains two timer groups, namely timer group 0 and timer group 1. Each timer group consists of two general purpose timers referred to as T*x* (where *x* is 0 or 1) and one Main System Watchdog Timer. All general purpose timers are based on 16-bit prescalers and 54-bit auto-reload-capable up-down counters.

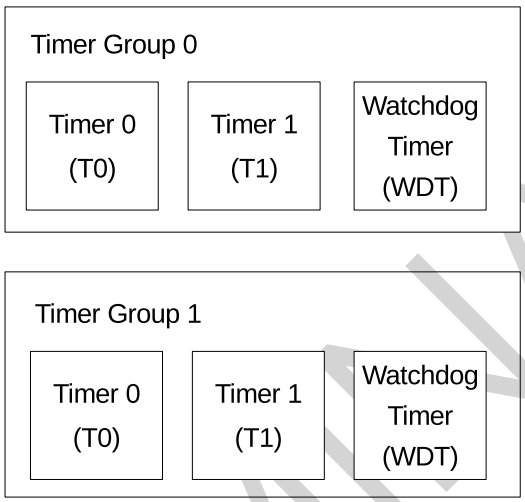


Figure 10-1. Timer Units within Groups

Note that while the Main System Watchdog Timer registers are described in this chapter, their functional description is included in the Chapter 11 *Watchdog Timers (WDT)*. Therefore, the term 'timers' within this chapter refers to the general purpose timers.

The timers' features are summarized as follows:

- A 16-bit clock prescaler, from 2 to 65536
- A 54-bit time-base counter programmable to incrementing or decrementing
- Able to read real-time value of the time-base counter
- Halting and resuming the time-base counter
- Programmable alarm generation
- Timer value reload (Auto-reload at alarm or software-controlled instant reload)
- Level interrupt generation

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10.2 Functional Description

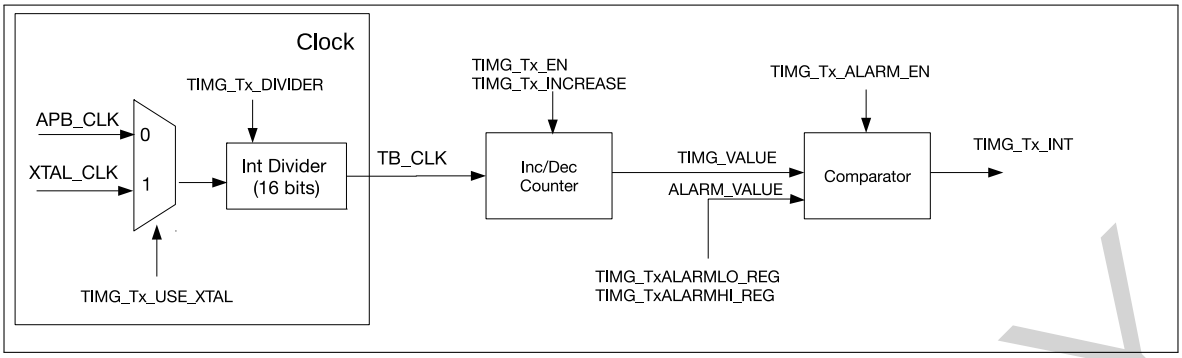


Figure 10-2. Timer Group Architecture

Figure10-2 is a diagram of timer T*x* in a timer group. T*x* contains a clock selector, a 16-bit integer divider as a prescaler, a timer-based counter and a comparator for alarm generation.

10.2.1 16-bit Prescaler and Clock Selection

Each timer can select between the APB clock (APB_CLK) or external clock (XTAL_CLK) as its clock source by setting the TIMG_T*x*_USE_XTAL field of the TIMG_T*x*CONFIG_REG register. The clock is then divided by a 16-bit prescaler to generate the time-base counter clock (TB_CLK) used by the time-base counter. When the TIMG_T*x*_DIVIDER field is configured as 2 ~ 65536, the divisor of the prescaler would be 2 ~ 65536. Note that programming value 0 to TIMG_T*x*_DIVIDER will result in the divisor being 65536. When the prescaler is set to 1, the actual divisor is 2, so the timer counter value represents the half of real time.

Before you modify the 16-bit prescaler, the timer must be disabled (i.e. TIMG_T*x*_EN should be cleared). Otherwise, the result can be unpredictable.

10.2.2 54-bit Time-base Counter

The 54-bit time-base counters are based on TB_CLK and can be configured to increment or decrement via the TIMG_T*x*_INCREASE field. The time-base counter can be enabled or disabled by setting or clearing the TIMG_T*x*_EN field, respectively. When enabled, the time-base counter increments or decrements on each cycle of TB_CLK. When disabled, the time-base counter is essentially frozen. Note that the TIMG_T*x*_INCREASE field can be changed while TIMG_T*x*_EN is set and this will cause the time-base counter to change direction instantly.

To read the 54-bit value of the time-base counter, the timer value must be latched to two registers before being read by the CPU (due to the CPU being 32-bit). By writing any value to the TIMG_T*x*UPDATE_REG, the current value of the 54-bit timer is instantly latched into the TIMG_T*x*LO_REG and TIMG_T*x*HI_REG registers containing the lower 32-bits and higher 22-bits, respectively. TIMG_T*x*LO_REG and TIMG_T*x*HI_REG registers will remain unchanged for the CPU to read in its own time until TIMG_T*x*UPDATE_REG is written to again.

10.2.3 Alarm Generation

A timer can be configured to trigger an alarm when the timer's current value matches the alarm value. An alarm will cause an interrupt to occur and (optionally) an automatic reload of the timer's current value (see Section 10.2.4). The 54-bit alarm value is configured using TIMG_T*x*ALARMLO_REG and TIMG_T*x*ALARMHI_REG, which represent the lower 32-bits and higher 22-bits of the alarm value, respectively. However, the configured

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alarm value is ineffective until the alarm is enabled by setting the TIMG_T*x*_ALARM_EN field. To avoid alarm being enabled 'too late' (i.e. the timer value has already passed the alarm value when the alarm is enabled), the hardware will trigger the alarm immediately if the current timer value is higher than the alarm value (within a defined range) when the up-down counter increments, or lower than the alarm value (within a defined range) of when the up-down counter decrements. Table 10-1 and Table 10-2 show the relationship between the current value of the timer, the alarm value, and when an alarm is triggered.The current time value and the alarm value are defined as follows:

- TIMG_VALUE = {TIMG_T*x*HI_REG, TIMG_T*x*LO_REG}
- ALARM_VALUE = {TIMG_T*x*ALARMHI_REG, TIMG_T*x*ALARMLO_REG}

Table 10-1. Alarm Generation When Up-Down Counter Increments

Scenario	Range	Alarm
1	ALARM_VALUE − TIMG_VALUE $> 2^{53}$	Triggered
2	$0 <$ ALARM_VALUE − TIMG_VALUE $\leq 2^{53}$	Triggered when the up-down counter counts TIMG_VALUE up to ALARM_VALUE
3	$0 \leq$ TIMG_VALUE − ALARM_VALUE $< 2^{53}$	Triggered
4	TIMG_VALUE − ALARM_VALUE $\geq 2^{53}$	Triggered when the up-down counter restarts counting up from 0 after reaching the timer's maximum value and counts TIMG_VALUE up to ALARM_VALUE

Table 10-2. Alarm Generation When Up-Down Counter Decrements

Scenario	Range	Alarm
5	TIMG_VALUE − ALARM_VALUE $> 2^{53}$	Triggered
6	$0 <$ TIMG_VALUE − ALARM_VALUE $\leq 2^{53}$	Triggered when the up-down counter counts TIMG_VALUE down to ALARM_VALUE
7	$0 \leq$ ALARM_VALUE − TIMG_VALUE $< 2^{53}$	Triggered
8	ALARM_VALUE − TIMG_VALUE $\geq 2^{53}$	Triggered when the up-down counter restarts counting down from the timer's maximum value after reaching the minimum value and counts TIMG_VALUE down to ALARM_VALUE

When an alarm occurs, the TIMG_T*x*_ALARM_EN field is automatically cleared and no alarm will occur again until the TIMG_T*x*_ALARM_EN is set next time.

10.2.4 Timer Reload

A timer is reloaded when a timer's current value is overwritten with a reload value stored in the TIMG_T*x*_LOAD_LO and TIMG_T*x*_LOAD_HI fields that correspond to the lower 32-bits and higher 22-bits of the timer's new value, respectively. However, writing a reload value to TIMG_T*x*_LOAD_LO and TIMG_T*x*_LOAD_HI will not cause the timer's current value to change. Instead, the reload value is ignored by the timer until a reload event occurs. A reload event can be triggered either by a software instant reload or an auto-reload at alarm.

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A software instant reload is triggered by the CPU writing any value to TIMG_TxLOAD_REG, which causes the timer's current value to be instantly reloaded. If TIMG_Tx_EN is set, the timer will continue incrementing or decrementing from the new value. If TIMG_Tx_EN is cleared, the timer will remain frozen at the new value until counting is re-enabled.

An auto-reload at alarm will cause a timer reload when an alarm occurs, thus allowing the timer to continue incrementing or decrementing from the reload value. This is generally useful for resetting the timer's value when using periodic alarms. To enable auto-reload at alarm, the TIMG_Tx_AUTORELOAD field should be set. If not enabled, the timer's value will continue to increment or decrement past the alarm value after an alarm.

10.2.5 SLOW_CLK Frequency Calculation

Via XTAL_CLK, a timer could calculate the frequency of clock sources for SLOW_CLK (i.e. RTC_CLK, FOSC_DIV_CLK, and XTAL32K_CLK) as follows:

1. Start periodic or one-shot frequency calculation;
2. Once receiving the signal to start calculation, the counter of XTAL_CLK and the counter of SLOW_CLK begin to work at the same time. When the counter of SLOW_CLK counts to C0, the two counters stop counting simultaneously;
3. Assume the value of XTAL_CLK's counter is C1, and the frequency of SLOW_CLK would be calculated as: $f\_rtc = \frac{C0 \times f\_XTAL\_CLK}{C1}$

10.2.6 Interrupts

Each timer has its own interrupt line that can be routed to the CPU, and thus each timer group has a total of three interrupt lines. Timers generate level interrupts that must be explicitly cleared by the CPU on each triggering.

Interrupts are triggered after an alarm (or stage timeout for watchdog timers) occurs. Level interrupts will be held high after an alarm (or stage timeout) occurs, and will remain so until manually cleared. To enable a timer's interrupt, the TIMG_Tx_INT_ENA bit should be set.

The interrupts of each timer group are governed by a set of registers. Each timer within the group has a corresponding bit in each of these registers:

- TIMG_Tx_INT_RAW : An alarm event sets it to 1. The bit will remain set until the timer's corresponding bit in TIMG_Tx_INT_CLR is written.
- TIMG_WDT_INT_RAW : A stage time out will set the timer's bit to 1. The bit will remain set until the timer's corresponding bit in TIMG_WDT_INT_CLR is written.
- TIMG_Tx_INT_ST : Reflects the status of each timer's interrupt and is generated by masking the bits of TIMG_Tx_INT_RAW with TIMG_Tx_INT_ENA.
- TIMG_WDT_INT_ST : Reflects the status of each watchdog timer's interrupt and is generated by masking the bits of TIMG_WDT_INT_RAW with TIMG_WDT_INT_ENA.
- TIMG_Tx_INT_ENA : Used to enable or mask the interrupt status bits of timers within the group.
- TIMG_WDT_INT_ENA : Used to enable or mask the interrupt status bits of watchdog timer within the group.

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- TIMG_T*x*_INT_CLR : Used to clear a timer's interrupt by setting its corresponding bit to 1. The timer's corresponding bit in TIMG_T*x*_INT_RAW and TIMG_T*x*_INT_ST will be cleared as a result. Note that a timer's interrupt must be cleared before the next interrupt occurs.
- TIMG_WDT_INT_CLR : Used to clear a timer's interrupt by setting its corresponding bit to 1. The watchdog timer's corresponding bit in TIMG_WDT_INT_RAW and TIMG_WDT_INT_ST will be cleared as a result. Note that a watchdog timer's interrupt must be cleared before the next interrupt occurs.

10.3 Configuration and Usage

10.3.1 Timer as a Simple Clock

1. Configure the time-base counter
   - Select clock source by setting or clearing TIMG_T*x*_USE_XTAL field.
   - Configure the 16-bit prescaler by setting TIMG_T*x*_DIVIDER.
   - Configure the timer direction by setting or clearing TIMG_T*x*_INCREASE.
   - Set the timer's starting value by writing the starting value to TIMG_T*x*_LOAD_LO and TIMG_T*x*_LOAD_HI, then reloading it into the timer by writing any value to TIMG_T*x*LOAD_REG.
2. Start the timer by setting TIMG_T*x*_EN.
3. Get the timer's current value.
   - Write any value to TIMG_T*x*UPDATE_REG to latch the timer's current value.
   - Read the latched timer value from TIMG_T*x*LO_REG and TIMG_T*x*HI_REG.

10.3.2 Timer as One-shot Alarm

1. Configure the time-base counter following step 1 of Section 10.3.1.
2. Configure the alarm.
   - Configure the alarm value by setting TIMG_T*x*ALARMLO_REG and TIMG_T*x*ALARMHI_REG.
   - Enable interrupt by setting TIMG_T*x*_INT_ENA.
3. Disable auto reload by clearing TIMG_T*x*_AUTORELOAD.
4. Start the alarm by setting TIMG_T*x*_ALARM_EN.
5. Handle the alarm interrupt.
   - Clear the interrupt by setting the timer's corresponding bit in TIMG_T*x*_INT_CLR.
   - Disable the timer by clearing TIMG_T*x*_EN.

10.3.3 Timer as Periodic Alarm

1. Configure the time-base counter following step 1 in Section 10.3.1.
2. Configure the alarm following step 2 in Section 10.3.2.
3. Enable auto reload by setting TIMG_T*x*_AUTORELOAD and configure the reload value via TIMG_T*x*_LOAD_LO and TIMG_T*x*_LOAD_HI.

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4. Start the alarm by setting TIMG_T*x*_ALARM_EN.
5. Handle the alarm interrupt (repeat on each alarm iteration).
   - Clear the interrupt by setting the timer's corresponding bit in TIMG_T*x*_INT_CLR.
   - If the next alarm requires a new alarm value and reload value (i.e. different alarm interval per iteration), then TIMG_T*x*ALARMLO_REG, TIMG_T*x*ALARMHI_REG, TIMG_T*x*_LOAD_LO, and TIMG_T*x*_LOAD_HI should be reconfigured as needed. Otherwise, the aforementioned registers should remain unchanged.
   - Re-enable the alarm by setting TIMG_T*x*_ALARM_EN.
6. Stop the timer (on final alarm iteration).
   - Clear the interrupt by setting the timer's corresponding bit in TIMG_T*x*_INT_CLR.
   - Disable the timer by clearing TIMG_T*x*_EN.

10.3.4 SLOW_CLK Frequency Calculation

1. One-shot frequency calculation
   - Select the clock whose frequency is to be calculated (clock source of SLOW_CLK) via TIMG_RTC_CALI_CLK_SEL, and configure the time of calculation via TIMG_RTC_CALI_MAX.
   - Select one-shot frequency calculation by clearing TIMG_RTC_CALI_START_CYCLING, and enable the two counters via TIMG_RTC_CALI_START.
   - Once TIMG_RTC_CALI_RDY becomes 1, read TIMG_RTC_CALI_VALUE to get the value of XTAL_CLK's counter, and calculate the frequency of SLOW_CLK.
2. Periodic frequency calculation
   - Select the clock whose frequency is to be calculated (clock source of SLOW_CLK) via TIMG_RTC_CALI_CLK_SEL, and configure the time of calculation via TIMG_RTC_CALI_MAX.
   - Select periodic frequency calculation by enabling TIMG_RTC_CALI_START_CYCLING.
   - When TIMG_RTC_CALI_CYCLING_DATA_VLD is 1, TIMG_RTC_CALI_VALUE is valid.
3. Timeout
   If the counter of SLOW_CLK cannot finish counting in TIMG_RTC_CALI_TIMEOUT_RST_CNT cycles, TIMG_RTC_CALI_TIMEOUT will be set to indicate a timeout.

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10.4 Register Summary

The addresses in this section are relative to Timer Group base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
Timer 0 configuration and control registers			
TIMG_T0CONFIG_REG	Timer 0 configuration register	0x0000	varies
TIMG_T0LO_REG	Timer 0 current value, low 32 bits	0x0004	RO
TIMG_T0HI_REG	Timer 0 current value, high 22 bits	0x0008	RO
TIMG_T0UPDATE_REG	Write to copy current timer value to TIMG_T0LO_REG or TIMG_T0HI_REG	0x000C	R/W/SC
TIMG_T0ALARMLO_REG	Timer 0 alarm value, low 32 bits	0x0010	R/W
TIMG_T0ALARMHI_REG	Timer 0 alarm value, high bits	0x0014	R/W
TIMG_T0LOADLO_REG	Timer 0 reload value, low 32 bits	0x0018	R/W
TIMG_T0LOADHI_REG	Timer 0 reload value, high 22 bits	0x001C	R/W
TIMG_T0LOAD_REG	Write to reload timer from TIMG_T0LOADLO_REG or TIMG_T0LOADHI_REG	0x0020	WT
Timer 1 configuration and control registers			
TIMG_T1CONFIG_REG	Timer 1 configuration register	0x0024	varies
TIMG_T1LO_REG	Timer 1 current value, low 32 bits	0x0028	RO
TIMG_T1HI_REG	Timer 1 current value, high 22 bits	0x002C	RO
TIMG_T1UPDATE_REG	Write to copy current timer value to TIMG_T1LO_REG or TIMG_T1HI_REG	0x0030	R/W/SC
TIMG_T1ALARMLO_REG	Timer 1 alarm value, low 32 bits	0x0034	R/W
TIMG_T1ALARMHI_REG	Timer 1 alarm value, high bits	0x0038	R/W
TIMG_T1LOADLO_REG	Timer 1 reload value, low 32 bits	0x003C	R/W
TIMG_T1LOADHI_REG	Timer 1 reload value, high 22 bits	0x0040	R/W
TIMG_T1LOAD_REG	Write to reload timer from TIMG_T1LOADLO_REG or TIMG_T1LOADHI_REG	0x0044	WT
Configuration and control registers for WDT			
TIMG_WDTCONFIG0_REG	Watchdog timer configuration register	0x0048	R/W
TIMG_WDTCONFIG1_REG	Watchdog timer prescaler register	0x004C	R/W
TIMG_WDTCONFIG2_REG	Watchdog timer stage 0 timeout value	0x0050	R/W
TIMG_WDTCONFIG3_REG	Watchdog timer stage 1 timeout value	0x0054	R/W
TIMG_WDTCONFIG4_REG	Watchdog timer stage 2 timeout value	0x0058	R/W
TIMG_WDTCONFIG5_REG	Watchdog timer stage 3 timeout value	0x005C	R/W
TIMG_WDTFEED_REG	Write to feed the watchdog timer	0x0060	WT
TIMG_WDTWPROTECT_REG	Watchdog write protect register	0x0064	R/W
Configuration and control registers for RTC frequency calculation			
TIMG_RTCCALICFG_REG	RTC frequency calculation configuration register 0	0x0068	varies

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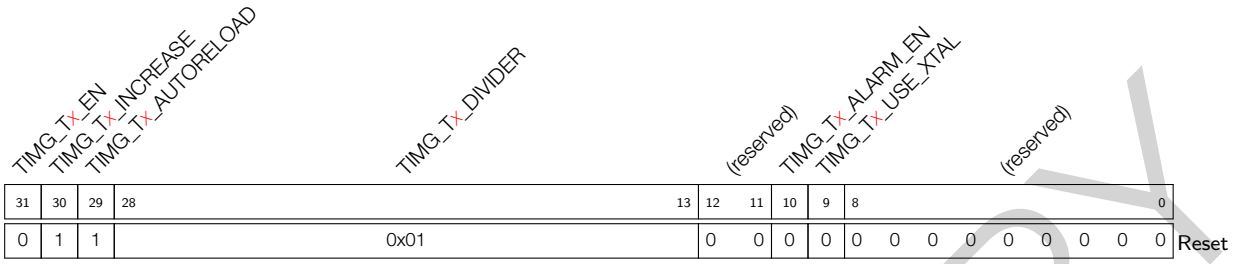
Name	Description	Address	Access
TIMG_RTCCALICFG1_REG	RTC frequency calculation configuration register 1	0x006C	RO
TIMG_RTCCALICFG2_REG	RTC frequency calculation calibration register 2	0x0080	varies
Interrupt registers			
TIMG_INT_ENA_TIMERS_REG	Interrupt enable bits	0x0070	R/W
TIMG_INT_RAW_TIMERS_REG	Raw interrupt status	0x0074	R/WTC/SS
TIMG_INT_ST_TIMERS_REG	Masked interrupt status	0x0078	RO
TIMG_INT_CLR_TIMERS_REG	Interrupt clear bits	0x007C	WT
Version register			
TIMG_NTIMERS_DATE_REG	Timer version control register	0x00F8	R/W
Timer group configuration registers			
TIMG_REGCLK_REG	Timer group clock gate register	0x00FC	R/W

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10.5 Registers

The addresses in this section are relative to Timer Group base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 10.1. TIMG_TxCONFIG_REG (x: 0-1) (0x0000+0x24*x)



TIMG_Tx_USE_XTAL 0: Use APB_CLK as the source clock of timer group; 1: Use XTAL_CLK as the source clock of timer group. (R/W)

TIMG_Tx_ALARM_EN When set, the alarm is enabled. This bit is automatically cleared once an alarm occurs. (R/W/SC)

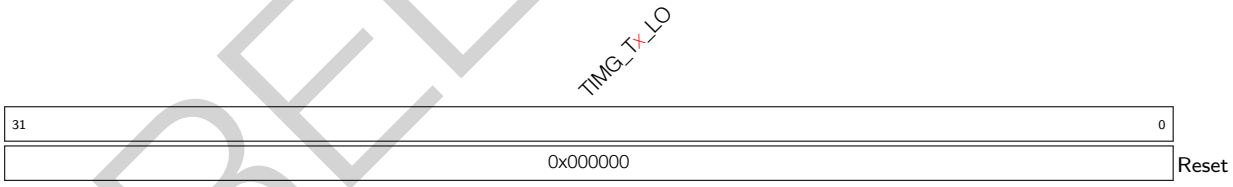
TIMG_Tx_DIVIDER Timer *x* clock (Tx_clk) prescaler value. (R/W)

TIMG_Tx_AUTORELOAD When set, timer *x* auto-reload at alarm is enabled. (R/W)

TIMG_Tx_INCREASE When set, the timer *x* time-base counter will increment every clock tick. When cleared, the timer *x* time-base counter will decrement. (R/W)

TIMG_Tx_EN When set, the timer *x* time-base counter is enabled. (R/W)

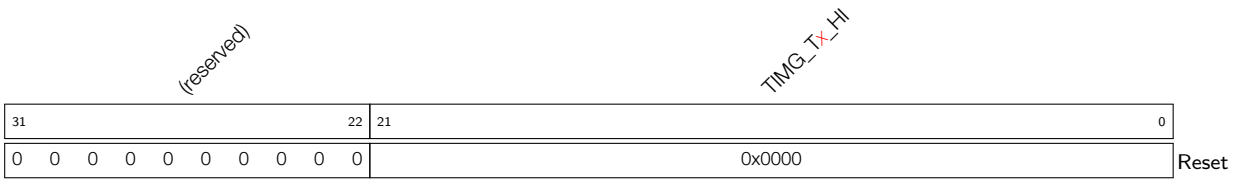
Register 10.2. TIMG_TxLO_REG (x: 0-1) (0x0004+0x24*x)



TIMG_Tx_LO After writing to TIMG_TxUPDATE_REG, the low 32 bits of the time-base counter of timer *x* can be read here. (RO)

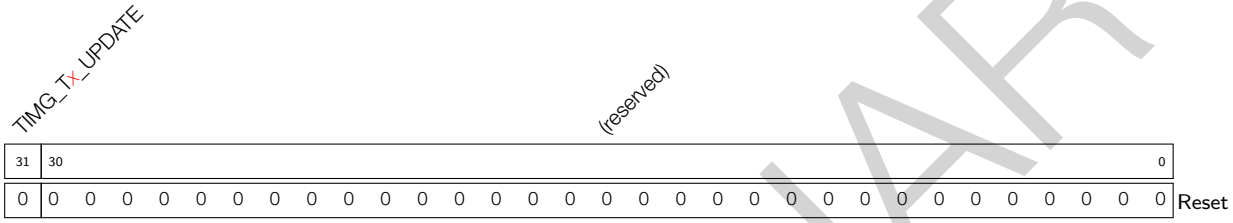
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Register 10.3. TIMG_TxHI_REG (x: 0-1) (0x0008+0x24*x)



TIMG_Tx_HI After writing to TIMG_TxUPDATE_REG, the high 22 bits of the time-base counter of timer *x* can be read here. (RO)

Register 10.4. TIMG_TxUPDATE_REG (x: 0-1) (0x000C+0x24*x)



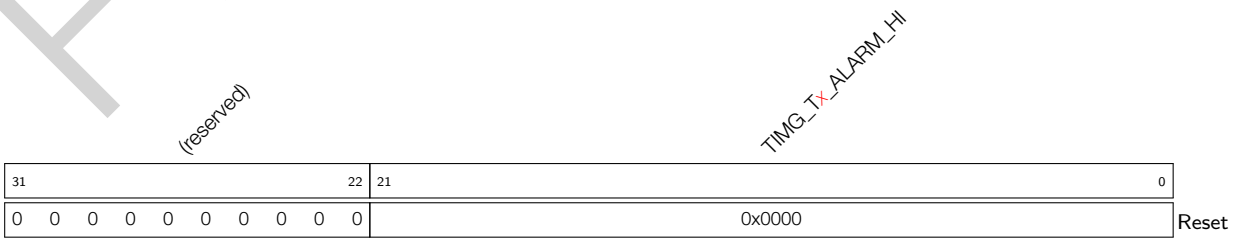
TIMG_Tx_UPDATE After writing 0 or 1 to TIMG_TxUPDATE_REG, the counter value is latched. (R/W/SC)

Register 10.5. TIMG_TxALARMLO_REG (x: 0-1) (0x0010+0x24*x)



TIMG_Tx_ALARM_LO Timer *x* alarm trigger time-base counter value, low 32 bits. (R/W)

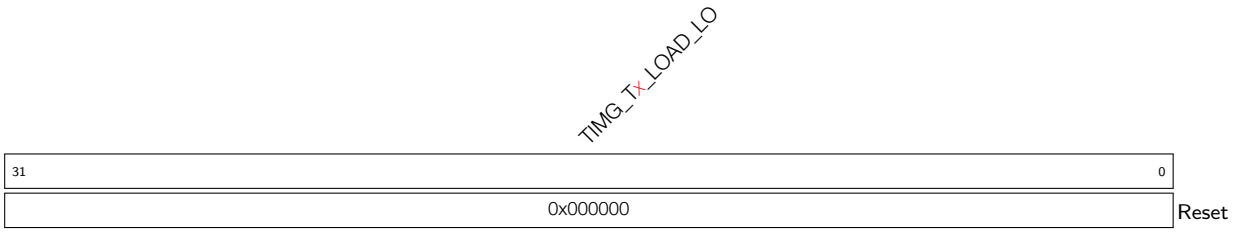
Register 10.6. TIMG_TxALARMHI_REG (x: 0-1) (0x0014+0x24*x)



TIMG_Tx_ALARM_HI Timer *x* alarm trigger time-base counter value, high 22 bits. (R/W)

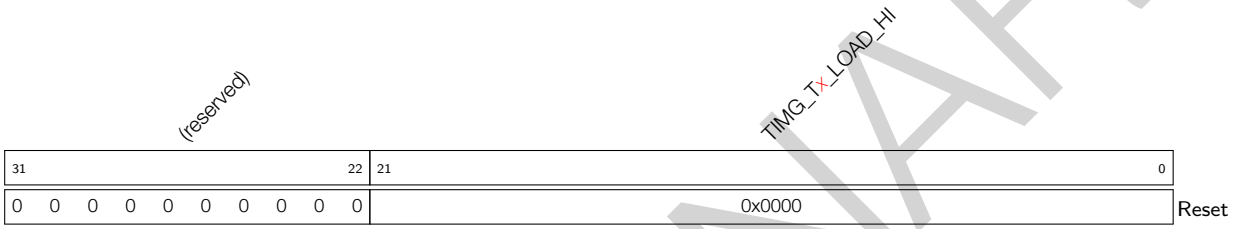
PRELIMINARY

Register 10.7. TIMG_TxLOADLO_REG (x: 0-1) (0x0018+0x24*x)



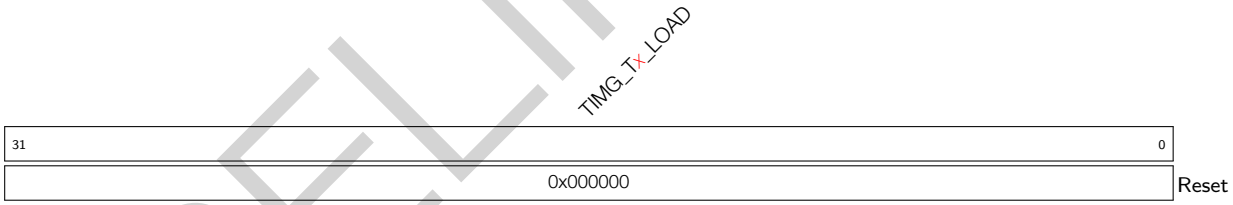
TIMG_Tx_LOAD_LO Low 32 bits of the value that a reload will load onto timer *x* time-base counter. (R/W)

Register 10.8. TIMG_TxLOADHI_REG (x: 0-1) (0x001C+0x24*x)



TIMG_Tx_LOAD_HI High 22 bits of the value that a reload will load onto timer *x* time-base counter. (R/W)

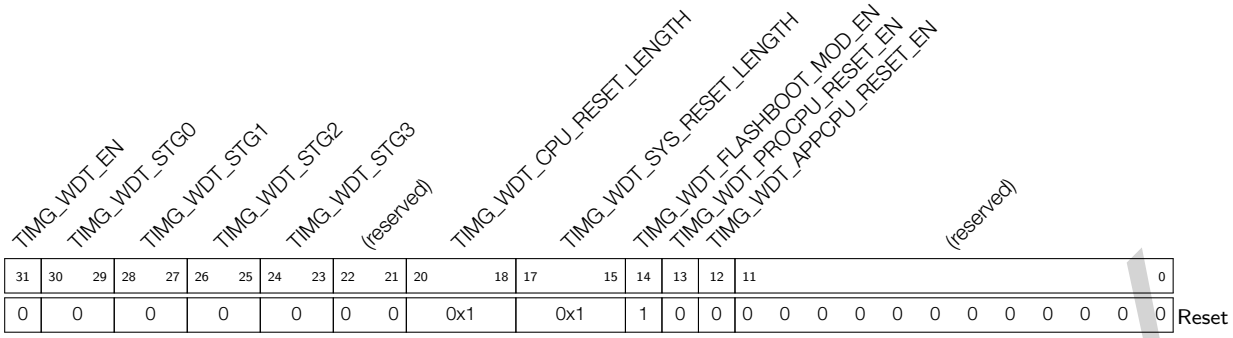
Register 10.9. TIMG_TxLOAD_REG (x: 0-1) (0x0020+0x24*x)



TIMG_Tx_LOAD Write any value to trigger a timer *x* time-base counter reload. (WT)

PRELIMINARY

Register 10.10. TIMG_WDTCONFIG0_REG (0x0048)



TIMG_WDT_APPCPU_RESET_EN Reserved. (R/W)

TIMG_WDT_PROCPU_RESET_EN WDT reset CPU enable. (R/W)

TIMG_WDT_FLASHBOOT_MOD_EN When set, Flash boot protection is enabled. (R/W)

TIMG_WDT_SYS_RESET_LENGTH System reset signal length selection. 0: 100 ns; 1: 200 ns; 2: 300 ns; 3: 400 ns; 4: 500 ns; 5: 800 ns; 6: 1.6 μs; 7: 3.2 μs. (R/W)

TIMG_WDT_CPU_RESET_LENGTH CPU reset signal length selection. 0: 100 ns; 1: 200 ns; 2: 300 ns; 3: 400 ns; 4: 500 ns; 5: 800 ns; 6: 1.6 μs; 7: 3.2 μs. (R/W)

TIMG_WDT_STG3 Stage 3 configuration. 0: off; 1: interrupt; 2: reset CPU; 3: reset system. (R/W)

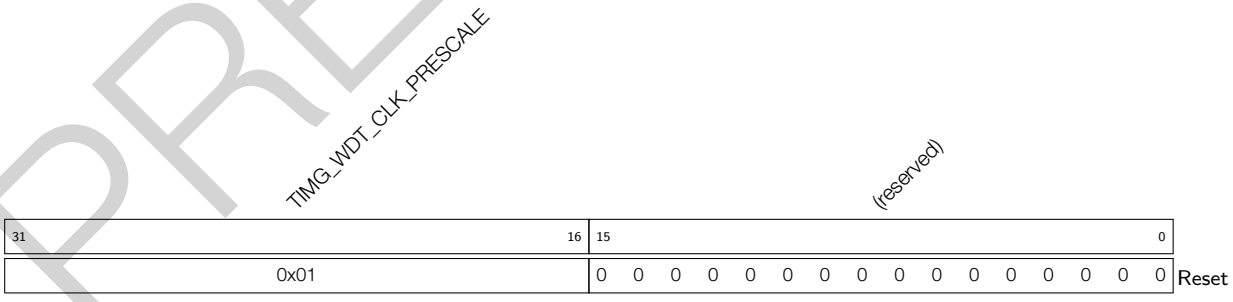
TIMG_WDT_STG2 Stage 2 configuration. 0: off; 1: interrupt; 2: reset CPU; 3: reset system. (R/W)

TIMG_WDT_STG1 Stage 1 configuration. 0: off; 1: interrupt; 2: reset CPU; 3: reset system. (R/W)

TIMG_WDT_STG0 Stage 0 configuration. 0: off; 1: interrupt; 2: reset CPU; 3: reset system. (R/W)

TIMG_WDT_EN When set, MWDT is enabled. (R/W)

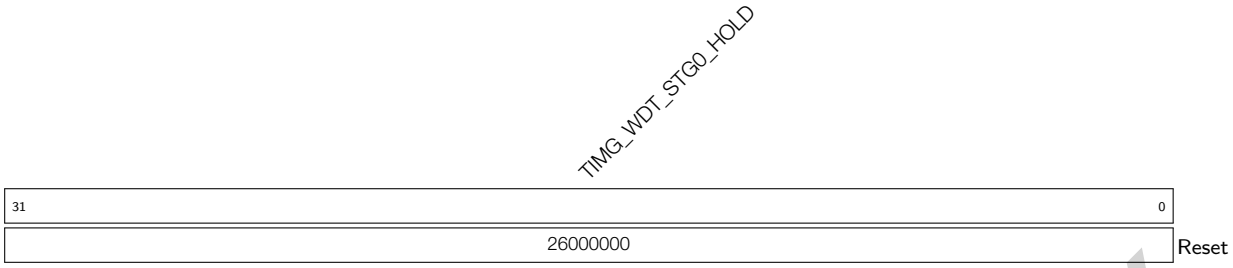
Register 10.11. TIMG_WDTCONFIG1_REG (0x004C)



TIMG_WDT_CLK_PRESCALE MWDT clock prescaler value. MWDT clock period = 12.5 ns * TIMG_WDT_CLK_PRESCALE. (R/W)

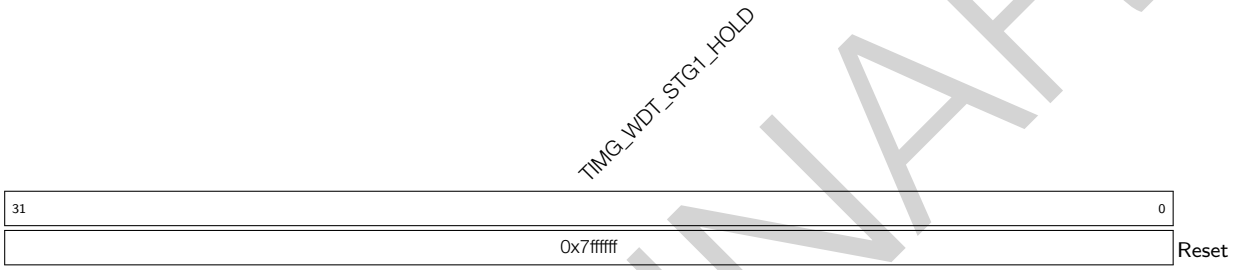
PRELIMINARY

Register 10.12. TIMG_WDTCONFIG2_REG (0x0050)



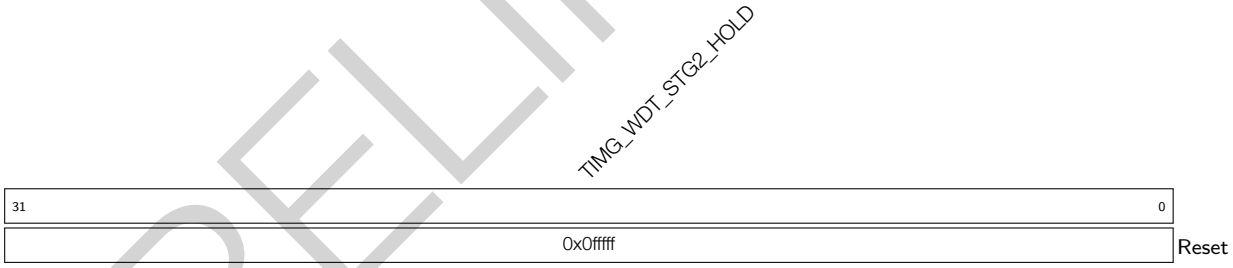
TIMG_WDT_STG0_HOLD Stage 0 timeout value, in MWDT clock cycles. (R/W)

Register 10.13. TIMG_WDTCONFIG3_REG (0x0054)



TIMG_WDT_STG1_HOLD Stage 1 timeout value, in MWDT clock cycles. (R/W)

Register 10.14. TIMG_WDTCONFIG4_REG (0x0058)



TIMG_WDT_STG2_HOLD Stage 2 timeout value, in MWDT clock cycles. (R/W)

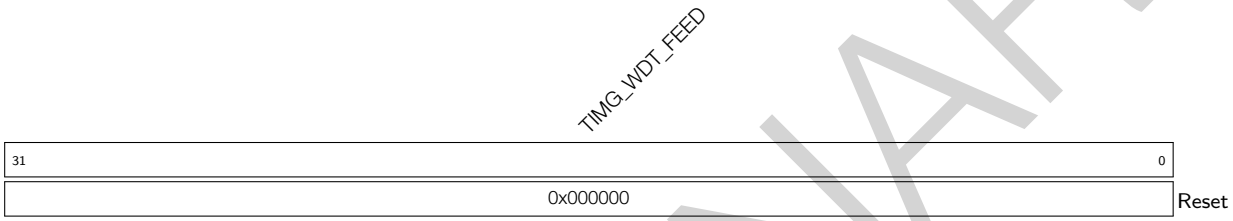
PRELIMINARY

Register 10.15. TIMG_WDTCONFIG5_REG (0x005C)



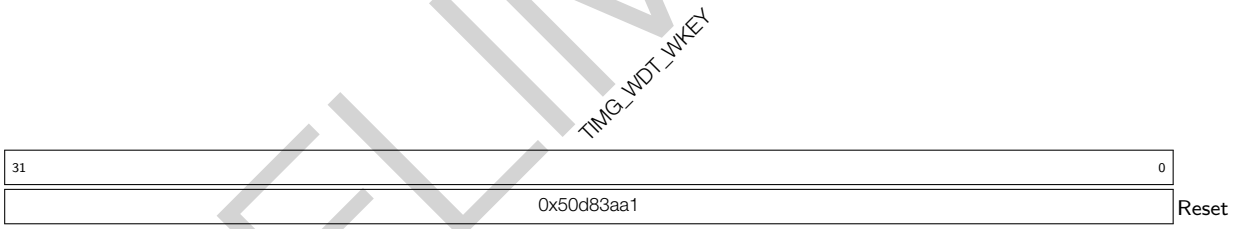
TIMG_WDT_STG3_HOLD Stage 3 timeout value, in MWDT clock cycles. (R/W)

Register 10.16. TIMG_WDTFEED_REG (0x0060)



TIMG_WDT_FEED Write any value to feed the MWDT. (WT)

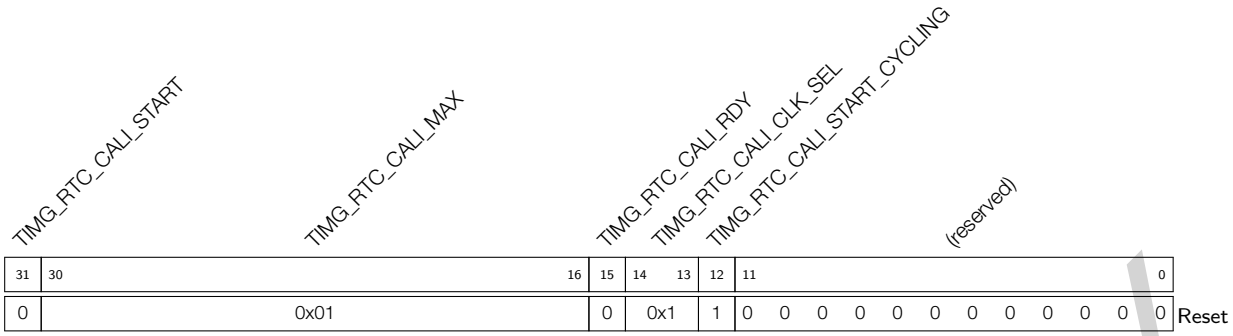
Register 10.17. TIMG_WDTWPROTECT_REG (0x0064)



TIMG_WDT_WKEY If the register contains a different value than its reset value, write protection is enabled. (R/W)

PRELIMINARY

Register 10.18. TIMG_RTCCALICFG_REG (0x0068)



TIMG_RTC_CALI_START_CYCLING Enables periodic frequency calculation. (R/W)

TIMG_RTC_CALI_CLK_SEL Used to select the clock to be calibrated. 0: RTC_CLK; 1: FOSC_DIV_CLK; 2: XTAL32K_CLK. (R/W)

TIMG_RTC_CALI_RDY Marks the completion of one-shot frequency calculation. (RO)

TIMG_RTC_CALI_MAX Configures the time to calculate the frequency of RTC slow clock SLOW_CLK. Measurement unit: SLOW_CLK cycle. (R/W)

TIMG_RTC_CALI_START Enables one-shot frequency calculation. (R/W)

Register 10.19. TIMG_RTCCALICFG1_REG (0x006C)

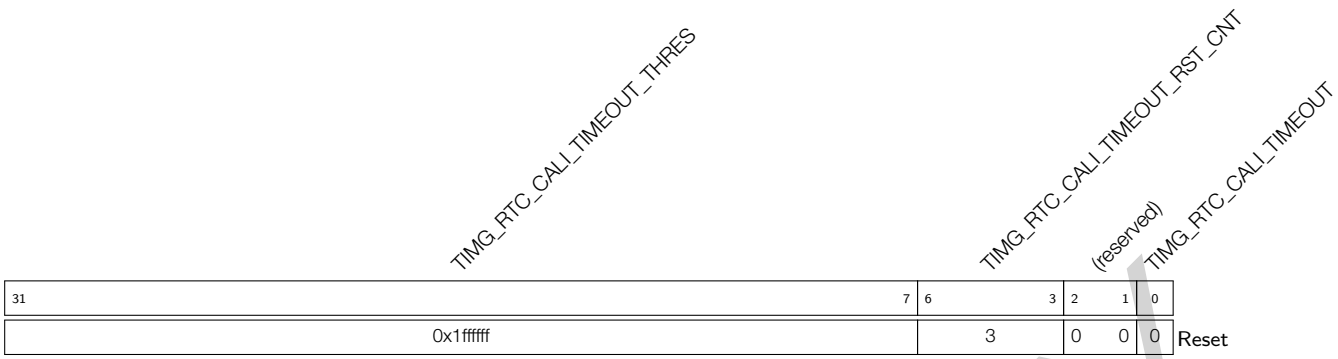


TIMG_RTC_CALI_CYCLING_DATA_VLD Marks the completion of periodic frequency calculation. (RO)

TIMG_RTC_CALI_VALUE When one-shot or periodic frequency calculation completes, read this value to calculate the frequency of RTC slow clock SLOW_CLK. Measurement unit: XTAL_CLK cycle. (RO)

PRELIMINARY

Register 10.20. TIMG_RTCCALICFG2_REG (0x0080)

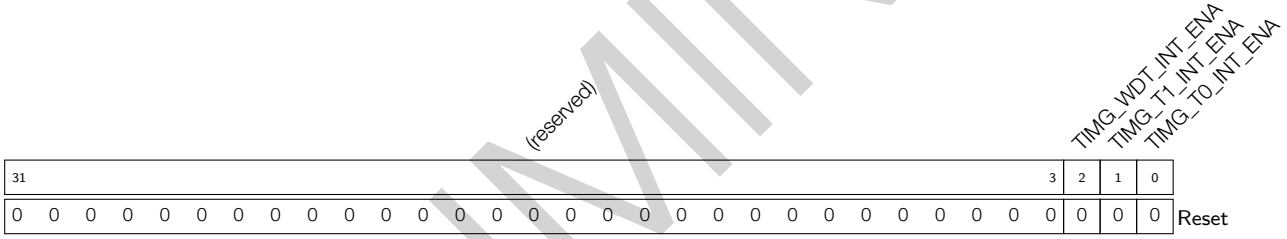


TIMG_RTC_CALI_TIMEOUT Indicates frequency calculation timeout. (RO)

TIMG_RTC_CALI_TIMEOUT_RST_CNT Cycles to reset frequency calculation timeout. (R/W)

TIMG_RTC_CALI_TIMEOUT_THRES Threshold value for the frequency calculation timer. If the timer's value exceeds this threshold, a timeout is triggered. (R/W)

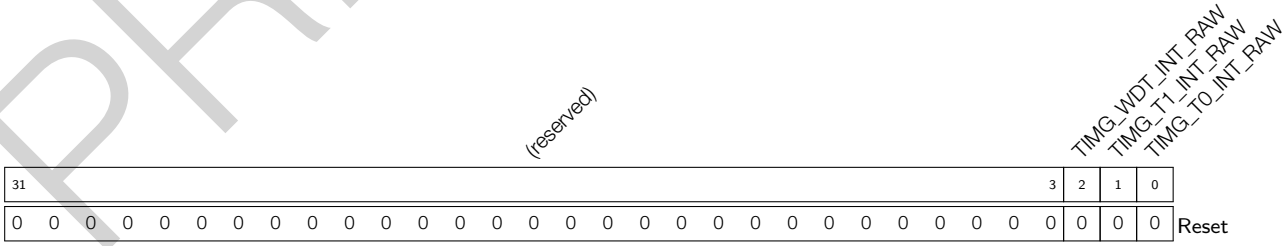
Register 10.21. TIMG_INT_ENA_TIMERS_REG (0x0070)



TIMG_T*x*_INT_ENA The interrupt enable bit for the TIMG_T*x*_INT interrupt. (R/W)

TIMG_WDT_INT_ENA The interrupt enable bit for the TIMG_WDT_INT interrupt. (R/W)

Register 10.22. TIMG_INT_RAW_TIMERS_REG (0x0074)

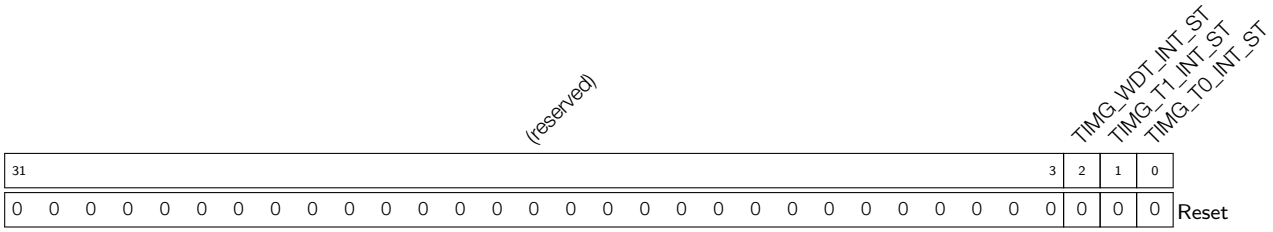


TIMG_T*x*_INT_RAW The raw interrupt status bit for the TIMG_T*x*_INT interrupt. (R/WTC/SS)

TIMG_WDT_INT_RAW The raw interrupt status bit for the TIMG_WDT_INT interrupt. (R/WTC/SS)

PRELIMINARY

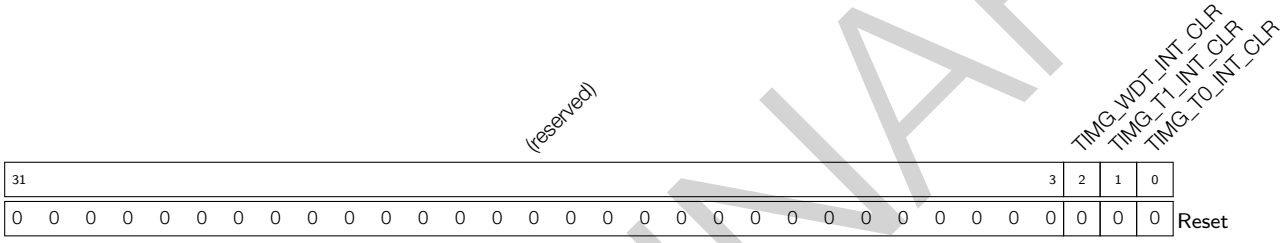
Register 10.23. TIMG_INT_ST_TIMERS_REG (0x0078)



TIMG_T*x*_INT_ST The masked interrupt status bit for the TIMG_T*x*_INT interrupt. (RO)

TIMG_WDT_INT_ST The masked interrupt status bit for the TIMG_WDT_INT interrupt. (RO)

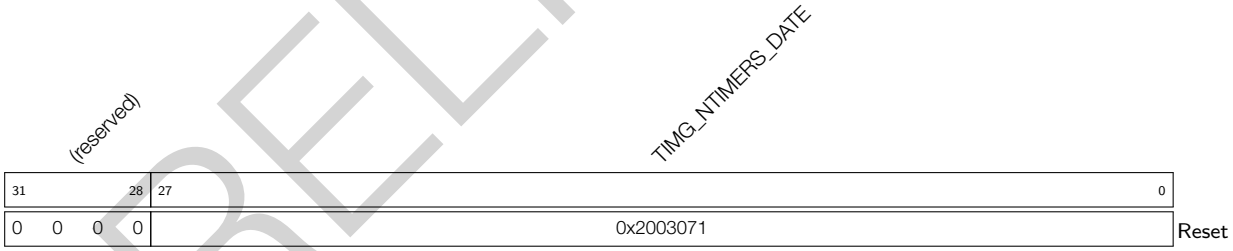
Register 10.24. TIMG_INT_CLR_TIMERS_REG (0x007C)



TIMG_T*x*_INT_CLR Set this bit to clear the TIMG_T*x*_INT interrupt. (WT)

TIMG_WDT_INT_CLR Set this bit to clear the TIMG_WDT_INT interrupt. (WT)

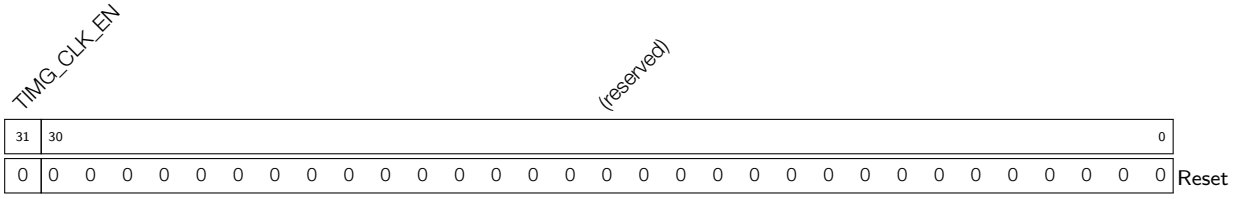
Register 10.25. TIMG_NTIMERS_DATE_REG (0x00F8)



TIMG_NTIMERS_DATE Timer version control register. (R/W)

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Register 10.26. TIMG_REGCLK_REG (0x00FC)



TIMG_CLK_EN Register clock gate signal. 0: The clock used by software to read and write registers is on only when there is software operation. 1: The clock used by software to read and write registers is always on. (R/W)

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11 Watchdog Timers (WDT)

11.1 Overview

Watchdog timers are hardware timers used to detect and recover from malfunctions. They must be periodically fed (reset) to prevent a timeout. A system/software that is behaving unexpectedly (e.g. is stuck in a software loop or in overdue events) will fail to feed the watchdog thus trigger a watchdog timeout. Therefore, watchdog timers are useful for detecting and handling erroneous system/software behavior.

As shown in Figure 11-1, ESP32-S3 contains three digital watchdog timers: one in each of the two timer groups in Chapter 10 *Timer Group (TIMG)*(called Main System Watchdog Timers, or MWDT) and one in the RTC Module (called the RTC Watchdog Timer, or RWDT). Each digital watchdog timer allows for four separately configurable stages and each stage can be programmed to take one action upon expiry, unless the watchdog is fed or disabled. MWDT supports three timeout actions: interrupt, CPU reset, and core reset, while RWDT supports four timeout actions: interrupt, CPU reset, core reset, and system reset (see details in Section 11.2.2.2 *Stages and Timeout Actions*). A timeout value can be set for each stage individually.

During the flash boot process, RWDT and the first MWDT in timergroup 0 are enabled automatically in order to detect and recover from booting errors.

ESP32-S3 also has one analog watchdog timer: Super watchdog (SWD). It is an ultra-low-power circuit in analog domain that helps to prevent the system from operating in a sub-optimal state and resets the system if required.

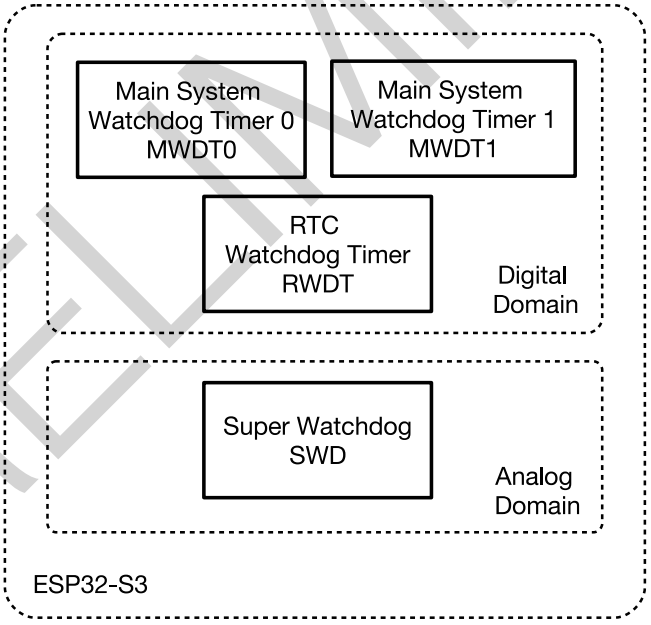


Figure 11-1. Watchdog Timers Overview

Note that while this chapter provides the functional descriptions of the watchdog timer's, their register descriptions are provided in Chapter 10 *Timer Group (TIMG)* and Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*.

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11.2 Digital Watchdog Timers

11.2.1 Features

Watchdog timers have the following features:

- Four stages, each with a programmable timeout value. Each stage can be configured and enabled/disabled separately
- Three timeout actions (interrupt, CPU reset, or core reset) for MWDT and four timeout actions (interrupt, CPU reset, core reset, or system reset) for RWDT upon expiry of each stage
- 32-bit expiry counter
- Write protection, to prevent RWDT and MWDT configuration from being altered inadvertently
- Flash boot protection
  If the boot process from an SPI flash does not complete within a predetermined period of time, the watchdog will reboot the entire main system.

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11.2.2 Functional Description

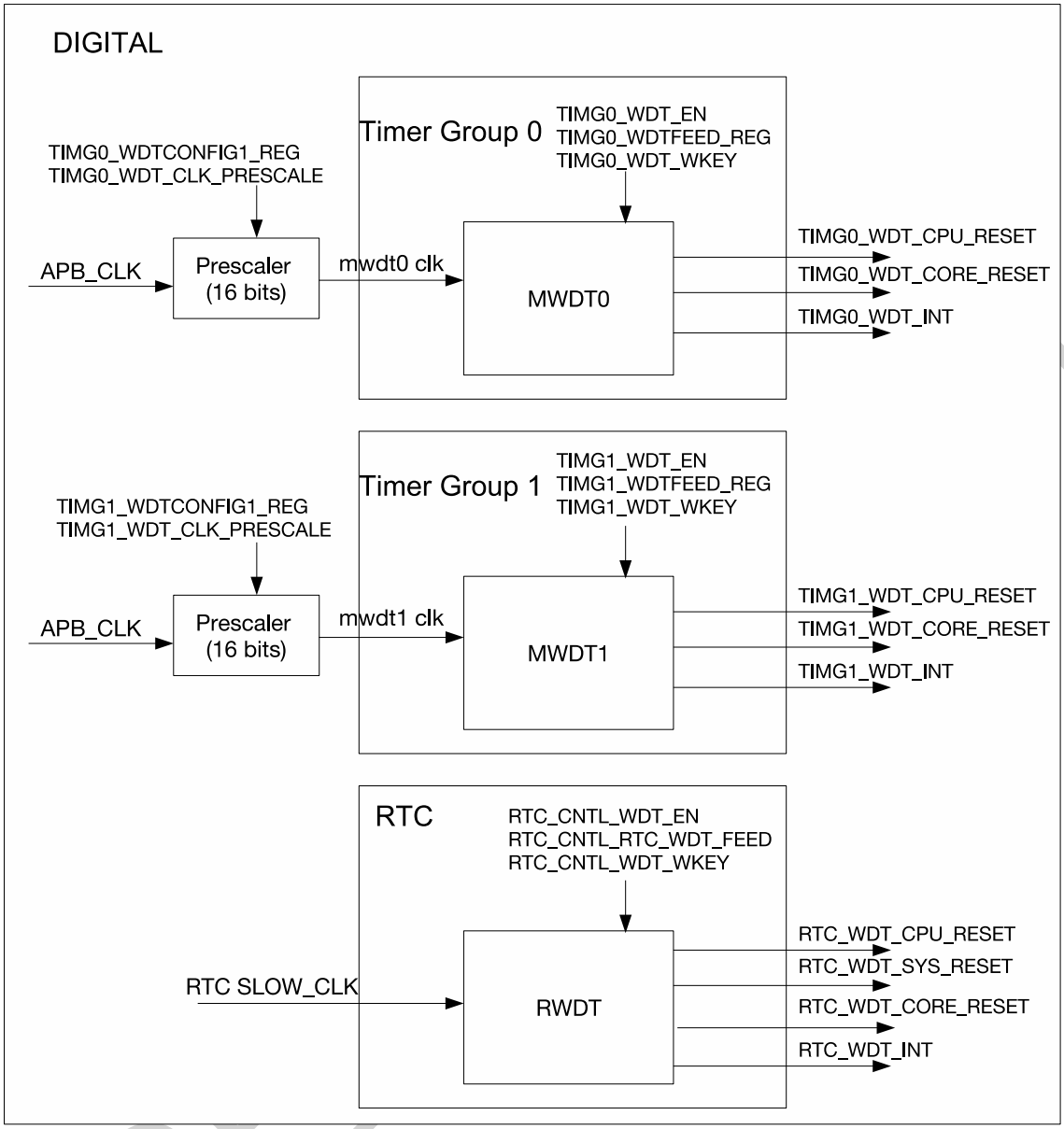


Figure 11-2. Watchdog Timers in ESP32-S3

Figure 11-2 shows the three watchdog timers in ESP32-S3 digital systems.

11.2.2.1 Clock Source and 32-Bit Counter

At the core of each watchdog timer is a 32-bit counter. The clock source of MWDTs is derived from the APB clock via a pre-MWDT 16-bit configurable prescaler. In contrast, the clock source of RWDT is derived directly from an RTC slow clock (the RTC slow clock source shown in Chapter 6 *Reset and Clock*). The 16-bit prescaler for MWDTs is configured via the TIMG_WDT_CLK_PRESCALE field of TIMG_WDTCONFIG1_REG.

MWDTs and RWDT are enabled by setting the TIMG_WDT_EN and RTC_CNTL_WDT_EN fields respectively. When enabled, the 32-bit counters of each watchdog will increment on each source clock cycle until the timeout value of the current stage is reached (i.e. expiry of the current stage). When this occurs, the current counter value is reset to zero and the next stage will become active. If a watchdog timer is fed by software, the timer will return

to stage 0 and reset its counter value to zero. Software can feed a watchdog timer by writing any value to TIMG_WDTFEED_REG for MDWTs and RTC_CNTL_RTC_WDT_FEED for RWDT.

11.2.2.2 Stages and Timeout Actions

Timer stages allow for a timer to have a series of different timeout values and corresponding expiry action. When one stage expires, the expiry action is triggered, the counter value is reset to zero, and the next stage becomes active. MWDTs/ RWDT provide four stages (called stages 0 to 3). The watchdog timers will progress through each stage in a loop (i.e. from stage 0 to 3, then back to stage 0).

Timeout values of each stage for MWDTs are configured in TIMG_WDTCONFIG*i*_REG (where *i* ranges from 2 to 5), whilst timeout values for RWDT are configured using RTC_CNTL_WDT_STG*j*_HOLD field (where *j* ranges from 0 to 3).

Please note that the timeout value of stage 0 for RWDT (T_{hold0}) is determined by the combination of the EFUSE_WDT_DELAY_SEL field of eFuse register EFUSE_RD_REPEAT_DATA1_REG and RTC_CNTL_WDT_STG0_HOLD. The relationship is as follows:

$$T_{hold0} = RTC\_CNTL\_WDT\_STG0\_HOLD << (EFUSE\_WDT\_DELAY\_SEL + 1)$$

where $<<$ is a left-shift operator.

Upon the expiry of each stage, one of the following expiry actions will be executed:

- Trigger an interrupt
  When the stage expires, an interrupt is triggered.
- CPU reset – Reset a CPU core
  When the stage expires, the CPU core will be reset.
- Core reset – Reset the main system
  When the stage expires, the main system (which includes MWDTs, CPU, and all peripherals) will be reset. The power management unit and RTC peripheral will not be reset.
- System reset – Reset the main system, power management unit and RTC peripheral
  When the stage expires the main system, power management unit and RTC peripheral (see details in Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*) will all be reset. This action is only available in RWDT.
- Disabled
  This stage will have no effects on the system.

Timeout values of each stage for MWDTs are configured in TIMG_WDTCONFIG*i*_REG (where *i* ranges from 2 to 5), whilst timeout values for RWDT are configured using RTC_CNTL_WDT_STG*j*_HOLD field (where *j* ranges from 0 to 3).

11.2.2.3 Write Protection

Watchdog timers are critical to detecting and handling erroneous system/software behavior, thus should not be disabled easily (e.g. due to a misplaced register write). Therefore, MWDTs and RWDT incorporate a write protection mechanism that prevent the watchdogs from being disabled or tampered with due to an accidental write.

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The write protection mechanism is implemented using a write-key field for each timer (TIMG_WDT_WKEY for MWDT, RTC_CNTL_WDT_WKEY for RWDT). The value 0x50D83AA1 must be written to the watchdog timer's write-key field before any other register of the same watchdog timer can be changed. Any attempts to write to a watchdog timer's registers (other than the write-key field itself) whilst the write-key field's value is not 0x50D83AA1 will be ignored. The recommended procedure for accessing a watchdog timer is as follows:

1. Disable the write protection by writing the value 0x50D83AA1 to the timer's write-key field.
2. Make the required modification of the watchdog such as feeding or changing its configuration.
3. Re-enable write protection by writing any value other than 0x50D83AA1 to the timer's write-key field.

11.2.2.4 Flash Boot Protection

During flash booting process, MWDT in timer group 0 (see Figure 10-1 *Timer Units within Groups*), as well as RWDT, are automatically enabled. Stage 0 for the enabled MWDT is automatically configured to reset the system upon expiry, known as core reset. Likewise, stage 0 for RWDT is configured to system reset, which resets the main system and RTC when it expires. After booting, TIMG_WDT_FLASHBOOT_MOD_EN and RTC_CNTL_WDT_FLASHBOOT_MOD_EN should be cleared to stop the flash boot protection procedure for both MWDT and RWDT respectively. After this, MWDT and RWDT can be configured by software.

11.3 Super Watchdog

Super watchdog (SWD) is an ultra-low-power circuit in analog domain that helps to prevent the system from operating in a sub-optimal state and resets the system if required. SWD contains a watchdog circuit that needs to be fed for at least once during its timeout period, which is slightly less than one second. About 100 ms before watchdog timeout, it will also send out a WD_INTR signal as a request to remind the system to feed the watchdog.

If the system doesn't respond to SWD feed request and watchdog finally times out, SWD will generate a system level signal SWD_RSTB to reset whole digital circuits on the chip.

11.3.1 Features

SWD has the following features:

- Ultra-low power
- Interrupt to indicate that the SWD timeout period is close to expiring
- Various dedicated methods for software to feed SWD, which enables SWD to monitor the working state of the whole operating system

11.3.2 Super Watchdog Controller

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11.3.2.1 Structure

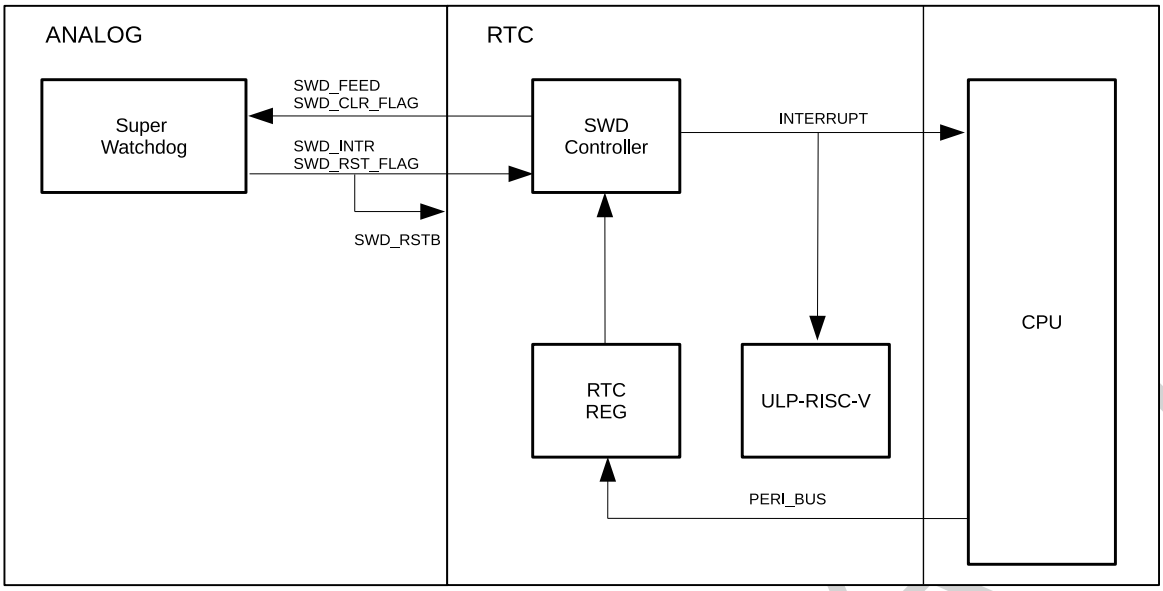


Figure 11-3. Super Watchdog Controller Structure

11.3.2.2 Workflow

In normal state:

- SWD controller receives feed request from SWD.
- SWD controller can send an interrupt to main CPU or ULP-RISC-V.
- Main CPU can decide whether to feed SWD directly by setting RTC_CNTL_SWD_FEED, or send an interrupt to ULP-RISC-V and ask ULP-RISC-V to feed SWD by setting RTC_CNTL_SWD_FEED.
- When trying to feed SWD, CPU or ULP-RISC-V needs to disable SWD controller's write protection by writing 0x8F1D312A to RTC_CNTL_SWD_WKEY. This prevents SWD from being fed by mistake when the system is operating in sub-optimal state.
- If setting RTC_CNTL_SWD_AUTO_FEED_EN to 1, SWD controller can also feed SWD itself without any interaction with CPU or ULP-RISC-V.

After reset:

- Check RTC_CNTL_RESET_CAUSE_PROCPU[5:0] for the cause of CPU reset.
  If RTC_CNTL_RESET_CAUSE_PROCPU[5:0] == 0x12, it indicates that the cause is SWD reset.
- Set RTC_CNTL_SWD_RST_FLAG_CLR to clear the SWD reset flag.

11.4 Interrupts

For watchdog timer interrupts, please refer to Section 10.2.6 *Interrupts* in Chapter 10 *Timer Group (TIMG)*.

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11.5 Registers

MWDT registers are part of the timer submodule and are described in Section 10.4 *Register Summary* in Chapter 10 *Timer Group (TIMG)*. RWDT and SWD registers are part of the RTC submodule and are described in Section 6 *Register Summary* in Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*.

PRELIMINARY

12 XTAL32K Watchdog Timers (XTWDT)

12.1 Overview

The XTAL32K watchdog timer on ESP32-S3 is used to monitor the status of external crystal XTAL32K_CLK. This watchdog timer can detect the oscillation failure of XTAL32K_CLK, change the clock source of RTC, etc. When XTAL32K_CLK works as the clock source of RTC SLOW_CLK (for clock description, see Chapter 6 *Reset and Clock*) and stops oscillating, the XTAL32K watchdog timer first switches to BACKUP32K_CLK derived from RTC_CLK and generates an interrupt (if the chip is in Light-sleep or Deep-sleep mode, the CPU will be woken up), and then switches back to XTAL32K_CLK after it is restarted by software.

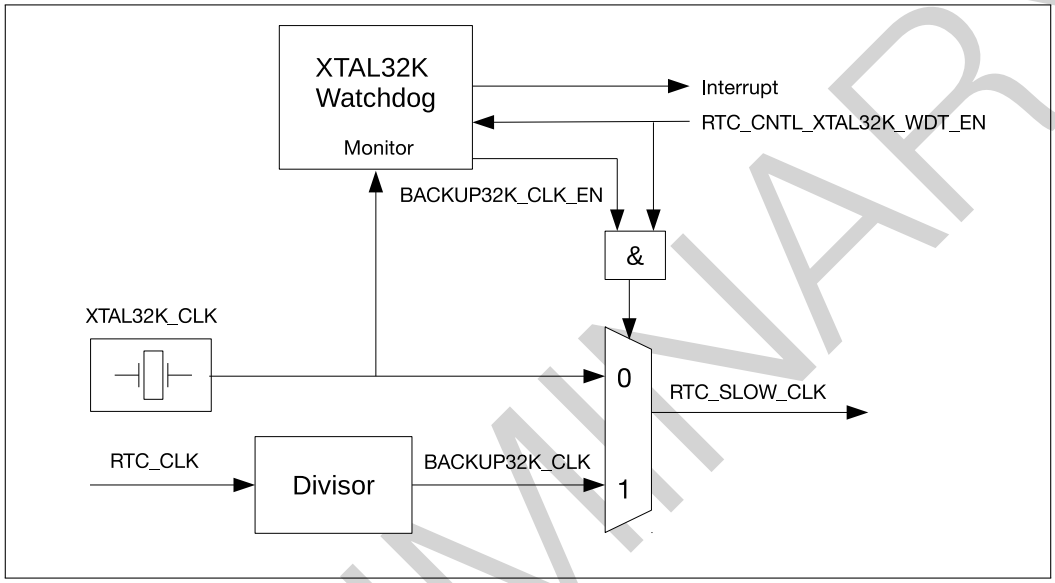


Figure 12-1. XTAL32K Watchdog Timer

12.2 Features

12.2.1 Interrupt and Wake-Up

When the XTAL32K watchdog timer detects the oscillation failure of XTAL32K_CLK, an oscillation failure interrupt RTC_XTAL32K_DEAD_INT (for interrupt description, please refer to Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*) is generated. At this point, the CPU will be woken up if in Light-sleep mode or Deep-sleep mode.

12.2.2 BACKUP32K_CLK

Once the XTAL32K watchdog timer detects the oscillation failure of XTAL32K_CLK, it replaces XTAL32K_CLK with BACKUP32K_CLK (with a frequency of 32 kHz or so) derived from RTC_CLK as RTC's SLOW_CLK, so as to ensure proper functioning of the system.

12.3 Functional Description

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12.3.1 Workflow

1. The XTAL32K watchdog timer starts counting when RTC_CNTL_XTAL32K_WDT_EN is enabled. The counter based on RTC_CLK keeps counting until it detects the positive edge of XTAL_32K and is then cleared. When the counter reaches RTC_CNTL_XTAL32K_WDT_TIMEOUT, it generates an interrupt or a wake-up signal and is then reset.
2. If RTC_CNTL_XTAL32K_AUTO_BACKUP is set and step 1 is finished, the XTAL32K watchdog timer will automatically enable BACKUP32K_CLK as the alternative clock source of RTC SLOW_CLK, to ensure the system's proper functioning and the accuracy of timers running on RTC SLOW_CLK (e.g. RTC_TIMER). For information about clock frequency configuration, please refer to Section 12.3.2.
3. To restore the XTAL32K watchdog timer, software restarts XTAL32K_CLK by turning its XPD (meaning no power-down) signal off and on again via RTC_CNTL_XPD_XTAL_32K bit. Then, the XTAL32K watchdog timer switches back to XTAL32K_CLK as the clock source of RTC SLOW_CLK by clearing RTC_CNTL_XTAL32K_WDT_EN (BACKUP32K_CLK_EN is also automatically cleared). If the chip is in Light-sleep or Deep-sleep mode mode, the XTAL32K watchdog timer will wake up the CPU to finish the above steps.

12.3.2 BACKUP32K_CLK Working Principle

Chips have different RTC_CLK frequencies due to production process variations. To ensure the accuracy of RTC_TIMER and other timers running on SLOW_CLK when BACKUP32K_CLK is at work, the divisor of BACKUP32K_CLK should be configured according to the actual frequency of RTC_CLK (see details in Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*) via RTC_CNTL_XTAL32K_CLK_FACTOR_REG register. Each byte in this register corresponds to a divisor component (x_0 ~x_7). BACKUP32K_CLK is divided by a fraction where the denominator is always 4, as calculated below.

$$f\_back\_clk/4 = f\_rtc\_clk/S$$
$$S = x_0 + x_1 + ... + x_7$$

f_back_clk is the desired frequency of BACKUP32K_CLK; f_rtc_clk is the actual frequency of RTC_CLK; x_0 ~x_7 correspond to the pulse width in high and low state of four BACKUP32K_CLK clock signals (unit: RTC_CLK clock cycle).

12.3.3 Configuring the Divisor Component of BACKUP32K_CLK

Based on principles described in Section 12.3.2, you can configure the divisor component as follows:

- Calculate the sum of divisor components S according to the frequency of RTC_CLK and the desired frequency of BACKUP32K_CLK;
- Calculate the integer part of divisor $N = f\_rtc\_clk/f\_back\_clk$;
- Calculate the integer part of divisor component $M = N/2$. The integer part of divisor N are separated into two parts because a divisor component corresponds to a pulse width in high or low state;
- Calculate the number of divisor components that equal M (x_n = M) and the number of divisor components that equal M + 1 (x_n = M + 1) according to the value of M and S. (M + 1) is the fractional part of divisor component.

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For example, if the frequency of RTC_CLK is 163 kHz, then $f\_rtc\_clk = 163000$, $f\_back\_clk = 32768$, $S = 20$, $M = 2$, and $\{x_0, x_1, x_2, x_3, x_4, x_5, x_6, x_7\} = \{2, 3, 2, 3, 2, 3, 2, 3\}$. As a result, the frequency of BACKUP32K_CLK is 32.6 kHz.

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13 Permission Control (PMS)

13.1 Overview

ESP32-S3 is specially designed for flexible access management to internal memory, external memory, and all peripherals. Once configured, CPU can only access a particular slave device according to the configured permission, thus protecting the slave device from unauthorized access (read, write, or instruction execution).

In addition, ESP32-S3 has integrated a World Controller, which when enabled can be used along with Permission Controller to allocate the chip's hardware and software resource into Secure World (World0) and Non-secure World (World1), and can switch the CPU between running from the Secure World or Non-secure World. For details, please refer to 14 *World Controller*.

This chapter mainly describes the access management to different internal memory, external memory and peripherals.

13.2 Features

ESP32-S3's Permission Control module supports:

- Independent access management for the Secure World and Non-secure World.
- Independent access management to internal memory, including
  - CPU access to internal memory
  - Allocate internal memory as CPU Trace
  - GDMA access to internal memory
- Independent access management to external memory, including
  - SPI1 access to external memory
  - GDMA access to external memory
  - CACHE access to external memory
- Independent access management to peripheral regions, including
  - CPU access to peripheral regions
  - Interrupt upon unsupported access alignment
- Address splitting for more flexible access management
- Interrupt upon unauthorized access
- Register locks to secure the integrity of Permission Control related registers
- Protection to secure the integrity of CPU's VECBASE registers

13.3 Internal Memory

ESP32-S3 has the following types of internal memory:

- ROM: 384 KB in total, including 256 KB Internal ROM0 and 128 KB Internal ROM1

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- SRAM: 512 KB in total, including 32 KB Internal SRAM0, 416 KB Internal SRAM1, and 64 KB Internal SRAM2
- RTC FAST Memory: 8 KB in total, which can be split into two regions with independent permission configuration
- RTC SLOW Memory: 8 KB in total, which can be further split into two regions each with independent permission configuration

This section describes how to configure the permission to each types of ESP32-S3's internal memory.

13.3.1 ROM

ESP32-S3's ROM can be accessed by CPU's instruction bus (IBUS) and data bus (DBUS) when configured. Note:

- Permission for Secure World and Non-secure World can be configured independently.
- Once configured, the permission applies for both CPU0 and CPU1.

13.3.1.1 Address

ESP32-S3's ROM address and the address ranges accessible for IBUS and DBUS respectively are listed in Table 13-1.

Table 13-1. ROM Address

ROM	IBUS Address		DBUS Address	
	Starting Address	Ending Address	Starting Address	Ending Address
Internal ROM0	0x4000_0000	0x4003_FFFF	-	-
Internal ROM1	0x4004_0000	0x4005_FFFF	0x3FF0_0000	0x3FF1_FFFF

13.3.1.2 Access Configuration

ESP32-S3 uses the registers listed in Table 13-2 to configure the instruction execution (X), write (W) and read (R) accesses of CPU's IBUS and DBUS, from the Secure World and Non-secure World, to ROM:

Table 13-2. Access Configuration to ROM

Bus	From World	Configuration Registers[A]	Access
IBUS	Secure World	PMS_CORE_X_IRAM0_PMS_CONSTRAIN_2_REG [20:18][B]	X/W/R
	Non-secure World	PMS_CORE_X_IRAM0_PMS_CONSTRAIN_1_REG [20:18]	X/W/R
DBUS	Secure World	PMS_CORE_X_DRAM0_PMS_CONSTRAIN_1_REG [25:24][C]	W/R
	Non-secure World	PMS_CORE_X_DRAM0_PMS_CONSTRAIN_1_REG [27:26]	W/R

[A] 1: with access; 0: without access

[B] For example, configuring this field to 0b101 indicates CPU's IBUS is granted with instruction execution and read accesses but not write access to ROM from the Secure World.

[C] For example, configuring this field to 0b01 indicates CPU's DBUS is granted with read access but not write access to ROM from the Secure World.

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13.3.2 SRAM

ESP32-S3's SRAM can be accessed by CPU's instruction bus (IBUS) and data bus (DBUS) when configured. Note:

- Permission for Secure World and Non-secure World can be configured independently.
- Once configured, the configuration applies for both CPU0 and CPU1.

13.3.2.1 Address

ESP32-S3's SRAM address and the address ranges accessible for IBUS and DBUS respectively are listed in Table 13-3.

Table 13-3. SRAM Address

SRAM	Block	IBUS Address		DBUS Address	
		Starting Address	Ending Address	Starting Address	Ending Address
Internal SRAM0	Block0	0x4037_0000	0x4037_3FFF	-	-
	Block1	0x4037_4000	0x4037_7FFF	-	-
Internal SRAM1	Block2	0x4037_8000	0x4037_FFFF	0x3FC8_8000	0x3FC8_FFFF
	Block3	0x4038_0000	0x4038_FFFF	0x3FC9_0000	0x3FC9_FFFF
	Block4	0x4039_0000	0x4039_FFFF	0x3FCA_0000	0x3FCA_FFFF
	Block5	0x403A_0000	0x403A_FFFF	0x3FCB_0000	0x3FCB_FFFF
	Block6	0x403B_0000	0x403B_FFFF	0x3FCC_0000	0x3FCC_FFFF
	Block7	0x403C_0000	0x403C_FFFF	0x3FCD_0000	0x3FCD_FFFF
	Block8	0x403D_0000	0x403D_FFFF	0x3FCE_0000	0x3FCE_FFFF
Internal SRAM 2	Block9	-	-	0x3FCF_0000	0x3FCF_7FFF
	Block10	-	-	0x3FCF_8000	0x3FCF_FFFF

Here, we will first introduce how to configure the permission to Internal SRAM0, Internal SRAM1, and Internal SRAM2, and also how to configure the Internal SRAM1 as CPU Trace memory.

13.3.2.2 Internal SRAM0 Access Configuration

ESP32-S3's Internal SRAM0 includes Block0 and Block1 (see details in Table 13-3) and can be allocated to either CPU or ICACHE.

Note that once configured, the configuration applies for both CPU0 and CPU1.

ESP32-S3 uses the register described in Table 13-4 to allocate the SRAM0 to either CPU or ICACHE:

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Table 13-4. Internal SRAM0 Usage Configuration

	Block	PMS_INTERNAL_SRAM_USAGE_1_REG[A]
SRAM	Block0	[0] [B]
	Block1	[1]

[A] Set this bit to allocate a certain block to CPU. Clear this bit to allocate a certain block to ICACHE.

[B] For example, setting this bit indicates Block0 is allocated to CPU.

When a certain block is allocated to CPU, ESP32-S3 uses the registers listed in Table 13-5 to configure the instruction execution (X), write (W) and read (R) accesses of CPU's IBUS, from the Secure World and Non-secure World, to this block:

Table 13-5. Access Configuration to Internal SRAM0

Bus[A]	From World	Configuration Registers[B]	SRAM0		Access
			Block0	Block1	
IBUS	Secure World	PMS_CORE_X_IRAM0_PMS_CONSTRAIN_2_REG	[14:12][C]	[17:15]	X/W/R
	Non-secure World	PMS_CORE_X_IRAM0_PMS_CONSTRAIN_1_REG	[14:12]	[17:15]	X/W/R

[A] To access the Internal SRAM0, CPU must be configured with both the usage permission and respective access permission.

[B] 1: with access; 0: without access

[C] For example, configuring this field to 0b101 indicates CPU's IBUS is granted with instruction execution and read accesses but not write access to SRAM Block0 from the Non-secure World.

13.3.2.3 Internal SRAM1 Access Configuration

ESP32-S3's Internal SRAM1 includes Block2 ~ Block8 (see details in Table 13-3) and can be:

- Accessed by CPU's DBUS, IBUS and GDMA at the same time
- Can be configured to be used as Trace memory
- Further split into up to 6 regions with independent access management for more flexible permission control.

ESP32-S3's Internal SRAM1 can be further split into up to 6 regions with 5 split lines. Users can configure different access to each region independently.

To be more specific, the Internal SRAM1 can be first split into Instruction Region and Data Region by IRam0_DRam0_split_line:

- Instruction Region:
  - Then the Instruction Region should be only configured to be accessed by IBUS;
  - And can be further split into three split regions by IRam0_split_line_0 and IRam0_split_line_1.
- Data Region:
  - The Data Region should be only configured to be accessed by DBUS;
  - And can be further split into three split regions by DRam0_split_line_0 and DRam0_split_line_1.

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See illustration in Figure 13-1 and Table 13-6 below.

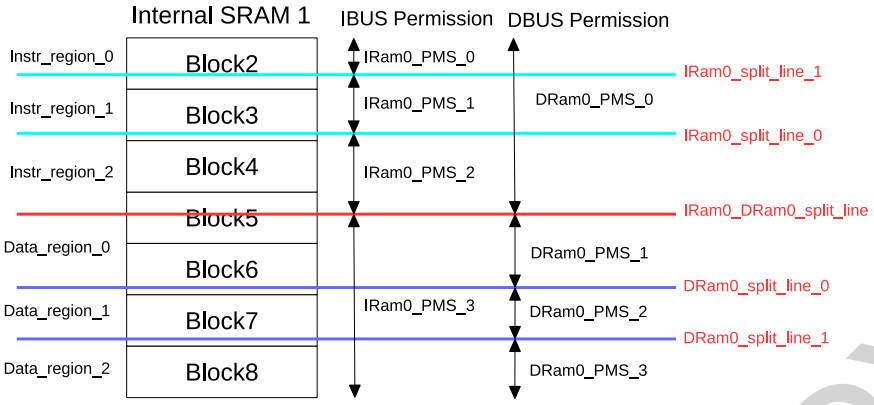


Figure 13-1. Split Lines for Internal SRAM1

Table 13-6. Internal SRAM1 Split Regions

Internal Memory [A]	Instruction / Data Regions	Split Regions[B]
SRAM1	Instruction Region	Instr_Region_0
		Instr_Region_1
		Instr_Region_2
	Data Region	Data_Region_0
		Data_Region_1
		Data_Region_2

[A] See description below on how to configure the split lines.

[B] Access to each split region can be configured independently. See details in Table 13-7 and 13-8.

Internal SRAM1 Split Regions

ESP32-S3 allows users to configure the split lines to their needs with registers below:

- Split line to split the Instruction and Data regions (IRam0_DRam0_split_line):
  - PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_1_REG
- The first split line to further split the Instruction Region (IRam0_split_line_0):
  - PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_2_REG
- The second split line to further split the Instruction Region (IRam0_split_line_1):
  - PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_3_REG
- The first split line to further split the data Region (DRam0_split_line_0):
  - PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_4_REG
- The second split line to further split the data Region (DRam0_split_line_1):
  - PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_5_REG

When configuring the split lines,

1. First configure the block in which the spilt line is by:

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- Configuring the Category_*x* field for the block in which the split line is to 0x1 or 0x2 (no difference)
- Configuring the Category_0 ~ Category_*x-1* fields for all the preceding blocks to 0x0
- Configuring the Category_*x+1* ~ Category_6 fields for all blocks afterwards to 0x3

For example, assuming you want to configure the split line in Block5, then first configure the Category_3 field for Block5 to 0x1 or 0x2; configure the Category_0 ~ Category_2 fields for Block2 ~ Block4 to 0x0; and configure the Category_4 ~ Category_6 fields for Block6 ~ Block8 to 0x3 (see illustration in Figure 13-2). On the other hand, when reading 0x1 or 0x2 from Category_3, then you know the split line is in Block5.

2. Configure the position of the split line inside of the configured block by:
   - Writing the [15:8] bits of the actual address at which you want to split the memory to the SPLITADDR field for the block in which the split line is.
   - Note that the split address must be aligned to 256 bytes, meaning you can only write the integral multiples of 0x100 to the SPLITADDR field.

   For example, if you want to split the instruction region at 0x3fc88000, then write the [15:8] bits of this address, which is 0b10000000, to SPLITADDR.

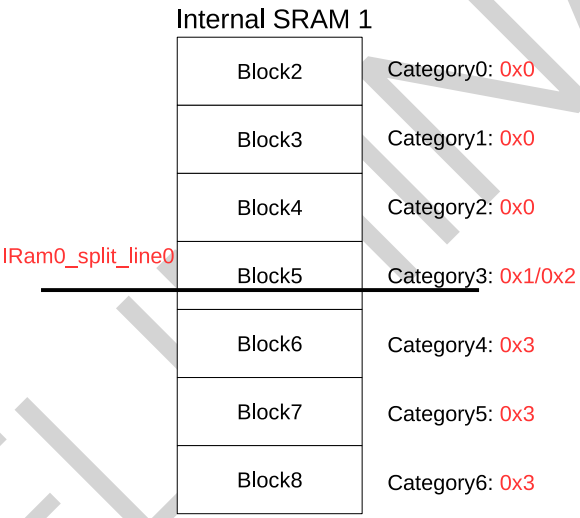


Figure 13-2. An illustration of Configuring the Category fields

Note the following points when configuring the split lines:

- Position:
  - The split line that splitting the Instruction Region and Data Region can be configured anywhere inside Internal SRAM1.
  - The two split lines further splitting the Instruction Region into 3 split regions must stay inside the Instruction Region.
  - The two split lines further splitting the Data Region into 3 split regions must stay inside the Data Region.
- Spilt lines can overlap with each other. For example,
  - When the two split lines inside the Data Region are not overlapping with each other, then the Data Region is split into 3 split regions

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- When the two split lines inside the Data Region are overlapping with each other, then the Data Region is only split into 2 split regions
- When the two split lines inside the Data Region are not only overlapping with each other but also with the split line that splits the Data Region and the Instruction Region, then the Data Region is not split at all and only has one region.

Access Configuration

After configuring the split lines, users can then use the registers described in the Table 13-7 and Table 13-8 below to configure the access of CPU's IBUS, DBUS and GDMA peripherals, from the Secure World and Non-secure World, to these split regions independently.

Table 13-7. Access Configuration to the Instruction Region of Internal SRAM1

Buses	From World	Configuration Registers	Instruction Region			Access
			instr_region_0	instr_region_1	instr_region_2	
IBUS	Secure World	PMS_CORE_X_IRAM0_PMS_CONSTRAIN_2_REG	[2:0]	[5:3]	[8:6]	X/W/R
	Non-secure World	PMS_Core_X_IRAM0_PMS_CONSTRAIN_1_REG	[2:0]	[5:3]	[8:6]	X/W/R
DBUS	Secure World	PMS_Core_X_DRAM0_PMS_CONSTRAIN_1_REG	[1:0][A]			W/R
	Non-secure World		[13:12][A]			W/R
GDMA	XX Peripherals [C]	PMS_DMA_APBPERI_XX_PMS_CONSTRAIN_1_REG	[1:0][B]			W/R

[A] Configure DBUS' access to the Instruction Region. However, it's recommended to configure these bits to 0.

[B] Configure GDMA's access to the Instruction Region. However, it's recommended to configure these bits to 0.

[C] ESP32-S3 has 9 peripherals, including SPI2, SPI3, UCHI0, I2S0, I2S1, AES, SHA, ADC, LCD_CAM, USB, SDIO_HOST, and RMT, which can access Internal SRAM1 via GDMA. Each peripherals can be configured with different access to the Internal SRAM1 independently.

Table 13-8. Access Configuration to the Data Region of Internal SRAM1

Buses	From World	Configuration Registers	Data Region			Access
			data_region_0	data_region_1	data_region_2	
IBUS	Secure World	PMS_CORE_X_IRAM0_PMS_CONSTRAIN_2_REG	[11:9][A]			X/W/R
	Non-secure World	PMS_CORE_X_IRAM0_PMS_CONSTRAIN_1_REG	[11:9][A]			X/W/R
DBUS	Secure World	PMS_Core_X_DRAM0_PMS_CONSTRAIN_1_REG	[3:2]	[5:4]	[7:6]	W/R
	Non-secure World		[15:14]	[17:16]	[19:18]	W/R
GDMA XX [B]	-	PMS_DMA_APBPERI_XX_PMS_CONSTRAIN_1_REG	[3:2]	[5:4]	[7:6]	W/R

[A] Configure IBUS' access to the Data Region. However, it's recommended to configure these bits to 0.

[B] ESP32-S3 has 9 peripherals, including SPI2, SPI3, UCHI0, I2S0, I2S1, AES, SHA, ADC, LCD_CAM, USB, SDIO_HOST, and RMT, which can access Internal SRAM1 via GDMA. Each peripherals can be configured with different access to the Internal SRAM1 independently.

For details on how to configure the split lines, see Section 13.3.2.3.

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Trace Memory

ESP32-S3 has a low-power Xtensa® dual-core 32-bit LX7 microprocessor, which integrates a TRAX (Real-time Trace) module for easier debugging. For the TRAX module to work, users need to allocate 16 KB from the Internal SRAM1 as Trace memory. Note that, the Trace memories for CPU0 and CPU1 can be configured independently.

Users can allocate 16 KB from Internal SRAM1 as Trace memory by configuring the PMS_INTERNAL_SRAM_USAGE_2_REG register.

Detailed steps are provided below:

1. First choose a block from Block2 ~ Block8 by writing 1 to the respective bit in the PMS_INTERNAL_SRAM_CORE*m*_TRACE_USAGE field
   - Block2: 0b00000001
   - Block3: 0b00000010
   - Block4: 0b00000100
   - Block5: 0b00001000
   - Block6: 0b00010000
   - Block7: 0b00100000
   - Block8: 0b01000000
2. Then choose 16 KB from this block as the Trace memory by configuring the PMS_INTERNAL_SRAM_CORE*m*_TRACE_ALLOC field
   - 2'b00: the first 16 KB
   - 2'b01: the second 16 KB
   - 2'b10: the third 16 KB
   - 2'b11: the fourth 16 KB

   Note that Block2 is only 32 KB, so you can only configure this field to 2'b00 or 2'b0 when Block2 is selected in the first step.

For example, if you want to choose the first 16 KB of Internal SRAM1 Block3's as CPU0's trace memory, then you need to:

- Write 0b0000010 to the PMS_INTERNAL_SRAM_CORE0_TRACE_USAGE field to select Block3
- Write 2'b00 to the PMS_INTERNAL_SRAM_CORE0_TRACE_ALLOC field to select the first 16 KB.

13.3.2.4 Internal SRAM2 Access Configuration

ESP32-S3's Internal SRAM2 includes Block9 and Block10 (see details in Table 13-3), which can be allocated to either CPU/GDMA or DCACHE. Note that once configured, the configuration applies to both CPU0 and CPU1.

ESP32-S3 uses registers described in Table 13-9 to configure the Internal SRAM2 for CPU/GDMA or DCACHE.

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Table 13-9. Internal SRAM2 Usage Configuration

	Block	PMS_INTERNAL_SRAM_USAGE_1_REG[A]
SRAM	Block9[B]	[3]
	Block10	[2]

[A] Set this bit to allocate a certain block to CPU/GDMA. Clear this bit to allocate a certain block to DCACHE.

[B] For example, setting this bit indicates Block9 is allocated to CPU/GDMA.

When a certain block is allocated to CPU/GDMA, ESP32-S3 uses the registers listed in Table 13-10 to configure the write (W) and read (R) accesses of CPU's DBUS, from the Secure World and Non-secure World, to this block:

Table 13-10. Access Configuration to Internal SRAM2

Bus [A]	From World	Configuration Registers	SRAM2		Access[B]
			Block9	Block10	
DBUS	Secure World	PMS_CORE_X_DRAM0_PMS_CONSTRAIN_1_REG	[9:8][C]	[11:10]	W/R
	Non-secure World	PMS_CORE_X_DRAM0_PMS_CONSTRAIN_1_REG	[21:20]	[23:22]	W/R
GDMA	*XX* Peripherals[B]	PMS_DMA_APBPERI_*XX*_PMS_CONSTRAIN_1_REG	[9:8]	[11:10]	W/R

[A] To access the Internal SRAM2, the CPU / GDMA must be configured with both the usage permission and respective access permission.

[B] 1: with access; 0: without access

[C] For example, configuring this field to 0b10 indicates CPU's DBUS is granted with write access but not read access from the Secure World to the Block9 of Internal SRAM2.

13.3.3 RTC FAST Memory

13.3.3.1 Address

ESP32-S3's RTC FAST Memory is 8 KB. See the address of RTC FAST Memory below:

Table 13-11. RTC FAST Memory Address

Memory	Starting Address	Ending Address
RTC FAST Memory	0x600F_E000	0x600F_FFFF

13.3.3.2 Access Configuration

ESP32-S3's RTC FAST Memory can be further split into 2 regions. Each split region can be configured independently with different access by configuring respective registers (PMS_CORE_*m*_PIF_PMS_CONSTRAN_*n*_REG).

Note that split regions can be configured independently for CPU0 and CPU1 and for the Secure World and Non-secure World.

The Register for configuring the split line is described below:

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Table 13-12. Split RTC FAST Memory into the Higher Region and the Lower Region

Memory	Split Regions	Configuration Register[1]	
		Secure World	Non-secure World
RTC FAST Memory	Higher Region	PIF_PMS_CONSTRAN_9_REG [10:0]	PIF_PMS_CONSTRAN_9_REG [21:11]
	Lower Region		

[1] The offset from the RTC FAST Memory base address should be used when configuring the split address. For example, if you want to split the RTC FAST Memory at 0x600F_F000, then write 0x1000 to this register.

Access configuration for the higher and lower regions of the RTC FAST Memory is described below:

Table 13-13. Access Configuration to the RTC FAST Memory

Bus	RTC FAST Memory	Configuration Registers		Access[A]
		Secure World	Non-secure World	
Peri Bus (PIF)	Higher Region	PIF_PMS_CONSTRAN_10_REG [5:3] [B]	PIF_PMS_CONSTRAN_10_REG [11:9]	X/W/R
	Lower Region	PIF_PMS_CONSTRAN_10_REG [2:0]	PIF_PMS_CONSTRAN_10_REG [8:6]	

[A] 1: with access; 0: without access

[B] For example, configuring this field to 0b101 indicates CPU's peripheral (PIF) bus is granted with the instruction execution and read accesses but not the read access from the Secure WORLD to the higher region of RTC FAST Memory.

13.3.4 RTC SLOW Memory

13.3.4.1 Address

ESP32-S3's RTC SLOW Memory is 8 KB. This memory can be accessed using two addresses, i.e, RTCSlow_0 and RTCSlow_1. See details in Table 13-14 below:

Table 13-14. RTC SLOW Memory Address

RTC SLOW Memory	Starting Address	Ending Address
RTCSlow_0	0x5000_0000	0x5000_1FFF
RTCSlow_1	0x6002_1000	0x6002_2FFF

13.3.4.2 Access Configuration

Both ESP32-S3's RTCSlow_0 and RTCSlow_1 can be further split into 2 regions. Each split region can be configured independently with different access by configuring respective registers (PMS_CORE_*m*_PIF_PMS_CONSTRAN_*n*_REG).

Note that split regions can be configured independently for CPU0 and CPU1 and for the Secure World and Non-secure World.

The registers for splitting RTC SLOW Memory into 4 split regions are described below:

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Table 13-15. Split RTCSlow_0 and RTCSlow_1 into Split Regions

Memory	Split Regions	Configuration Registers[1]	
		Secure World	Non-secure World
RTCSlow_0	Higher Region	PIF_PMS_CONSTRAN_11_REG [10:0]	PIF_PMS_CONSTRAN_9_REG [21:11]
	Lower Region		
RTCSlow_1	Higher Region	PIF_PMS_CONSTRAN_13_REG [10:0]	PIF_PMS_CONSTRAN_13_REG [21:11]
	Lower Region		

[1] The offset from the RTC SLOW Memory base address should be used when configuring the split address. For example, if you want to split the RTC SLOW Memory at 0x6002_2000, then write 0x1000 to this register.

Access configuration to the split regions of RTC SLOW Memory is described below:

Table 13-16. Access Configuration to the RTC SLOW Memory

Bus	Mem	Split Regions	Configuration Registers		Access
			Secure World	Non-secure World	
Peri Bus (PIF)	RTC Slow_0	Higher[A]	PIF_PMS_CONSTRAN_12_REG [5:3][C]	PIF_PMS_CONSTRAN_12_REG [11:9]	X/W/R
		Lower [B]	PIF_PMS_CONSTRAN_12_REG [2:0]	PIF_PMS_CONSTRAN_12_REG [8:6]	
	RTC Slow_1	Higher[A]	PIF_PMS_CONSTRAN_14_REG [5:3]	PIF_PMS_CONSTRAN_14_REG [11:9]	
		Lower[B]	PIF_PMS_CONSTRAN_14_REG [2:0]	PIF_PMS_CONSTRAN_14_REG [8:6]	

[A] Higher is short for Higher Region.

[B] Lower is short for Lower Region.

[C] For example, configuring this field to 0b100 indicates CPU's peripheral (PIF) bus is granted with the instruction execution access but not the write or read accesses from the Secure WORLD to the higher region of RTCSLOW_0.

13.4 Peripherals

13.4.1 Access Configuration

ESP32-S3's CPU can be configured with different read (R) and write (W) accesses to most of its modules and peripherals independently, from the Secure World and the Non-secure World, by configuring respective registers (PMS_CORE_*m*_PIF_PMS_CONSTRAN_*n*_REG).

Note that permission to modules and peripherals can be configured independently for CPU0 and CPU1 and for the Secure World and Non-secure World.

Notes on PMS_CORE_*m*_PIF_PMS_CONSTRAN_*n*_REG:

- *m* can be 0 or 1 for CPU0 and CPU1 respectively.
- *n* can be 1~8, in which 1~4 are for Secure World and 5~8 are for Non-secure World.

For example, users can configure PMS_CORE_0_PIF_PMS_CONSTRAIN_1_REG [1:0] to 0x2, meaning CPU0 is granted with read access but not write access from the Secure World to UART0. In this case, CPU0 won't be able to modify the UART0's internal registers when in Secure World.

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Table 13-17. Access Configuration of the Peripherals

Peripherals	Secure World	Non-secure World	Bit[3]
GDMA	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[7:6]
eFuse Controller & PMU[2]	PIF_PMS_CONSTRAN_1_REG	PIF_PMS_CONSTRAN_5_REG	[15:14]
IO_MUX	PIF_PMS_CONSTRAN_1_REG	PIF_PMS_CONSTRAN_5_REG	[17:16]
GPIO	PIF_PMS_CONSTRAN_1_REG	PIF_PMS_CONSTRAN_5_REG	[7:6]
Interrupt Matrix	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[21:20]
System Timer	PIF_PMS_CONSTRAN_2_REG	PIF_PMS_CONSTRAN_6_REG	[31:30]
Timer Group 0	PIF_PMS_CONSTRAN_2_REG	PIF_PMS_CONSTRAN_6_REG	[27:26]
Timer Group 1	PIF_PMS_CONSTRAN_2_REG	PIF_PMS_CONSTRAN_6_REG	[29:28]
World Controller	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[31:30]
System Registers	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[17:16]
Sensitive Registers	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[19:18]
Debug Assist	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[27:26]
Accelerators[1]	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[5:4]
CACHE & XTS_AES[2]	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[25:25]
UART 0	PIF_PMS_CONSTRAN_1_REG	PIF_PMS_CONSTRAN_5_REG	[1:0]
UART 1	PIF_PMS_CONSTRAN_1_REG	PIF_PMS_CONSTRAN_5_REG	[31:30]
UART 2	PIF_PMS_CONSTRAN_3_REG	PIF_PMS_CONSTRAN_7_REG	[17:16]
SPI 0	PIF_PMS_CONSTRAN_1_REG	PIF_PMS_CONSTRAN_5_REG	[5:4]
SPI 1	PIF_PMS_CONSTRAN_1_REG	PIF_PMS_CONSTRAN_5_REG	[3:2]
SPI 2	PIF_PMS_CONSTRAN_3_REG	PIF_PMS_CONSTRAN_7_REG	[1:0]
SPI 3	PIF_PMS_CONSTRAN_3_REG	PIF_PMS_CONSTRAN_7_REG	[3:2]
I2C 0	PIF_PMS_CONSTRAN_2_REG	PIF_PMS_CONSTRAN_6_REG	[5:4]
I2C 1	PIF_PMS_CONSTRAN_3_REG	PIF_PMS_CONSTRAN_7_REG	[7:6]
I2S 0	PIF_PMS_CONSTRAN_1_REG	PIF_PMS_CONSTRAN_5_REG	[29:28]
I2S 1	PIF_PMS_CONSTRAN_3_REG	PIF_PMS_CONSTRAN_7_REG	[15:14]
Pulse Count Controller	PIF_PMS_CONSTRAN_2_REG	PIF_PMS_CONSTRAN_6_REG	[13:12]
USB Serial/JTAG Controller	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[1:0]
USB OTG Core	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[15:14]
USB OTG External	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[3:2]
Two-wire Automotive Interface	PIF_PMS_CONSTRAN_3_REG	PIF_PMS_CONSTRAN_7_REG	[11:10]
UHCI 0	PIF_PMS_CONSTRAN_2_REG	PIF_PMS_CONSTRAN_6_REG	[7:6]
SD/MMC Host Controller	PIF_PMS_CONSTRAN_3_REG	PIF_PMS_CONSTRAN_7_REG	[9:8]
LED PWM Controller	PIF_PMS_CONSTRAN_2_REG	PIF_PMS_CONSTRAN_6_REG	[17:16]
Motor Control PWM 0	PIF_PMS_CONSTRAN_2_REG	PIF_PMS_CONSTRAN_6_REG	[25:24]
Motor Control PWM 1	PIF_PMS_CONSTRAN_3_REG	PIF_PMS_CONSTRAN_7_REG	[13:12]
Remote Control Peripheral	PIF_PMS_CONSTRAN_2_REG	PIF_PMS_CONSTRAN_6_REG	[11:10]
Camera-LCD Controller	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[11:10]
APB Controller	PIF_PMS_CONSTRAN_3_REG	PIF_PMS_CONSTRAN_7_REG	[5:4]
ADC Controller	PIF_PMS_CONSTRAN_4_REG	PIF_PMS_CONSTRAN_8_REG	[9:8]

[1] : Accelerators: AES, SHA, RSA, Digital Signatures, HMAC

[2] : This is shared by more than one peripherals.

[3] : Access: R/W

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13.4.2 Split Peripheral Regions into Split Regions

Each of ESP32-S3's peripheral region can be further split into 11 regions (from Peri Region0 ~ Peri Region10) for more flexible permission control.

For example, the registers for ESP32-S3's GDMA controller are allocated as:

- 5 sets of registers for 5 of each RX channel
- 5 sets of registers for 5 of each TX channel
- 1 set of registers for configuration

As seen above, GDMA's peripheral region is divided into 11 split regions (implemented in hardware), which can be configured with different permission independently, thus achieving independent permission control to each GDMA channel.

Users can configure CPU's read (R) and write (W) accesses to a specific split region (Peri Region*n*) from the Secure World and the Non-secure World by configuring PMS_CORE_*m*_Region_PMS_CONSTRAN_*n*_REG. Note that permission can be configured independently for CPU0 and CPU1.

Notes on PMS_CORE_*m*_Region_PMS_CONSTRAN_*n*_REG:

- *m* can be 0 or 1 for CPU0 and CPU1 respectively.
- *n* can be 1~14, in which
  - Region_PMS_CONSTRAN_1_REG is for configuring CPU's permission from the Secure World.
  - Region_PMS_CONSTRAN_2_REG is for configuring CPU's permission from the Non-secure World.
  - Region_PMS_CONSTRAN_*n*_REG *n* = 3~14 are used to configuring the starting addresses for each Peri Regions. Note the starting address of each Peri Region is also the ending address of the previous Peri Region.

Table 13-18. Access Configuration of Peri Regions

Peri Regions	Starting Address Configuration	Access Configuration	
		Secure World	NOn-secure World
Peri Region0	Region_PMS_CONSTRAN_3_REG	Region_PMS_CONSTRAN_1_REG [1:0]	Region_PMS_CONSTRAN_2_REG [1:0]
Peri Region1	Region_PMS_CONSTRAN_4_REG	Region_PMS_CONSTRAN_1_REG [3:2]	Region_PMS_CONSTRAN_2_REG [3:2]
Peri Region2	Region_PMS_CONSTRAN_5_REG	Region_PMS_CONSTRAN_1_REG [5:4]	Region_PMS_CONSTRAN_2_REG [5:4]
Peri Region3	Region_PMS_CONSTRAN_6_REG	Region_PMS_CONSTRAN_1_REG [7:6]	Region_PMS_CONSTRAN_2_REG [7:6]
Peri Region4	Region_PMS_CONSTRAN_7_REG	Region_PMS_CONSTRAN_1_REG [9:8]	Region_PMS_CONSTRAN_2_REG [9:8]
Peri Region5	Region_PMS_CONSTRAN_8_REG	Region_PMS_CONSTRAN_1_REG [11:10]	Region_PMS_CONSTRAN_2_REG [11:10]
Peri Region6	Region_PMS_CONSTRAN_9_REG	Region_PMS_CONSTRAN_1_REG [13:12]	Region_PMS_CONSTRAN_2_REG [13:12]
Peri Region7	Region_PMS_CONSTRAN_10_REG	Region_PMS_CONSTRAN_1_REG [15:14]	Region_PMS_CONSTRAN_2_REG [15:14]
Peri Region8	Region_PMS_CONSTRAN_11_REG	Region_PMS_CONSTRAN_1_REG [17:16]	Region_PMS_CONSTRAN_2_REG [17:16]
Peri Region9	Region_PMS_CONSTRAN_12_REG	Region_PMS_CONSTRAN_1_REG [19:18]	Region_PMS_CONSTRAN_2_REG [19:18]
Peri Region10	Region_PMS_CONSTRAN_13_REG	Region_PMS_CONSTRAN_1_REG [21:20]	Region_PMS_CONSTRAN_2_REG [21:20]

13.5 External Memory

ESP32-S3 can access the external memory via one of the three ways illustrated in Figure 13-3 below.

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- CPU via SPI1
- CPU via CACHE
- GDMA

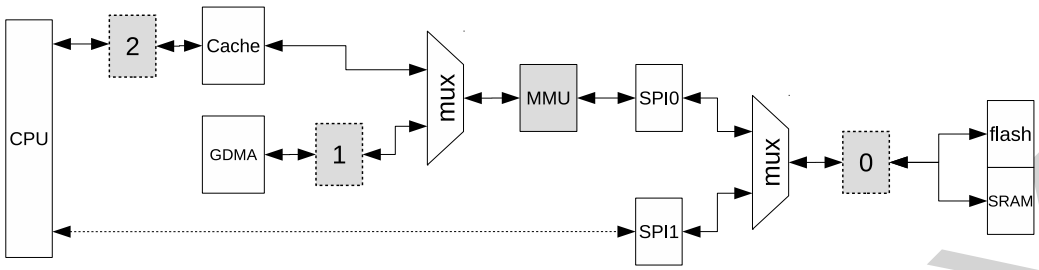


Figure 13-3. Three Ways to Access External Memory

SPI1, CACHE or GDMA must be configured with specific permission before accessing external memory. see illustration in Figure 13-3:

- Box 0 checks the CPU's access to external flash and SRAM
- Box 1 checks GDMA's access to external SRAM
- Box 2 checks CPU's access to external flash and SRAM via CACHE

13.5.1 Address

Both ESP32-S3's flash and SRAM can be further split to achieve more flexible permission control. Each split region can be configured with different access independently.

- Flash can be split into 4 regions, the length of each should be the integral multiples of 64 KB.
- SRAM can be split into 4 regions, the length of each should be the integral multiples of 64 KB.
- Also, the starting address of each region should also be aligned to 64 KB.

The following registers can be used to configure how the flash or SRAM are split.

Table 13-19. Split the External Memory into Split Regions

Split Regions	Split Region Configuration[3]	
	Starting Address[1]	Length[2]
Flash Region*n* (*n*: 0~3)	APB_CTRL_FLASH_ACE_*n*_ADDR_REG	APB_CTRL_FLASH_ACE_*n*_SIZE_REG
SRAM Region*n* (*n*: 0~3)	APB_CTRL_SRAM_ACE_*n*_ADDR_REG	APB_CTRL_SRAM_ACE_*n*_SIZE_REG

[1] Configuring this field with the actual address, which should be aligned to 64 KB.

[2] When configuring the length of Region*n*, note the total length of all flash or SRAM regions should be less than 1 GB, respectively.

[3] Each region cannot overlap with others.

13.5.2 Access Configuration

Each split regions for flash and SRAM can be configured with different permission independently via Registers APB_CTRL_SRAM_ACE*n*_ATTR_REG and APB_CTRL_FLASH_ACE*n*_ATTR.

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Table 13-20. Access Configuration of External Memory Regions

Split Regions	Access Configuration			
	Configuration Registers	CACHE		SPI1 Access[B]
		Secure World[A]	Non-secure World[A]	
Flash Region *n* (*n*: 0 ~ 3)	APB_CTRL_FLASH_ACE*n*_ATTR	[2:0][C]	[5:3]	[7:6][D]
SRAM Region *n* (*n*: 0 ~ 3)	APB_CTRL_SRAM_ACE*n*_ATTR_REG	[2:0]	[5:3]	[7:6]

[A] These bits are configured in order W/R/X

[B] These bits are configured in order W/R

[C] For example, configuring this field to 0b010 indicates CACHE is granted with the read access but not the write or instruction execution accesses from the Secure WORLD to the Flash Region *n*.

[D] For example, configuring this field to 0b01 indicates SPI is granted with the read access but not the write access to the Flash Region *n*.

13.5.3 GDMA

ESP32-S3's 32 MB External SRAM can be independently split into four regions, of which the Region1 and Region2 are accessible to GDMA.

Table 13-21. Split the External SRAM into Four Split Regions for GDMA

Split Regions	Starting Address (included)	Ending Address (not included)[2]
Region0 [3]	0x3C000000	PMS_EDMA_BOUNDARY_0_REG [1,2]
Region1 [4]	PMS_EDMA_BOUNDARY_0_REG [1]	PMS_EDMA_BOUNDARY_1_REG [1,2]
Region2 [4]	PMS_EDMA_BOUNDARY_1_REG [1]	PMS_EDMA_BOUNDARY_2_REG [1,2]
Region3 [3]	PMS_EDMA_BOUNDARY_2_REG [1]	0x3E000000 [2]

[1] When configuring this register, note that you need to write an offset to 0x3C000000 and the unit is 4 KB. For example, configuring the register to 0x80 means that the address is 0x3C000000 + 0x80 * 4KB = 0x3C080000.

[2] The address value filled here is the Ending address plus one. For example, 0x3E000000 means that the end address is 0x3DFFFFFF.

[3] This region cannot be accessed by peripherals via GDMA.

[4] This region can be accessed by some peripherals via GDMA, including SPI2, SPI3, UHCI0, I2S0, I2S1, Camera-LCD Controller, AES, SHA, ADC Controller, and Remote Control Peripheral. See details below.

Users can use the registers below to configure peripherals' access to the second and third External SRAM regions via GDMA.

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Table 13-22. Access Configuration of External SRAM via GDMA

Peripherals	Access Configuration		
	Region1	Region2	Access
SPI2	PMS_EDMA_PMS_SPI2_ATTR1	PMS_EDMA_PMS_SPI2_ATTR2	W/R
SPI3	PMS_EDMA_PMS_SPI3_ATTR1	PMS_EDMA_PMS_SPI3_ATTR2	
UHCI0	PMS_EDMA_PMS_UHCI0_ATTR1	PMS_EDMA_PMS_UHCI0_ATTR2	
I2S0	PMS_EDMA_PMS_I2S0_ATTR1	PMS_EDMA_PMS_I2S0_ATTR2	
I2S1	PMS_EDMA_PMS_I2S1_ATTR1	PMS_EDMA_PMS_I2S1_ATTR2	
Camera-LCD Controller	PMS_EDMA_PMS_LCD_CAM_ATTR1	PMS_EDMA_PMS_LCD_CAM_ATTR2	
AES	PMS_EDMA_PMS_AES_ATTR1	PMS_EDMA_PMS_AES_ATTR2	
SHA	PMS_EDMA_PMS_SHA_ATTR1[A]	PMS_EDMA_PMS_SHA_ATTR2	
ADC Controller	PMS_EDMA_PMS_ADC_DAC_ATTR1	PMS_EDMA_PMS_ADC_DAC_ATTR2	
Remote Control Peripheral	PMS_EDMA_PMS_RMT_ATTR1	PMS_EDMA_PMS_RMT_ATTR2	

[A] For example, configuring this field to 0b10 indicates SHA is granted with the write access but not the read access via GDMA to SRAM Region1.

13.6 Unauthorized Access and Interrupts

Any attempt to access ESP32-S3's slave device without configured permission is considered an **unauthorized access** and will be handled as described below:

- This attempt will only be responded with default values, in particular,
  - All instruction execution or read attempts will be responded with 0 (for internal memory) or 0xdeadbeaf (for external memory)
  - All write attempts will fail
- An interrupt will be triggered (when enabled). See details below.

Note that:

- All permission control related interrupts described in this section can be independently configured for CPU0 and CPU1.
- Only the information of the first interrupt is logged. Therefore, it's advised to handle interrupt signals and clear interrupts in-time, so the information of next interrupt can be logged correctly.

13.6.1 Interrupt upon Unauthorized IBUS Access

ESP32-S3 can be configured to trigger interrupts when IBUS attempts to access internal ROM and SRAM without configured permission, and log the information about this unauthorized access. Note that, once this interrupt is enabled, it's enabled for all internal ROM and SRAM memory, and cannot be only enabled for a certain address field. This interrupt corresponds to the CORE_*m*_IRAM0_PMS_MONITOR_VIOLATE_INTR interrupt source described in Table 8-1 from Chapter 8 *Interrupt Matrix (INTERRUPT)*.

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Table 13-23. Interrupt Registers for Unauthorized IBUS Access

Registers	Bit	Description
PMS_CORE_*m*_IRAM0_PMS_MONITOR_1_REG	[0]	Clears interrupt signal
	[1]	Enables interrupt
PMS_CORE_*m*_IRAM0_PMS_MONITOR_2_REG	[0]	Stores interrupt status of unauthorized IBUS access
	[1]	Stores the access direction. 1: write; 0: read.
	[2]	Stores the instruction direction. 1: load/store; 0: instruction execution.
	[4:3]	Stores the world the CPU was in when the unauthorized IBUS access happened. 0b01: Secure World; 0b10: Non-secure World
	[28:5]	Stores the address that CPU's IBUS was trying to access unauthorized.

13.6.2 Interrupt upon Unauthorized DBUS Access

ESP32-S3 can be configured to trigger interrupts when DBUS attempts to access internal ROM and SRAM without configured permission, and log the information about this unauthorized access. Note that, once this interrupt is enabled, it's enabled for all internal ROM and SRAM memory, and cannot be only enabled for a certain address field. This interrupt corresponds to the CORE_*m*_DRAM0_PMS_MONITOR_VIOLATE_INTR interrupt source described in Table 8-1 from Chapter 8 *Interrupt Matrix (INTERRUPT)*.

Table 13-24. Interrupt Registers for Unauthorized DBUS Access

Registers	Bit	Description
PMS_CORE_*m*_DRAM0_PMS_MONITOR_1_REG	[0]	Clears interrupt signal
	[1]	Enables interrupt
PMS_CORE_*m*_DRAM0_PMS_MONITOR_2_REG	[0]	Stores interrupt status of unauthorized DBUS access
	[1]	Flags atomic access. 1: atomic access; 0: not atomic access.
	[3:2]	Stores the world the CPU was in when the unauthorized DBUS access happened. 0b01: Secure World; 0b10: Non-secure World
	[25:4]	Stores the address that CPU's DBUS was trying to access unauthorized.
PMS_CORE_*m*_DRAM0_PMS_MONITOR_3_REG	[0]	Stores the access direction. 1: write; 0: read.
	[25:4]	Stores the byte information of the unauthorized DBUS access.

13.6.3 Interrupt upon Unauthorized Access to External Memory

ESP32-S3 can be configured to trigger Interrupt upon unauthorized access to external memory, and log the information about this unauthorized access. This interrupt corresponds to the SPI_MEM_REJECT_INTR interrupt source described in Table 8-1 from Chapter 8 *Interrupt Matrix (INTERRUPT)*.

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Table 13-25. Interrupt Registers for Unauthorized Access to External Memory

Registers	Bit	Description
APB_CTRL_SPI_MEM_PMS_CTRL_REG	[0]	Stores exception signal
	[1]	Clears exception signal and logged information
	[2]	Indicates unauthorized instruction execution
	[3]	Indicates unauthorized read
	[4]	Indicates unauthorized write
	[5]	Indicates overlapping split regions
	[6]	Indicates invalid address

13.6.4 Interrupt upon Unauthorized Access to Internal Memory via GDMA

ESP32-S3 can be configured to trigger Interrupt upon unauthorized access to internal memory via GDMA, and log the information about this unauthorized access. This interrupt corresponds to the DMA_APB_PMS_MONITOR_VIOLATE_INTR interrupt source described in Table 8-1 from Chapter 8 *Interrupt Matrix (INTERRUPT)*.

Table 13-26. Interrupt Registers for Unauthorized Access to Internal Memory via GDMA

Registers	Bit	Description
PMS_DMA_APBPERI_PMS_MONITOR_1_REG	[0]	Clears interrupt signal
	[1]	Enables interrupt
PMS_DMA_APBPERI_PMS_MONITOR_2_REG	[0]	Stores interrupt signal
	[2:1]	Stores the world the CPU was in when the unauthorized access happened. 0b01: Secure World; 0b10: Non-secure World
	[24:3]	Stores the address that GDMA was trying to access unauthorized
PMS_DMA_APBPERI_PMS_MONITOR_3_REG	[0]	Stores the access direction. 1: write; 0: read
	[16:1]	Stores the byte information of unauthorized access

For information about Interrupt upon unauthorized access to external memory via GDMA, please refer to Chapter 2 *GDMA Controller (GDMA)*

13.6.5 Interrupt upon Unauthorized peripheral bus (PIF) Access

ESP32-S3 can be configured to trigger interrupts when PIF attempts to access RTC FAST memory, RTC SLOW memory, and peripheral regions without configured permission, and log the information about this unauthorized access. Note that, once this interrupt is enabled, it's enabled for all RTC FAST memory, RTC SLOW memory, and peripheral regions, and cannot be only enabled for a certain address field. This interrupt corresponds to the CORE_*m*_PIF_PMS_MONITOR_VIOLATE_INTR interrupt source described in Table 8-1 from Chapter 8 *Interrupt Matrix (INTERRUPT)*.

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Table 13-27. Interrupt Registers for Unauthorized PIF Access

Registers	Bit	Description
PMS_CORE_*m*_PIF_PMS_MONITOR_1_REG	[1]	Enables interrupt
	[0]	Clears interrupt signal and logged information
PMS_CORE_*m*_PIF_PMS_MONITOR_2_REG	[7:6]	Stores the world the CPU was in when the unauthorized PIF access happened. 0b01: Secure World; 0b10: Non-secure World
	[5]	Stores the access direction. 1: write; 0: read
	[4:2]	Stores the data type of unauthorized access. 0: byte; 1: half-word; 2: word
	[1]	Stores the access type. 0: instruction; 1: data
	[0]	Stores the interrupt signal
PMS_CORE_*m*_PIF_PMS_MONITOR_3_REG	[31:0]	Stores the address of unauthorized access

In particular, ESP32-S3 can also be configured to check the access alignment when PIF attempts to access the peripheral regions, and trigger Interrupt upon unauthorized alignment. See detailed description in the following section.

13.6.6 Interrupt upon Unauthorized PIF Access Alignment

Access to all of ESP32-S3's modules / peripherals (excluding RTC FAST memory and SLOW memory) is **word aligned**.

ESP32-S3 can be configured to check the access alignment to all modules / peripherals, and trigger Interrupt upon **non-word aligned access**.

This interrupt corresponds to the CORE_*m*_PIF_PMS_MONITOR_VIOLATE_SIZE_INTR interrupt source described in Table 8-1 from Chapter 8 *Interrupt Matrix (INTERRUPT)*.

Note that CPU can convert some non-word aligned access to word aligned access, thus avoiding triggering alignment interrupt.

Table 13-28 below lists all the possible access alignments and their results (when interrupt is enabled), in which:

- **INTR**: interrupt
- √: access succeeds and no interrupt.

Table 13-28. All Possible Access Alignment and their Results

Accessed Address	Access Alignment	Read	Write
0x0	Byte aligned	INTR	INTR
	Half-word aligned	INTR	INTR
	Word aligned	√	√
0x1	Byte aligned	INTR	INTR
	Half-word aligned	√	INTR
	Word aligned	√	INTR
0x2	Byte aligned	INTR	INTR
	Half-word aligned	INTR	INTR

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Accessed Address	Access Alignment	Read	Write
	Word aligned	√	INTR
0x3	Byte aligned	INTR	INTR
	Half-word aligned	√	INTR
	Word aligned	√	INTR

Table 13-29. Interrupt Registers for Unauthorized Access Alignment

Registers	Bit	Description
PMS_CORE_*m*_PIF_PMS_MONITOR_4_REG	[1]	Enables interrupt
	[0]	Clears interrupt signal and logged information
PMS_CORE_*m*_PIF_PMS_MONITOR_5_REG	[4:3]	Stores the world the CPU was in when the unauthorized access happened. 0b01: Secure World; 0b10: Non-secure World
	[2:1]	Stores the unauthroized access type. 0: byte aligned; 1: half-word aligned; 2: word aligned
	[0]	Stores the interrupt status. 0: no interrupt; 1: interrupt
PMS_CORE_*m*_PIF_PMS_MONITOR_6_REG	[31:0]	Stores the address of the unauthorized access

13.7 Protection of CPU VECBASE Registers

CPU's VECBASE registers store the base addresses of interrupts and exceptions table. To protect these registers from unauthorized modification, ESP32-S3 has implemented a special mechanism.

Users can first configure values stored in VECBASE registers to the PMS_CORE_*m*_VECBASE_OVERRIDE_WORLD*n*_VALUE field of the PMS_CORE_*m*_VECBASE_OVERRIDE_*n*_REG register, and then use the configured PMS_CORE_*m*_VECBASE_OVERRIDE_WORLD*n*_VALUE values, instead of VECBASE values. Then by only allowing modification to the PMS_CORE_*m*_VECBASE_OVERRIDE_*n*_REG register values from the Secure World, the integrity of values stored in VECBASE registers are protected.

The detailed steps are described below:

1. Write the CPU*m*'s VECBASE value in Secure World to the PMS_CORE_*m*_VECBASE_OVERRIDE_WORLD0_VALUE field.
2. Write the CPU*m*'s VECBASE value in Non-secure World to the PMS_CORE_*m*_VECBASE_OVERRIDE_WORLD1_VALUE field.
3. Configure the PMS_CORE_*m*_VECBASE_OVERRIDE_SEL field of the PMS_CORE_*m*_VECBASE_OVERRIDE_1_REG register by setting it to:
   - 2'b00: just use CPU*m*'s VECBASE register directly.
   - 2'b11: use the value configured in PMS_CORE_*m*_VECBASE_OVERRIDE_WORLD*n*_VALUE, instead of the value in CPU*m*'s VECBASE register
   - Do not configuring this field to other values.
4. Configure the PMS_CORE_*m*_VECBASE_WORLD_MASK field of the PMS_CORE_*m*_VECBASE_OVERRIDE_0_REG register by setting it to:

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- 1: CPU*m* uses WORLD0_VALUE in both the Secure World and the Non-secure World.
- 0: CPU*m* uses WORLD0_VALUE in the Secure World, and WORLD1_VALUE in the Non-secure World.

13.8 Register Locks

All ESP32-S3's permission control related registers can be locked by respective lock registers. When the lock registers are configured to 1, these registers themselves and their related permission control registers are all protected from modification until the next CPU reset.

Note that there isn't one-to-one correspondence between the lock registers and permission control registers. See details in Table 13-30.

Table 13-30. Lock Registers and Related Permission Control Registers

Lock Registers	Related Permission Control Registers
VECBASE Configuration	
PMS_CORE_*m*_VECBASE_OVERRIDE_LOCK_REG	PMS_CORE_*m*_VECBASE_OVERRIDE_LOCK_REG
	PMS_CORE_*m*_VECBASE_OVERRIDE_0_REG
	PMS_CORE_*m*_VECBASE_OVERRIDE_1_REG
	PMS_CORE_*m*_VECBASE_OVERRIDE_2_REG
Lock Internal SRAM's Usage and Access Configuration	
PMS_INTERNAL_SRAM_USAGE_0_REG	PMS_INTERNAL_SRAM_USAGE_0_REG
	PMS_INTERNAL_SRAM_USAGE_1_REG
	PMS_INTERNAL_SRAM_USAGE_2_REG
PMS_CORE_X_IRAM0_PMS_CONSTRAIN_0_REG	PMS_CORE_X_IRAM0_PMS_CONSTRAIN_0_REG
	PMS_CORE_X_IRAM0_PMS_CONSTRAIN_1_REG
	PMS_CORE_X_IRAM0_PMS_CONSTRAIN_2_REG
PMS_CORE_*m*_IRAM0_PMS_MONITOR_0_REG	PMS_CORE_*m*_IRAM0_PMS_MONITOR_0_REG
	PMS_CORE_*m*_IRAM0_PMS_MONITOR_1_REG
PMS_CORE_X_DRAM0_PMS_CONSTRAIN_0_REG	PMS_CORE_X_DRAM0_PMS_CONSTRAIN_0_REG
	PMS_CORE_X_DRAM0_PMS_CONSTRAIN_1_REG
PMS_CORE_*m*_DRAM0_PMS_MONITOR_0_REG	PMS_CORE_*m*_DRAM0_PMS_MONITOR_0_REG
	PMS_CORE_*m*_DRAM0_PMS_MONITOR_1_REG
Lock Internal SRAM's Split Lines Configuration	
PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_0_REG	PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_0_REG
	PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_*n*_REG (*n*: 1 - 5)
Lock CPU's Permission to Different Peripheral	
PMS_CORE_*m*_PIF_PMS_CONSTRAIN_0_REG	PMS_CORE_*m*_PIF_PMS_CONSTRAIN_0_REG
	PMS_CORE_*m*_PIF_PMS_CONSTRAIN_*n*_REG (*n*: 1 - 14)
PMS_CORE_*m*_REGION_PMS_CONSTRAIN_0_REG	PMS_CORE_*m*_REGION_PMS_CONSTRAIN_0_REG
	PMS_CORE_*m*_REGION_PMS_CONSTRAIN_*n*_REG (*n*: 1 - 14)
PMS_CORE_*m*_PIF_PMS_MONITOR_0_REG	PMS_CORE_*m*_PIF_PMS_CONSTRAIN_0_REG
	PMS_CORE_*m*_PIF_PMS_MONITOR_1_REG (*n*: 1 - 6)
Lock Peripherals' GDMA Access to Internal SRAM	

PRELIMINARY

Lock Registers	Related Permission Control Registers
PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_0_REG	PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_0_REG
	PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_1_REG
PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_0_REG	PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_0_REG
	PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_1_REG
PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_0 _REG	PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_0_REG
	PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_1_REG
PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_0_REG	PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_0_REG
	PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_1_REG
PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_1_REG	PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_0_REG
	PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_1_REG
PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_0_REG	PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_0_REG
	PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_1_REG
PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_0_REG	PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_0_REG
	PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_1_REG
PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_0 _REG	PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_0 _REG
	PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_1 _REG
PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_0_REG	PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_0_REG
	PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_1_REG
PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_0 _REG	PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_0 _REG
	PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_1 _REG
PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_0_REG	PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_0_REG
	PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_1_REG
PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_0_REG	PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_0_REG
	PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_1_REG
PMS_DMA_APBPERI_PMS_MONITOR_0_REG	PMS_DMA_APBPERI_PMS_MONITOR_0_REG
	PMS_DMA_APBPERI_PMS_MONITOR_1_REG
	PMS_DMA_APBPERI_PMS_MONITOR_2_REG
	PMS_DMA_APBPERI_PMS_MONITOR_3_REG
Lock Peripherals' Access to External SRAM	
PMS_EDMA_BOUNDARY_LOCK_REG	PMS_EDMA_BOUNDARY_LOCK_REG
	PMS_EDMA_BOUNDARY_0_REG
	PMS_EDMA_BOUNDARY_1_REG
	PMS_EDMA_BOUNDARY_2_REG
PMS_EDMA_PMS_SPI2_LOCK_REG	PMS_EDMA_PMS_SPI2_LOCK_REG
	PMS_EDMA_PMS_SPI2_REG
PMS_EDMA_PMS_SPI3_LOCK_REG	PMS_EDMA_PMS_SPI3_LOCK_REG
	PMS_EDMA_PMS_SPI3_REG
PMS_EDMA_PMS_UHCI0_LOCK_REG	PMS_EDMA_PMS_UHCI0_LOCK_REG
	PMS_EDMA_PMS_UHCI0_REG

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Lock Registers	Related Permission Control Registers
PMS_EDMA_PMS_I2S0_LOCK_REG	PMS_EDMA_PMS_I2S0_LOCK_REG
	PMS_EDMA_PMS_I2S0_REG
PMS_EDMA_PMS_I2S1_LOCK_REG	PMS_EDMA_PMS_I2S1_LOCK_REG
	PMS_EDMA_PMS_I2S1_REG
PMS_EDMA_PMS_LCD_CAM_LOCK_REG	PMS_EDMA_PMS_LCD_CAM_LOCK_REG
	PMS_EDMA_PMS_LCD_CAM_REG
PMS_EDMA_PMS_AES_LOCK_REG	PMS_EDMA_PMS_AES_LOCK_REG
	PMS_EDMA_PMS_AES_REG
PMS_EDMA_PMS_AES_LOCK_REG	PMS_EDMA_PMS_AES_LOCK_REG
	PMS_EDMA_PMS_AES_REG
PMS_EDMA_PMS_SHA_LOCK_REG	PMS_EDMA_PMS_SHA_LOCK_REG
	PMS_EDMA_PMS_SHA_REG
PMS_EDMA_PMS_ADC_DAC_LOCK_REG	PMS_EDMA_PMS_ADC_DAC_LOCK_REG
	PMS_EDMA_PMS_ADC_DAC_REG
PMS_EDMA_PMS_RMT_LOCK_REG	PMS_EDMA_PMS_RMT_LOCK_REG
	PMS_EDMA_PMS_RMT_REG

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13.9 Register Summary

The addresses of registers starting from PMS in this section are relative to the Permission Control base address, and the addresses of registers starting from APB in this section are relative to the ABP Controller base address. Both base address are provided in Table 3-3 in Chapter 3 *System and Memory*.

Note that, all registers with CORE_X in this section apply to both CPUs. The list of registers below is for CPU0 only. CPU1 shares exactly the same set of registers. Adding 0x0400 to the offset of the equivalent of CPU0 register gives you address for CPU1 registers.

For example, the offset for CPU0 register PMS_CORE_0_IRAM0_PMS_MONITOR_0_REG is 0x00E4, the offset for CPU1 equivalent PMS_CORE_1_IRAM0_PMS_MONITOR_0_REG should be 0x00E4 + 0x0400, which is 0x04E4.

Name	Description	Address	Access
Configuration Register			
PMS_APB_PERIPHERAL_ACCESS_0_REG	APB peripheral configuration register 0	0x0008	R/W
PMS_APB_PERIPHERAL_ACCESS_1_REG	APB peripheral configuration register 1	0x000C	R/W
PMS_INTERNAL_SRAM_USAGE_0_REG	Internal SRAM configuration register 0	0x0010	R/W
PMS_INTERNAL_SRAM_USAGE_1_REG	Internal SRAM configuration register 1	0x0014	R/W
PMS_INTERNAL_SRAM_USAGE_2_REG	Internal SRAM configuration register 2	0x0018	R/W
PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_0_REG	SPI2 GDMA Permission Config Register 0	0x0038	R/W
PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_1_REG	SPI2 GDMA Permission Config Register 1	0x003C	R/W
PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_0_REG	SPI3 GDMA Permission Config Register 0	0x0040	R/W
PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_1_REG	SPI3 GDMA Permission Config Register 1	0x0044	R/W
PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_0_REG	UHCI0 GDMA Permission Config Register 0	0x0048	R/W
PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_1_REG	UHCI0 GDMA Permission Config Register 1	0x004C	R/W
PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_0_REG	I2S0 GDMA Permission Config Register 0	0x0050	R/W
PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_1_REG	I2S0 GDMA Permission Config Register 1	0x0054	R/W
PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_0_REG	I2S1 GDMA Permission Config Register 0	0x0058	R/W
PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_1_REG	I2S1 GDMA Permission Config Register 1	0x005C	R/W
PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_0_REG	AES GDMA Permission Config Register 0	0x0070	R/W
PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_1_REG	AES GDMA Permission Config Register 1	0x0074	R/W
PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_0_REG	SHA GDMA Permission Config Register 0	0x0078	R/W
PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_1_REG	SHA GDMA Permission Config Register 1	0x007C	R/W

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Name	Description	Address	Access
PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_0_REG	ADC_DAC GDMA Permission Config Register 0	0x0080	R/W
PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_1_REG	ADC_DAC GDMA Permission Config Register 1	0x0084	R/W
PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_0_REG	RMT GDMA Permission Config Register 0	0x0088	R/W
PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_1_REG	RMT GDMA Permission Config Register 1	0x008C	R/W
PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_0_REG	LCD_CAM GDMA Permission Config Register 0	0x0090	R/W
PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_1_REG	LCD_CAM GDMA Permission Config Register 1	0x0094	R/W
PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_0_REG	USB GDMA Permission Config Register 0	0x0098	R/W
PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_1_REG	USB GDMA Permission Config Register 0	0x009C	R/W
PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_0_REG	SDI0 GDMA Permission Config Register 0	0x00A8	R/W
PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_1_REG	SDI0 GDMA Permission Config Register 1	0x00AC	R/W
PMS_DMA_APBPERI_PMS_MONITOR_0_REG	GDMA Permission Interrupt Register 0	0x00B0	R/W
PMS_DMA_APBPERI_PMS_MONITOR_1_REG	GDMA Permission Interrupt Register 1	0x00B4	R/W
PMS_DMA_APBPERI_PMS_MONITOR_2_REG	GDMA Permission Interrupt Register 2	0x00B8	RO
PMS_DMA_APBPERI_PMS_MONITOR_3_REG	GDMA Permission Interrupt Register 3	0x00BC	RO
PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_0_REG	SRAM Split Line Config Register 0	0x00C0	R/W
PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_1_REG	SRAM Split Line Config Register 1	0x00C4	R/W
PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_2_REG	SRAM Split Line Config Register 2	0x00C8	R/W
PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_3_REG	SRAM Split Line Config Register 3	0x00CC	R/W
PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_4_REG	SRAM Split Line Config Register 4	0x00D0	R/W
PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_5_REG	SRAM Split Line Config Register 5	0x00D4	R/W
PMS_CORE_X_IRAM0_PMS_CONSTRAIN_0_REG	IBUS Permission Config Register 0	0x00D8	R/W
PMS_CORE_X_IRAM0_PMS_CONSTRAIN_1_REG	IBUS Permission Config Register 1	0x00DC	R/W
PMS_CORE_X_IRAM0_PMS_CONSTRAIN_2_REG	IBUS Permission Config Register 2	0x00E0	R/W

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Name	Description	Address	Access
PMS_CORE_0_IRAM0_PMS_MONITOR_0_REG	CPU0 IBUS Permission Interrupt Register 0	0x00E4	R/W
PMS_CORE_0_IRAM0_PMS_MONITOR_1_REG	CPU0 IBUS Permission Interrupt Register 1	0x00E8	R/W
PMS_CORE_X_DRAM0_PMS_CONSTRAIN_0_REG	DBUS Permission Config Register 0	0x00FC	R/W
PMS_CORE_X_DRAM0_PMS_CONSTRAIN_1_REG	DBUS Permission Config Register 1	0x0100	R/W
PMS_CORE_0_DRAM0_PMS_MONITOR_0_REG	CPU0 dBUS Permission Interrupt Register 0	0x0104	R/W
PMS_CORE_0_DRAM0_PMS_MONITOR_1_REG	CPU0 dBUS Permission Interrupt Register 1	0x0108	R/W
PMS_CORE_0_PIF_PMS_CONSTRAIN_*n*_REG (*n*: 0 -14)	Peripheral Permission Configuration Registers	0x0124	R/W
PMS_CORE_0_REGION_PMS_CONSTRAIN_0_REG	CPU0 Split_Region Permission Register 0	0x0160	R/W
PMS_CORE_0_REGION_PMS_CONSTRAIN_1_REG	CPU0 Split_Region Permission Register 1	0x0164	R/W
PMS_CORE_0_REGION_PMS_CONSTRAIN_2_REG	CPU0 Split_Region Permission Register 2	0x0168	R/W
PMS_CORE_0_REGION_PMS_CONSTRAIN_3_REG	CPU0 Split_Region Permission Register 3	0x016C	R/W
PMS_CORE_0_PIF_PMS_MONITOR_0_REG	CPU0 PIF Permission Interrupt Register 0	0x019C	R/W
PMS_CORE_0_PIF_PMS_MONITOR_1_REG	CPU0 PIF Permission Interrupt Register 1	0x01A0	R/W
PMS_CORE_0_PIF_PMS_MONITOR_4_REG	CPU0 PIF Permission Interrupt Register 4	0x01AC	R/W
PMS_CORE_0_VECBASE_OVERRIDE_LOCK_REG	CPU0 vecbase override configuration register 0	0x01B8	R/W
PMS_CORE_0_VECBASE_OVERRIDE_0_REG	CPU0 vecbase override configuration register 0	0x01BC	R/W
PMS_CORE_0_VECBASE_OVERRIDE_1_REG	CPU0 vecbase override configuration register 1	0x01C0	R/W
PMS_CORE_0_VECBASE_OVERRIDE_2_REG	CPU0 vecbase override configuration register 1	0x01C4	R/W
PMS_EDMA_BOUNDARY_LOCK_REG	EDMA Boundary Lock Register	0x02A8	R/W
PMS_EDMA_BOUNDARY_0_REG	EDMA Boundary 0 Config Register	0x02AC	R/W
PMS_EDMA_BOUNDARY_1_REG	EDMA Boundary 1 Config Register	0x02B0	R/W
PMS_EDMA_BOUNDARY_2_REG	EDMA Boundary 2 Config Register 0	0x02B4	R/W
PMS_EDMA_PMS_SPI2_LOCK_REG	SPI2 External Memory Permission Lock Register	0x02B8	R/W
PMS_EDMA_PMS_SPI2_REG	SPI2 External Memory Permission Config Register	0x02BC	R/W
PMS_EDMA_PMS_SPI3_LOCK_REG	SPI3 External Memory Permission Lock Register	0x02C0	R/W
PMS_EDMA_PMS_SPI3_REG	SPI3 External Memory Permission Config Register	0x02C4	R/W
PMS_EDMA_PMS_UHCI0_LOCK_REG	UHCI0 External Memory Permission Lock Register	0x02C8	R/W

PRELIMINARY

Name	Description	Address	Access
PMS_EDMA_PMS_UHCI0_REG	UHCI0 External Memory Permission Config Register	0x02CC	R/W
PMS_EDMA_PMS_I2S0_LOCK_REG	I2S0 External Memory Permission Lock Register	0x02D0	R/W
PMS_EDMA_PMS_I2S0_REG	I2S0 External Memory Permission Config Register	0x02D4	R/W
PMS_EDMA_PMS_I2S1_LOCK_REG	I2S1 External Memory Permission Lock Register	0x02D8	R/W
PMS_EDMA_PMS_I2S1_REG	I2S1 External Memory Permission Config Register	0x02DC	R/W
PMS_EDMA_PMS_LCD_CAM_LOCK_REG	LCD/CAM External Memory Permission Lock Register	0x02E0	R/W
PMS_EDMA_PMS_LCD_CAM_REG	LCD/CAM External Memory Permission Config Register	0x02E4	R/W
PMS_EDMA_PMS_AES_LOCK_REG	AES External Memory Permission Lock Register	0x02E8	R/W
PMS_EDMA_PMS_AES_REG	AES External Memory Permission Config Register	0x02EC	R/W
PMS_EDMA_PMS_SHA_LOCK_REG	SHA External Memory Permission Lock Register	0x02F0	R/W
PMS_EDMA_PMS_SHA_REG	SHA External Memory Permission Config Register	0x02F4	R/W
PMS_EDMA_PMS_ADC_DAC_LOCK_REG	ADC/DAC External Memory Permission Lock Register	0x02F8	R/W
PMS_EDMA_PMS_ADC_DAC_REG	ADC/DAC External Memory Permission Config Register	0x02FC	R/W
PMS_EDMA_PMS_RMT_LOCK_REG	RMT External Memory Permission Lock Register	0x0300	R/W
PMS_EDMA_PMS_RMT_REG	RMT Permission Config Register	0x0304	R/W
PMS_CLOCK_GATE_REG_REG	Clock Gate Config Register	0x0308	R/W
Status Register			
PMS_CORE_0_IRAM0_PMS_MONITOR_2_REG	CPU0 IBUS Permission Interrupt Register 2	0x00EC	RO
PMS_CORE_0_DRAM0_PMS_MONITOR_2_REG	CPU0 dBUS Permission Interrupt Register 2	0x010C	RO
PMS_CORE_0_DRAM0_PMS_MONITOR_3_REG	CPU0 dBUS Permission Interrupt Register 3	0x0110	RO
PMS_CORE_0_PIF_PMS_MONITOR_2_REG	CPU0 PIF Permission Interrupt Register 2	0x01A4	RO
PMS_CORE_0_PIF_PMS_MONITOR_3_REG	CPU0 PIF Permission Interrupt Register 3	0x01A8	RO
PMS_CORE_0_PIF_PMS_MONITOR_5_REG	CPU0 PIF Permission Interrupt Register 5	0x01B0	RO
PMS_CORE_0_PIF_PMS_MONITOR_6_REG	CPU0 PIF Permission Interrupt Register 6	0x01B4	RO

PRELIMINARY

Name	Description	Address	Access
Version Register			
PMS_DATE_REG	Sensitive Version Register	0x0FFC	R/W

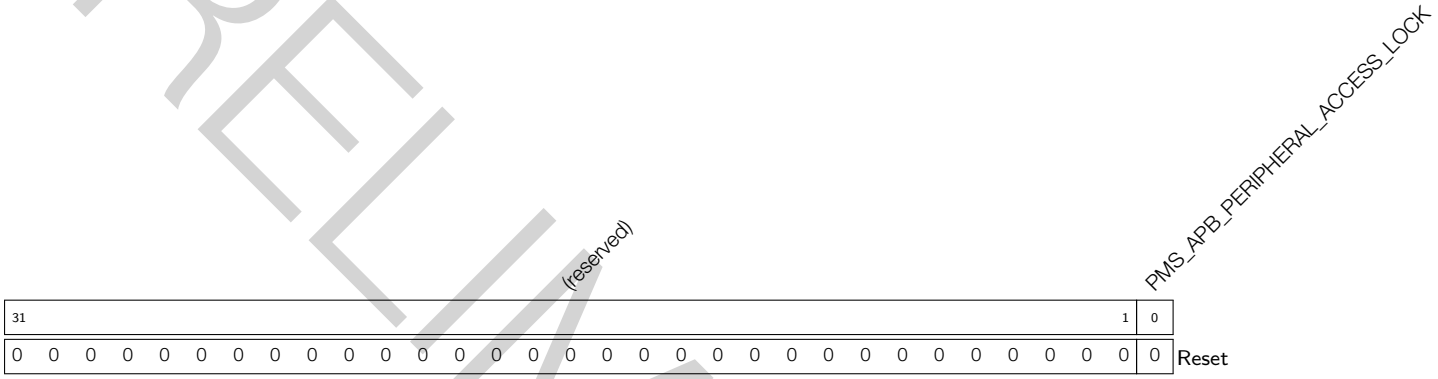
Name	Description	Address	Access
Configuration Registers			
APB_CTRL_EXT_MEM_PMS_LOCK_REG	External Memory Permission Lock Register	0x0020	R/W
APB_CTRL_FLASH_ACE*n*_ATTR_REG	Flash Area*n* Permission Config Register	0x0028	R/W
APB_CTRL_SRAM_ACE*n*_ADDR_S	Flash Area*n* Starting Address Config Register	0x0038	R/W
APB_CTRL_FLASH_ACE*n*_SIZE_REG	Flash Area*n* Length Config Register	0x0048	R/W
APB_CTRL_SRAM_ACE*n*_ATTR_REG	External SRAM Area*n* Permission Config Register	0x0058	R/W
APB_CTRL_SRAM_ACE*n*_ADDR_REG	External SRAM Area*n* Starting Address Config Register	0x0068	R/W
APB_CTRL_SRAM_ACE*n*_SIZE_REG	External SRAM Area*n* Length Config Register	0x0078	R/W
APB_CTRL_SPI_MEM_PMS_CTRL_REG	External Memory Unauthorized Access Interrupt Register	0x0088	varies
APB_CTRL_SPI_MEM_REJECT_ADDR_REG	External Memory Unauthorized Access Address Register	0x008C	RO

PRELIMINARY

13.10 Registers

The addresses of registers starting from PMS in this section are relative to the Permission Control base address, and the addresses of registers starting from APB in this section are relative to the ABP Controller base address. Both base address are provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 13.1. PMS_APB_PERIPHERAL_ACCESS_0_REG (0x0008)



PMS_APB_PERIPHERAL_ACCESS_LOCK Set this bit to lock APB peripheral configuration register. (R/W)

PRELIMINARY

Register 13.2. PMS_APB_PERIPHERAL_ACCESS_1_REG (0x000C)

PMS_APB_PERIPHERAL_ACCESS_SPLIT_BURST Set this bit to allow the PIF bus to initiate back to back access to peripheral regions. (R/W)

Register 13.3. PMS_INTERNAL_SRAM_USAGE_0_REG (0x0010)

PMS_INTERNAL_SRAM_USAGE_LOCK Set this bit to lock internal SRAM Configuration Register. (R/W)

PRELIMINARY

Register 13.4. PMS_INTERNAL_SRAM_USAGE_1_REG (0x0014)

PMS_INTERNAL_SRAM_ICACHE_USAGE Configures certain blocks of SRAM0 are allocated for CPU or ICACHE. (R/W)

PMS_INTERNAL_SRAM_DCACHE_USAGE Configures certain blocks of SRAM2 are allocated for CPU or DCACHE. (R/W)

PMS_INTERNAL_SRAM_CPU_USAGE Configures this field to allow CPU to use certain blocks of SRAM1. (R/W)

PRELIMINARY

Register 13.5. PMS_INTERNAL_SRAM_USAGE_2_REG (0x0018)

PMS_INTERNAL_SRAM_CORE0_TRACE_USAGE Configure this field to choose a certain block in SRAM1 as the trace memory block for CPU0. (R/W)

PMS_INTERNAL_SRAM_CORE1_TRACE_USAGE Configure this field to choose a certain block in SRAM1 as the trace memory block for CPU1. (R/W)

PMS_INTERNAL_SRAM_CORE0_TRACE_ALLOC Configure this field to choose a certain 16 KB in the selected trace memory block as trace memory for CPU0. (R/W)

PMS_INTERNAL_SRAM_CORE1_TRACE_ALLOC Configure this field to choose a certain 16 KB in the selected trace memory block as trace memory for CPU1. (R/W)

PRELIMINARY

Register 13.6. PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_0_REG (0x0038)

PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_LOCK Set this bit to lock SPI2's GDMA permission configuration register. (R/W)

PRELIMINARY

Register 13.7. PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_1_REG (0x003C)

PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_SRAM_PMS_0 Configure SPI2's permission to the instruction region. (R/W)

PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_SRAM_PMS_1 Configure SPI2's permission to data region0 of SRAM. (R/W)

PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_SRAM_PMS_2 Configure SPI2's permission to data region1 of SRAM. (R/W)

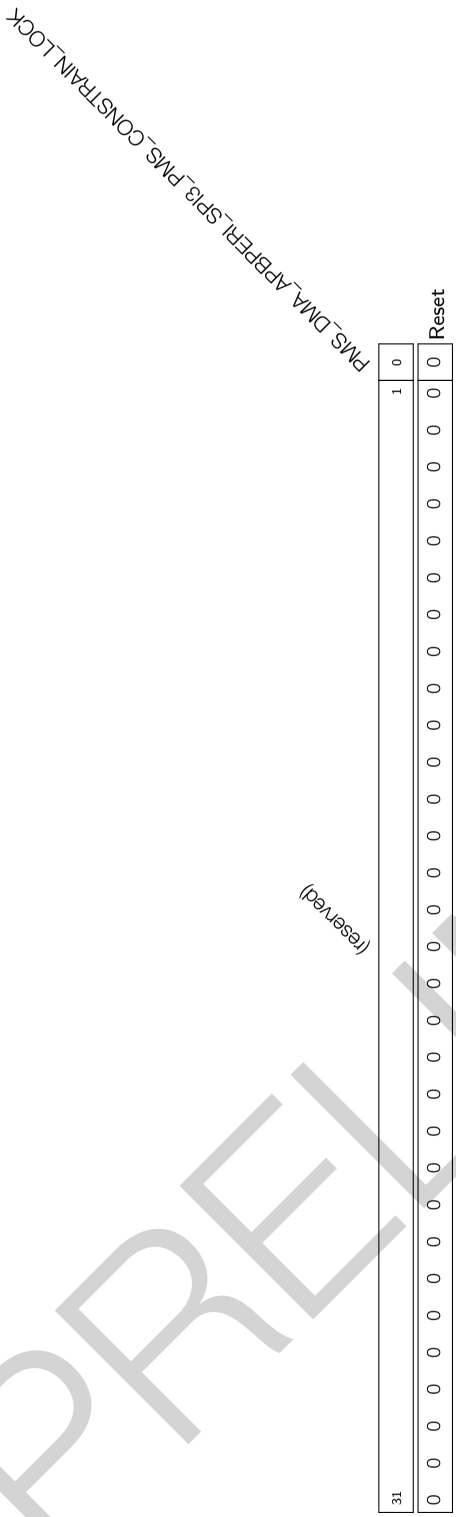
PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_SRAM_PMS_3 Configure SPI2's permission to data region2 of SRAM. (R/W)

PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure SPI2's permission to SRAM block9. (R/W)

PMS_DMA_APBPERI_SPI2_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure SPI2's permission to SRAM block10. (R/W)

PRELIMINARY

Register 13.8. PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_0_REG (0x0040)



PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_LOCK Set this bit to lock SPI3's GDMA permission configuration register. (R/W)

PRELIMINARY

Register 13.9. PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_1_REG (0x0044)

PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_SRAM_PMS_0 Configure SPI3's permission to the instruction region. (R/W)

PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_SRAM_PMS_1 Configure SPI3's permission to the data region0. (R/W)

PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_SRAM_PMS_2 Configure SPI3's permission to the data region1. (R/W)

PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_SRAM_PMS_3 Configure SPI3's permission to the data region2. (R/W)

PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure SPI3's permission to SRAM block9. (R/W)

PMS_DMA_APBPERI_SPI3_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure SPI3's permission to SRAM block10. (R/W)

PRELIMINARY

Register 13.10. PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_0_REG (0x0048)

PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_LOCK Set this bit to lock UHCI0's GDMA permission configuration register. (R/W)

PRELIMINARY

Register 13.11. PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_1_REG (0x004C)

PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_SRAM_PMS_0 Configure UHCI0's permission to the instruction region. (R/W)

PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_SRAM_PMS_1 Configure UHCI0's permission to data region0 of SRAM. (R/W)

PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_SRAM_PMS_2 Configure UHCI0's permission to data region1 of SRAM. (R/W)

PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_SRAM_PMS_3 Configure UHCI0's permission to data region2 of SRAM. (R/W)

PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure UHCI0's permission to SRAM block9. (R/W)

PMS_DMA_APBPERI_UHCI0_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure UHCI0's permission to SRAM block10. (R/W)

PRELIMINARY

Register 13.12. PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_0_REG (0x0050)

PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_LOCK Set this bit to lock I2S0's GDMA permission configuration register. (R/W)

PRELIMINARY

Register 13.13. PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_1_REG (0x0054)

PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_SRAM_PMS_0 Configure I2S0's permission to the instruction region. (R/W)

PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_SRAM_PMS_1 Configure I2S0's permission to data region0 of SRAM. (R/W)

PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_SRAM_PMS_2 Configure I2S0's permission to data region1 of SRAM. (R/W)

PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_SRAM_PMS_3 Configure I2S0's permission to data region2 of SRAM. (R/W)

PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure I2S0's permission to SRAM block9. (R/W)

PMS_DMA_APBPERI_I2S0_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure I2S0's permission to SRAM block10. (R/W)

PRELIMINARY

Register 13.14. PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_0_REG (0x0058)

PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_LOCK Set this bit to lock I2S1's GDMA permission configuration register.(R/W)

PRELIMINARY

Register 13.15. PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_1_REG (0x005C)

PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_SRAM_PMS_0 Configure I2S1's permission to the instruction region. (R/W)

PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_SRAM_PMS_1 Configure I2S1's permission to data region0 of SRAM. (R/W)

PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_SRAM_PMS_2 Configure I2S1's permission to data region1 of SRAM. (R/W)

PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_SRAM_PMS_3 Configure I2S1's permission to data region2 of SRAM.(R/W)

PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure I2S1's permission to SRAM block9. (R/W)

PMS_DMA_APBPERI_I2S1_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure I2S1's permission to SRAM block10. (R/W)

PRELIMINARY

Register 13.16. PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_0_REG (0x0070)

PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_LOCK Set this bit to lock AES's GDMA permission configuration register. (R/W)

PRELIMINARY

Register 13.17. PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_1_REG (0x0074)

PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_SRAM_PMS_0 Configure AES's permission to the instruction region.(R/W)

PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_SRAM_PMS_1 Configure AES's permission to data region0 of SRAM. (R/W)

PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_SRAM_PMS_2 Configure AES's permission to data region1 of SRAM. (R/W)

PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_SRAM_PMS_3 Configure AES's permission to data region2 of SRAM. (R/W)

PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure AES's permission to SRAM block9. (R/W)

PMS_DMA_APBPERI_AES_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure AES's permission to SRAM block10. (R/W)

PRELIMINARY

Register 13.18. PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_0_REG (0x0078)

PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_LOCK Set this bit to lock SHA's GDMA permission configuration register. (R/W)

PRELIMINARY

Register 13.19. PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_1_REG (0x007C)

PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_SRAM_PMS_0 Configure SHA's permission to the instruction region. (R/W)

PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_SRAM_PMS_1 Configure SHA's permission to data region0 of SRAM. (R/W)

PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_SRAM_PMS_2 Configure SHA's permission to data region1 of SRAM. (R/W)

PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_SRAM_PMS_3 Configure SHA's permission to data region2 of SRAM. (R/W)

PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure SHA's permission to SRAM block9. (R/W)

PMS_DMA_APBPERI_SHA_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure SHA's permission to SRAM block10. (R/W)

PRELIMINARY

Register 13.20. PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_0_REG (0x0080)

PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_LOCK Set this bit to lock ADC_DAC's GDMA permission configuration register. (R/W)

PRELIMINARY

Register 13.21. PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_1_REG (0x0084)

PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_SRAM_PMS_0 Configure ADC_DAC's permission to the instruction region. (R/W)

PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_SRAM_PMS_1 Configure ADC_DAC's permission to data region0 of SRAM. (R/W)

PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_SRAM_PMS_2 Configure ADC_DAC's permission to data region1 of SRAM. (R/W)

PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_SRAM_PMS_3 Configure ADC_DAC's permission to data region2 of SRAM. (R/W)

PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure ADC_DAC's permission to SRAM block9. (R/W)

PMS_DMA_APBPERI_ADC_DAC_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure ADC_DAC's permission to SRAM block10. (R/W)

PRELIMINARY

Register 13.22. PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_0_REG (0x0088)

PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_LOCK Set this bit to lock RMT's GDMA permission configuration register. (R/W)

PRELIMINARY

Register 13.23. PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_1_REG (0x008C)

PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_SRAM_PMS_0 Configure RMT's permission to the instruction region. (R/W)

PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_SRAM_PMS_1 Configure RMT's permission to data region0 of SRAM. (R/W)

PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_SRAM_PMS_2 Configure RMT's permission to data region1 of SRAM. (R/W)

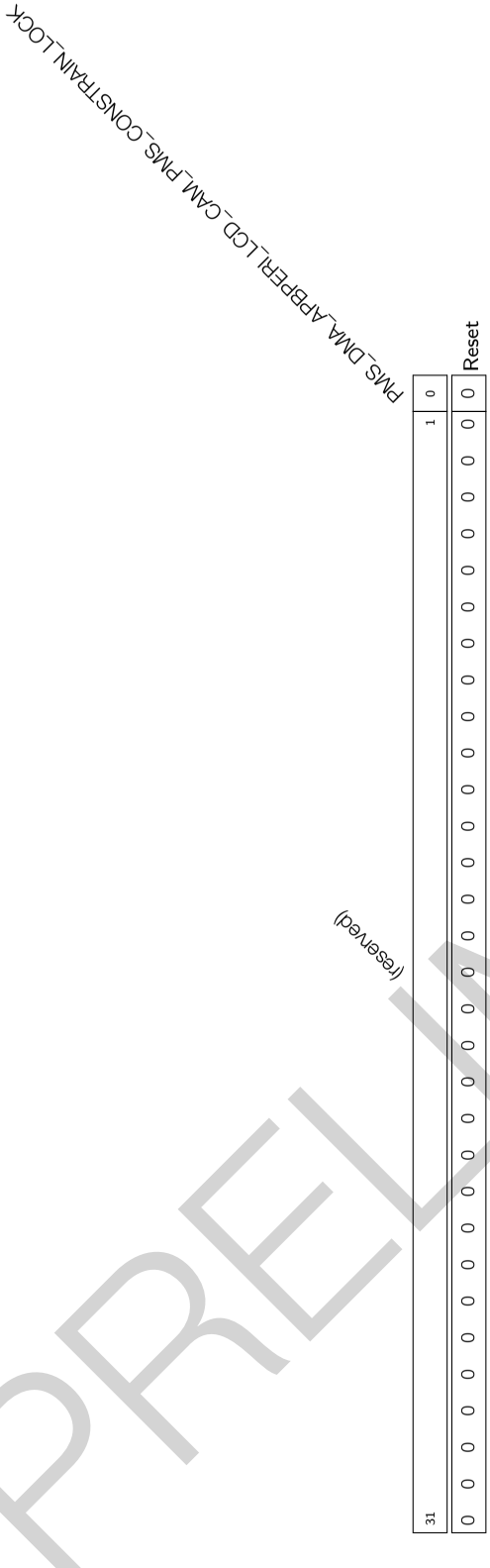
PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_SRAM_PMS_3 Configure RMT's permission to data region2 of SRAM. (R/W)

PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure RMT's permission to SRAM block9. (R/W)

PMS_DMA_APBPERI_RMT_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure RMT's permission to SRAM block10. (R/W)

PRELIMINARY

Register 13.24. PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_0_REG (0x0090)



PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_LOCK Set this bit to lock LCD_CAM's GDMA permission configuration register. (R/W)

PRELIMINARY

Register 13.25. PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_1_REG (0x0094)

PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_SRAM_PMS_0 Configure LCD_CAM's permission to the instruction region. (R/W)

PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_SRAM_PMS_1 Configure LCD_CAM's permission to data region0 of SRAM. (R/W)

PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_SRAM_PMS_2 Configure LCD_CAM's permission to data region1 of SRAM. (R/W)

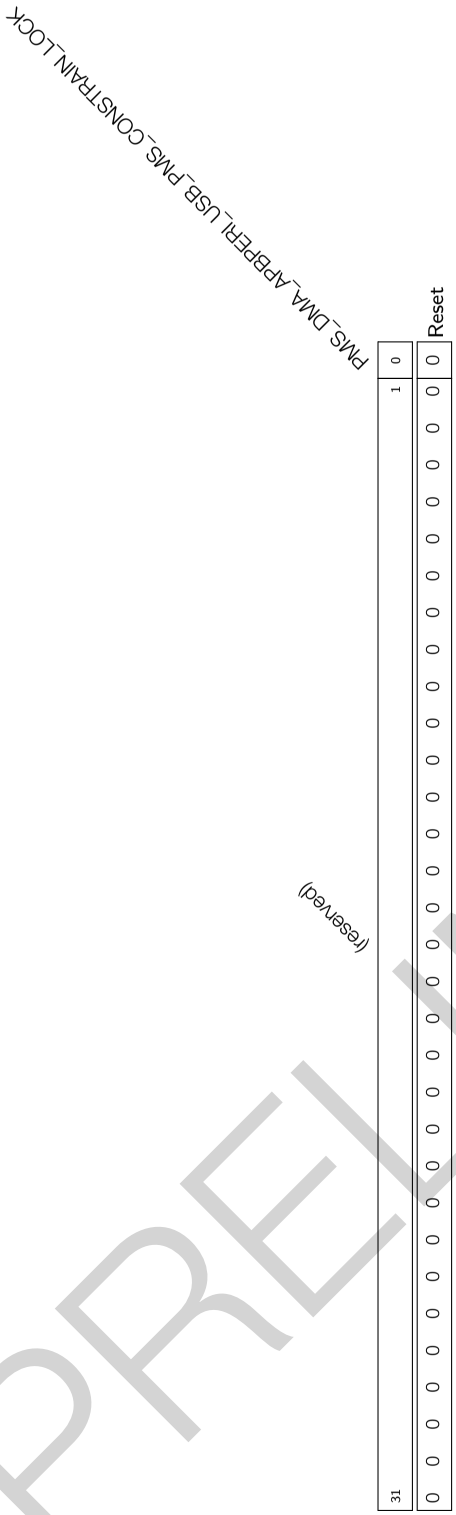
PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_SRAM_PMS_3 Configure LCD_CAM's permission to data region2 of SRAM. (R/W)

PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure LCD_CAM's permission to SRAM block9. (R/W)

PMS_DMA_APBPERI_LCD_CAM_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure LCD_CAM's permission to SRAM block10. (R/W)

PRELIMINARY

Register 13.26. PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_0_REG (0x0098)



PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_LOCK Set this bit to lock USB's GDMA permission configuration register. (R/W)

PRELIMINARY

Register 13.27. PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_1_REG (0x009C)

PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_SRAM_PMS_0 Configure USB's permission to the instruction region. (R/W)

PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_SRAM_PMS_1 Configure USB's permission to data region0 of SRAM. (R/W)

PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_SRAM_PMS_2 Configure USB's permission to data region1 of SRAM. (R/W)

PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_SRAM_PMS_3 Configure USB's permission to data region2 of SRAM. (R/W)

PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure USB's permission to SRAM block9. (R/W)

PMS_DMA_APBPERI_USB_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure USB's permission to SRAM block10. (R/W)

PRELIMINARY

Register 13.28. PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_0_REG (0x00A8)

PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_LOCK Set this bit to lock SDIO's GDMA permission configuration register. (R/W)

PRELIMINARY

Register 13.29. PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_1_REG (0x00AC)

PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_SRAM_PMS_0 Configure SDIO's permission to the instruction region. (R/W)

PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_SRAM_PMS_1 Configure SDIO's permission to data region0 of SRAM. (R/W)

PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_SRAM_PMS_2 Configure SDIO's permission to data region1 of SRAM. (R/W)

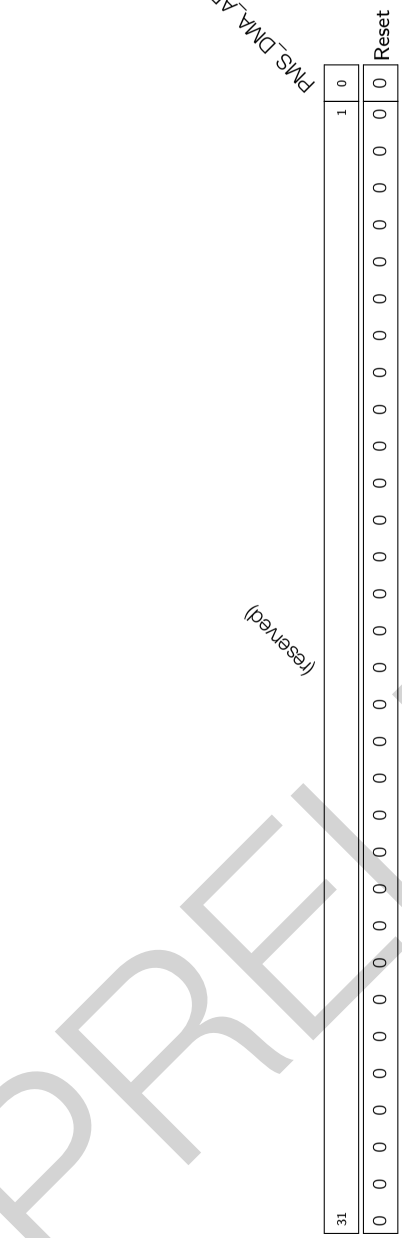
PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_SRAM_PMS_3 Configure SDIO's permission to data region2 of SRAM. (R/W)

PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_0 Configure SDIO's permission to SRAM block9 (R/W)

PMS_DMA_APBPERI_SDIO_PMS_CONSTRAIN_SRAM_CACHEDATAARRAY_PMS_1 Configure SDIO's permission to SRAM block10 (R/W)

PRELIMINARY

Register 13.30. PMS_DMA_APBPERI_PMS_MONITOR_0_REG (0x00B0)



PMS_DMA_APBPERI_PMS_MONITOR_LOCK Set this bit to lock GDMA access interrupt configuration register. (R/W)

PRELIMINARY

Register 13.31. PMS_DMA_APBPERI_PMS_MONITOR_1_REG (0x00B4)

PMS_DMA_APBPERI_PMS_MONITOR_VIOLATE_CLR Set this bit to clear GDMA access interrupt status. (R/W)

PMS_DMA_APBPERI_PMS_MONITOR_VIOLATE_EN Set this bit to enable interrupt upon unauthorized GDMA access. (R/W)

PRELIMINARY

Register 13.32. PMS_DMA_APBPERI_PMS_MONITOR_2_REG (0x00B8)

PMS_DMA_APBPERI_PMS_MONITOR_VIOLATE_INTR Stores unauthorized GDMA access interrupt status. (RO)

PMS_DMA_APBPERI_PMS_MONITOR_VIOLATE_STATUS_WORLD Stores the world the CPU was in when the unauthorized GDMA access happened. 0b01: Secure World; 0b10: Non-secure World. (RO)

PMS_DMA_APBPERI_PMS_MONITOR_VIOLATE_STATUS_ADDR Stores the address that triggered the unauthorized GDMA address. Note that this is an offset to 0x3c000000 and the unit is 16, which means the actual address should be 0x3c000000 + PMS_DMA_APBPERI_PMS_MONITOR_VIOLATE_STATUS_ADDR * 16. (RO)

PRELIMINARY

Register 13.33. PMS_DMA_APBPERI_PMS_MONITOR_3_REG (0x00BC)

PMS_DMA_APBPERI_PMS_MONITOR_VIOLATE_STATUS_WR Store the direction of unauthorized GDMA access. 1: write; 0: read. (RO)

PMS_DMA_APBPERI_PMS_MONITOR_VIOLATE_STATUS_BYTEEN Stores the byte information of unauthorized GDMA access. (RO)

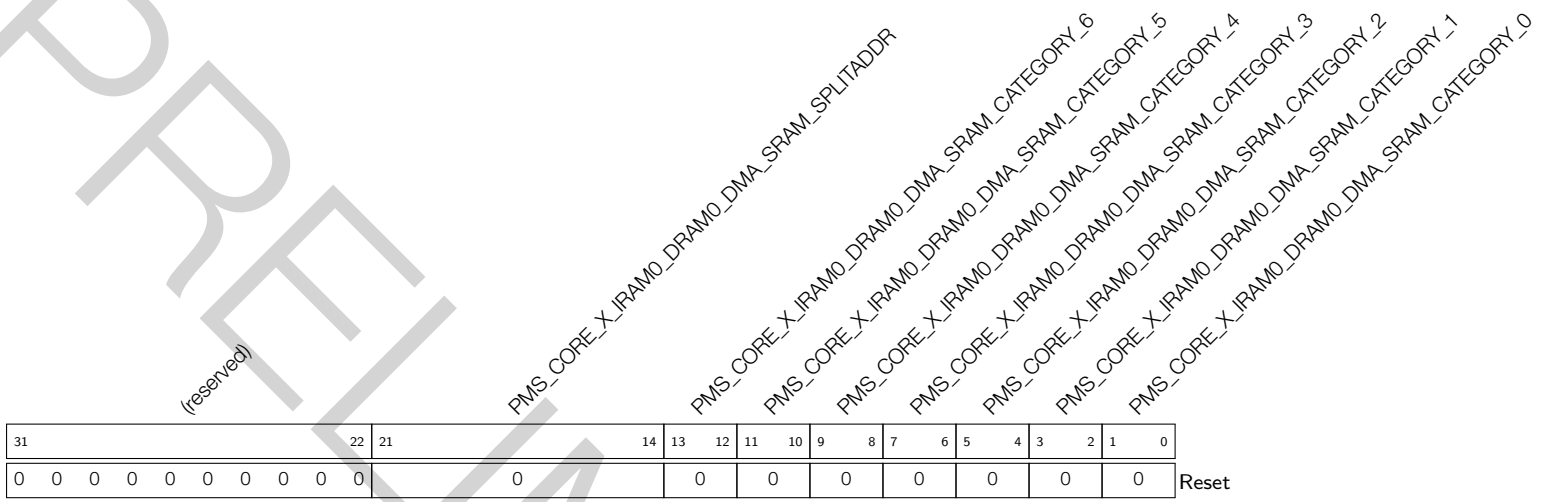
PRELIMINARY

Register 13.34. PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_0_REG (0x00C0)

PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_LOCK Set this bit to lock internal SRAM's split lines configuration. (R/W)

PRELIMINARY

Register 13.35. PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_1_REG (0x00C4)



PMS_CORE_X_IRAM0_DRAM0_DMA_SRAM_CATEGORY_0 Configures Block2's category field for the instruction and data split line IRAM0_DRAM0_Split_Line. (R/W)

PMS_CORE_X_IRAM0_DRAM0_DMA_SRAM_CATEGORY_1 Configures Block3's category field for the instruction and data split line IRAM0_DRAM0_Split_Line. (R/W)

PMS_CORE_X_IRAM0_DRAM0_DMA_SRAM_CATEGORY_2 Configures Block4's category field for the instruction and data split line IRAM0_DRAM0_Split_Line. (R/W)

PMS_CORE_X_IRAM0_DRAM0_DMA_SRAM_CATEGORY_3 Configures Block5's category field for the instruction and data split line IRAM0_DRAM0_Split_Line. (R/W)

PMS_CORE_X_IRAM0_DRAM0_DMA_SRAM_CATEGORY_4 Configures Block6's category field for the instruction and data split line IRAM0_DRAM0_Split_Line. (R/W)

PMS_CORE_X_IRAM0_DRAM0_DMA_SRAM_CATEGORY_5 Configures Block7's category field for the instruction and data split line IRAM0_DRAM0_Split_Line. (R/W)

PMS_CORE_X_IRAM0_DRAM0_DMA_SRAM_CATEGORY_6 Configures Block8's category field for the instruction and data split line IRAM0_DRAM0_Split_Line. (R/W)

PMS_CORE_X_IRAM0_DRAM0_DMA_SRAM_SPLITADDR Configures the split address of the instruction and data split line IRAM0_DRAM0_Split_Line. (R/W)

PRELIMINARY

Register 13.36. PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_2_REG (0x00C8)

PMS_CORE_X_IRAM0_SRAM_LINE_0_CATEGORY_0 Configures Block2's category field for the instruction internal split line IRAM0_Split_Line_0. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_0_CATEGORY_1 Configures Block3's category field for the instruction internal split line IRAM0_Split_Line_0. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_0_CATEGORY_2 Configures Block4's category field for the instruction internal split line IRAM0_Split_Line_0. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_0_CATEGORY_3 Configures Block5's category field for the instruction internal split line IRAM0_Split_Line_0. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_0_CATEGORY_4 Configures Block6's category field for the instruction internal split line IRAM0_Split_Line_0. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_0_CATEGORY_5 Configures Block7's category field for the instruction internal split line IRAM0_Split_Line_0. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_0_CATEGORY_6 Configures Block8's category field for the instruction internal split line IRAM0_Split_Line_0. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_0_SPLITADDR Configures the split address of the instruction internal split line IRAM0_Split_Line_0. (R/W)

PRELIMINARY

Register 13.37. PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_3_REG (0x00CC)

PMS_CORE_X_IRAM0_SRAM_LINE_1_CATEGORY_0 Configures Block2's category field for the instruction internal split line IRAM0_Split_Line_1. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_1_CATEGORY_1 Configures Block3's category field for the instruction internal split line IRAM0_Split_Line_1. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_1_CATEGORY_2 Configures Block4's category field for the instruction internal split line IRAM0_Split_Line_1. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_1_CATEGORY_3 Configures Block5's category field for the instruction internal split line IRAM0_Split_Line_1. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_1_CATEGORY_4 Configures Block6's category field for the instruction internal split line IRAM0_Split_Line_1. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_1_CATEGORY_5 Configures Block7's category field for the instruction internal split line IRAM0_Split_Line_1. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_1_CATEGORY_6 Configures Block8's category field for the instruction internal split line IRAM0_Split_Line_1. (R/W)

PMS_CORE_X_IRAM0_SRAM_LINE_1_SPLITADDR Configures the split address of the instruction internal split line IRAM0_Split_Line_1. (R/W)

PRELIMINARY

Register 13.38. PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_4_REG (0x00D0)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_0_CATEGORY_0 Configures Block2's category field for data internal split line DRAM0_Split_Line_0. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_0_CATEGORY_1 Configures Block3's category field for data internal split line DRAM0_Split_Line_0. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_0_CATEGORY_2 Configures Block4's category field for data internal split line DRAM0_Split_Line_0. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_0_CATEGORY_3 Configures Block5's category field for data internal split line DRAM0_Split_Line_0. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_0_CATEGORY_4 Configures Block6's category field for data internal split line DRAM0_Split_Line_0. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_0_CATEGORY_5 Configures Block7's category field for data internal split line DRAM0_Split_Line_0. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_0_CATEGORY_6 Configures Block8's category field for data internal split line DRAM0_Split_Line_0. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_0_SPLITADDR Configures the split address of data internal split line DRAM0_Split_Line_0. (R/W)

PRELIMINARY

Register 13.39. PMS_CORE_X_IRAM0_DRAM0_DMA_SPLIT_LINE_CONSTRAIN_5_REG (0x00D4)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_1_CATEGORY_0 Configures Block2's category field for data internal split line DRAM0_Split_Line_1. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_1_CATEGORY_1 Configures Block3's category field for data internal split line DRAM0_Split_Line_1. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_1_CATEGORY_2 Configures Block4's category field for data internal split line DRAM0_Split_Line_1. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_1_CATEGORY_3 Configures Block5's category field for data internal split line DRAM0_Split_Line_1. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_1_CATEGORY_4 Configures Block6's category field for data internal split line DRAM0_Split_Line_1. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_1_CATEGORY_5 Configures Block7's category field for data internal split line DRAM0_Split_Line_1. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_1_CATEGORY_6 Configures Block8's category field for data internal split line DRAM0_Split_Line_1. (R/W)

PMS_CORE_X_DRAM0_DMA_SRAM_LINE_1_SPLITADDR Configures the split address of data internal split line DRAM0_Split_Line_1. (R/W)

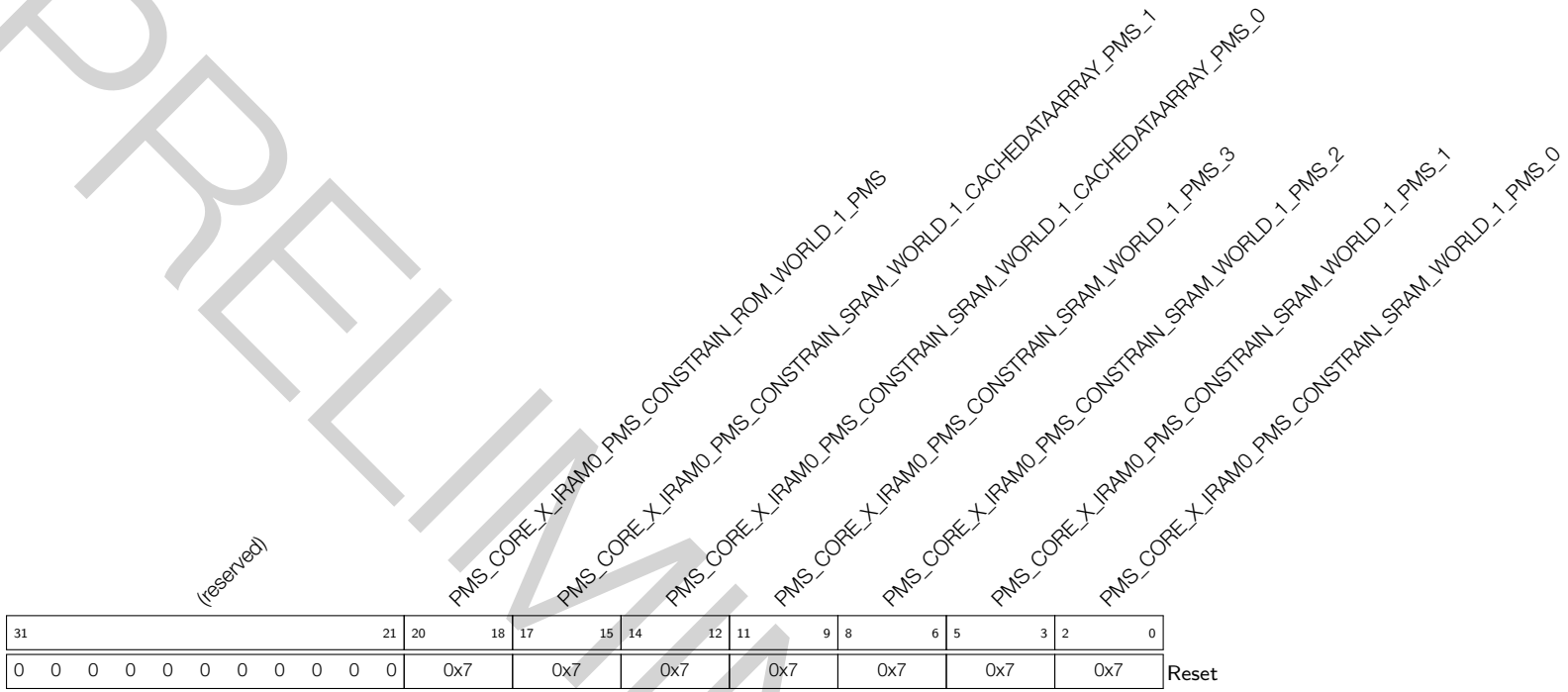
PRELIMINARY

Register 13.40. PMS_CORE_X_IRAM0_PMS_CONSTRAIN_0_REG (0x00D8)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_LOCK Set this bit to lock the permission of CPU IBUS to internal SRAM. (R/W)

PRELIMINARY

Register 13.41. PMS_CORE_X_IRAM0_PMS_CONSTRAIN_1_REG (0x00DC)



PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_PMS_0 Configures the permission of CPU's IBUS to instruction region0 of SRAM from the Non-secure World. (R/W)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_PMS_1 Configures the permission of CPU's IBUS to instruction region1 of SRAM from the Non-secure World. (R/W)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_PMS_2 Configures the permission of CPU's IBUS to instruction region2 of SRAM from the Non-secure World. (R/W)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_PMS_3 Configures the permission of CPU's IBUS to data region of SRAM from the Non-secure World. It's advised to configure this field to 0. (R/W)

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PRELIMINARY

Register 13.41. PMS_CORE_X_IRAM0_PMS_CONSTRAIN_1_REG (0x00DC)

Continued from the previous page...

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_CACHEDATAARRAY_PMS_0 Configure the permission of CPU's IBUS to Block0 of SRAM0 from the Non-secure World. (R/W)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_CACHEDATAARRAY_PMS_1 Configure the permission of CPU's IBUS to Block1 of SRAM0 from the Non-secure World. (R/W)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_ROM_WORLD_1_PMS Configures the permission of CPU's IBUS to ROM from the Non-secure World. (R/W)

PRELIMINARY

Register 13.42. PMS_CORE_X_IRAM0_PMS_CONSTRAIN_2_REG (0x00E0)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_PMS_0 Configures the permission of CPU's IBUS to instruction region0 of SRAM from the Secure World. (R/W)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_PMS_1 Configures the permission of CPU's IBUS to instruction region1 of SRAM from the Secure World. (R/W)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_PMS_2 Configures the permission of CPU's IBUS to instruction region2 of SRAM from the Secure World. (R/W)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_PMS_3 Configures the permission of CPU's IBUS to data region of SRAM from the Secure World. It's advised to configure this field to 0. (R/W)

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PRELIMINARY

Register 13.42. PMS_CORE_X_IRAM0_PMS_CONSTRAIN_2_REG (0x00E0)

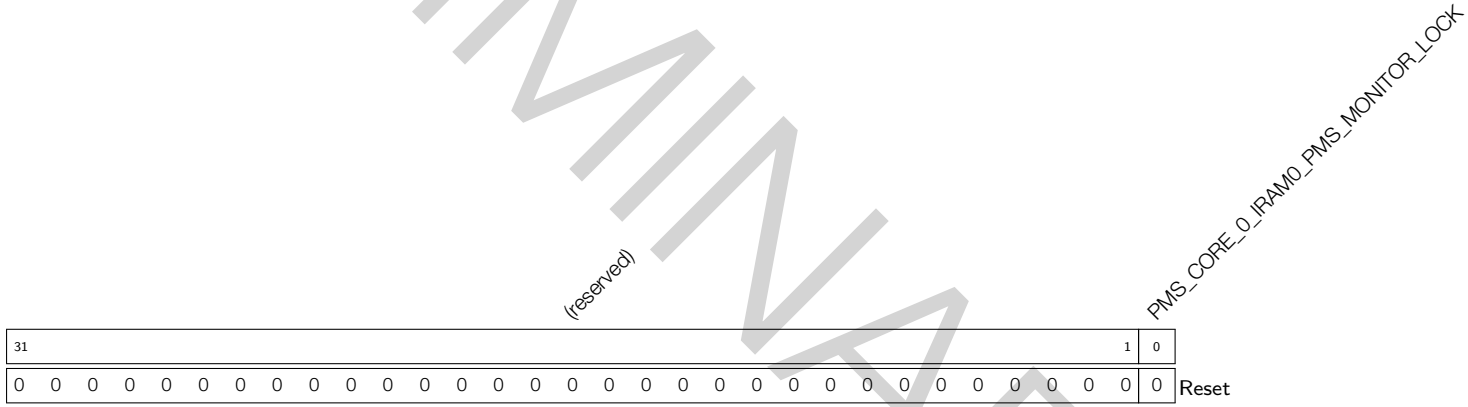
Continued from the previous page...

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_CACHEDATAARRAY_PMS_0 Configure the permission of CPU's IBUS to Block0 of SRAM0 from the Secure World. (R/W)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_CACHEDATAARRAY_PMS_1 Configure the permission of CPU's IBUS to Block1 of SRAM0 from the Secure World. (R/W)

PMS_CORE_X_IRAM0_PMS_CONSTRAIN_ROM_WORLD_0_PMS Configures the permission of CPU's IBUS to ROM from the Secure World. (R/W)

Register 13.43. PMS_CORE_0_IRAM0_PMS_MONITOR_0_REG (0x00E4)



PMS_CORE_0_IRAM0_PMS_MONITOR_LOCK Set this bit to lock CPU0's IBUS interrupt configuration. (R/W)

PRELIMINARY

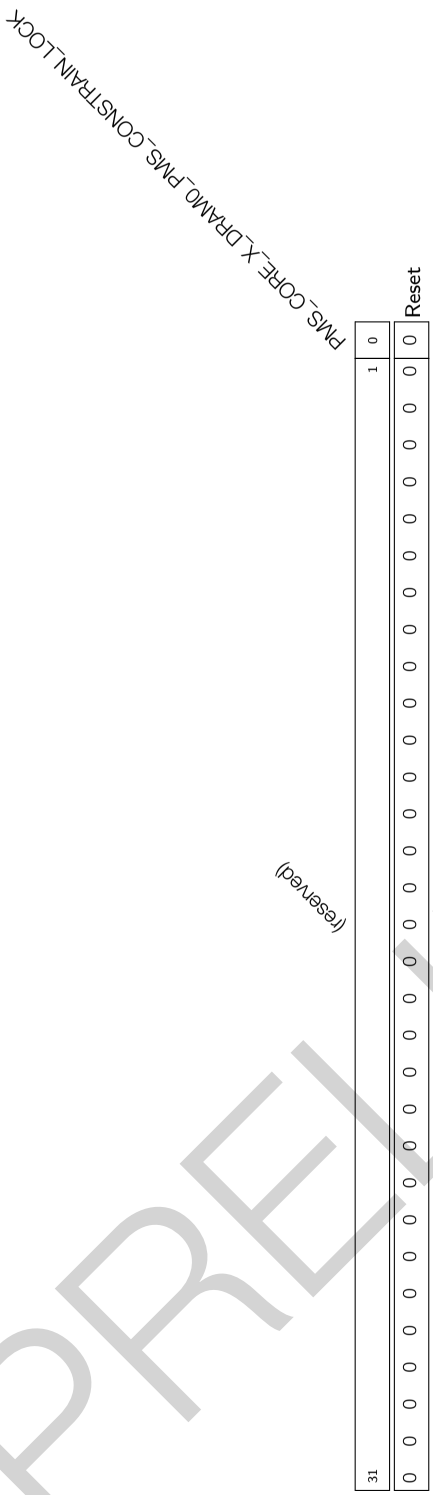
Register 13.44. PMS_CORE_0_IRAM0_PMS_MONITOR_1_REG (0x00E8)

PMS_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_CLR Set this bit to clear the interrupt triggered when CPU0's IBUS tries to access SRAM or ROM unauthorized. (R/W)

PMS_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_EN Set this bit to enable interrupt when CPU0's IBUS tries to access SRAM or ROM unauthorized. (R/W)

PRELIMINARY

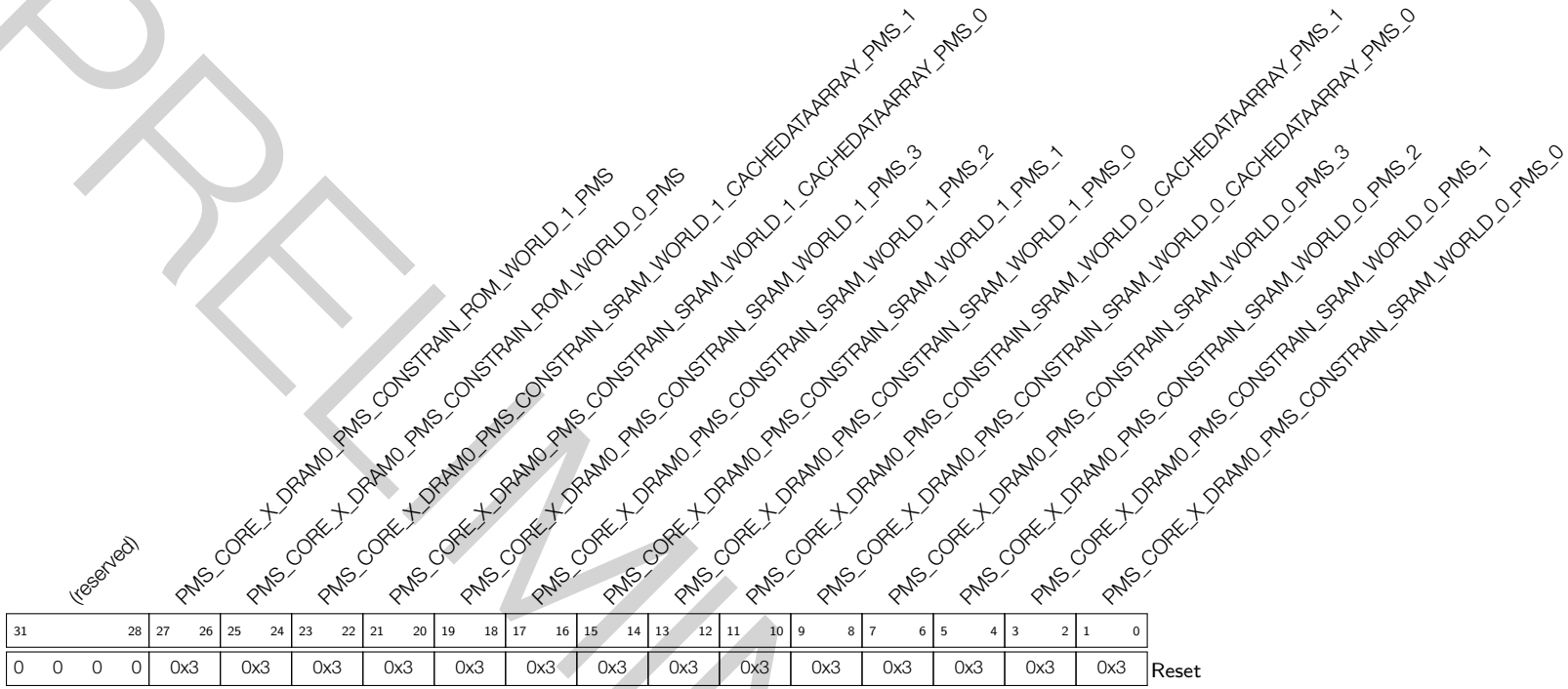
Register 13.45. PMS_CORE_X_DRAM0_PMS_CONSTRAIN_0_REG (0x00FC)



PMS_CORE_X_DRAM0_PMS_CONSTRAIN_LOCK Set this bit to lock the permission of CPU DBUS to internal SRAM. (R/W)

PRELIMINARY

Register 13.46. PMS_CORE_X_DRAM0_PMS_CONSTRAIN_1_REG (0x0100)



PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_PMS_0 Configures the permission of CPU's DBUS to instruction region of SRAM from the Secure World. It's advised to configure this field to 0. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_PMS_1 Configures the permission of CPU's DBUS to data region0 of SRAM from the Secure World. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_PMS_2 Configures the permission of CPU's DBUS to data region1 of SRAM from the Secure World. (R/W)

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PRELIMINARY

Register 13.46. PMS_CORE_X_DRAM0_PMS_CONSTRAIN_1_REG (0x0100)

Continued from the previous page...

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_PMS_3 Configures the permission of CPU's DBUS to data region2 of SRAM from the Secure World. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_CACHEDATAARRAY_PMS_0 Configures the permission of CPU's DBUS to block9 of SRAM2 from the Secure World. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_0_CACHEDATAARRAY_PMS_1 Configures the permission of CPU's DBUS to block10 of SRAM2 from the Secure World. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_PMS_0 Configures the permission of CPU's DBUS to instruction region of SRAM from the Non-secure World. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_PMS_1 Configures the permission of CPU's DBUS to data region0 of SRAM from the Non-secure World. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_PMS_2 Configures the permission of CPU's DBUS to data region1 of SRAM from the Non-secure World. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_PMS_3 Configures the permission of CPU's DBUS to data region2 of SRAM from the Non-secure World. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_CACHEDATAARRAY_PMS_0 Configures the permission of CPU's DBUS to block9 of SRAM2 from the Non-secure World. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_SRAM_WORLD_1_CACHEDATAARRAY_PMS_1 Configures the permission of CPU's DBUS to block10 of SRAM2 from the Non-secure World. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_ROM_WORLD_0_PMS Configures the permission of CPU's DBUS to ROM from the Secure World. (R/W)

PMS_CORE_X_DRAM0_PMS_CONSTRAIN_ROM_WORLD_1_PMS Configures the permission of CPU's DBUS to ROM from the Non-secure World. (R/W)

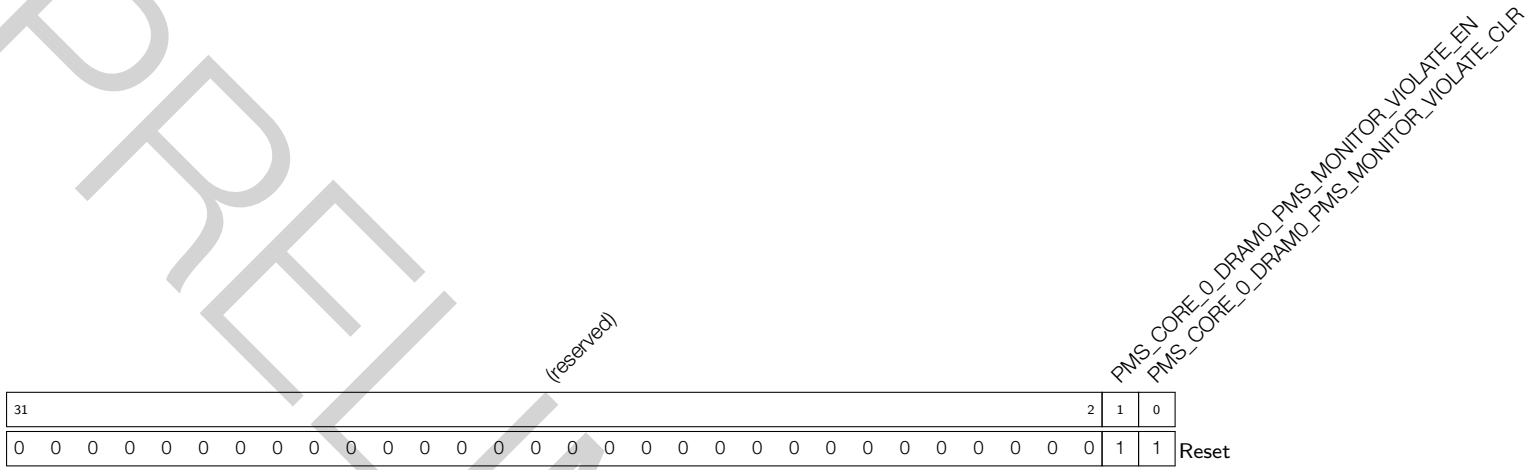
PRELIMINARY

Register 13.47. PMS_CORE_0_DRAM0_PMS_MONITOR_0_REG (0x0104)

PMS_CORE_0_DRAM0_PMS_MONITOR_LOCK Set this bit to lock CPU0's DBUS interrupt configuration. (R/W)

PRELIMINARY

Register 13.48. PMS_CORE_0_DRAM0_PMS_MONITOR_1_REG (0x0108)



PMS_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_CLR Set this bit to clear the interrupt triggered when CPU0's dBUS tries to access SRAM or ROM unauthorized. (R/W)

PMS_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_EN Set this bit to enable interrupt when CPU0's dBUS tries to access SRAM or ROM unauthorized. (R/W)

PRELIMINARY

Register 13.49. PMS_CORE_0_PIF_PMS_CONSTRAIN_0_REG (0x0124)

PMS_CORE_0_PIF_PMS_CONSTRAIN_LOCK Set this bit to lock Core0's permission to different peripherals. (R/W)

PRELIMINARY

Register 13.50. PMS_CORE_0_PIF_PMS_CONSTRAIN_*n*_REG (*n*: 1 - 8) (0x0128 + 4n*)**

PMS_CORE_0_PIF_PMS_CONSTRAIN_WORLD_0_UART Configures CPU0's permission to access UART0 from the Secure World. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_WORLD_0_G0SPI_1 Configures CPU0's permission to access SPI1 from the Secure World. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_WORLD_0_G0SPI_0 Configures CPU0's permission to access SPI0 from the Secure World. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_WORLD_0_GPIO Configures CPU0's permission to access GPIO from the Secure World. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_WORLD_0_RTC Configures CPU0's permission to access eFuse Controller & PMU from the Secure World. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_WORLD_0_IO_MUX Configures CPU0's permission to access IO_MUX from the Secure World. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_WORLD_0_I2S0 Configures CPU0's permission to access I2S0 from the Secure World. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_WORLD_0_UART1 Configures CPU0's permission to access UART1 from the Secure World. (R/W)

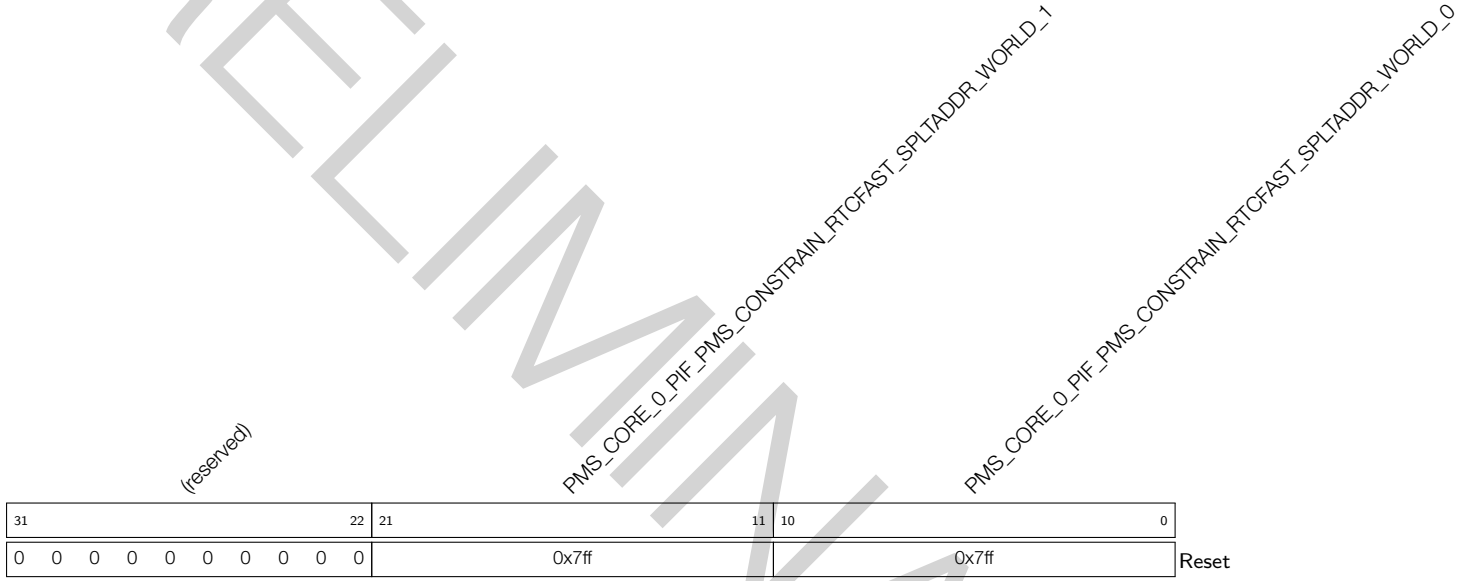
PRELIMINARY

Note:

- Registers PMS_CORE_0_PIF_PMS_CONSTRAIN_*n*_REG (*n*: 1 - 4) are for configuring the CPU0's permission to different peripherals from the Secure World.
- Registers PMS_CORE_0_PIF_PMS_CONSTRAIN_*n*_REG (*n*: 5 - 8) are for configuring the CPU0's permission to different peripherals from the Non-secure World.
- Detailed information are already provided in Table 13-17. For brevity, these registers are not described separately in this section.

PRELIMINARY

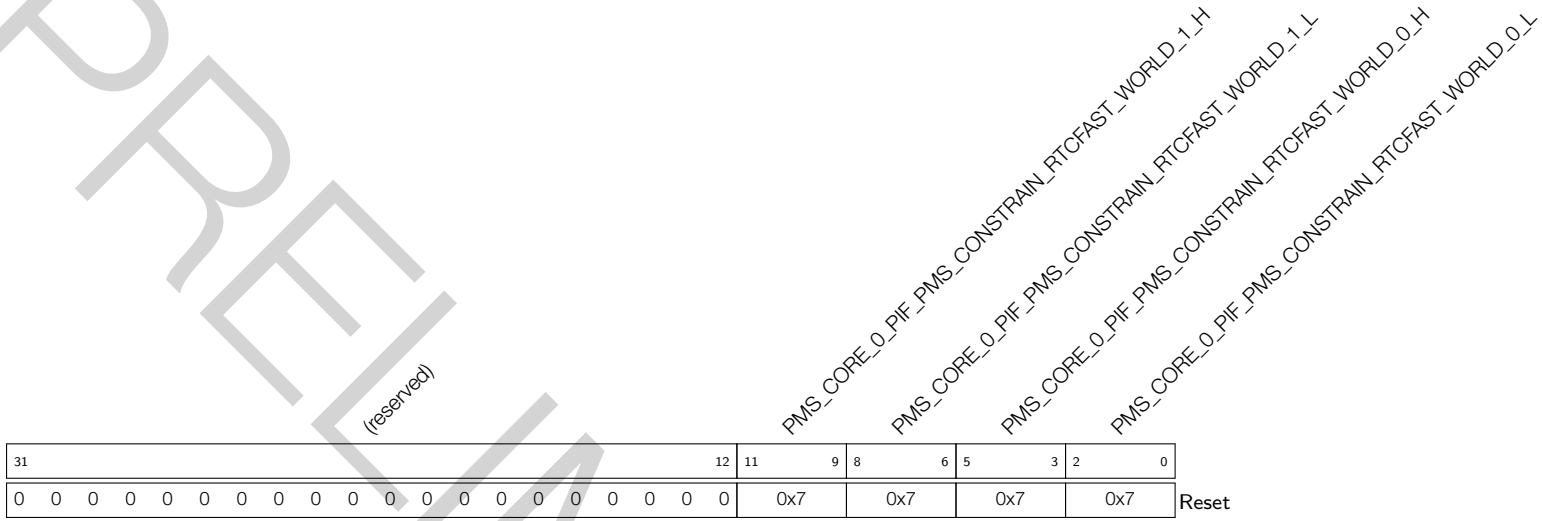
Register 13.51. PMS_CORE_0_PIF_PMS_CONSTRAIN_9_REG (0x0148)



PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCFAST_SPLTADDR_WORLD_0 Configures the address to split RTC Fast Memory into two regions in Non-secure World for CPU0. Note you should use address offset, instead of absolute address. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCFAST_SPLTADDR_WORLD_1 Configures the address to split RTC Fast Memory into two regions in Secure World for CPU0. Note you should use address offset, instead of absolute address. (R/W)

Register 13.52. PMS_CORE_0_PIF_PMS_CONSTRAIN_10_REG (0x014C)



PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCFAST_WORLD_0_L Configures the permission of CPU0 from Non-secure World to the lower region of RTC Fast Memory. (R/W)

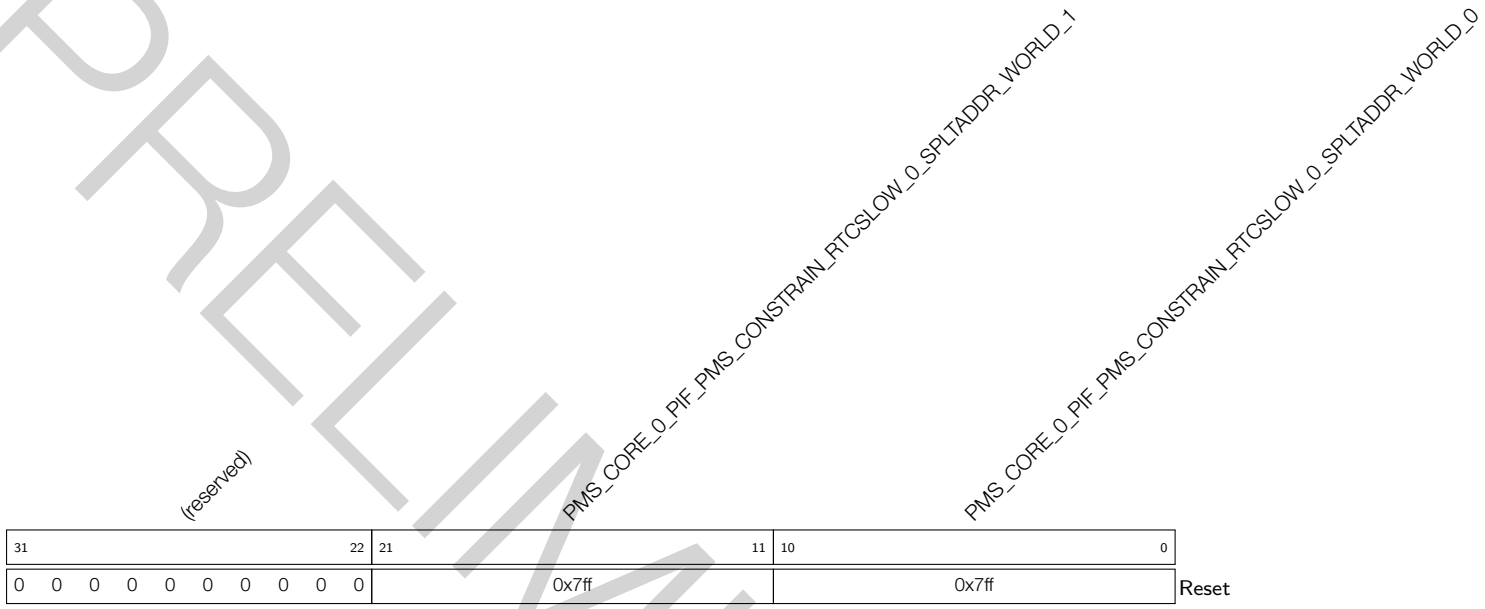
PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCFAST_WORLD_0_H Configures the permission of CPU0 from Non-secure World to the higher region of RTC Fast Memory. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCFAST_WORLD_1_L Configures the permission of CPU0 from Secure World to the lower region of RTC Fast Memory. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCFAST_WORLD_1_H Configures the permission of CPU0 from Secure World to the higher region of RTC Fast Memory. (R/W)

PRELIMINARY

Register 13.53. PMS_CORE_0_PIF_PMS_CONSTRAIN_11_REG (0x0150)



PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_0_SPLTADDR_WORLD_0 Configures the address to split RTC Slow Memory 0 into two regions in Secure World for CPU0. Note you should use address offset, instead of absolute address. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_0_SPLTADDR_WORLD_1 Configures the address to split RTC Slow Memory 0 into two regions in Non-secure World for CPU0. Note you should use address offset, instead of absolute address. (R/W)

PRELIMINARY

Register 13.54. PMS_CORE_0_PIF_PMS_CONSTRAIN_12_REG (0x0154)

PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_0_WORLD_0_L Configures the permission of CPU0 from Secure World to the lower region of RTC Slow Memory 0. (R/W)

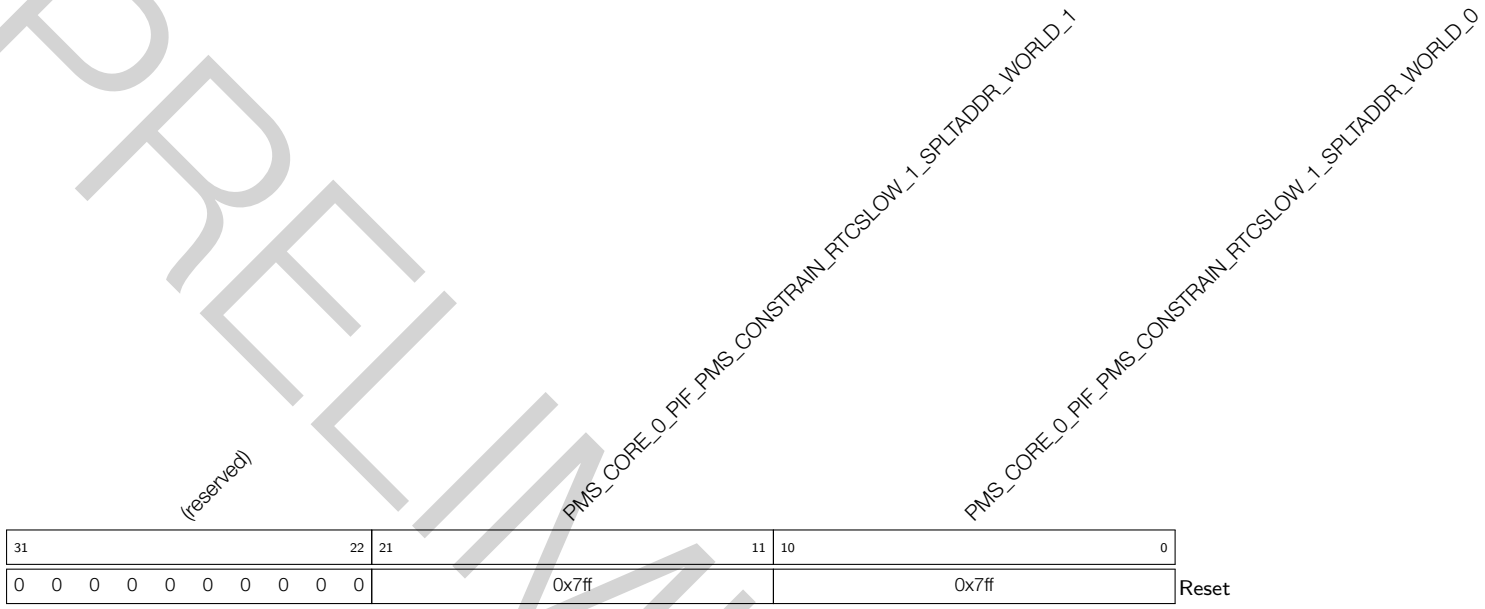
PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_0_WORLD_0_H Configures the permission of CPU0 from Secure World to the higher region of RTC Slow Memory 0. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_0_WORLD_1_L Configures the permission of CPU0 from Non-secure World to the lower region of RTC Slow Memory 0. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_0_WORLD_1_H Configures the permission of CPU0 from Non-secure World to the higher region of RTC Slow Memory 0. (R/W)

PRELIMINARY

Register 13.55. PMS_CORE_0_PIF_PMS_CONSTRAIN_13_REG (0x0158)

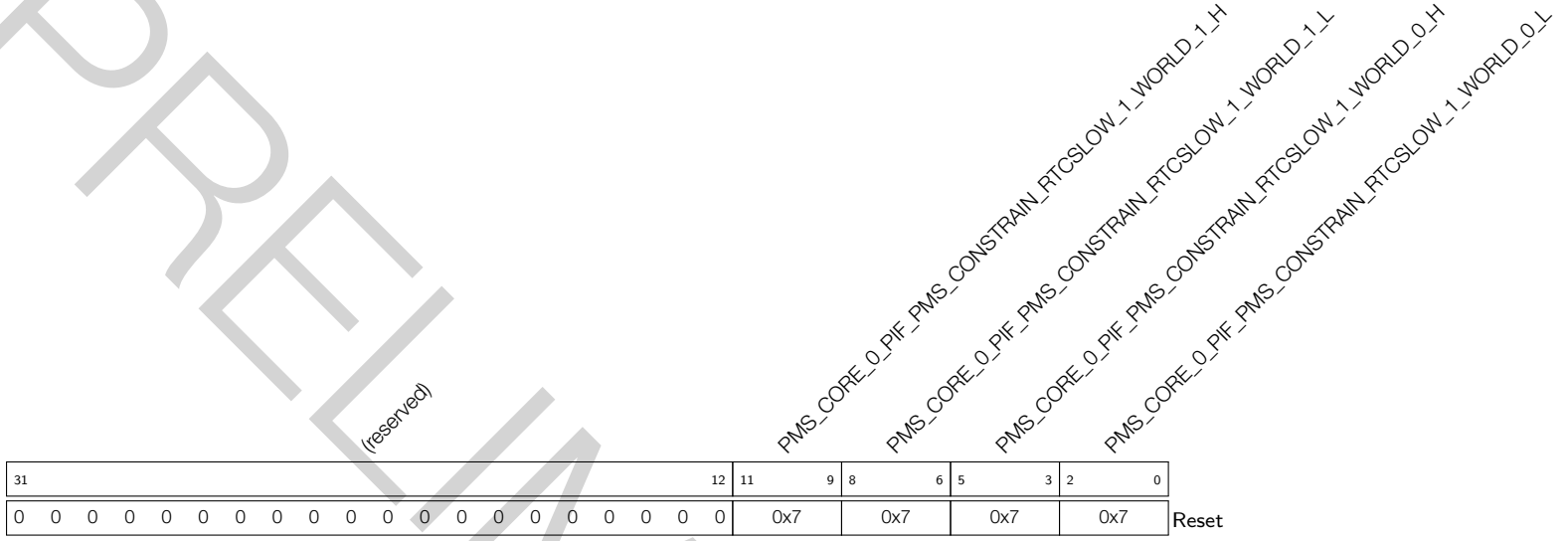


PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_1_SPLTADDR_WORLD_0 Configures the address to split RTC Slow Memory 1 into two regions in Secure World for CPU0. Note you should use address offset, instead of absolute address. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_1_SPLTADDR_WORLD_1 Configures the address to split RTC Slow Memory 1 into two regions in Non-secure World for CPU0. Note you should use address offset, instead of absolute address. (R/W)

PRELIMINARY

Register 13.56. PMS_CORE_0_PIF_PMS_CONSTRAIN_14_REG (0x015C)



PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_1_WORLD_0_L Configures the permission of CPU0 from Non-secure World to the lower region of RTC Slow Memory 1. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_1_WORLD_0_H Configures the permission of CPU0 from Non-secure World to the higher region of RTC Slow Memory 1. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_1_WORLD_1_L Configures the permission of CPU0 from Secure World to the lower region of RTC Slow Memory 1. (R/W)

PMS_CORE_0_PIF_PMS_CONSTRAIN_RTCSLOW_1_WORLD_1_H Configures the permission of CPU0 from Secure World to the higher region of RTC Slow Memory 1. (R/W)

PRELIMINARY

Register 13.57. PMS_CORE_0_REGION_PMS_CONSTRAIN_0_REG (0x0160)

PMS_CORE_0_REGION_PMS_CONSTRAIN_LOCK Set this bit to lock Core0's permission to peripheral regions. (R/W)

PRELIMINARY

Register 13.58. PMS_CORE_0_REGION_PMS_CONSTRAIN_1_REG (0x0164)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_0_AREA_0 Configures CPU0's permission to Peri Region0 from the Secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_0_AREA_1 Configures CPU0's permission to Peri Region1 from the Secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_0_AREA_2 Configures CPU0's permission to Peri Region2 from the Secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_0_AREA_3 Configures CPU0's permission to Peri Region3 from the Secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_0_AREA_4 Configures CPU0's permission to Peri Region4 from the Secure World (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_0_AREA_5 Configures CPU0's permission to Peri Region5 from the Secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_0_AREA_6 Configures CPU0's permission to Peri Region6 from the Secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_0_AREA_7 Configures CPU0's permission to Peri Region7 from the Secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_0_AREA_8 Configures CPU0's permission to Peri Region8 from the Secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_0_AREA_9 Configures CPU0's permission to Peri Region9 from the Secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_0_AREA_10 Configures CPU0's permission to Peri Region10 from the Secure World. (R/W)

PRELIMINARY

Register 13.59. PMS_CORE_0_REGION_PMS_CONSTRAIN_2_REG (0x0168)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_1_AREA_0 Configures CPU0's permission to Peri Region0 from the Non-secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_1_AREA_1 Configures CPU0's permission to Peri Region1 from the Non-secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_1_AREA_2 Configures CPU0's permission to Peri Region2 from the Non-secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_1_AREA_3 Configures CPU0's permission to Peri Region3 from the Non-secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_1_AREA_4 Configures CPU0's permission to Peri Region4 from the Non-secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_1_AREA_5 Configures CPU0's permission to Peri Region5 from the Non-secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_1_AREA_6 Configures CPU0's permission to Peri Region6 from the Non-secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_1_AREA_7 Configures CPU0's permission to Peri Region7 from the Non-secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_1_AREA_8 Configures CPU0's permission to Peri Region8 from the Non-secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_1_AREA_9 Configures CPU0's permission to Peri Region9 from the Non-secure World. (R/W)

PMS_CORE_0_REGION_PMS_CONSTRAIN_WORLD_1_AREA_10 Configures CPU0's permission to Peri Region10 from the Non-secure World. (R/W)

PRELIMINARY

Register 13.60. PMS_CORE_0_REGION_PMS_CONSTRAIN_*n*_REG (*n*: 3 - 14) (0x016C + 4*n*)

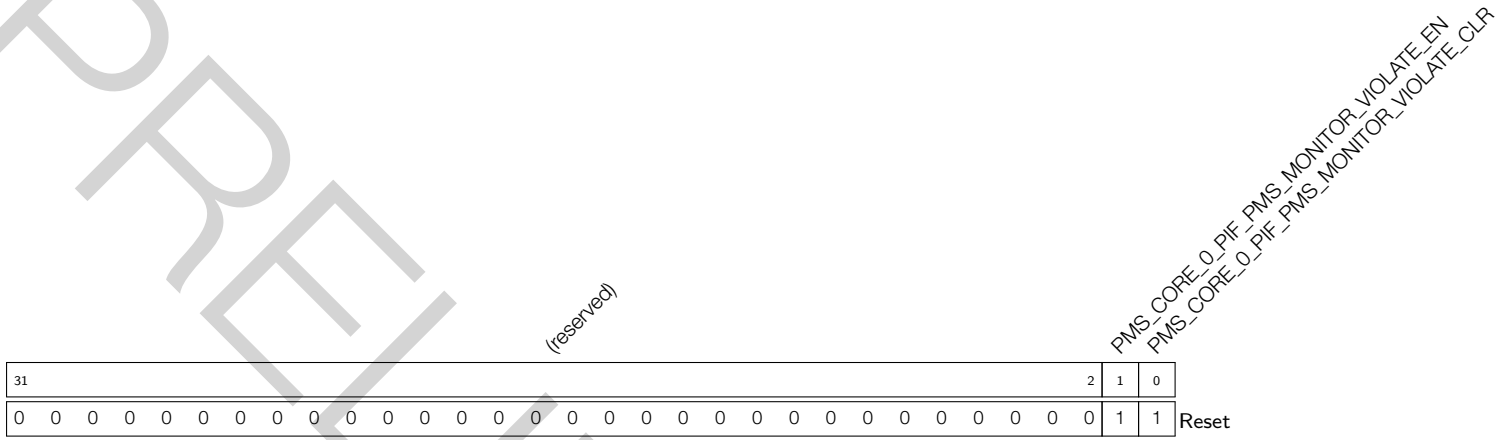
PMS_CORE_0_REGION_PMS_CONSTRAIN_ADDR_0 Configures the starting address of Region 0 for CPU0. (R/W)

Register 13.61. PMS_CORE_0_PIF_PMS_MONITOR_0_REG (0x019C)

PMS_CORE_0_PIF_PMS_MONITOR_LOCK Set this bit to lock CPU0's PIF interrupt configuration. (R/W)

PRELIMINARY

Register 13.62. PMS_CORE_0_PIF_PMS_MONITOR_1_REG (0x01A0)



PMS_CORE_0_PIF_PMS_MONITOR_VIOLATE_CLR Set this bit to clear the interrupt triggered when CPU0's PIF bus tries to access RTC memory or peripherals unauthorized. (R/W)

PMS_CORE_0_PIF_PMS_MONITOR_VIOLATE_EN Set this bit to enable interrupt when CPU0's PIF bus tries to access RTC memory or peripherals unauthorized. (R/W)

PRELIMINARY

Register 13.63. PMS_CORE_0_PIF_PMS_MONITOR_4_REG (0x01AC)

PMS_CORE_0_PIF_PMS_MONITOR_NONWORD_VIOLATE_CLR Set this bit to clear the interrupt triggered when CPU0's PIF bus tries to access RTC memory or peripherals using unsupported data type. (R/W)

PMS_CORE_0_PIF_PMS_MONITOR_NONWORD_VIOLATE_EN Set this bit to enable interrupt when CPU0's PIF bus tries to access RTC memory or peripherals using unsupported data type. (R/W)

PRELIMINARY

Register 13.64. PMS_CORE_0_VECBASE_OVERRIDE_LOCK_REG (0x01B8)

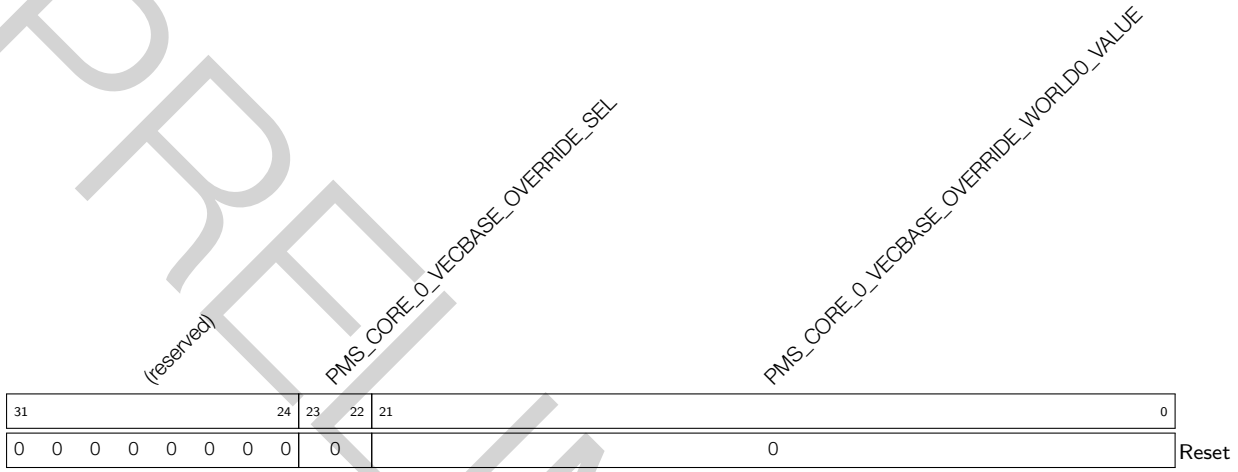
PMS_CORE_0_VECBASE_OVERRIDE_LOCK Set this bit to lock CPU0 VECBASE configuration register. (R/W)

Register 13.65. PMS_CORE_0_VECBASE_OVERRIDE_0_REG (0x01BC)

PMS_CORE_0_VECBASE_WORLD_MASK Set this bit so CPU uses WORLD0_VALUE in Secure World and Non-secure World. Clear this bit so CPU uses WORLD0_VALUE in Secure World and WORLD1_VALUE in Non-secure World. (R/W)

PRELIMINARY

Register 13.66. PMS_CORE_0_VECBASE_OVERRIDE_1_REG (0x01C0)



PMS_CORE_0_VECBASE_OVERRIDE_WORLD0_VALUE Configures the VECBASE value for the Secure World. (R/W)

PMS_CORE_0_VECBASE_OVERRIDE_SEL Configures VECBASE override. Set to 00 to select VECBASE; Set to 11 to select PMS_CORE_0_VECBASE_OVERRIDE_WORLD*n*_VALUE. (R/W)

PRELIMINARY

Register 13.67. PMS_CORE_0_VECBASE_OVERRIDE_2_REG (0x01C4)

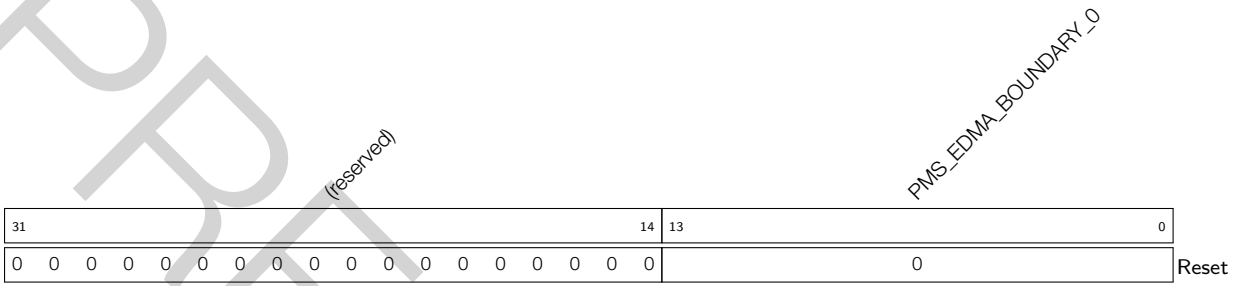
PMS_CORE_0_VECBASE_OVERRIDE_WORLD1_VALUE Configures the VECBASE value for the Non-secure World. (R/W)

Register 13.68. PMS_EDMA_BOUNDARY_LOCK_REG (0x02A8)

PMS_EDMA_BOUNDARY_LOCK Set this bit to lock EDMA boundary registers. (R/W)

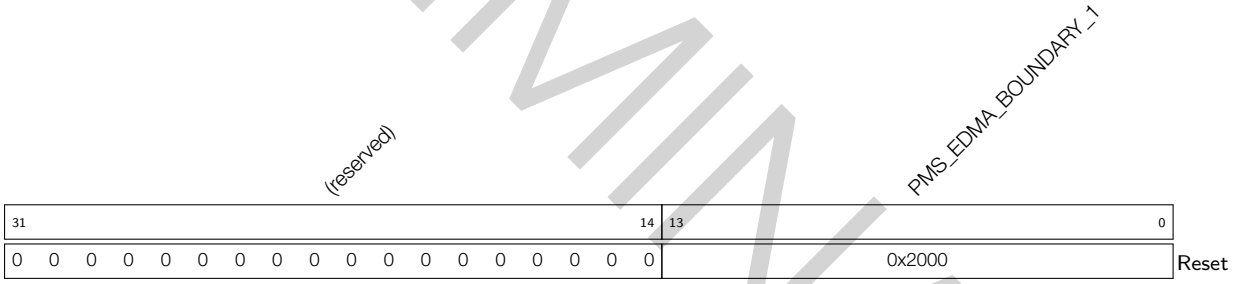
PRELIMINARY

Register 13.69. PMS_EDMA_BOUNDARY_0_REG (0x02AC)



PMS_EDMA_BOUNDARY_0 Configures the ending address of external SRAM area0. For details, see Table 13-21. (R/W)

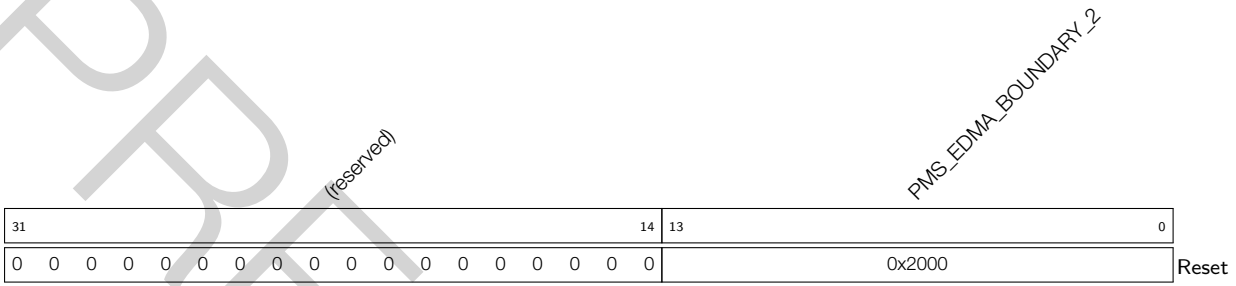
Register 13.70. PMS_EDMA_BOUNDARY_1_REG (0x02B0)



PMS_EDMA_BOUNDARY_1 Configures the ending address of external SRAM area1. For details, see Table 13-21. (R/W)

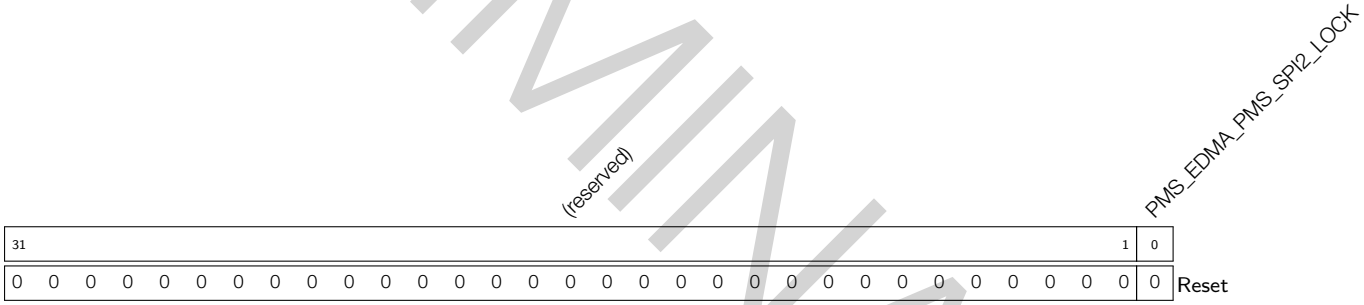
PRELIMINARY

Register 13.71. PMS_EDMA_BOUNDARY_2_REG (0x02B4)



PMS_EDMA_BOUNDARY_2 Configures the ending address of external SRAM area2. For details, see Table 13-21. (R/W)

Register 13.72. PMS_EDMA_PMS_SPI2_LOCK_REG (0x02B8)



PMS_EDMA_PMS_SPI2_LOCK Set this bit to lock the register that configures SPI2's access to external SRAM. (R/W)

PRELIMINARY

Register 13.73. PMS_EDMA_PMS_SPI2_REG (0x02BC)

PMS_EDMA_PMS_SPI2_ATTR1 Configures SPI2's access to external SRAM Area0. For details, see Table 13-22. (R/W)

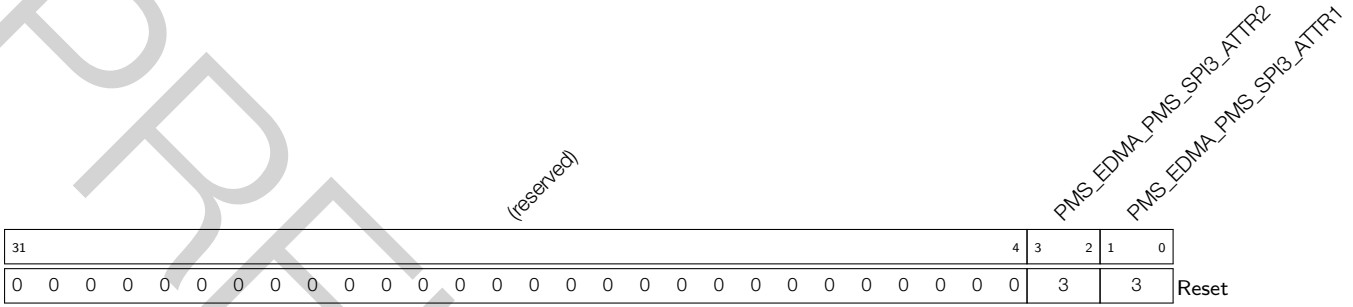
PMS_EDMA_PMS_SPI2_ATTR2 Configures SPI2's access to external SRAM Area1. For details, see Table 13-22. (R/W)

Register 13.74. PMS_EDMA_PMS_SPI3_LOCK_REG (0x02C0)

PMS_EDMA_PMS_SPI3_LOCK Set this bit to lock the register that configures SPI3's access to external SRAM. (R/W)

PRELIMINARY

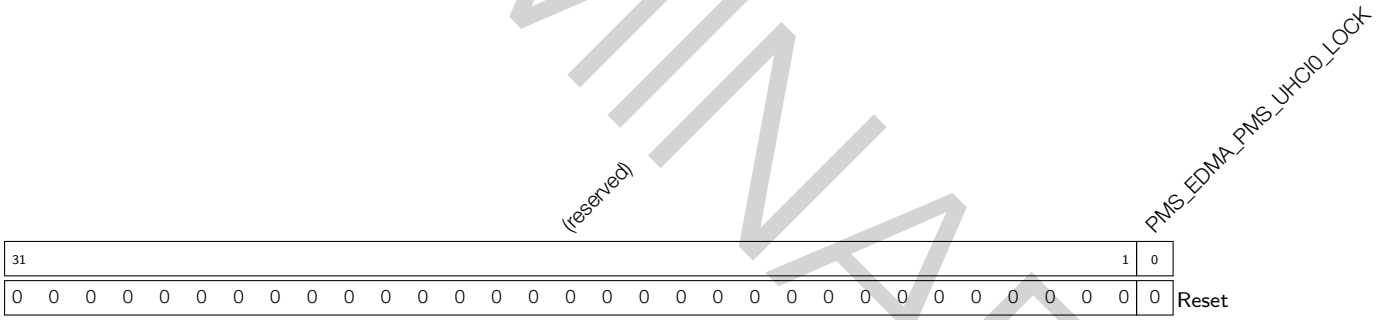
Register 13.75. PMS_EDMA_PMS_SPI3_REG (0x02C4)



PMS_EDMA_PMS_SPI3_ATTR1 Configures SPI3's access to external SRAM Area0. For details, see Table 13-22. (R/W)

PMS_EDMA_PMS_SPI3_ATTR2 Configures SPI3's access to external SRAM Area1. For details, see Table 13-22. (R/W)

Register 13.76. PMS_EDMA_PMS_UHCI0_LOCK_REG (0x02C8)



PMS_EDMA_PMS_UHCI0_LOCK Set this bit to lock the register that configures UHCI0's access to external SRAM. (R/W)

PRELIMINARY

Register 13.77. PMS_EDMA_PMS_UHCI0_REG (0x02CC)

PMS_EDMA_PMS_UHCI0_ATTR1 Configures UHCI0's access to external SRAM Area0. For details, see Table 13-22. (R/W)

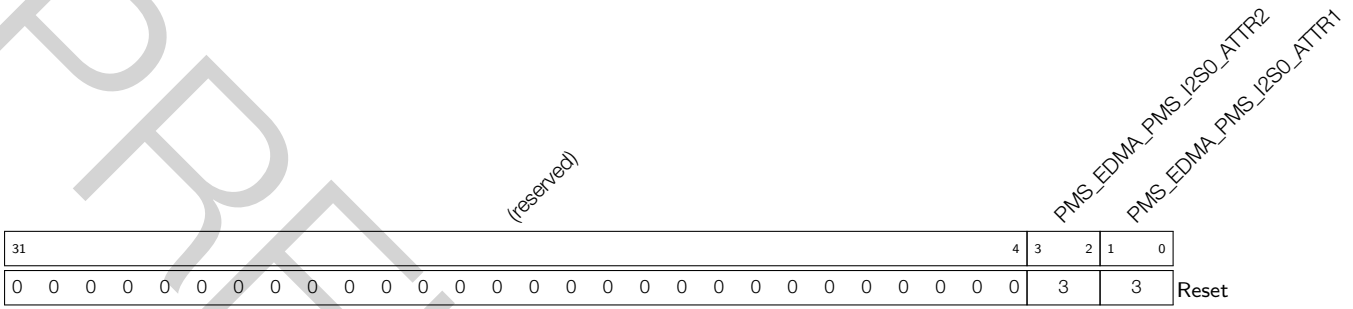
PMS_EDMA_PMS_UHCI0_ATTR2 Configures UHCI0's access to external SRAM Area1. For details, see Table 13-22. (R/W)

Register 13.78. PMS_EDMA_PMS_I2S0_LOCK_REG (0x02D0)

PMS_EDMA_PMS_I2S0_LOCK Set this bit to lock the register that configures I2S0's access to external SRAM. (R/W)

PRELIMINARY

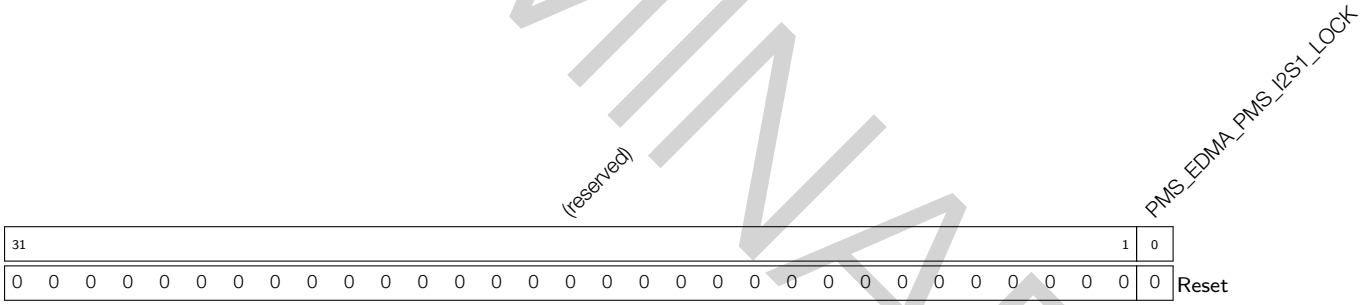
Register 13.79. PMS_EDMA_PMS_I2S0_REG (0x02D4)



PMS_EDMA_PMS_I2S0_ATTR1 Configures I2S0's access to external SRAM Area0. For details, see Table 13-22. (R/W)

PMS_EDMA_PMS_I2S0_ATTR2 Configures I2S0's access to external SRAM Area1. For details, see Table 13-22. (R/W)

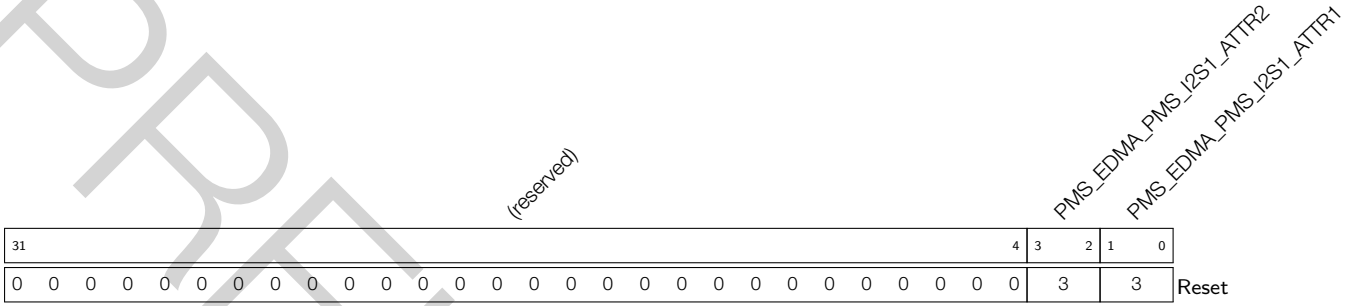
Register 13.80. PMS_EDMA_PMS_I2S1_LOCK_REG (0x02D8)



PMS_EDMA_PMS_I2S1_LOCK Set this bit to lock the register that configures I2S1's access to external SRAM. (R/W)

PRELIMINARY

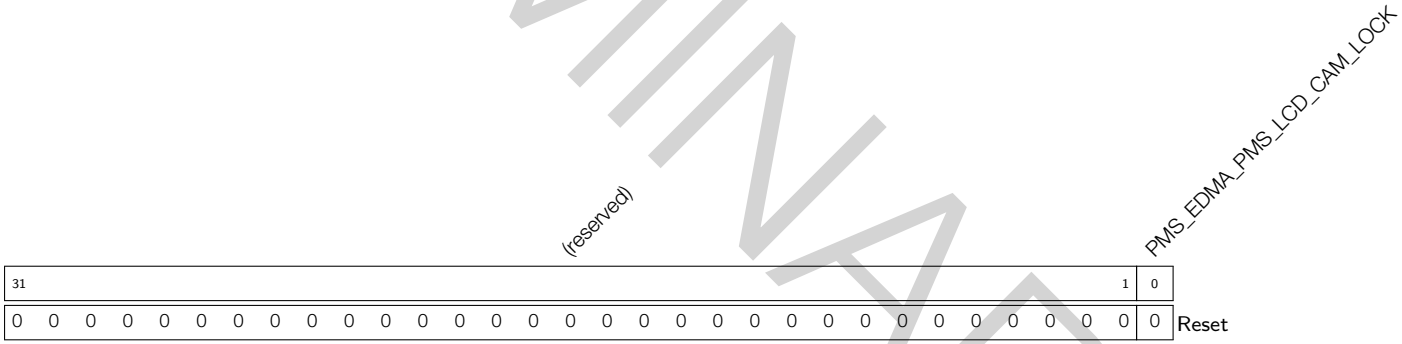
Register 13.81. PMS_EDMA_PMS_I2S1_REG (0x02DC)



PMS_EDMA_PMS_I2S1_ATTR1 Configures I2S1's access to external SRAM Area0. For details, see Table 13-22. (R/W)

PMS_EDMA_PMS_I2S1_ATTR2 Configures I2S1's access to external SRAM Area0. For details, see Table 13-22. (R/W)

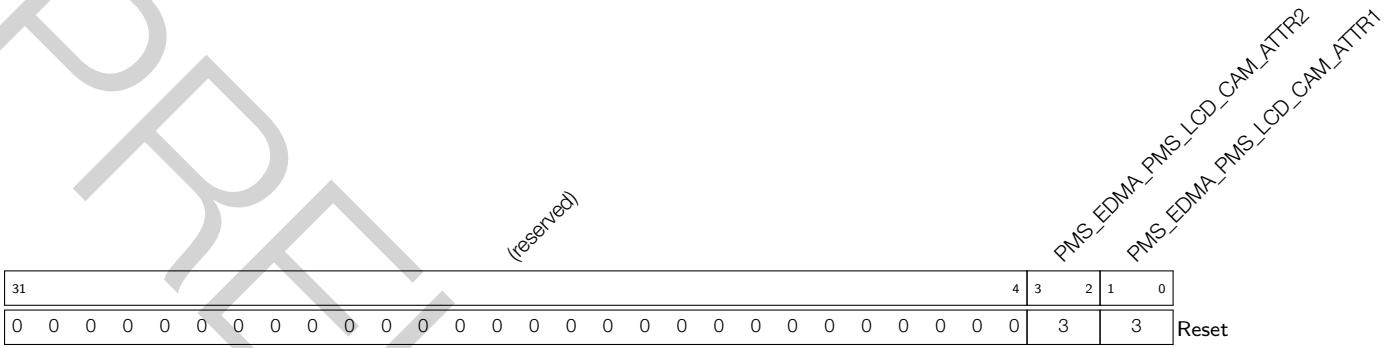
Register 13.82. PMS_EDMA_PMS_LCD_CAM_LOCK_REG (0x02E0)



PMS_EDMA_PMS_LCD_CAM_LOCK Set this bit to lock the register that configures Camera-LCD Controller's access to external SRAM. (R/W)

PRELIMINARY

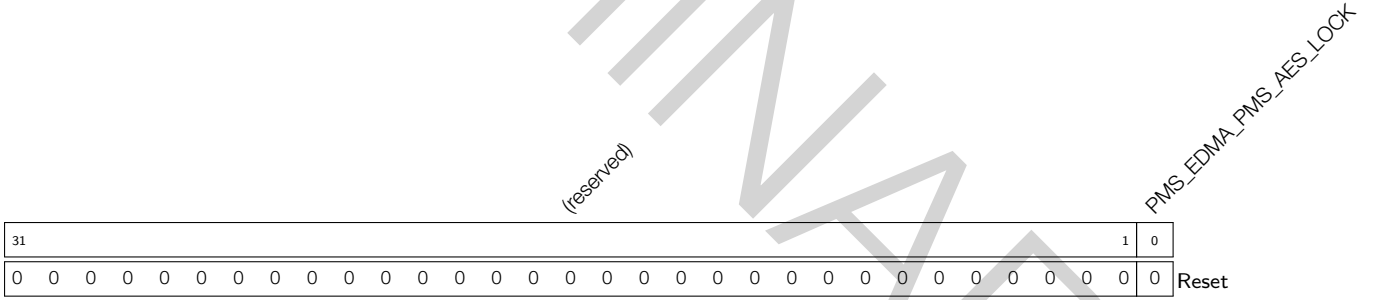
Register 13.83. PMS_EDMA_PMS_LCD_CAM_REG (0x02E4)



PMS_EDMA_PMS_LCD_CAM_ATTR1 Configures Camera-LCD Controller's access to external SRAM Area0. For details, see Table 13-22. (R/W)

PMS_EDMA_PMS_LCD_CAM_ATTR2 Configures Camera-LCD Controller's access to external SRAM Area1. For details, see Table 13-22. (R/W)

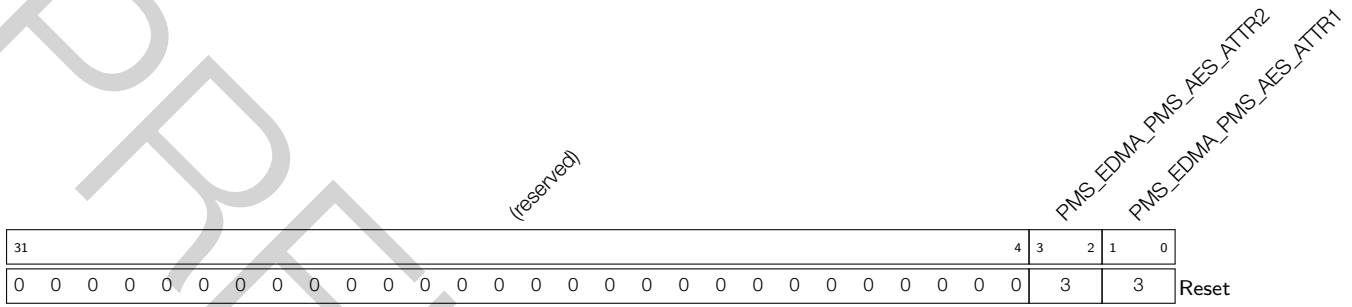
Register 13.84. PMS_EDMA_PMS_AES_LOCK_REG (0x02E8)



PMS_EDMA_PMS_AES_LOCK Set this bit to lock the register that configures AES's access to external SRAM. (R/W)

PRELIMINARY

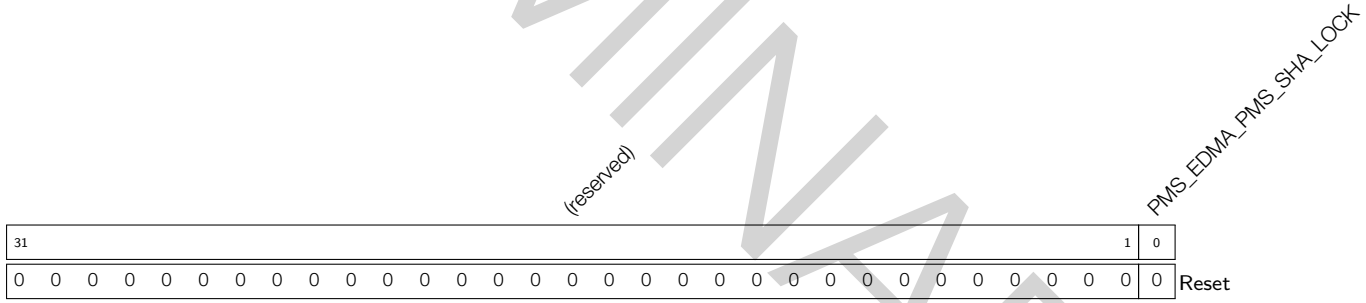
Register 13.85. PMS_EDMA_PMS_AES_REG (0x02EC)



PMS_EDMA_PMS_AES_ATTR1 Configures AES's access to external SRAM Area0. For details, see Table 13-22. (R/W)

PMS_EDMA_PMS_AES_ATTR2 Configures AES's access to external SRAM Area1. For details, see Table 13-22. (R/W)

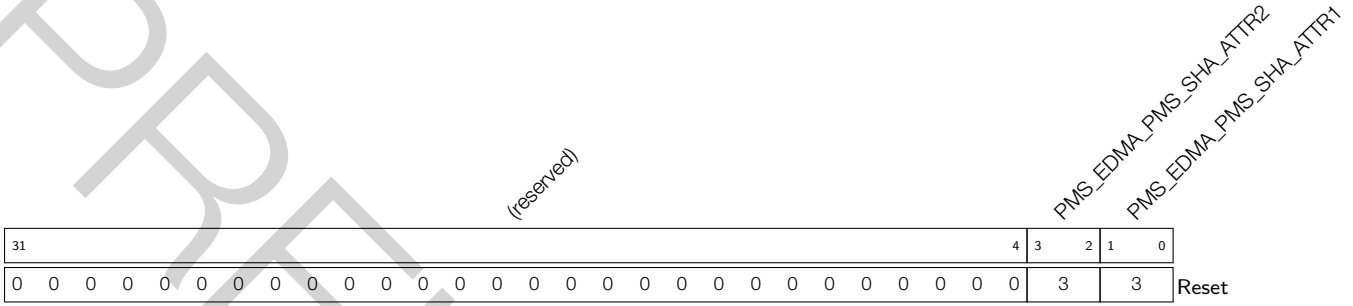
Register 13.86. PMS_EDMA_PMS_SHA_LOCK_REG (0x02F0)



PMS_EDMA_PMS_SHA_LOCK Set this bit to lock the register that configures SHA's access to external SRAM. (R/W)

PRELIMINARY

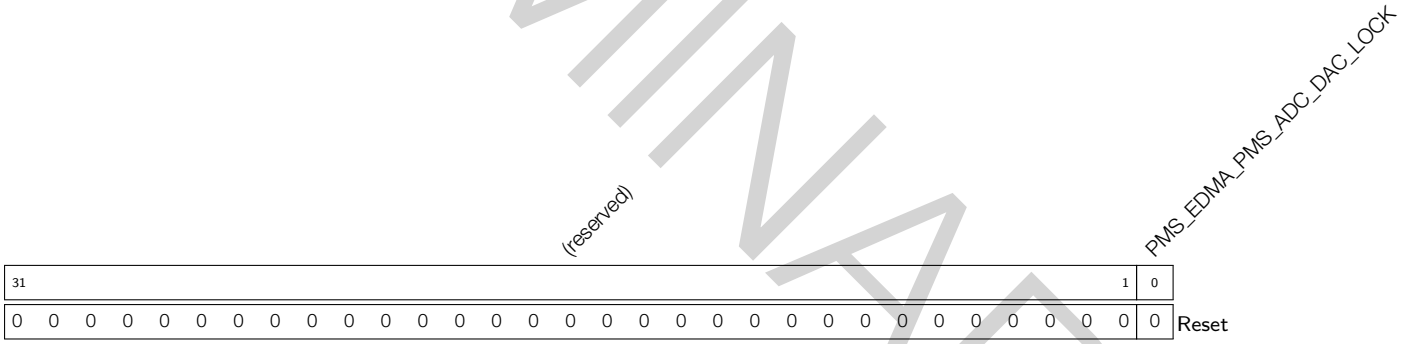
Register 13.87. PMS_EDMA_PMS_SHA_REG (0x02F4)



PMS_EDMA_PMS_SHA_ATTR1 Configures SHA's access to external SRAM Area0. For details, see Table 13-22. (R/W)

PMS_EDMA_PMS_SHA_ATTR2 Configures SHA's access to external SRAM Area1. For details, see Table 13-22. (R/W)

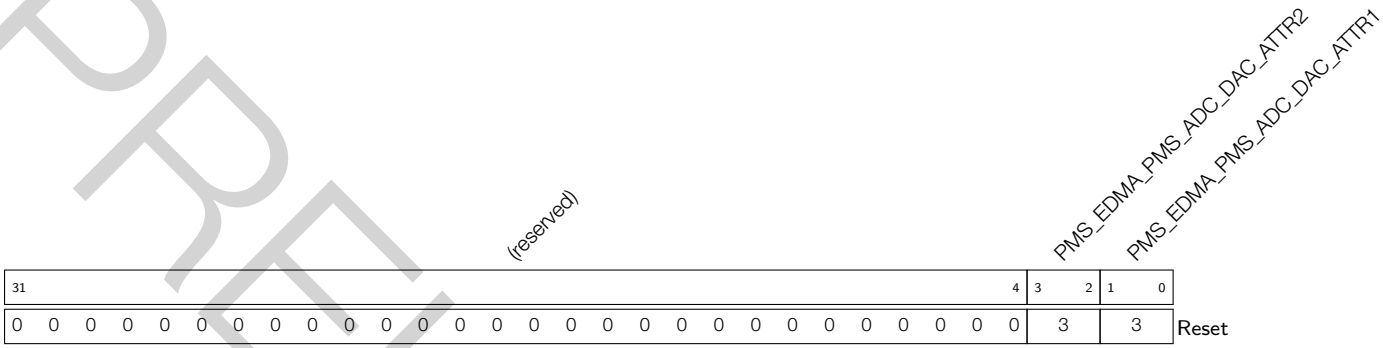
Register 13.88. PMS_EDMA_PMS_ADC_DAC_LOCK_REG (0x02F8)



PMS_EDMA_PMS_ADC_DAC_LOCK Set this bit to lock the register that configures ADC Controller's access to external SRAM. (R/W)

PRELIMINARY

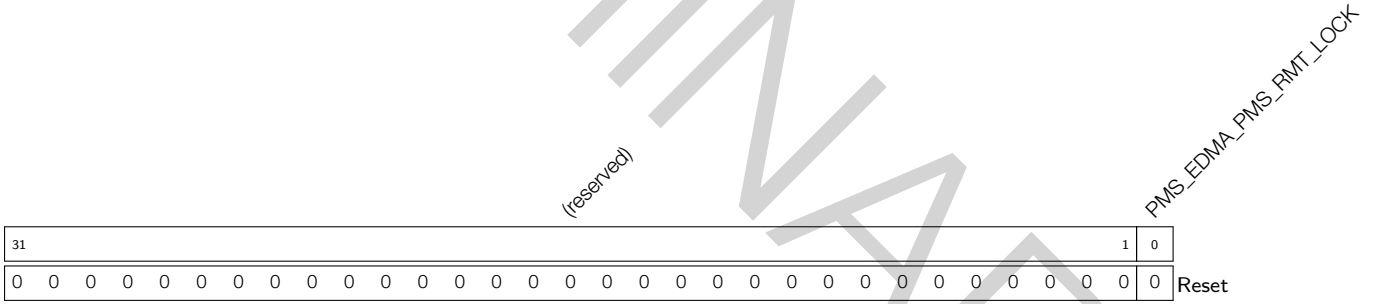
Register 13.89. PMS_EDMA_PMS_ADC_DAC_REG (0x02FC)



PMS_EDMA_PMS_ADC_DAC_ATTR1 Configures ADC Controller's access to external SRAM Area0. For details, see Table 13-22. (R/W)

PMS_EDMA_PMS_ADC_DAC_ATTR2 Configures ADC Controller's access to external SRAM Area1. For details, see Table 13-22. (R/W)

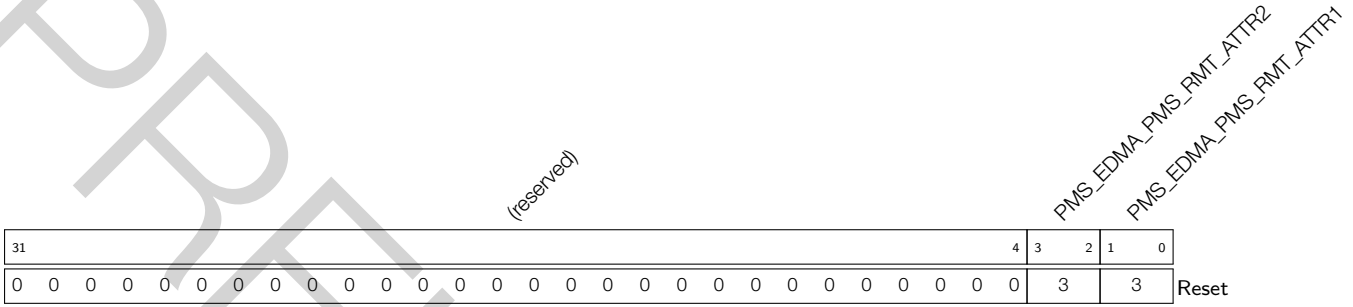
Register 13.90. PMS_EDMA_PMS_RMT_LOCK_REG (0x0300)



PMS_EDMA_PMS_RMT_LOCK Set this bit to lock the register that configures Remote Control Peripheral's access to external SRAM. (R/W)

PRELIMINARY

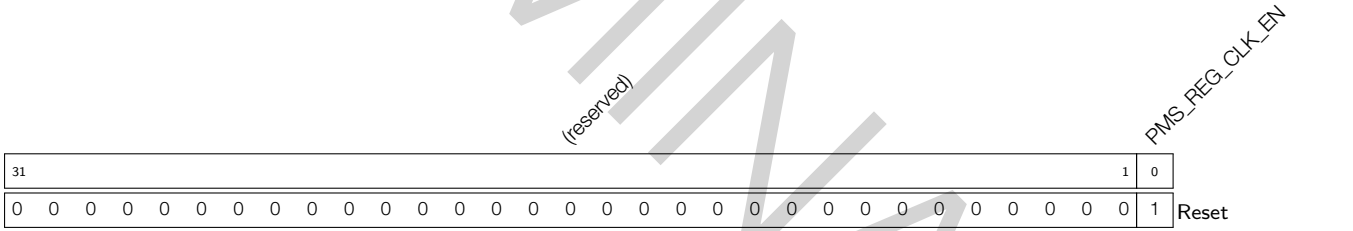
Register 13.91. PMS_EDMA_PMS_RMT_REG (0x0304)



PMS_EDMA_PMS_RMT_ATTR1 Configures Remote Control Peripheral's access to external SRAM Area0. For details, see Table 13-22. (R/W)

PMS_EDMA_PMS_RMT_ATTR2 Configures Remote Control Peripheral's access to external SRAM Area1. For details, see Table 13-22. (R/W)

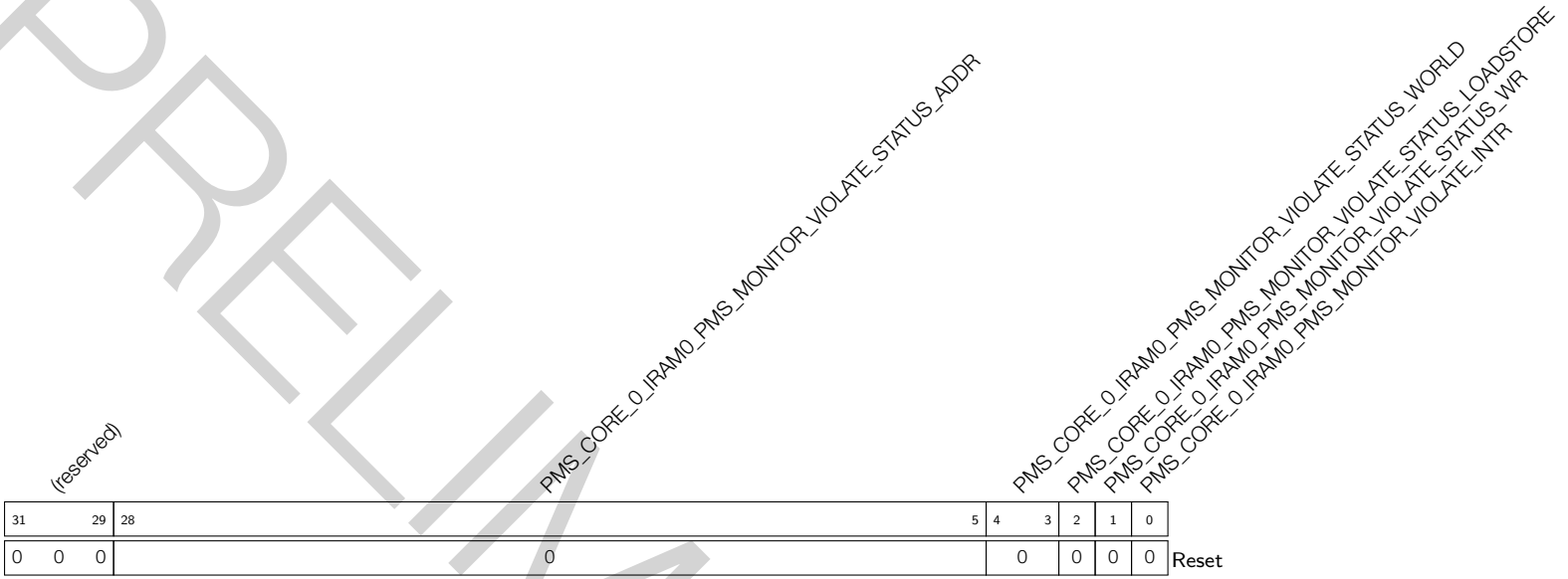
Register 13.92. PMS_CLOCK_GATE_REG_REG (0x0308)



PMS_REG_CLK_EN Set this bit to enable the clock gating function. (R/W)

PRELIMINARY

Register 13.93. PMS_CORE_0_IRAM0_PMS_MONITOR_2_REG (0x00EC)



PMS_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_INTR Stores the interrupt status of CPU0's unauthorized IBUS access. (RO)

PMS_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_STATUS_WR Indicates the access direction. 1: write; 0: read. Note that this field is only valid when PMS_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_STATUS_LOADSTORE is 1. (RO)

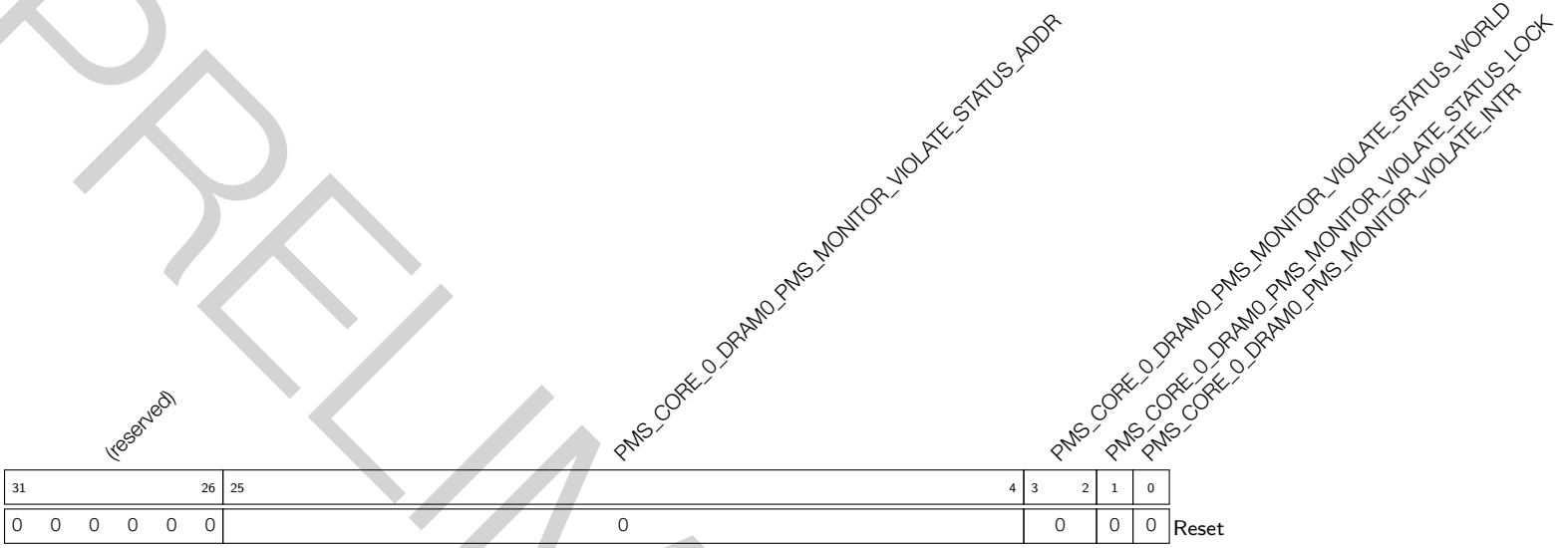
PMS_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_STATUS_LOADSTORE Indicates the instruction direction. 1: load/store; 0: instruction execution. (RO)

PMS_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_STATUS_WORLD Stores the world the CPU0 was in when the illegal access happened. 0b01: Secure World; 0b10: Non-secure World. (RO)

PMS_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_STATUS_ADDR Stores the address that CPU0's IBUS was trying to access unauthorized. Note that this is an offset to 0x40000000 and the unit is 4, which means the actual address should be 0x40000000 + PMS_CORE_0_IRAM0_PMS_MONITOR_VIOLATE_STATUS_ADDR * 4. (RO)

PRELIMINARY

Register 13.94. PMS_CORE_0_DRAM0_PMS_MONITOR_2_REG (0x010C)



PMS_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_INTR Stores the interrupt status of dBUS unauthorized access. (RO)

PMS_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_STATUS_LOCK Flags atomic access. 1: atomic access; 0: not atomic access. (RO)

PMS_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_STATUS_WORLD Stores the world the CPU was in when the unauthorized access happened. 0b01: Secure World; 0b10: Non-secure World. (RO)

PMS_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_STATUS_ADDR Stores the address that CPU0's dBUS was trying to access unauthorized. Note that this is an offset to 0x3c000000 and the unit is 16, which means the actual address should be 0x3c000000 + PMS_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_STATUS_ADDR * 16. (RO)

PRELIMINARY

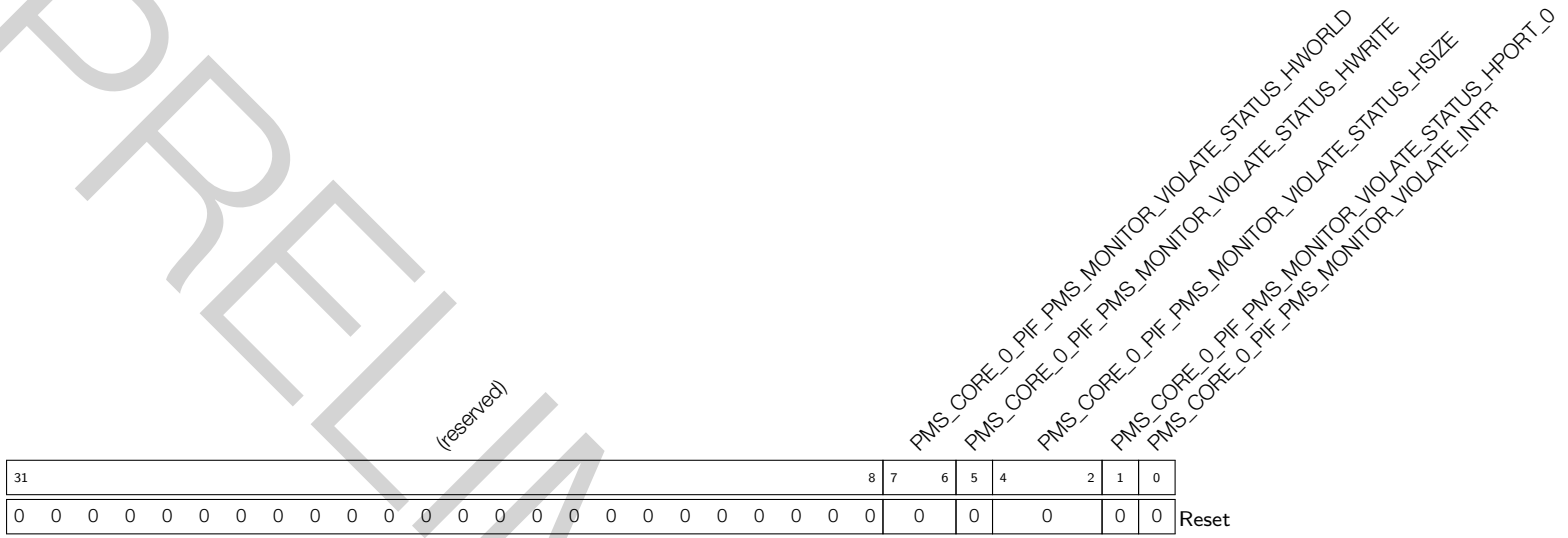
Register 13.95. PMS_CORE_0_DRAM0_PMS_MONITOR_3_REG (0x0110)

PMS_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_STATUS_WR Stores the direction of unauthorized access. 0: read; 1: write. (RO)

PMS_CORE_0_DRAM0_PMS_MONITOR_VIOLATE_STATUS_BYTEEN Stores the byte information of illegal access. (RO)

PRELIMINARY

Register 13.96. PMS_CORE_0_PIF_PMS_MONITOR_2_REG (0x01A4)



PMS_CORE_0_PIF_PMS_MONITOR_VIOLATE_INTR Stores the interrupt status of PIF bus unauthorized access. (RO)

PMS_CORE_0_PIF_PMS_MONITOR_VIOLATE_STATUS_HPORT_0 Stores the type of unauthorized access. 0: instruction; 1: data. (RO)

PMS_CORE_0_PIF_PMS_MONITOR_VIOLATE_STATUS_HSIZE Stores the data type of unauthorized access. 0: byte; 1: half-word; 2: word. (RO)

PMS_CORE_0_PIF_PMS_MONITOR_VIOLATE_STATUS_HWRITE Stores the direction of unauthorized access. 0: read; 1: write. (RO)

PMS_CORE_0_PIF_PMS_MONITOR_VIOLATE_STATUS_HWORLD Stores the world the CPU was in when the unauthorized access happened. 01: Secure World; 10: Non-secure World. (RO)

PRELIMINARY

Register 13.97. PMS_CORE_0_PIF_PMS_MONITOR_3_REG (0x01A8)

PMS_CORE_0_PIF_PMS_MONITOR_VIOLATE_STATUS_HADDR Stores the address that CPU0's PIF bus was trying to access unauthorized. (RO)

PRELIMINARY

Register 13.98. PMS_CORE_0_PIF_PMS_MONITOR_5_REG (0x01B0)

PMS_CORE_0_PIF_PMS_MONITOR_NONWORD_VIOLATE_INTR Stores the interrupt status of PIF upsupported data type. (RO)

PMS_CORE_0_PIF_PMS_MONITOR_NONWORD_VIOLATE_STATUS_HSIZE Stores the data type when the unauthorized access happened. (RO)

PMS_CORE_0_PIF_PMS_MONITOR_NONWORD_VIOLATE_STATUS_HWORLD Stores the world the CPU was in when the unauthorized access happened. 01: Secure World; 10: Non-secure World. (RO)

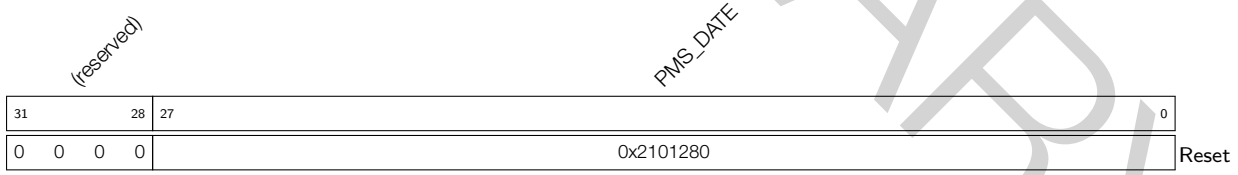
PRELIMINARY

Register 13.99. PMS_CORE_0_PIF_PMS_MONITOR_6_REG (0x01B4)



PMS_CORE_0_PIF_PMS_MONITOR_NONWORD_VIOLATE_STATUS_HADDR Stores the address that CPU0's PIF bus was trying to access using unsupported data type. (RO)

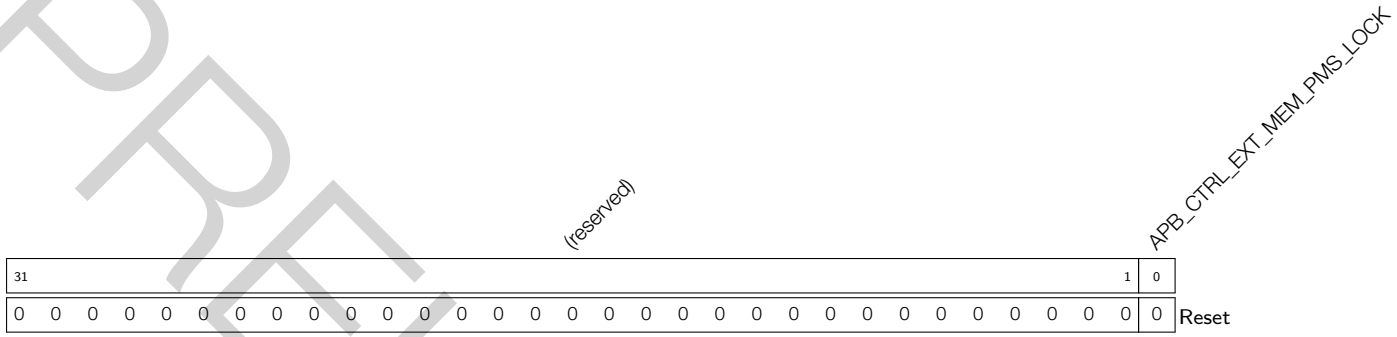
Register 13.100. PMS_DATE_REG (0x0FFC)



PMS_DATE Sensitive Date register. (R/W)

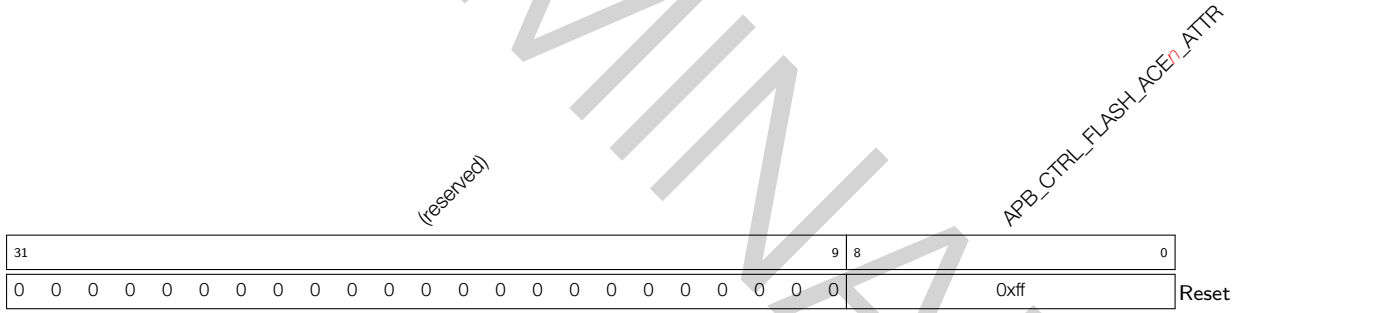
PRELIMINARY

Register 13.101. APB_CTRL_EXT_MEM_PMS_LOCK_REG (0x0020)



APB_CTRL_EXT_MEM_PMS_LOCK Set this bit to lock the permission configuration related to external memory. (R/W)

Register 13.102. APB_CTRL_FLASH_ACE*n*_ATTR_REG (*n*: 0 - 3) (0x0028 + 4**n*)



APB_CTRL_FLASH_ACE*n*_ATTR Configures the permission to Region *n* of Flash. (R/W)

PRELIMINARY

Register 13.103. APB_CTRL_FLASH_ACE*n*_ADDR_REG (*n*: 0-3) (0x0038 + 4n*)**

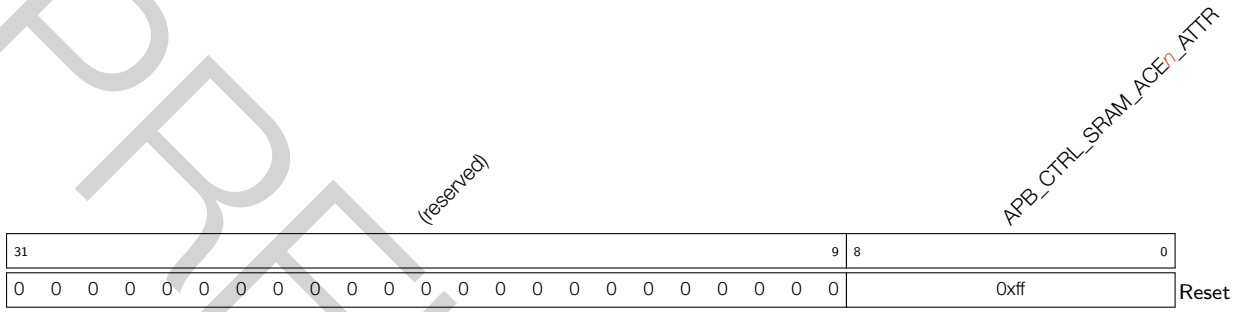
APB_CTRL_FLASH_ACE0_ADDR_S Configure the starting address of Flash Region *n*. The size of each region should be aligned to 64 KB. (R/W)

Register 13.104. APB_CTRL_FLASH_ACE*n*_SIZE_REG (*n*: 0-3) (0x0048 + 4n*)**

APB_CTRL_FLASH_ACE*n*_SIZE Configure the length of Flash Region *n*. The size of each region should be aligned to 64 KB. (R/W)

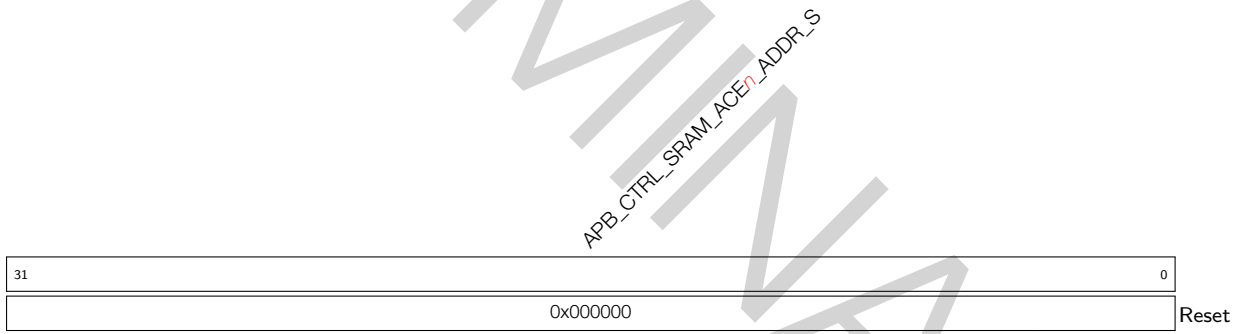
PRELIMINARY

Register 13.105. APB_CTRL_SRAM_ACE*n*_ATTR_REG (0x0058)



APB_CTRL_SRAM_ACE*n*_ATTR Configures the permission to Region *n* of SRAM. (R/W)

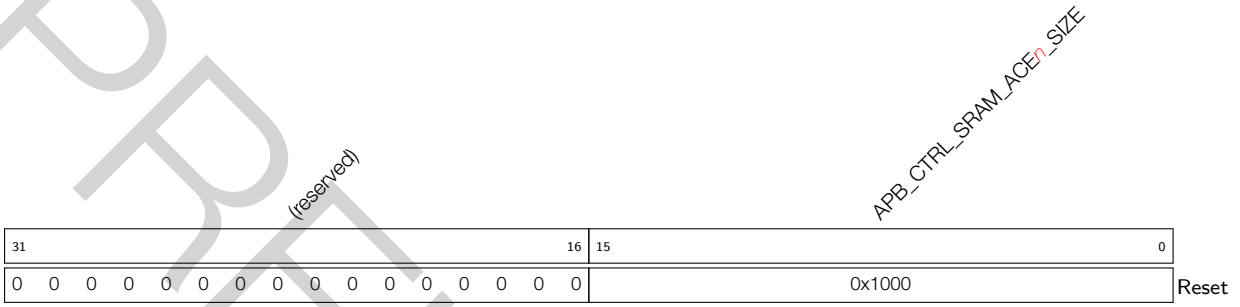
Register 13.106. APB_CTRL_SRAM_ACE*n*_ADDR_REG (*n*: 0-3) (0x0068 + 4n*)**



APB_CTRL_SRAM_ACE*n*_ADDR_S Configure the starting address of SRAM Region *n*. The size of each region should be aligned to 64 KB. (R/W)

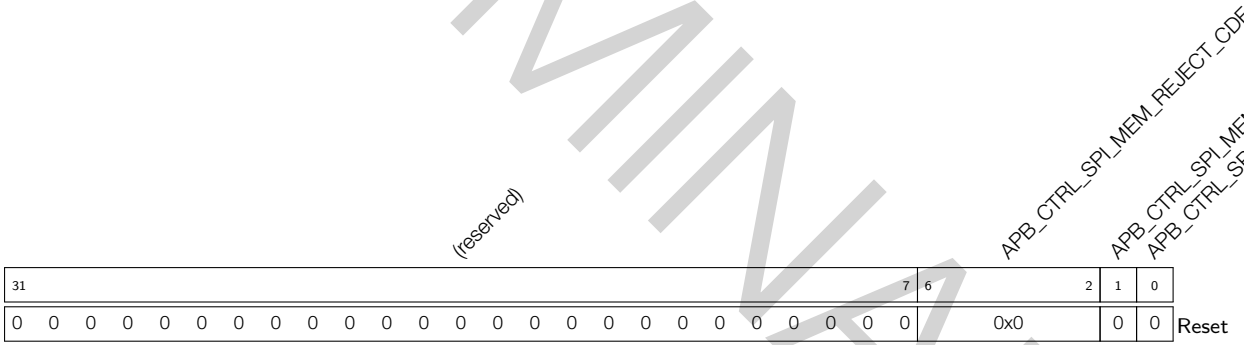
PRELIMINARY

Register 13.107. APB_CTRL_SRAM_ACE*n*_SIZE_REG (*n*: 0-3) (0x0078 + 4**n*)



APB_CTRL_SRAM_ACE*n*_SIZE Configure the lenght of SRAM Region *n*. The size of each region should be aligned to 64 KB. (R/W)

Register 13.108. APB_CTRL_SPI_MEM_PMS_CTRL_REG (0x0088)



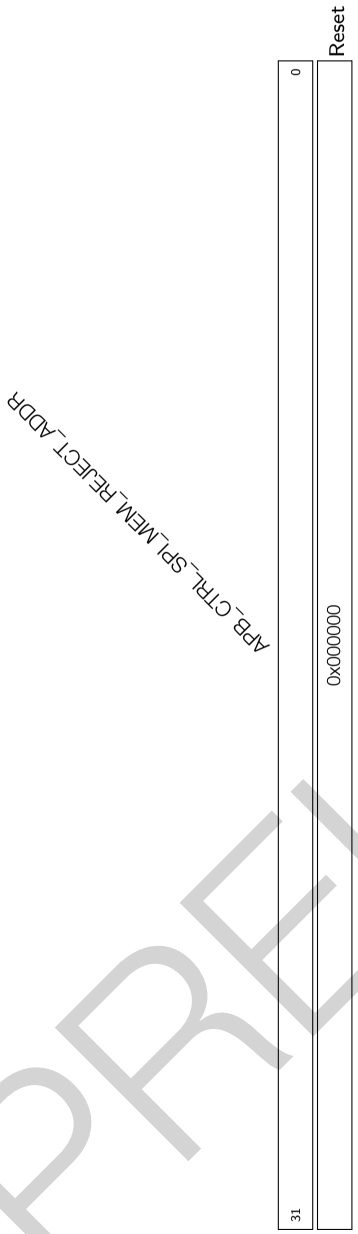
APB_CTRL_SPI_MEM_REJECT_INT Indicates exception accessing external memory and triggers an interrupt. (RO)

APB_CTRL_SPI_MEM_REJECT_CLR Set this bit to clear the exception status. (WOD)

APB_CTRL_SPI_MEM_REJECT_CDE Stores the exception cause: invalid region, overlapping regions, illegal write, illegal read and illegal instruction execution. (RO)

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Register 13.109. APB_CTRL_SPI_MEM_REJECT_ADDR_REG (0x008C)



APB_CTRL_SPI_MEM_REJECT_ADDR Store the exception address.(RO)

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14 World Controller

14.1 Introduction

ESP32-S3 allows users to allocate its hardware and software resource into Secure World (World0) and Non-secure World (World1), thus protecting resource from unauthorized access (read or write), and from malicious attacks such as malware, hardware-based monitoring, hardware-level intervention, and so on. CPUs can switch between Secure World and Non-secure World with the help of the World Controller.

By default, all resource in ESP32-S3 are shareable. Users can allocate the resource into two worlds by managing respective permission (For details, please refer to Chapter 13 *Permission Control (PMS)*). This chapter only introduces the World Controller and how CPUs can switch between worlds with the help of World Controller.

14.2 Features

ESP32-S3's World Controller:

- Controls the CPUs to switch between the Secure World and Non-secure World
- Logs CPU's world switches
- Allows NMI masking
- Allows independent world switches of CPUs (CORE_*m*: CPU0 and CPU1)

14.3 Functional Description

With the help of World Controller, we can allocate different resources to the Secure World and the Non-secure World:

- Secure World (World0):
  - Can access all peripherals and memories;
  - Performs all confidential operations, such as fingerprint identification, password processing, data encryption and decryption, security authentication, etc.
- Non-secure World (World1):
  - Can access some peripherals and memories;
  - Performs other operations, such as user operation and different applications, etc.

ESP32-S3's CPU and slave devices are both configurable with permission to either Secure World and/or Non-Secure World:

- CPU can be in either world at a particular time:
  - In Secure World: performs confidential operations;
  - In Non-secure World: performs non-confidential operations;
  - By default, CPU runs in Secure World after power-up, then can be programmed to switch between two worlds.

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- All slave devices (including peripherals* and memories) can be configured to be accessible from the Secure World and/or the Non-secure World:
  - Secure World Access: this slave can be called from Secure World only, meaning it can be accessed only when CPU is in Secure World;
  - Non-secure World Access: this slave can be called from Non-secure World only, meaning it can be accessed only when CPU is in Non-secure World.
  - Note that a slave can be configured to be accessible from both Secure World and Non-secure World simultaneously.

  For details, please refer to Chapter 13 *Permission Control (PMS)*.

Note:

* World Controller itself is a peripheral, meaning it also can be granted with Secure World access and/or Non-secure World access, just like all other peripherals. However, to secure the world switch mechanism, World Controller should not be accessible from Non-secure world. Therefore, world controller **should not be granted with** Non-secure World access, preventing any modification to world controller from the Non-secure World.

When CPU accesses any slaves:

1. First, CPU notifies the salve about its own world information;
2. Second, slave decides if it can be accessed by CPU based on the CPU's world information and it's own world permission configuration.
   - if allowed, then this slave responds to CPU;
   - if not allowed, then this slave will not respond to CPU and trigger an interrupt.

In this way, the resources in the Secure World will not be illegally accessible by the Non-secure World in an unauthorized way.

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14.4 CPU's World Switch

CPU can switch from Secure World to Non-secure World, and from Non-secure World to Secure World.

14.4.1 From Secure World to Non-secure World

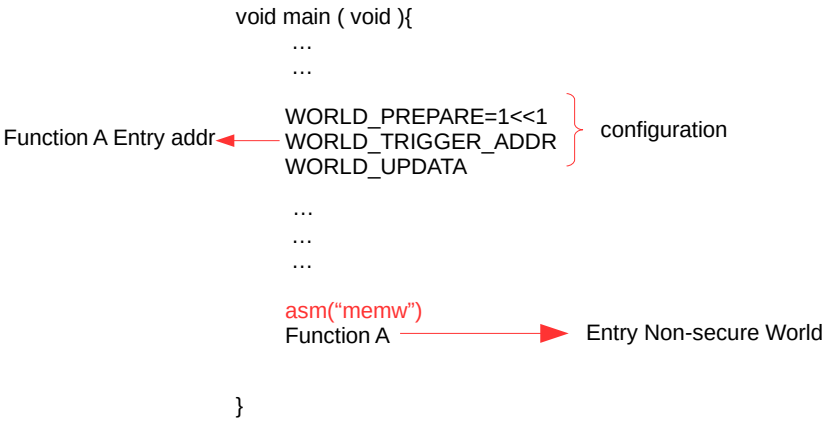


Figure 14-1. Switching From Secure World to Non-secure World

ESP32-S3's CPU only needs to complete the following steps to switch from Secure World to Non-secure World:

1. Configure the World Controller, as described below.
2. Clear the data stored in write_buffer, as described in Section 14.4.3.

After that, CPU can switch to the Non-secure World.

However, it's worth noting that you cannot call the application in Non-secure world immediately after configuring the World Controller. For reasons such as CPU pre-indexed addressing and pipeline, it is possible that the CPU have already executed the application in Non-secure World before the World Controller configuration is effective, meaning the CPU runs unsecured application in the Secure World.

Therefore, you need to make sure the CPU only calls applications in the Non-secure world after the World Controller configuration takes effect. This can be guaranteed by **declaring the applications in the Non-secure World as "noinline"**.

Configuring the World Controller

The steps to configure the World Controller to switch the CPU from the Secure World to the Non-secure World are described below:

1. Write 0x2 to Register WCL_CORE_*m*_WORLD_PERPARE_REG, indicating the CPU needs to switch to the Non-secure World.
2. Configure Register WCL_CORE_*m*_World_TRIGGER_ADDR_REG as the entry address to the Non-secure World, i.e., the address of the application in the Non-secure World that needs to be executed.
3. Write any value to Register WCL_CORE_*m*_World_UPDATE_REG, indicating the configuration is done.

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Note:

- Register WCL_CORE_*m*_World_UPDATE_REG must be configured at last.
- Registers WCL_CORE*m*_WORLD_PERPARE_REG and WCL_CORE_*m*_World_TRIGGER_ADDR_REG can be configured in any order.
- After the configuration, you also need to use assembly instruction memw (memory wait) to clear write_buffer. For details, see Section 14.4.3.

Afterwards, the World Controller keeps monitoring if CPU is executing the configured address of the application in Non-secure World. CPU switches to the Non-secure World once it executes the configured address, and executes the applications in the Non-secure World.

After configuration, the World Controller:

- Keeps monitoring until the CPU executes the configured address and switches to the Non-secure World.
  - Write any value to Register WCL_CORE_*m*_World_Cancel_REG to cancel the World Controller configuration. After the cancellation, CPU will not switch to the Non-secure World even it executes to the configured address. Note that you also need to use assembly instruction memw (memory wait) to clear write_buffer. For details, see Section 14.4.3.
- The World Controller can only switch from the Secure World to Non-secure World once per configuration. Therefore, the World Controller needs to be configured again after each world switch to prepare it for the next world switch.

14.4.2 From Non-secure World to Secure World

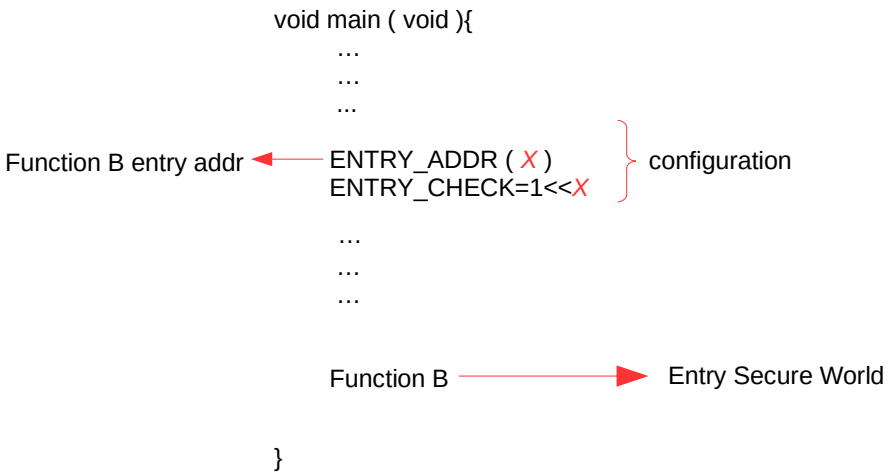


Figure 14-2. Switching From Non-secure World to Secure World

CPU can only switch from Non-secure World to Secure World via **Interrupts (or Exceptions)**. After configuring the World Controller, the CPU can switch back Non-secure World to Secure World upon the configured Interrupt trigger.

See details below:

1. Configure Registers WCL_CORE_*m*_MESSAGE_ADDR_REG and WCL_CORE_*m*_MESSAGE_MAX_REG to clear write_buffer, as described in Section 14.4.3.
2. Configure Registers WCL_CORE_*m*_ENTRY_*n*_ADDR_REG (*n*: 1-13) as the entry address of interrupts (or exceptions).
   - Note that all of ESP32-S3's interrupts and exceptions are using VecBase + offset as its address. Therefore, you need to configure WCL_CORE_*m*_ENTRY_*n*_ADDR_REG (*n*: 1-13) whenever you modify the VecBase.
3. Configure Register WCL_CORE_*m*_ENTRY_CHECK_REG to enable the monitor of a certain entry. In this way, the CPU switches to the Secure World immediately when it executes the address monitored at this particular entry.
   - Bit *x* controls the entry monitoring of Entry *x* (WCL_CORE_*m*_ENTRY_*x*_ADDR_REG). You can enable monitoring for more than one entry.
     - 0: Disable monitoring
     - 1: Enable monitoring
   - Register WCL_CORE_*m*_ENTRY_CHECK_REG is effective after configuration all the time till it's disabled, meaning you don't need to configure this register every time after each world switch.

14.4.3 Clearing the write_buffer

ESP32-S3 has implemented write_buffer, which means the CPU buses can still hold some data from or execute instructions from the other world after world switches. To improve data security, we need to clear the writer_buffer before world switching:

- **Switching from Secure World to Non-secure World**
  - Use assembly instruction memw (memory wait).
- **Switching from Non-secure World to Secure World**
  - Switch CPU data bus:
    1. Pre-configure the following registers:
       * Configures Register WCL_CORE_*m*_MESSAGE_ADDR_REG to an address in the Non-secure World;
       * Configure Register WCL_CORE_*m*_MESSAGE_MAX_REG to *Z* ($Z \in \{3, 4, \ldots, 16\}$)
    2. Write sequences of 0, 1, …, *Z-1*, *Z* to the address configured in Register WCL_CORE_*m*_MESSAGE_ADDR_REG before world switching. For example, if *Z* is configured to 3, then you need to write sequences of 0, 1, 2, 3 into the configured address; if *Z* is 5, then write 0, 1, 2, 3, 4, 5.
    3. Afterwards, the CPU will switch its data bus to the other world once it detects the agreed sequences configured in WCL_CORE_*m*_MESSAGE_MAX_REG are being written to the agreed address configured in WCL_CORE_*m*_MESSAGE_ADDR_REG.

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14.5 World Switch Log

In actual use cases, CPU is switching between two worlds quite frequently and has to deal with nested interrupts. To be able to restore to the previous world, World Controller keeps a world switching log in a series of registers, which is called “World Switch Log Table”.

14.5.1 Structure of World Switch Log Register

ESP32-S3’s World Switch Log Table consists of 13 WCL_CORE_*m*_STATUSTABLE*n*_REG(*n*: 1-13) registers (see Figure 14-3). The world switching of address configured in WCL_CORE_*m*_ENTRY_*x*_ADDR_REG, which is monitored at Entry *x*, is logged in WCL_CORE_*m*_STATUSTABLE*x*_REG.

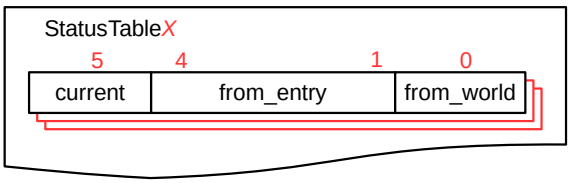


Figure 14-3. World Switch Log Register

- WCL_CORE_*m*_FROM_WORLD_*n*: logs the world information before the world switch.
  - 0: CUP was in Secure World
  - 1: CPU was in Non-secure World
- WCL_CORE_*m*_FROM_ENTRY_*n*: logs the entry information before the world switch.
  - 0: CPU was not at any interrupts monitored at any entry.
  - 1 - 13: CPU was at the interrupt monitored at a certain entry.
- WCL_CORE_*m*_CURRENT_*n*: indicates if CPU is at the interrupt monitored at the current entry. When CPU is at the interrupt monitored at Entry *x*,
  - WCL_CORE_*m*_CURRENT_*x* is updated to 1,
  - and the same fields of all other entries are updated to 0.

14.5.2 How World Switch Log Registers are Updated

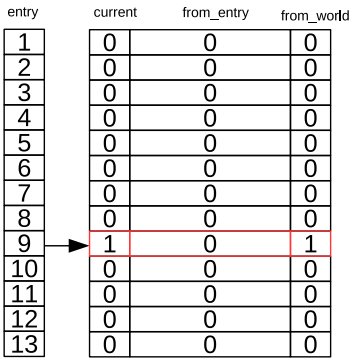
To explain this process, assuming:

1. At the beginning:
   - CPU is running in the Non-secure World;
   - Registers WCL_CORE_*m*_STATUSTABLE*n*_REG(*n*: 1-13) are all empty.
2. Then an interrupt occurs at Entry 9;
3. Then another interrupt with higher priority occurs at Entry 1;
4. Then the last interrupt with highest priority occurs at Entry 4.

The World Switch Log Table is updated as described below:

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1. First, an interrupt occurs at Entry 9. At this time, CPU executes to the entry address of this interrupt. The World Switch Log Table is updated as described in Figure 14-4:

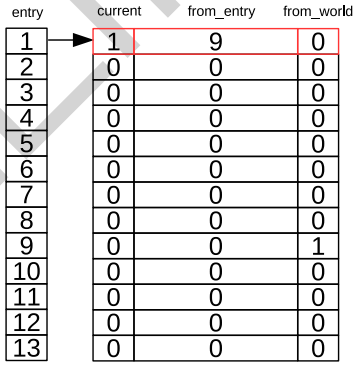


entry	current	from_entry	from_world
1	0	0	0
2	0	0	0
3	0	0	0
4	0	0	0
5	0	0	0
6	0	0	0
7	0	0	0
8	0	0	0
9	1	0	1
10	0	0	0
11	0	0	0
12	0	0	0
13	0	0	0

Figure 14-4. Nested Interrupts Handling - Entry 9

   - WCL_CORE_*m*_STATUSTABLE9_REG
     - Field WCL_CORE_*m*_FROM_WORLD_9 is updated to 1, indicating CPU was in Non-secure World before the interrupt.
     - Field WCL_CORE_*m*_FROM_ENTRY_9 is updated to 0, indicating there was not any interrupt before this one.
     - Field WCL_CORE_*m*_CURRENT_9 is updated to 1, indicating the CPU is currently at the interrupt monitored at Entry 9.
   - Other WCL_CORE_*m*_STATUSTABLE*n*_REG registers are not updated.

2. Then another interrupt with higher priority occurs at Entry 1. At this time, CPU executes to the entry address of this interrupt. The World Switch Log Table is updated again as described in Figure 14-5:



entry	current	from_entry	from_world
1	1	9	0
2	0	0	0
3	0	0	0
4	0	0	0
5	0	0	0
6	0	0	0
7	0	0	0
8	0	0	0
9	0	0	1
10	0	0	0
11	0	0	0
12	0	0	0
13	0	0	0

Figure 14-5. Nested Interrupts Handling - Entry 1

   - WCL_CORE_*m*_STATUSTABLE1_REG
     - Field WCL_CORE_*m*_FROM_WORLD_1 is updated to 0, indicating the CPU was in Secure World before this interrupt.
     - Field WCL_CORE_*m*_FROM_ENTRY_1 is updated to 9, indicating the CPU was executing the interrupt at Entry 9.
     - Field WCL_CORE_*m*_CURRENT_1 is updated to 1, indicating CPU is currently at the interrupt monitored at Entry 1.

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- WCL_CORE_*m*_STATUSTABLE9_REG
  - Field WCL_CORE_*m*_CURRENT_9 is updated to 0, indicating CPU is no longer at the interrupt monitored at Entry 9 (Instead, CPU is at the interrupt monitored at Entry 1 already).
  - Fields WCL_CORE_*m*_FROM_WORLD_9 and WCL_CORE_*m*_FROM_ENTRY_9 stay the same.
- Other WCL_CORE_*m*_STATUSTABLE*n*_REG registers are not updated.

3. Then the last interrupt with highest priority occurs at Entry 4. At this time, CPU executes to the entry address of interrupt 4. The World Switch Log Table is updated again as described in Figure 14-6:

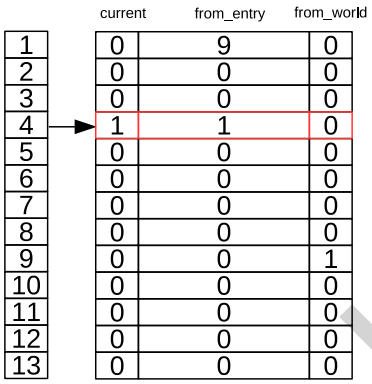


Figure 14-6. Nested Interrupts Handling - Entry 4

- WCL_CORE_*m*_STATUSTABLE4_REG
  - Field WCL_CORE_*m*_FROM_WORLD_4 is updated to 0, indicating the CPU was in Secure World before this interrupt.
  - Field WCL_CORE_*m*_FROM_ENTRY_4 is updated to 1, indicating the CPU was the interrupt at Entry 1.
  - Field WCL_CORE_*m*_CURRENT_4 is updated to 1, indicating the CPU is currently at the interrupt monitored an Entry 4.
- WCL_CORE_*m*_STATUSTABLE1_REG
  - Field WCL_CORE_*m*_CURRENT_1 is updated to 0, indicating the CPU is no longer at the interrupt monitored at Entry 1 (Instead CPU is at the interrupt monitored at Entry 4 already).
  - Fields WCL_CORE_*m*_FROM_WORLD_1 and WCL_CORE_*m*_FROM_ENTRY_1 are not updated.
- Other WCL_CORE_*m*_STATUSTABLE*n*_REG registers are not updated.

14.5.3 How to Read World Switch Log Registers

By reading World Switch Log Registers, we get to understand the information of previous world switches and nested interrupts, thus being able to restore to previous world.

Steps are described below: (See Figure 14-6 as an example):

1. Read Register WCL_CORE_*m*_STATUSTABLE_CURRENT_REG, and understand CPU is now at the interrupt monitored at Entry 4.
2. Read 1 from Field WCL_CORE_*m*_FROM_ENTRY_4, and understand the CPU was at an interrupt monitored at Entry 1.

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3. Read 9 from Field WCL_CORE_*m*_FROM_ENTRY_1, and understand the CPU was at an interrupt monitored at Entry 9.
4. Read 0 from WCL_CORE_*m*_FROM_ENTRY_9, and understand CPU wasn't at any interrupt. Then read 1 from WCL_CORE_*m*_FROM_WORLD_9, and understand CPU was in Non-secure World at the begining.

14.5.4 Nested Interrupts

ESP32-S3 supports nested interrupts, for example:

1. An interrupt A occurs. CPU jumps to interrupt A entry, which triggers world switches.
2. When CPU is handling interrupt A, an interrupt B with higher priority occurs.
3. Then the CPU drops the current interrupt A and switches to the higher priority interrupt B first.
4. After returning from interrupt B, CPU resumes executing the instruction at interrupt A entry, which triggers world switches again.

In this way, CPU executes the entry address of the first interrupt twice (one time when the interrupt occurs and another time when CPU returns to this interrupt), and thus triggering the world switches twice, which inevitably leads to multiple records tracked for the same interrupt in World Switch Log and prevents the CPU from restoring to the previous world correctly.

14.5.4.1 How to Handle Nested Interrupts

To avoid multiple records being logged incorrectly in the World Switch Log, the following actions must be completed:

- During the design stage, add two assembly instruction NOP.N (No Operation) to the vector entrance of all interrupts and exceptions.
- During the execution, update the address where the interrupts return to following the instructions described in 14.5.4.2.

In this way, when returning to the interrupt at Entry *B*, the interrupt monitored at Entry *A* will not return to the entry address of Entry *B*, but the address after the NOP instructions, thus preventing to trigger the world controller unexpectedly. Also, the NOP instruction doesn't do anything, so nothing is changed even when the NOP instructions are skipped.

14.5.4.2 Programming Procedure

Handling the interrupt at Entry *A*:

1. Clear the write_buffer by writing the agreed sequences configured in Register WCL_CORE_*m*_MESSAGE_MAX_REG to the address configured in WCL_CORE_*m*_MESSAGE_ADDR_REG. For details, see Section 14.4.3.
2. Execute the interrupt programs.
3. Disable all interrupts.
4. Update the address where the interrupt at Entry *A* returns to:
    - Read Field WCL_CORE_*m*_FROM_ENTRY_*A* for Entry *A*:

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- 0: indicates all interrupts are handled, and returns to a normal program:
  (a) Update Field WCL_CORE_*m*_CURRENT_*A* of Entry *A* to 0, indicating the CPU is no longer at the interrupt monitored at Entry *A*.
  (b) Go to Step 5.
- 1 - 13: indicates the CPU returns to another interrupt monitored at Entry *B*,
  (a) First, check the return address of the interrupt at Entry *A*:
    * If it points to the first NOP.N instruction of the interrupt at Entry *B*, then add 4 to the return address of the interrupt at Entry *A*.
    * If it points to the second NOP.N instruction of the interrupt at Entry *B*, then add 2 to the return address of the interrupt at Entry *A*.
    * If it points to other address, then no need to update the return address.
  (b) Update the How to Read World Switch Log Registers:
    * Update the world switch register of Entry *A*:
      · Update Field WCL_CORE_*m*_CURRENT_*A* to 0, indicating the CPU is no longer at the interrupt monitored at Entry *A*.
      · Fields WCL_CORE_*m*_FROM_WORLD_*A* and WCL_CORE_*m*_FROM_ENTRY_*A* stay the same.
    * Update the world switch register of Entry *B*:
      · Update Field WCL_CORE_*m*_CURRENT_*B* to 1, indicating the CPU will return to Entry *B*.

5. Prepare to exit interrupt.
   (a) Check if CPU needs to switch to the other world:
   - If world switch not required, then go to Step 6.
   - If world switch required, then switch the CPU to the other world following instructions described in Section 14.4, then go to Step 6.
6. Enable interrupts, and exit.

Note:
Steps 4 and 5 should not be interrupted by any interrupts. Therefore, users need to disable all the interrupts before these steps, and enable interrupts once done.

14.6 NMI Interrupt Masking

Some software process of ESP32-S3 should not be interrupted. For example, the configuration of World Controller should not be interrupted by any interrupts, including the NMI interrupts.

Normally, we can configure some CPU registers to mask different kinds of interrupts, but NMI interrupt is not one of them. To mask an NMI interrupt, you need to configure the interrupt sources, which is more complicated. For details, see Chapter 8 *Interrupt Matrix (INTERRUPT)*.

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World Controller has implemented some hardware mechanism to simplify the process to mask NMI interrupts for:

- **All** applications:
  - Configure WCL_CORE_*m*_NMI_MASK:
    * 1: Enable
    * 0: Disable
- **Some** applications:
  1. Configures WCL_CORE_*m*_NMI_MASK_TRIGGER_ADDR to the address at which the NMI interrupt masking ends, meaning the CPU stops masking NMI interrupts after this address.
  2. Write any value to WCL_CORE_*m*_NMI_MASK_DISABLE, indicating the completion of TRIGGER_ADDR configuration.
  3. Write any value to WCL_CORE_*m*_NMI_MASK_ENABLE to start masking NMI interrupts till the address configured in WCL_CORE_*m*_NMI_MASK_TRIGGER_ADDR.

Note:

- Only one of the above two methods should be used at the same time.
- The configuration to mask NMI interrupts is effective all the time until trigger address executes. Therefore, you need to configure the world controller to mask NMI interrupts again once trigger address executes.

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14.7 Register Summary

The addresses in this section are relative to the World Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Note that, the table below only lists the registers for CPU0. CPU1 shares exactly the same set of registers. Adding 0x0400 to the offset of the equivalent of CPU0 register gives you address for CPU1 registers.

For example, the offset for CPU0 register WCL_CORE_0_ENTRY_CHECK_REG is 0x007C, the offset for CPU1 equivalent WCL_CORE_1_ENTRY_CHECK_REG should be 0x007C + 0x0400, which is 0x047C.

Name	Description	Address	Access
Non-secure World to Secure World Configuration Registers			
WCL_CORE_0_ENTRY_*n*_ADDR_REG (*n*: 1-13)	CPU0 Entry *n* Address Configuration Register	0x0000	R/W
WCL_CORE_0_ENTRY_CHECK_REG	CPU0 Entry Check Enable Register	0x007C	R/W
WCL_CORE_0_MESSAGE_ADDR_REG	CPU0 Clear Writer_buffer Configuration Register - Configures Address	0x0100	R/W
WCL_CORE_0_MESSAGE_MAX_REG	CPU0 Clear Writer_buffer Configuration Register - Configures sequence	0x0104	R/W
WCL_CORE_0_MESSAGE_PHASE_REG	CPU0 Clear Writer_buffer Configuration Register - Checks Status	0x0108	RO
Status Table Registers			
WCL_CORE_0_STATUSTABLE*n*_REG(*n*: 1-13)	CPU0 World Switch Status Register for Entry *n*	0x0080	R/W
WCL_CORE_0_STATUSTABLE_CURRENT_REG	CPU0 Status Register of Statustable Current Field	0x00FC	R/W
Secure World to Non-secure World Configuration Registers			
WCL_CORE_0_World_TRIGGER_ADDR_REG	CPU0 Trigger Address Configuration Register	0x0140	RW
WCL_CORE_0_World_PREPARE_REG	CPU0 World Configuration Register - Configures Entry Address	0x0144	R/W
WCL_CORE_0_World_UPDATE_REG	CPU0 World Configuration Register - Confirms Configuration Done	0x0148	WO
WCL_CORE_0_World_Cancel_REG	CPU0 World Configuration Register - Cancels Configuration	0x014C	WO
WCL_CORE_0_World_IRam0_REG	CPU0 IRAM0 World Status Register	0x0150	R/W
WCL_CORE_0_World_DRam0_PIF_REG	CPU0 Dram0 and PIF World Status Register	0x0154	R/W
WCL_CORE_0_World_Phase_REG	CPU0 World Status Register	0x0158	RO
NMI Mask Configuration Registers			
WCL_CORE_0_NMI_MASK_ENABLE_REG	CPU0 NMI Mask Enable Register	0x0180	WO
WCL_CORE_0_NMI_MASK_TRIGGER_ADDR_REG	CPU0 NMI Mask Trigger Address Register	0x0184	R/W
WCL_CORE_0_NMI_MASK_DISABLE_REG	CPU0 NMI Mask Disable Register	0x0188	WO
WCL_CORE_0_NMI_MASK_CANCLE_REG	CPU0 NMI Mask Cancel Register	0x018C	WO
WCL_CORE_0_NMI_MASK_REG	CPU0 NMI Mask Register	0x0190	R/W
WCL_CORE_0_NMI_MASK_PHASE_REG	CPU0 NMI Mask Status Register	0x0194	RO

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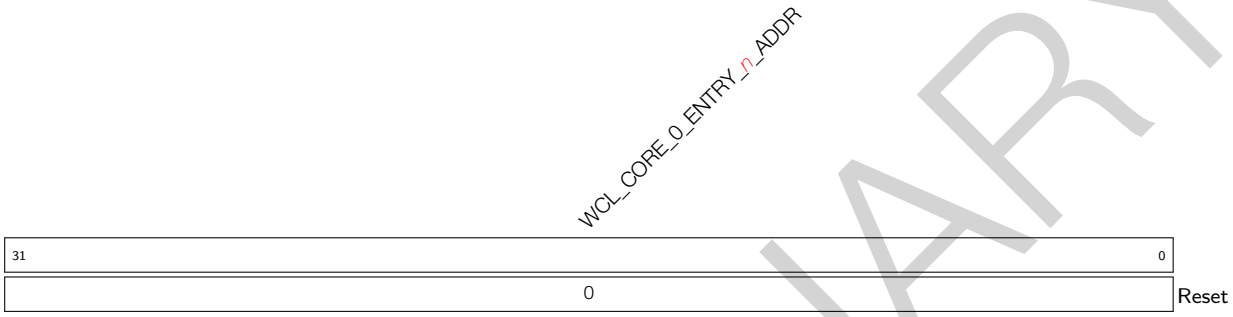
14.8 Registers

The addresses in this section are relative to the World Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Note that, the section below only lists the registers for CPU0. CPU1 shares exactly the same set of registers. Adding 0x0400 to the offset of the equivalent of CPU0 register gives you address for CPU1 registers.

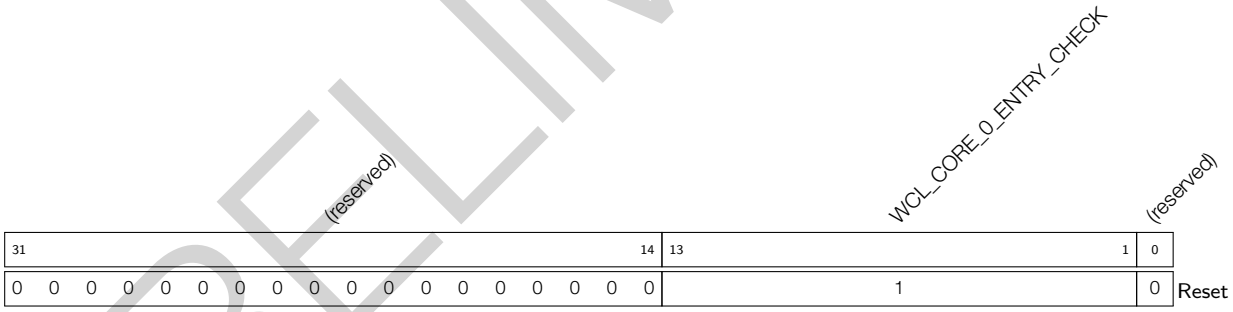
For example, the offset for CPU0 register WCL_CORE_0_ENTRY_CHECK_REG is 0x007C, the offset for CPU1 equivalent WCL_CORE_1_ENTRY_CHECK_REG should be 0x007C + 0x0400, which is 0x047C.

Register 14.1. WCL_CORE_0_ENTRY_*n*_ADDR_REG (*n*: 1-13) (0x0000+4n*)**



WCL_CORE_0_ENTRY_*n*_ADDR Configures the CPU0 Entry *n* address from Non-secure World to Secure World. (R/W)

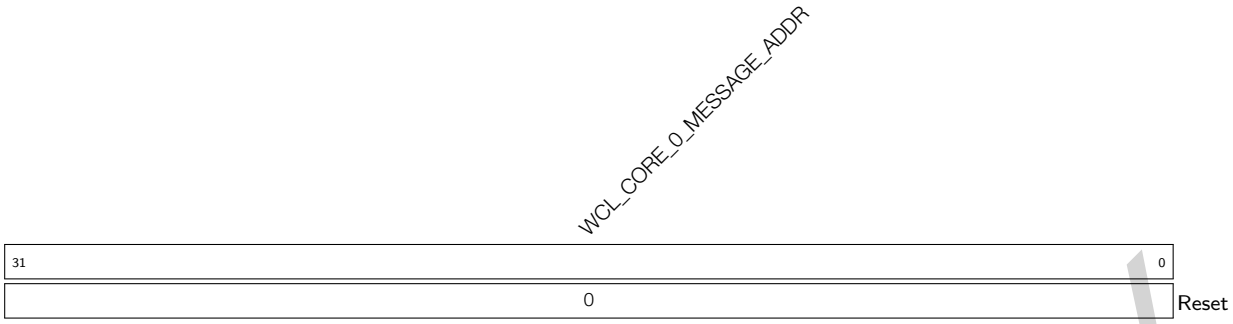
Register 14.2. WCL_CORE_0_ENTRY_CHECK_REG (0x007C)



WCL_CORE_0_ENTRY_CHECK Set this bit to enable CPU0 switching from Non-secure World to Secure world upon the monitored address. (R/W)

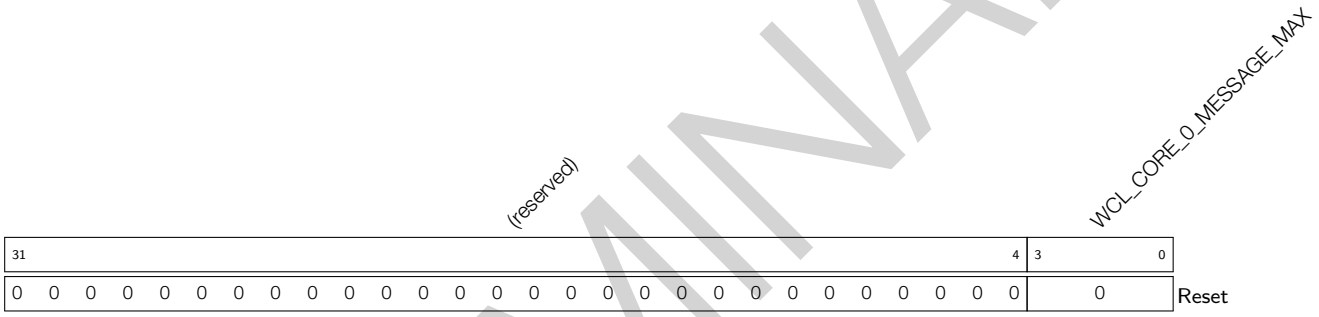
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Register 14.3. WCL_CORE_0_MESSAGE_ADDR_REG (0x0100)



WCL_CORE_0_MESSAGE_ADDR Configures the address to write agreed sequence to clear write_buffer for CPU0. (R/W)

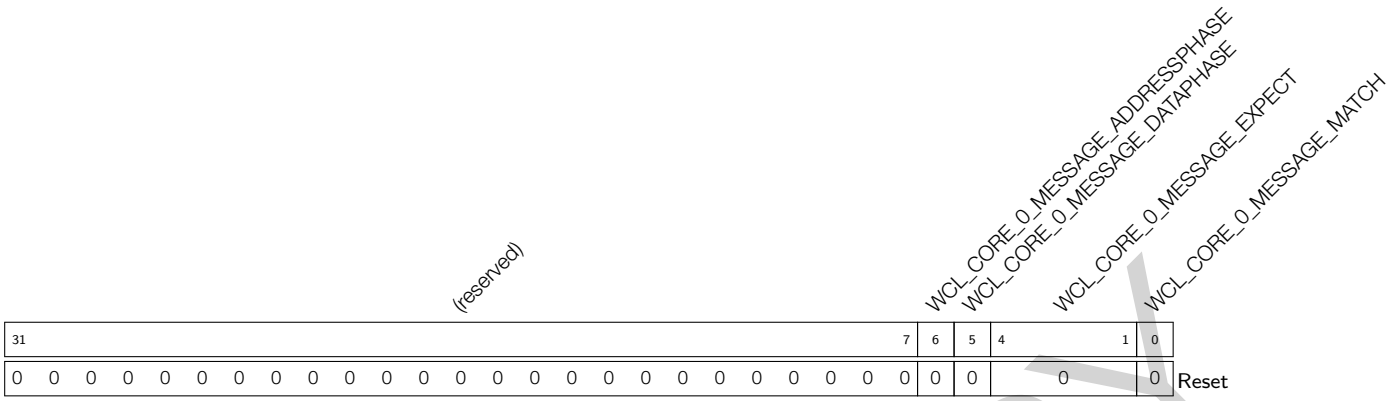
Register 14.4. WCL_CORE_0_MESSAGE_MAX_REG (0x0104)



WCL_CORE_0_MESSAGE_MAX Configures the agreed sequence to write to clear write_buffer for CPU0. It's advised to set this field to no less than 3. (R/W)

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Register 14.5. WCL_CORE_0_MESSAGE_PHASE_REG (0x0108)



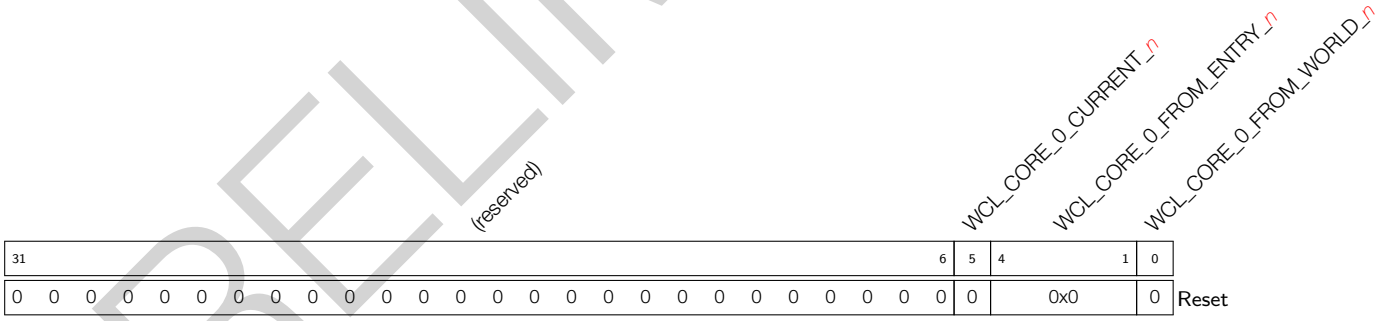
WCL_CORE_0_MESSAGE_MATCH Indicates if CPU0's world switch is successful. This field is only used for debugging. (RO)

WCL_CORE_0_MESSAGE_EXPECT Indicates the number to be written next for CPU0. This field is only used for debugging. (RO)

WCL_CORE_0_MESSAGE_DATAPHASE When 1, indicates CPU0 is checking if the agreed sequence is written to clear write_buffer. This field is only used for debugging. (RO)

WCL_CORE_0_MESSAGE_ADDRESSPHASE When 1, indicates CPU0 is checking if any sequence is written to the agreed address to clear write_buffer. This field is only used for debugging. (RO)

Register 14.6. WCL_CORE_0_STATUSTABLE*n*_REG (*n*: 1-13) (0x0080+4n*)**



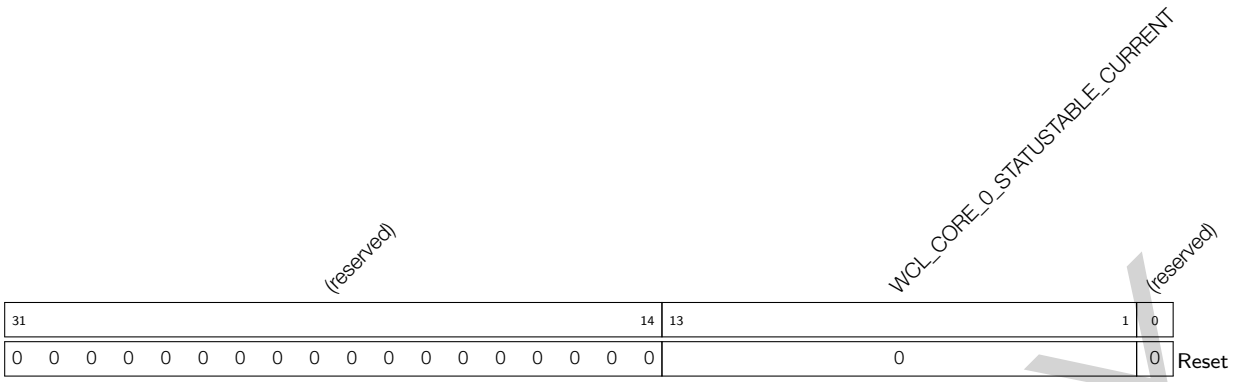
WCL_CORE_0_FROM_WORLD_*n* Stores the world info for CPU0 before entering entry *n*. (R/W)

WCL_CORE_0_FROM_ENTRY_*n* Stores the previous entry info for CPU0 before entering entry *n*. (R/W)

WCL_CORE_0_CURRENT_*n* Indicates if the interrupt is at entry *n* for CPU0. (R/W)

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Register 14.7. WCL_CORE_0_STATUSTABLE_CURRENT_REG (0x00FC)



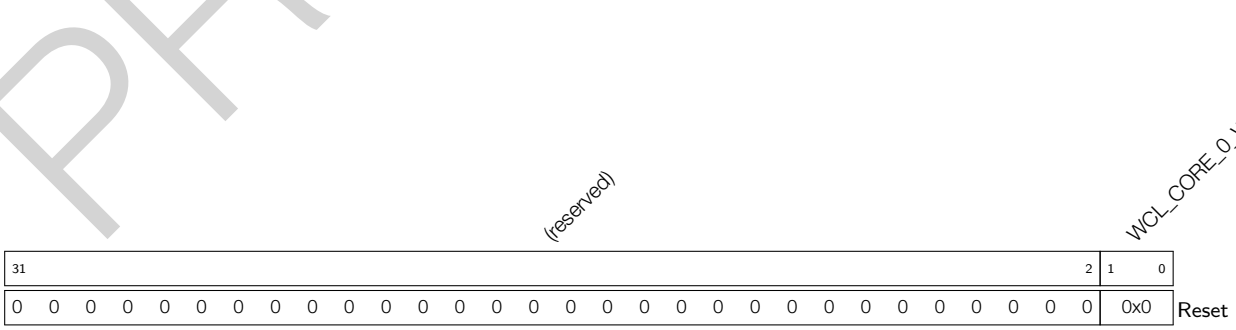
WCL_CORE_0_STATUSTABLE_CURRENT Indicates the entry where the interrupt is currently at for CPU0. (R/W)

Register 14.8. WCL_CORE_0_World_TRIGGER_ADDR_REG (0x0140)



WCL_CORE_0_WORLD_TRIGGER_ADDR Configures the entry address at which CPU0 switches from Secure World to Non-secure World. (RW)

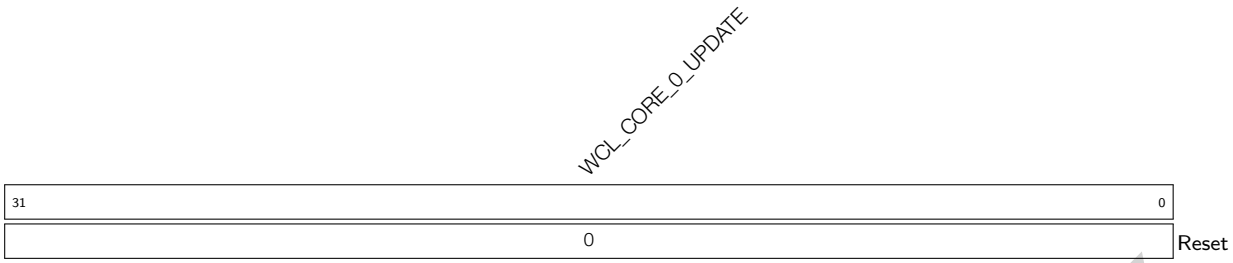
Register 14.9. WCL_CORE_0_World_PREPARE_REG (0x0144)



WCL_CORE_0_WORLD_PREPARE Write 0x2 to this field to ready CPU0 for world switch from Secure World to Non-secure World. This field is only used for debugging.(R/W)

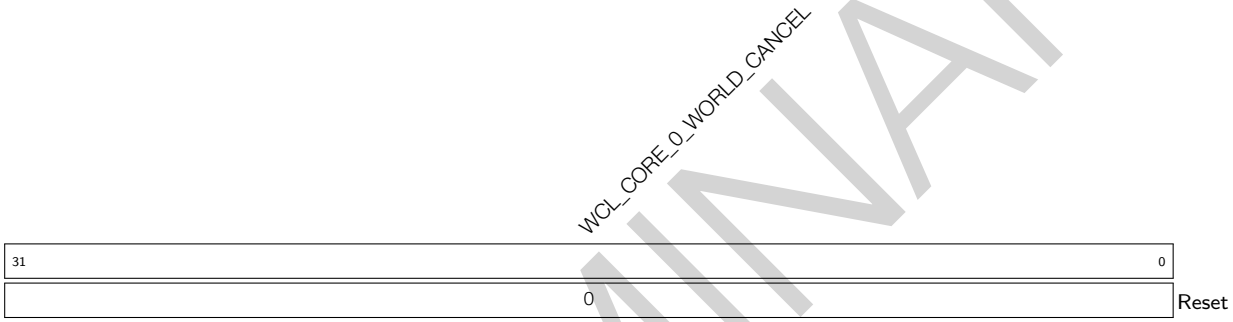
PRELIMINARY

Register 14.10. WCL_CORE_0_World_UPDATE_REG (0x0148)



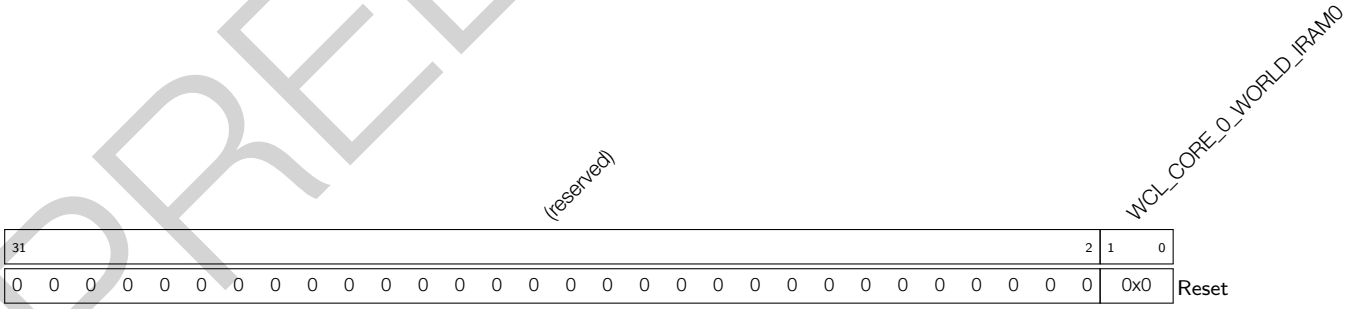
WCL_CORE_0_UPDATE Write any value to this field to indicate the completion of CPU0 configuration for switching from Secure World to Non-Secure World. (WO)

Register 14.11. WCL_CORE_0_World_Cancel_REG (0x014C)



WCL_CORE_0_WORLD_CANCEL Write any value to this filed to cancel the CPU0 configuration for switching from Secure World to Non-Secure World. (WO)

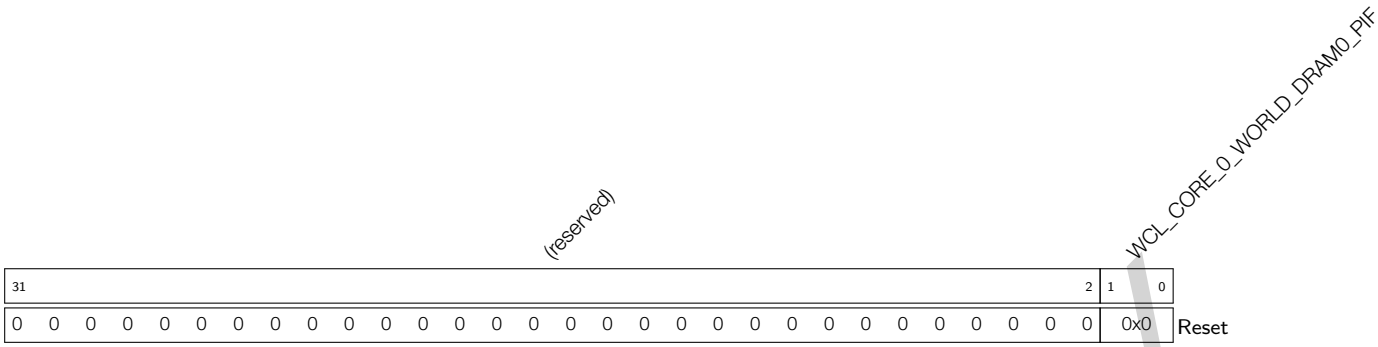
Register 14.12. WCL_CORE_0_World_IRam0_REG (0x0150)



WCL_CORE_0_WORLD_IRAM0 Stores the world info of CPU0's instruction bus. This field is only used for debugging. (R/W)

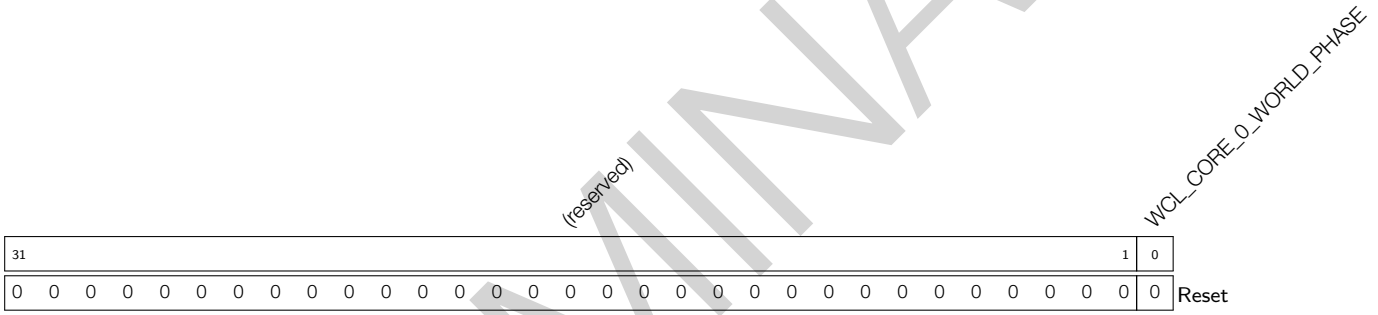
PRELIMINARY

Register 14.13. WCL_CORE_0_World_DRam0_PIF_REG (0x0154)



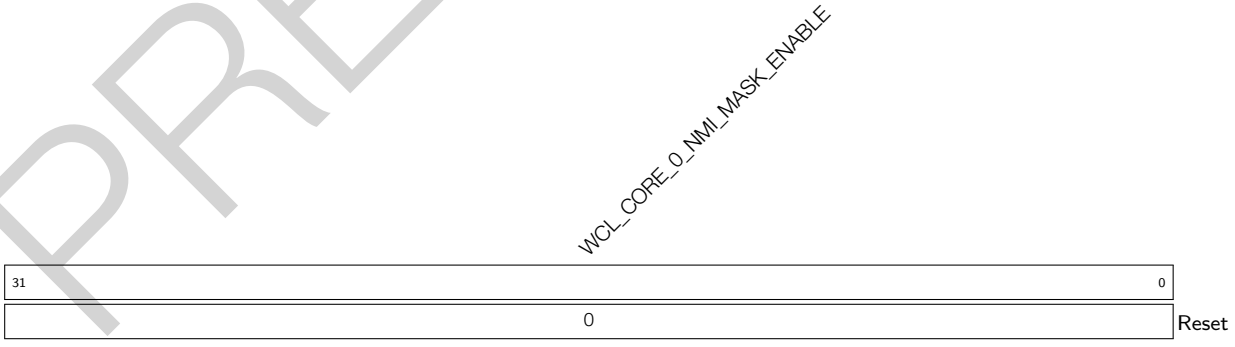
WCL_CORE_0_WORLD_DRAM0_PIF Stores the world info of CPU0's data bus and peripheral bus. This field is only used for debugging. (R/W)

Register 14.14. WCL_CORE_0_World_Phase_REG (0x0158)



WCL_CORE_0_WORLD_PHASE Indicates if the CPU0 is ready to switch from Non-secure World to Secure World. 1: ready; 2: not ready. (RO)

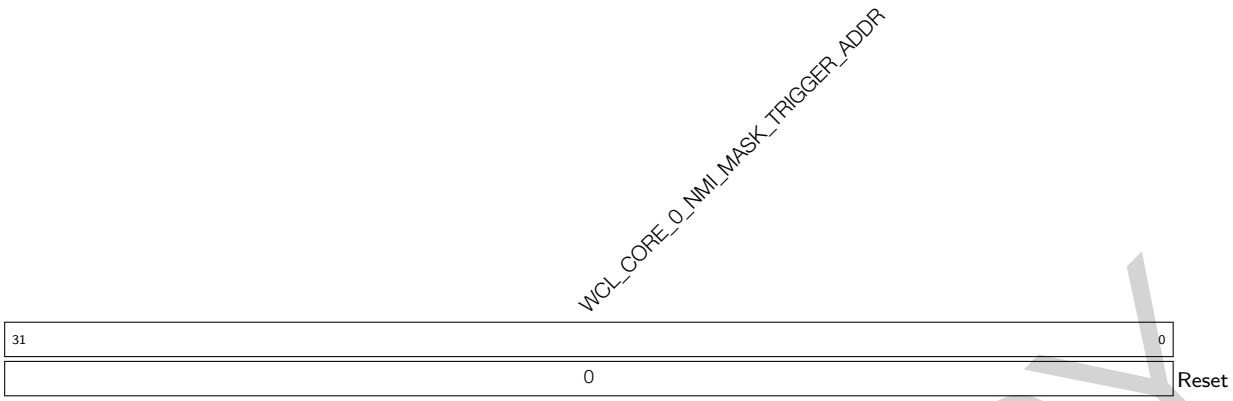
Register 14.15. WCL_CORE_0_NMI_MASK_ENABLE_REG (0x0180)



WCL_CORE_0_NMI_MASK_ENABLE Write any value to this field to start CPU0 masking any NMI interrupt. (WO)

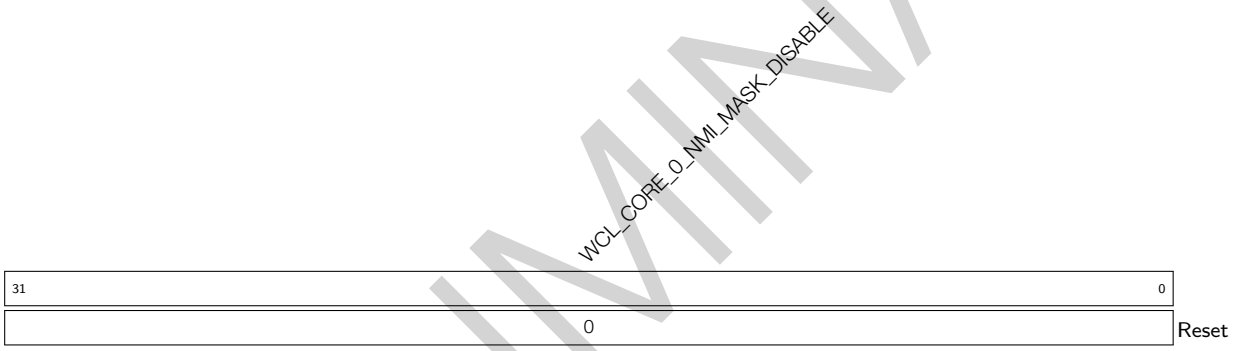
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Register 14.16. WCL_CORE_0_NMI_MASK_TRIGGER_ADDR_REG (0x0184)



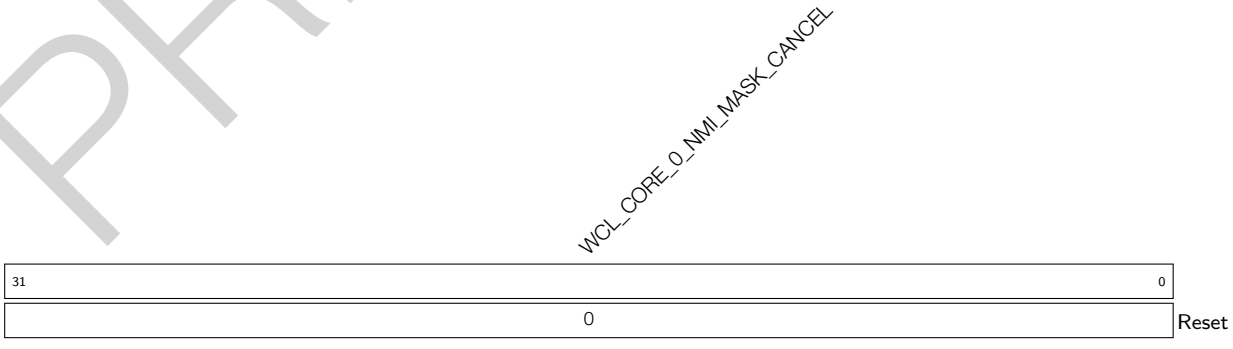
WCL_CORE_0_NMI_MASK_TRIGGER_ADDR Configures the address at which the NMI masking stops for CPU0. (R/W)

Register 14.17. WCL_CORE_0_NMI_MASK_DISABLE_REG (0x0188)



WCL_CORE_0_NMI_MASK_DISABLE Write any value to this field so CPU0 checks NMI masking. (WO)

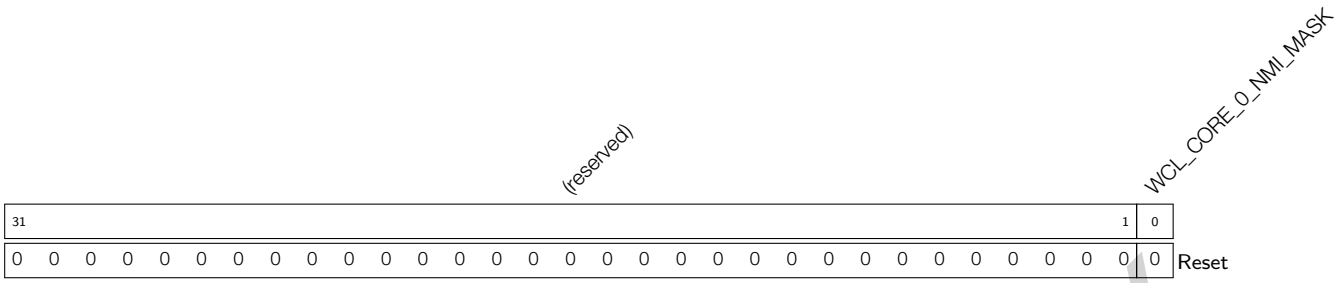
Register 14.18. WCL_CORE_0_NMI_MASK_CANCLE_REG (0x018C)



WCL_CORE_0_NMI_MASK_CANCEL Write any value to this field to cancel CPU0's NMI masking. (WO)

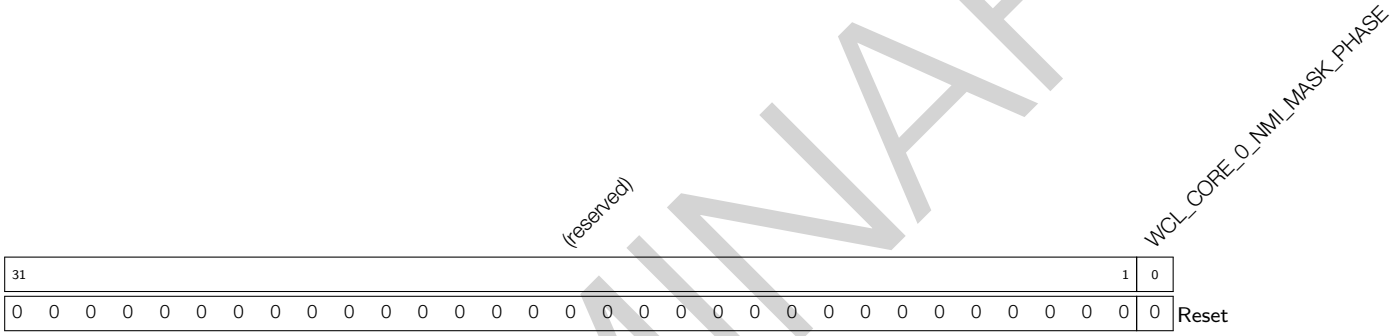
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Register 14.19. WCL_CORE_0_NMI_MASK_REG (0x0190)



WCL_CORE_0_NMI_MASK Set this bit to mask all the NMI interrupts in CPU0. (R/W)

Register 14.20. WCL_CORE_0_NMI_MASK_PHASE_REG (0x0194)



WCL_CORE_0_NMI_MASK_PHASE Indicates if the NMI interrupt is being masked in CPU0. 1: masked; 0: not masked. (RO)

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15 System Registers

15.1 Overview

The ESP32-S3 integrates a large number of peripherals, and enables the control of individual peripherals to achieve optimal characteristics in performance-vs-power-consumption scenarios. Specifically, ESP32-S3 has a various of system configuration registers that can be used for the chip's clock management (clock gating), power management, and the configuration of peripherals and core-system modules. This chapter lists all these system registers and their functions.

15.2 Features

ESP32-S3 system registers can be used to control the following peripheral blocks and core modules:

- System and memory
- Clock
- Software Interrupt
- Low-power management
- Peripheral clock gating and reset
- CPU Control

15.3 Function Description

15.3.1 System and Memory Registers

15.3.1.1 Internal Memory

The following registers can be used to control ESP32-S3's internal memory:

- In register APB_CTRL_CLKGATE_FORCE_ON_REG:
  - Setting different bits of the APB_CTRL_ROM_CLKGATE_FORCE_ON field forces on the clock gates of different blocks of Internal ROM 0 and Internal ROM 1.
  - Setting different bits of the APB_CTRL_SRAM_CLKGATE_FORCE_ON field forces on the clock gates of different blocks of Internal SRAM.
  - This means when the respective bits of this register are set to 1, the clock gate of the corresponding ROM or SRAM blocks will always be on. Otherwise, the clock gate will turn on automatically when the corresponding ROM or SRAM blocks are accessed and turn off automatically when the corresponding ROM or SRAM blocks are not accessed. Therefore, it's recommended to configure these bits to 0 to lower power consumption.
- In register APB_CTRL_MEM_POWER_DOWN_REG:
  - Setting different bits of the APB_CTRL_ROM_POWER_DOWN field sends different blocks of Internal ROM 0 and Internal ROM 1 into retention state.

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  - Setting different bits of the APB_CTRL_SRAM_POWER_DOWN field sends different blocks of Internal SRAM into retention state.
  - The “Retention” state is a low-power state of a memory block. In this state, the memory block still holds all the data stored but cannot be accessed, thus reducing the power consumption. Therefore, you can send a certain block of memory into the retention state to reduce power consumption if you know you are not going to use such memory block for some time.

- In register APB_CTRL_MEM_POWER_UP_REG:
  - By default, all memory enters low-power state when the chip enters the Light-sleep mode.
  - Setting different bits of the APB_CTRL_ROM_POWER_UP field forces different blocks of Internal ROM 0 and Internal ROM 1 to work as normal (do not enter the retention state) when the chip enters Light-sleep.
  - Setting different bits of the APB_CTRL_SRAM_POWER_UP field forces different blocks of Internal SRAM to work as normal (do not enter the retention state) when the chip enters Light-sleep.

For detailed information about the controlling bits of different blocks, please see Table 15-1 below.

Table 15-1. Internal Memory Controlling Bit

Internal Memory	Lowest Address1	Highest Address1	Lowest Address2	Highest Address2	Controlling Bit
Internal ROM 0	0x4000_0000	0x4003_FFFF	-	-	Bit0
Internal ROM 1	0x4004_0000	0x4004_FFFF	-	-	Bit1
Internal ROM 2	0x4005_0000	0x4005_FFFF	0x3FF0_0000	0x3FF0_FFFF	Bit2
SRAM Block0	0x4037_0000	0x4037_3FFF	-	-	Bit0
SRAM Block1	0x4037_4000	0x4037_7FFF	-	-	Bit1
SRAM Block2	0x4037_8000	0x4037_FFFF	0x3FC8_8000	0x3FC8_FFFF	Bit2
SRAM Block3	0x4038_0000	0x4038_FFFF	0x3FC9_0000	0x3FC9_FFFF	Bit3
SRAM Block4	0x4039_8000	0x4039_FFFF	0x3FCA_0000	0x3FCA_FFFF	Bit4
SRAM Block5	0x403A_C000	0x403A_FFFF	0x3FCB_C000	0x3FCB_FFFF	Bit5
SRAM Block6	0x403B_0000	0x403B_FFFF	0x3FCC_0000	0x3FCC_FFFF	Bit6
SRAM Block7	0x403C_0000	0x403C_FFFF	0x3FCD_4000	0x3FCD_FFFF	Bit7
SRAM Block8	0x403D_0000	0x403D_BFFF	0x3FCE_8000	0x3FCE_FFFF	Bit8
SRAM Block9	-	-	0x3FCF_0000	0x3FCF_7FFF	Bit9
SRAM Block10	-	-	0x3FCF_8000	0x3FCF_FFFF	Bit10

For detailed information about the controlling bits of different blocks, please see Table 15-1 below.

15.3.1.2 External Memory

SYSTEM_EXTERNAL_DEVICE_ENCRYPT_DECRYPT_CONTROL_REG configures encryption and decryption options of the external memory. For details, please refer to Chapter 21 *External Memory Encryption and Decryption (XTS_AES)*.

15.3.1.3 RSA Memory

SYSTEM_RSA_PD_CTRL_REG controls the SRAM memory in the RSA accelerator.

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- Setting the SYSTEM_RSA_MEM_PD bit to send the RSA memory into retention state. This bit has the lowest priority, meaning it can be masked by the SYSTEM_RSA_MEM_FORCE_PU field. This bit is invalid when the *Digital Signature (DS)* occupies the RSA.
- Setting the SYSTEM_RSA_MEM_FORCE_PU bit to force the RSA memory to work as normal when the chip enters light sleep. This bit has the second highest priority, meaning it overrides the SYSTEM_RSA_MEM_PD field.
- Setting the SYSTEM_RSA_MEM_FORCE_PD bit to send the RSA memory into retention state. This bit has the highest priority, meaning it sends the RSA memory into retention state regardless of the SYSTEM_RSA_MEM_FORCE_PU field.

15.3.2 Clock Registers

The following registers are used to set clock sources and frequency. For more information, please refer to Chapter 6 *Reset and Clock*.

- SYSTEM_CPU_PER_CONF_REG
- SYSTEM_SYSCLK_CONF_REG
- SYSTEM_BT_LPCK_DIV_FRAC_REG

15.3.3 Interrupt Signal Registers

The following registers are used for generating the interrupt signals, which then can be routed to the CPU peripheral interrupts via the interrupt matrix. To be more specific, writing 1 to any of the following registers generates an interrupt signal. Therefore, these registers can be used by software to control interrupts. For more information, please refer to Chapter 8 *Interrupt Matrix (INTERRUPT)*.

- SYSTEM_CPU_INTR_FROM_CPU_0_REG
- SYSTEM_CPU_INTR_FROM_CPU_1_REG
- SYSTEM_CPU_INTR_FROM_CPU_2_REG
- SYSTEM_CPU_INTR_FROM_CPU_3_REG

15.3.4 Low-power Management Registers

The following registers are used for low-power management. For more information, please refer to Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]*.

- SYSTEM_RTC_FASTMEM_CONFIG_REG: configures the RTC CRC check.
- SYSTEM_RTC_FASTMEM_CRC_REG: configures the CRC check value.

15.3.5 Peripheral Clock Gating and Reset Registers

The following registers are used for controlling the clock gating and reset of different peripherals. Details can be seen in Table 15-2.

- SYSTEM_CACHE_CONTROL_REG
- SYSTEM_EDMA_CTRL_REG
- SYSTEM_PERIP_CLK_EN0_REG

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- SYSTEM_PERIP_RST_EN0_REG
- SYSTEM_PERIP_CLK_EN1_REG
- SYSTEM_PERIP_RST_EN1_REG

Table 15-2. Peripheral Clock Gating and Reset Bits

Peripheral	Clock Enabling Bit[1]	Reset Controlling Bit[2][3]
EDMA Ctrl	**SYSTEM_EDMA_CTRL_REG**	
EDMA	SYSTEM_EDMA_CLK_ON	SYSTEM_EDMA_RESET
CACHE Ctrl	**SYSTEM_CACHE_CONTROL_REG**	
DCACHE	SYSTEM_DCACHE_CLK_ON	SYSTEM_DCACHE_RESET
ICACHE	SYSTEM_ICACHE_CLK_ON	SYSTEM_ICACHE_RESET
Peripheral	**SYSTEM_PERIP_CLK_EN0_REG**	**SYSTEM_PERIP_RST_EN0_REG**
Timer Group0	SYSTEM_TIMERGROUP_CLK_EN	SYSTEM_TIMERGROUP_RST
Timer Group1	SYSTEM_TIMERGROUP1_CLK_EN	SYSTEM_TIMERGROUP1_RST
System Timer	SYSTEM_SYSTIMER_CLK_EN	SYSTEM_SYSTIMER_RST
UART0	SYSTEM_UART_CLK_EN	SYSTEM_UART_RST
UART1	SYSTEM_UART1_CLK_EN	SYSTEM_UART1_RST
UART MEM	SYSTEM_UART_MEM_CLK_EN [4]	SYSTEM_UART_MEM_RST
SPI0 SPI1	SYSTEM_SPI01_CLK_EN	SYSTEM_SPI01_RST
SPI2	SYSTEM_SPI2_CLK_EN	SYSTEM_SPI2_RST
SPI3	SYSTEM_SPI3_CLK_EN	SYSTEM_SPI3_RST
I2C0	SYSTEM_I2C_EXT0_CLK_EN	SYSTEM_I2C_EXT0_RST
I2C1	SYSTEM_I2C_EXT1_CLK_EN	SYSTEM_I2C_EXT1_RST
I2S0	SYSTEM_I2S0_CLK_EN	SYSTEM_I2S0_RST
I2S1	SYSTEM_I2S1_CLK_EN	SYSTEM_I2S1_RST
TWAI Controller	SYSTEM_CAN_CLK_EN	SYSTEM_CAN_RST
UHCI0	SYSTEM_UHCI0_CLK_EN	SYSTEM_UHCI0_RST
USB	SYSTEM_USB_CLK_EN	SYSTEM_USB_RST
RMT	SYSTEM_RMT_CLK_EN	SYSTEM_RMT_RST
PCNT	SYSTEM_PCNT_CLK_EN	SYSTEM_PCNT_RST
PWM0	SYSTEM_PWM0_CLK_EN	SYSTEM_PWM0_RST
PWM1	SYSTEM_PWM1_CLK_EN	SYSTEM_PWM1_RST
LED_PWM Controller	SYSTEM_LEDC_CLK_EN	SYSTEM_LEDC_RST
ADC Controller	SYSTEM_ADC2_ARB_CLK_EN	SYSTEM_ADC2_ARB_RST
Accelerators	**SYSTEM_PERIP_CLK_EN1_REG**	**SYSTEM_PERIP_RST_EN1_REG**
USB_DEVICE	SYSTEM_USB_DEVICE_CLK_EN	SYSTEM_USB_DEVICE_RST
UART2	SYSTEM_UART2_CLK_EN	SYSTEM_UART2_RST
LCD_CAM	SYSTEM_LCD_CAM_CLK_EN	SYSTEM_LCD_CAM_RST
SDIO_HOST	SYSTEM_SDIO_HOST_CLK_EN	SYSTEM_SDIO_HOST_RST
DMA	SYSTEM_DMA_CLK_EN	SYSTEM_DMA_RST [5]
HMAC	SYSTEM_CRYPTO_HMAC_CLK_EN	SYSTEM_CRYPTO_HMAC_RST [6]
Digital Signature	SYSTEM_CRYPTO_DS_CLK_EN	SYSTEM_CRYPTO_DS_RST [7]
RSA Accelerator	SYSTEM_CRYPTO_RSA_CLK_EN	SYSTEM_CRYPTO_RSA_RST
SHA Accelerator	SYSTEM_CRYPTO_SHA_CLK_EN	SYSTEM_CRYPTO_SHA_RST

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AES Accelerator	SYSTEM_CRYPTO_AES_CLK_EN	SYSTEM_CRYPTO_AES_RST
peri backup	SYSTEM_PERI_BACKUP_CLK_EN	SYSTEM_PERI_BACKUP_RST

Note:

1. Setting the clock enable register to 1 enables the clock, and to 0 disables the clock;
2. Setting the reset enabling register to 1 resets a peripheral, and to 0 disables the reset.
3. Reset registers cannot be cleared by hardware. Therefore, SW reset clear is required after setting the reset registers.
4. UART memory is shared by all UART peripherals, meaning having any active UART peripherals will prevent the UART memory from entering the clock-gated state.
5. When DMA is required for peripheral communications, for example, UCHI0, SPI, I2S, LCD_CAM, AES, SHA and ADC, DMA clock should also be enabled.
6. Resetting this bit also resets the SHA accelerator.
7. Resetting this bit also resets the AES, SHA, and RSA accelerators.

15.3.6 CPU Control Registers

These registers control CPU0 and CPU1 of ESP32-S3. Note that, by default, only CPU0 is started when the SoC powers up. During this time, the clock of CPU1 is disabled. Therefore, users need to enable CPU1 clock manually to use both CPU0 and CPU1.

- SYSTEM_CORE_1_CONTROL_0_REG
  - Setting the SYSTEM_CONTROL_CORE_1_RESETING bit resets CPU1.
  - SYSTEM_CONTROL_CORE_1_CLKGATE_EN controls the CPU1 clock.
  - Setting the SYSTEM_CONTROL_CORE_1_RUNSTALL bit stalls CPU1. When this bit is set, CPU1 will finish the on-going task and stalls.
- Register SYSTEM_CORE_1_CONTROL_1_REG is used to facilitate the communication between CPU0 and CPU1. To be more specific, one CPU can write this register, using the agreed-on formats, which will then be read by the other CPU, thus achieving communication between these two CPUs. Note that the value in this register will not affect any hardware configuration, which allows CPU communication solely controlled by software.

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15.4 Register Summary

In this section, the addresses of all the registers starting with SYSTEM are relative to the base address of system registers provided in Table 3-3 in Chapter 3 *System and Memory*; and those starting with APB are relative to the base address of APB control also provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
SYSTEM_CORE_1_CONTROL_0_REG	Core1 control register 0	0x0000	R/W
SYSTEM_CORE_1_CONTROL_1_REG	Core1 control register 1	0x0004	R/W
SYSTEM_CPU_PER_CONF_REG	CPU peripheral clock configuration register	0x0010	R/W
SYSTEM_PERIP_CLK_EN0_REG	System peripheral clock enable register 0	0x0018	R/W
SYSTEM_PERIP_CLK_EN1_REG	System peripheral clock enable register 1	0x001C	R/W
SYSTEM_PERIP_RST_EN0_REG	System peripheral reset register 0	0x0020	R/W
SYSTEM_PERIP_RST_EN1_REG	System peripheral reset register 1	0x0024	R/W
SYSTEM_BT_LPCK_DIV_FRAC_REG	Low-power clock configuration register 1	0x002C	R/W
SYSTEM_CPU_INTR_FROM_CPU_0_REG	Software interrupt source register 0	0x0030	R/W
SYSTEM_CPU_INTR_FROM_CPU_1_REG	Software interrupt source register 1	0x0034	R/W
SYSTEM_CPU_INTR_FROM_CPU_2_REG	Software interrupt source register 2	0x0038	R/W
SYSTEM_CPU_INTR_FROM_CPU_3_REG	Software interrupt source register 3	0x003C	R/W
SYSTEM_RSA_PD_CTRL_REG	RSA memory power control register	0x0040	R/W
SYSTEM_EDMA_CTRL_REG	EDMA control register	0x0044	R/W
SYSTEM_CACHE_CONTROL_REG	Cache control register	0x0048	R/W
SYSTEM_EXTERNAL_DEVICE_ENCRYPT_DECRYPT_CONTROL_REG	External memory encryption and decryption control register	0x004C	R/W
SYSTEM_RTC_FASTMEM_CONFIG_REG	Fast memory CRC configuration register	0x0050	varies
SYSTEM_RTC_FASTMEM_CRC_REG	Fast memory CRC result register	0x0054	RO
SYSTEM_CLOCK_GATE_REG	System clock control register	0x005C	R/W
SYSTEM_SYSCLK_CONF_REG	System clock configuration register	0x0060	varies
SYSTEM_DATE_REG	Version register	0x0FFC	R/W

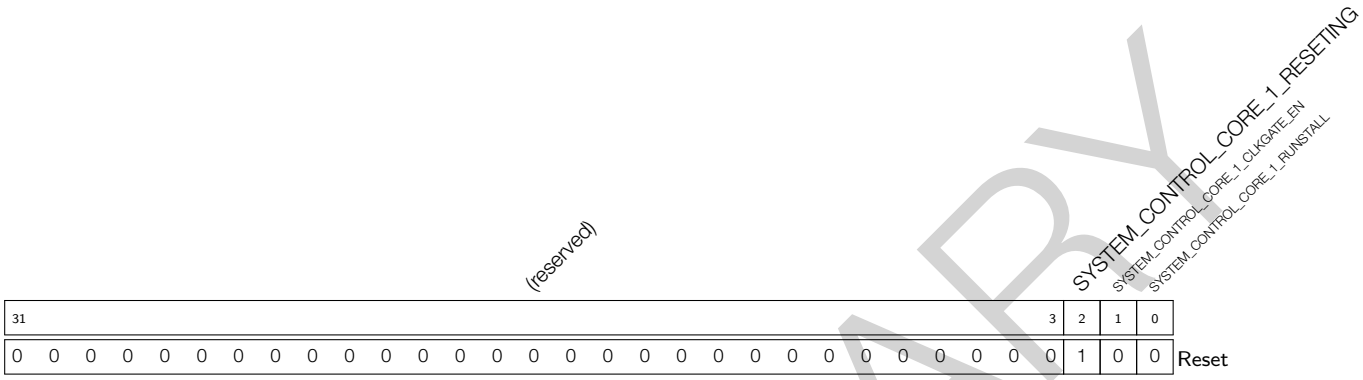
Name	Description	Address	Access
APB_CTRL_CLKGATE_FORCE_ON_REG	Internal memory clock gate enable register	0x00A8	R/W
APB_CTRL_MEM_POWER_DOWN_REG	Internal memory control register	0x00AC	R/W
APB_CTRL_MEM_POWER_UP_REG	Internal memory control register	0x00B0	R/W

PRELIMINARY

15.5 Registers

In this section, the addresses of all the registers starting with SYSTEM are relative to the base address of system registers provided in Table 3-3 in Chapter 3 *System and Memory*; and those starting with APB are relative to the base address of APB control also provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 15.1. SYSTEM_CORE_1_CONTROL_0_REG (0x0000)



SYSTEM_CONTROL_CORE_1_RUNSTALL Set this bit to stall Core 1. (R/W)

SYSTEM_CONTROL_CORE_1_CLKGATE_EN Set this bit to enable Core 1 clock. (R/W)

SYSTEM_CONTROL_CORE_1_RESETING Set this bit to reset Core 1. (R/W)

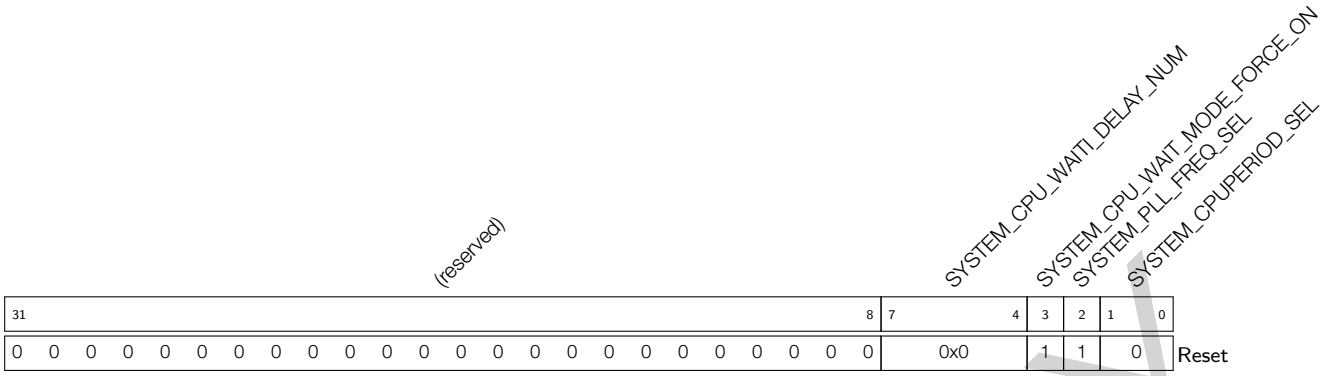
Register 15.2. SYSTEM_CORE_1_CONTROL_1_REG (0x0004)



SYSTEM_CONTROL_CORE_1_MESSAGE This field is used to facilitate the communication between CPU0 and CPU1. (R/W)

PRELIMINARY

Register 15.3. SYSTEM_CPU_PER_CONF_REG (0x0010)



SYSTEM_CPUPERIOD_SEL Set this field to select the CPU clock frequency. (R/W)

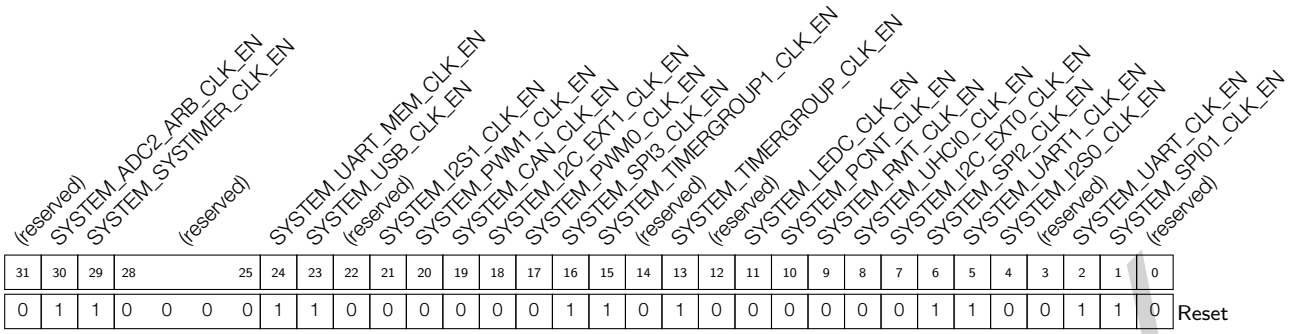
SYSTEM_PLL_FREQ_SEL Set this bit to select the PLL clock frequency. (R/W)

SYSTEM_CPU_WAIT_MODE_FORCE_ON Set this bit to force on the clock gate of CPU wait mode. Usually, after executing the WAITI instruction, CPU enters the wait mode, during which the clock gate of CPU is turned off until any interrupts occur. In this way, power consumption is reduced. However, if this bit is set, the clock gate of CPU is always on and will not be turned off by the WAITI instruction. (R/W)

SYSTEM_CPU_WAITI_DELAY_NUM Sets the number of delay cycles to turn off the CPU clock gate after the CPU enters the wait mode because of a WAITI instruction. (R/W)

PRELIMINARY

Register 15.4. SYSTEM_PERIP_CLK_EN0_REG (0x0018)



SYSTEM_SPI01_CLK_EN Set this bit to enable SPI01 clock. (R/W)

SYSTEM_UART_CLK_EN Set this bit to enable UART clock. (R/W)

SYSTEM_I2S0_CLK_EN Set this bit to enable I2S0 clock. (R/W)

SYSTEM_UART1_CLK_EN Set this bit to enable UART1 clock. (R/W)

SYSTEM_SPI2_CLK_EN Set this bit to enable SPI2 clock. (R/W)

SYSTEM_I2C_EXT0_CLK_EN Set this bit to enable I2C_EXT0 clock. (R/W)

SYSTEM_UHCI0_CLK_EN Set this bit to enable UHCI0 clock. (R/W)

SYSTEM_RMT_CLK_EN Set this bit to enable RMT clock. (R/W)

SYSTEM_PCNT_CLK_EN Set this bit to enable PCNT clock. (R/W)

SYSTEM_LEDC_CLK_EN Set this bit to enable LEDC clock. (R/W)

SYSTEM_TIMERGROUP_CLK_EN Set this bit to enable TIMERGROUP0 clock. (R/W)

SYSTEM_TIMERGROUP1_CLK_EN Set this bit to enable TIMERGROUP1 clock. (R/W)

SYSTEM_SPI3_CLK_EN Set this bit to enable SPI3 clock. (R/W)

SYSTEM_PWM0_CLK_EN Set this bit to enable PWM0 clock. (R/W)

SYSTEM_I2C_EXT1_CLK_EN Set this bit to enable I2C_EXT1 clock. (R/W)

SYSTEM_CAN_CLK_EN Set this bit to enable CAN clock. (R/W)

SYSTEM_PWM1_CLK_EN Set this bit to enable PWM1 clock. (R/W)

SYSTEM_I2S1_CLK_EN Set this bit to enable I2S1 clock. (R/W)

SYSTEM_USB_CLK_EN Set this bit to enable USB clock. (R/W)

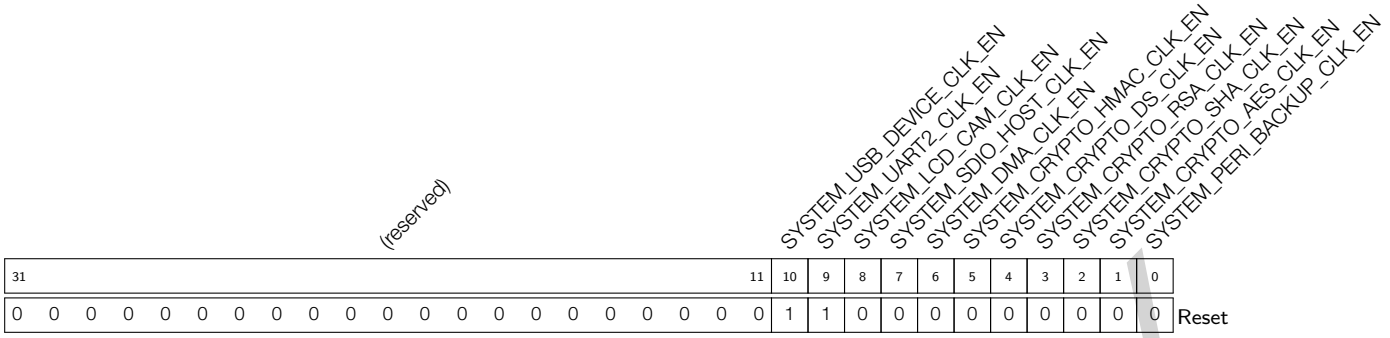
SYSTEM_UART_MEM_CLK_EN Set this bit to enable UART_MEM clock. (R/W)

SYSTEM_SYSTIMER_CLK_EN Set this bit to enable SYSTEM TIMER clock. (R/W)

SYSTEM_ADC2_ARB_CLK_EN Set this bit to enable ADC2_ARB clock. (R/W)

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Register 15.5. SYSTEM_PERIP_CLK_EN1_REG (0x001C)



SYSTEM_PERI_BACKUP_CLK_EN Set this bit to enable peri backup clock. (R/W)

SYSTEM_CRYPTO_AES_CLK_EN Set this bit to enable AES clock. (R/W)

SYSTEM_CRYPTO_SHA_CLK_EN Set this bit to enable SHA clock. (R/W)

SYSTEM_CRYPTO_RSA_CLK_EN Set this bit to enable RSA clock. (R/W)

SYSTEM_CRYPTO_DS_CLK_EN Set this bit to enable DS clock. (R/W)

SYSTEM_CRYPTO_HMAC_CLK_EN Set this bit to enable HMAC clock. (R/W)

SYSTEM_DMA_CLK_EN Set this bit to enable DMA clock. (R/W)

SYSTEM_SDIO_HOST_CLK_EN Set this bit to enable SDIO_HOST clock. (R/W)

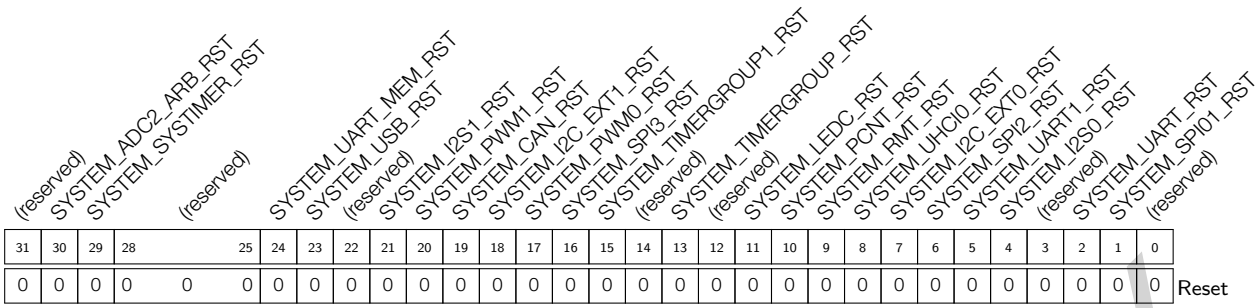
SYSTEM_LCD_CAM_CLK_EN Set this bit to enable LCD_CAM clock. (R/W)

SYSTEM_UART2_CLK_EN Set this bit to enable UART2 clock. (R/W)

SYSTEM_USB_DEVICE_CLK_EN Set this bit to enable USB_DEVICE clock. (R/W)

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Register 15.6. SYSTEM_PERIP_RST_EN0_REG (0x0020)



SYSTEM_SPI01_RST Set this bit to reset SPI01. (R/W)

SYSTEM_UART_RST Set this bit to reset UART. (R/W)

SYSTEM_I2S0_RST Set this bit to reset I2S0. (R/W)

SYSTEM_UART1_RST Set this bit to reset UART1. (R/W)

SYSTEM_SPI2_RST Set this bit to reset SPI2. (R/W)

SYSTEM_I2C_EXT0_RST Set this bit to reset I2C_EXT0. (R/W)

SYSTEM_UHCI0_RST Set this bit to reset UHCI0. (R/W)

SYSTEM_RMT_RST Set this bit to reset RMT. (R/W)

SYSTEM_PCNT_RST Set this bit to reset PCNT. (R/W)

SYSTEM_LEDC_RST Set this bit to reset LEDC. (R/W)

SYSTEM_TIMERGROUP_RST Set this bit to reset TIMERGROUP0. (R/W)

SYSTEM_TIMERGROUP1_RST Set this bit to reset TIMERGROUP1. (R/W)

SYSTEM_SPI3_RST Set this bit to reset SPI3. (R/W)

SYSTEM_PWM0_RST Set this bit to reset PWM0. (R/W)

SYSTEM_I2C_EXT1_RST Set this bit to reset I2C_EXT1. (R/W)

SYSTEM_CAN_RST Set this bit to reset CAN. (R/W)

SYSTEM_PWM1_RST Set this bit to reset PWM1. (R/W)

SYSTEM_I2S1_RST Set this bit to reset I2S1. (R/W)

SYSTEM_USB_RST Set this bit to reset USB. (R/W)

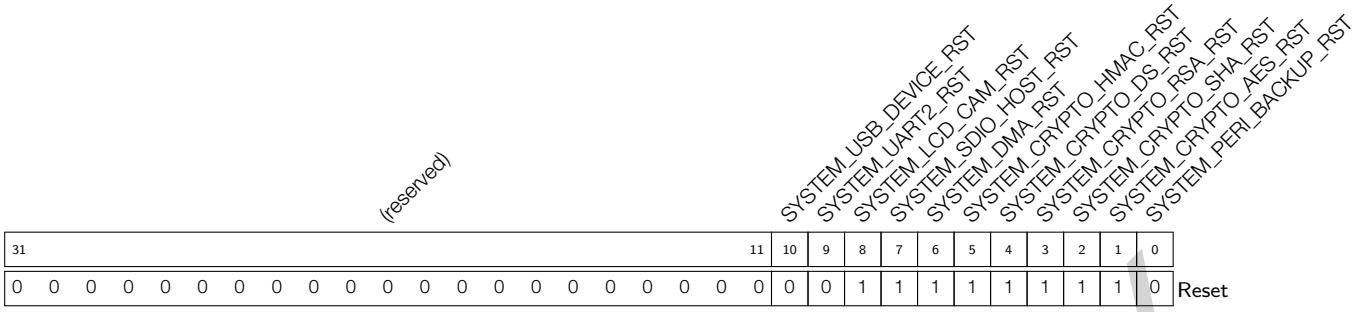
SYSTEM_UART_MEM_RST Set this bit to reset UART_MEM. (R/W)

SYSTEM_SYSTIMER_RST Set this bit to reset SYSTIMER. (R/W)

SYSTEM_ADC2_ARB_RST Set this bit to reset ADC2_ARB. (R/W)

PRELIMINARY

Register 15.7. SYSTEM_PERIP_RST_EN1_REG (0x0024)



SYSTEM_PERI_BACKUP_RST Set this bit to reset BACKUP. (R/W)

SYSTEM_CRYPTO_AES_RST Set this bit to reset CRYPTO_AES. (R/W)

SYSTEM_CRYPTO_SHA_RST Set this bit to reset CRYPTO_SHA. (R/W)

SYSTEM_CRYPTO_RSA_RST Set this bit to reset CRYPTO_RSA. (R/W)

SYSTEM_CRYPTO_DS_RST Set this bit to reset CRYPTO_DS. (R/W)

SYSTEM_CRYPTO_HMAC_RST Set this bit to reset CRYPTO_HMAC. (R/W)

SYSTEM_DMA_RST Set this bit to reset DMA. (R/W)

SYSTEM_SDIO_HOST_RST Set this bit to reset SDIO_HOST. (R/W)

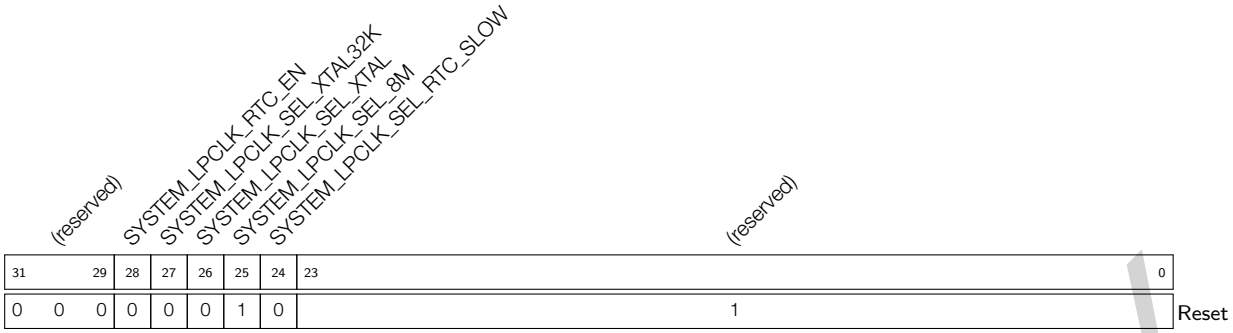
SYSTEM_LCD_CAM_RST Set this bit to reset LCD_CAM. (R/W)

SYSTEM_UART2_RST Set this bit to reset UART2. (R/W)

SYSTEM_USB_DEVICE_RST Set this bit to reset USB_DEVICE. (R/W)

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Register 15.8. SYSTEM_BT_LPCK_DIV_FRAC_REG (0x002C)



SYSTEM_LPCLK_SEL_RTC_SLOW Set this bit to select RTC slow clock as the low-power clock. (R/W)

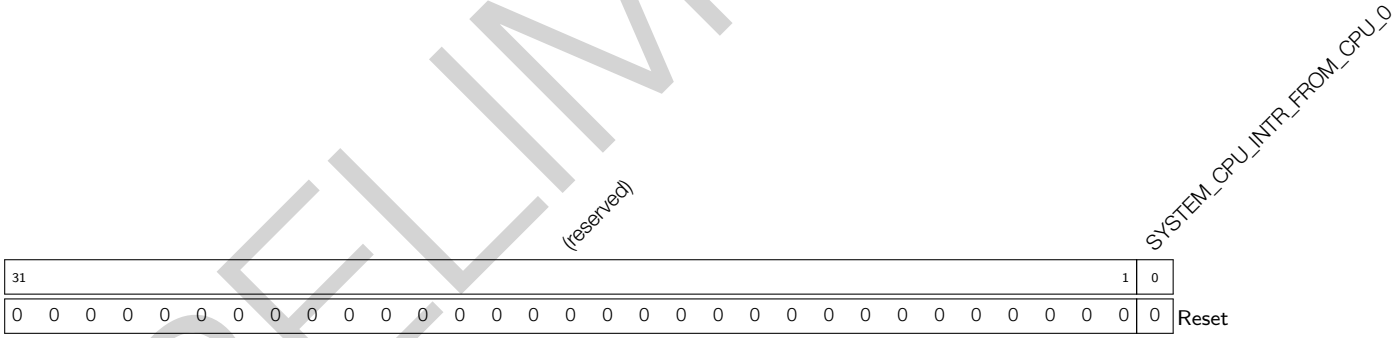
SYSTEM_LPCLK_SEL_8M Set this bit to select 8 MHz clock as the low-power clock. (R/W)

SYSTEM_LPCLK_SEL_XTAL Set this bit to select XTAL clock as the low-power clock. (R/W)

SYSTEM_LPCLK_SEL_XTAL32K Set this bit to select XTAL32K clock as the low-power clock. (R/W)

SYSTEM_LPCLK_RTC_EN Set this bit to enable the RTC low-power clock. (R/W)

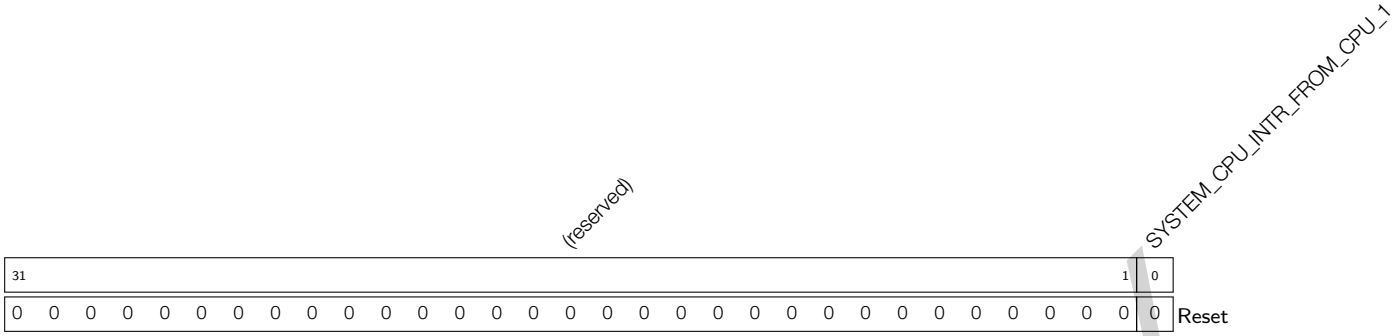
Register 15.9. SYSTEM_CPU_INTR_FROM_CPU_0_REG (0x0030)



SYSTEM_CPU_INTR_FROM_CPU_0 Set this bit to generate CPU interrupt 0. This bit needs to be reset by software in the ISR process. (R/W)

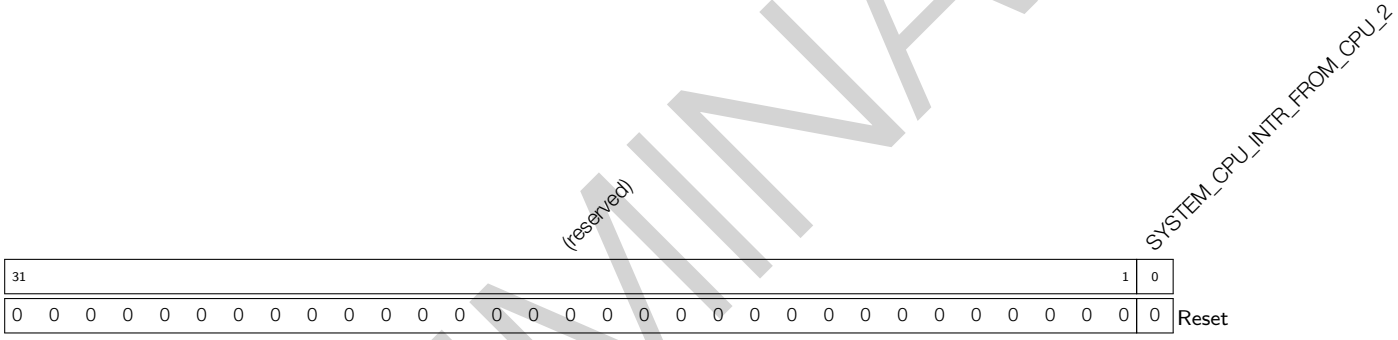
PRELIMINARY

Register 15.10. SYSTEM_CPU_INTR_FROM_CPU_1_REG (0x0034)



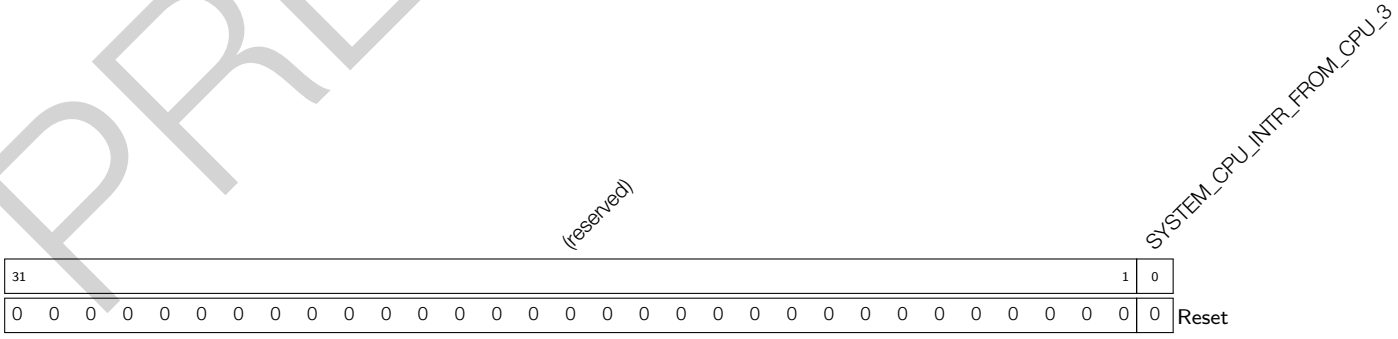
SYSTEM_CPU_INTR_FROM_CPU_1 Set this bit to generate CPU interrupt 1. This bit needs to be reset by software in the ISR process. (R/W)

Register 15.11. SYSTEM_CPU_INTR_FROM_CPU_2_REG (0x0038)



SYSTEM_CPU_INTR_FROM_CPU_2 Set this bit to generate CPU interrupt 2. This bit needs to be reset by software in the ISR process. (R/W)

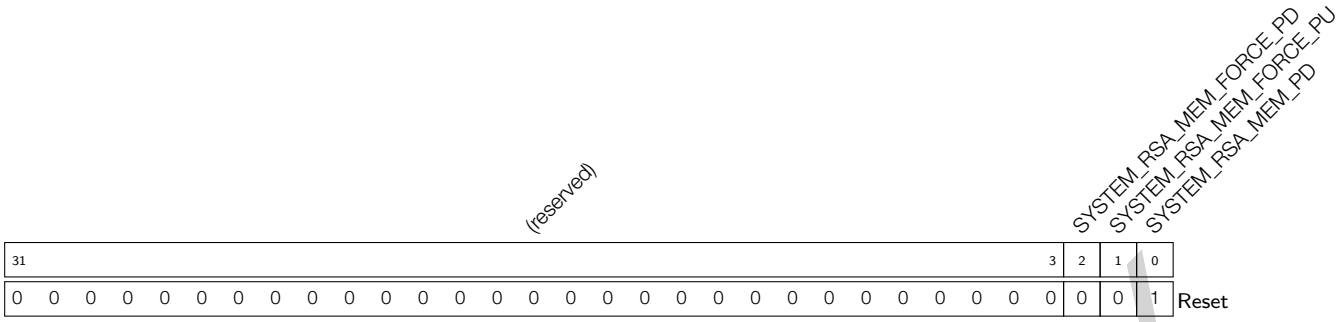
Register 15.12. SYSTEM_CPU_INTR_FROM_CPU_3_REG (0x003C)



SYSTEM_CPU_INTR_FROM_CPU_3 Set this bit to generate CPU interrupt 3. This bit needs to be reset by software in the ISR process. (R/W)

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Register 15.13. SYSTEM_RSA_PD_CTRL_REG (0x0040)

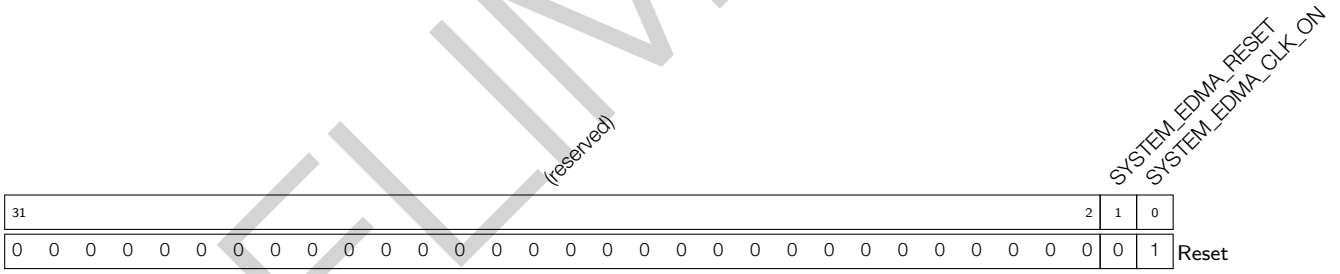


SYSTEM_RSA_MEM_PD Set this bit to send the RSA memory into retention state. This bit has the lowest priority, meaning it can be masked by the SYSTEM_RSA_MEM_FORCE_PU field. When Digital Signature occupies the RSA, this bit is invalid. (R/W)

SYSTEM_RSA_MEM_FORCE_PU Set this bit to force the RSA memory to work as normal when the chip enters light sleep. This bit has the second highest priority, meaning it overrides the SYSTEM_RSA_MEM_PD field. (R/W)

SYSTEM_RSA_MEM_FORCE_PD Set this bit to send the RSA memory into retention state. This bit has the highest priority, meaning it sends the RSA memory into retention state regardless of the SYSTEM_RSA_MEM_FORCE_PU field. (R/W)

Register 15.14. SYSTEM_EDMA_CTRL_REG (0x0044)

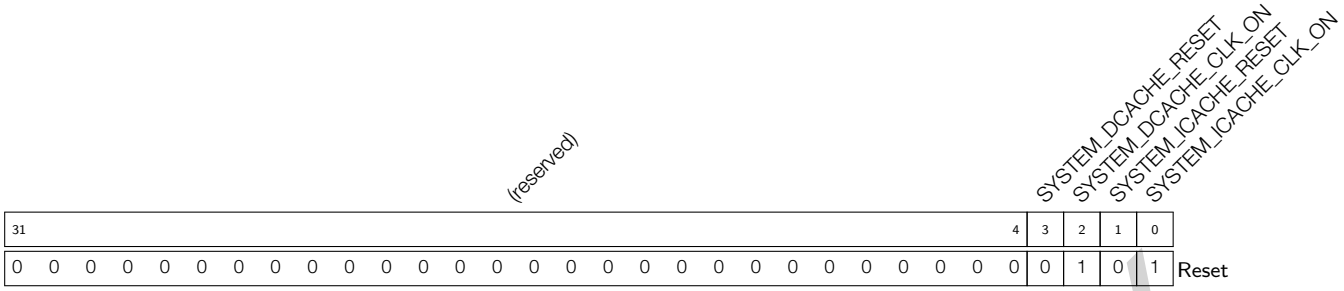


SYSTEM_EDMA_CLK_ON Set this bit to enable EDMA clock. (R/W)

SYSTEM_EDMA_RESET Set this bit to reset EDMA. (R/W)

PRELIMINARY

Register 15.15. SYSTEM_CACHE_CONTROL_REG (0x0048)



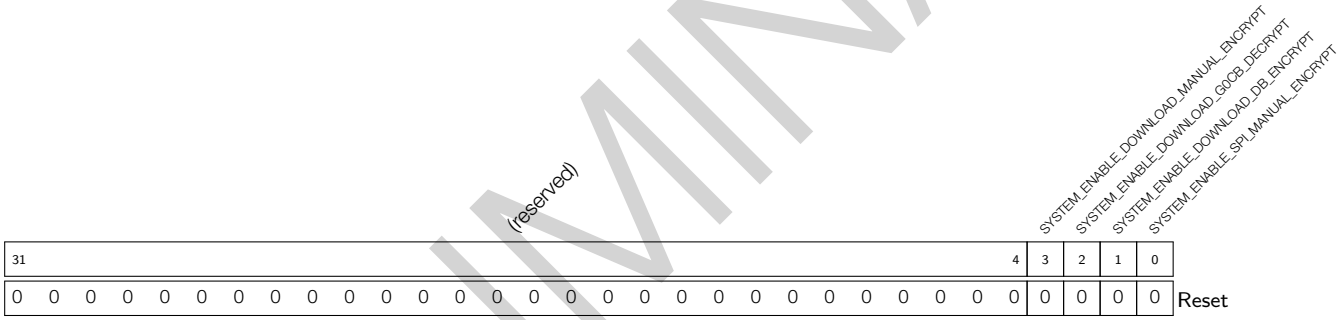
SYSTEM_ICACHE_CLK_ON Set this bit to enable i-cache clock. (R/W)

SYSTEM_ICACHE_RESET Set this bit to reset i-cache. (R/W)

SYSTEM_DCACHE_CLK_ON Set this bit to enable d-cache clock. (R/W)

SYSTEM_DCACHE_RESET Set this bit to reset d-cache. (R/W)

Register 15.16. SYSTEM_EXTERNAL_DEVICE_ENCRYPT_DECRYPT_CONTROL_REG (0x004C)



SYSTEM_ENABLE_SPI_MANUAL_ENCRYPT Set this bit to enable Manual Encryption under SPI Boot mode. (R/W)

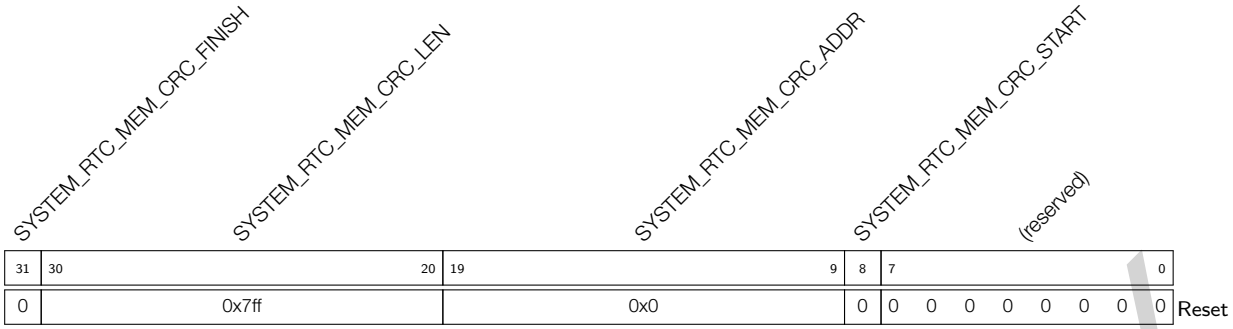
SYSTEM_ENABLE_DOWNLOAD_DB_ENCRYPT Set this bit to enable Auto Encryption under Download Boot mode. (R/W)

SYSTEM_ENABLE_DOWNLOAD_G0CB_DECRYPT Set this bit to enable Auto Decryption under Download Boot mode. (R/W)

SYSTEM_ENABLE_DOWNLOAD_MANUAL_ENCRYPT Set this bit to enable Manual Encryption under Download Boot mode. (R/W)

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Register 15.17. SYSTEM_RTC_FASTMEM_CONFIG_REG (0x0050)



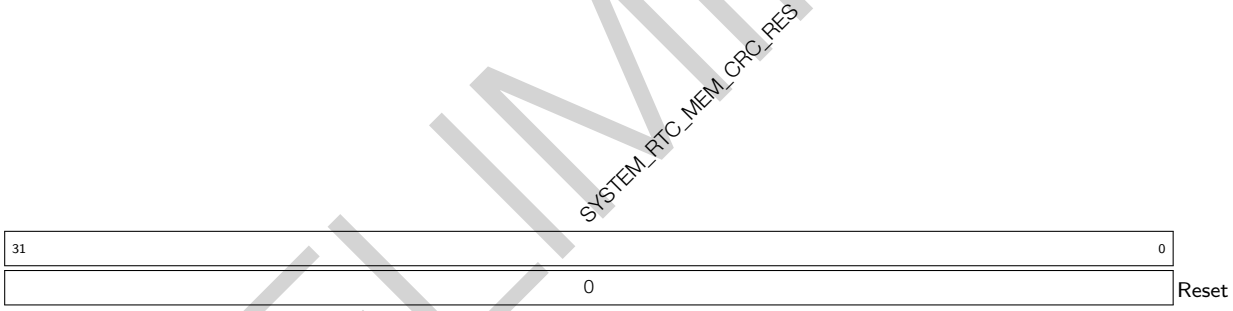
SYSTEM_RTC_MEM_CRC_START Set this bit to start the CRC of RTC memory (R/W)

SYSTEM_RTC_MEM_CRC_ADDR This field is used to set address of RTC memory for CRC. (R/W)

SYSTEM_RTC_MEM_CRC_LEN This field is used to set length of RTC memory for CRC based on start address. (R/W)

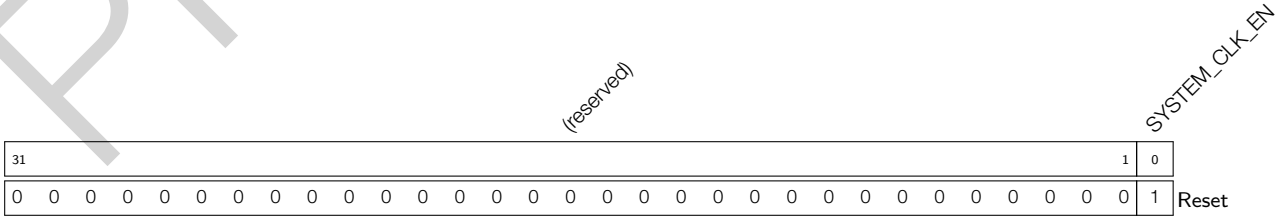
SYSTEM_RTC_MEM_CRC_FINISH This bit stores the status of RTC memory CRC. High level means finished while low level means not finished. (RO)

Register 15.18. SYSTEM_RTC_FASTMEM_CRC_REG (0x0054)



SYSTEM_RTC_MEM_CRC_RES This field stores the CRC result of RTC memory. (RO)

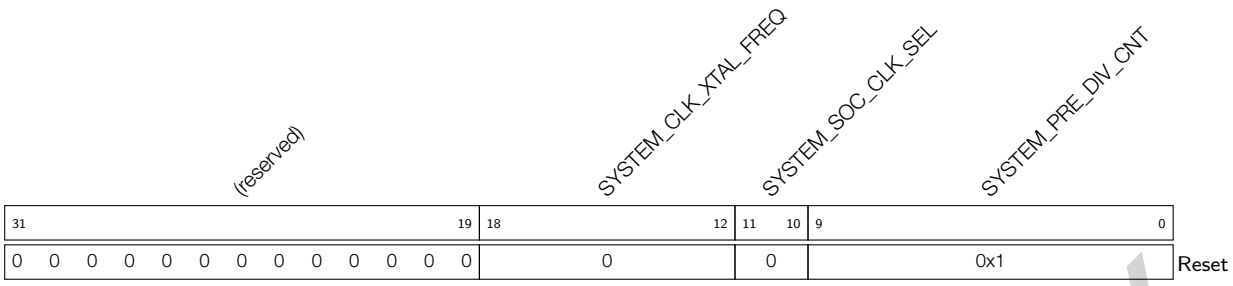
Register 15.19. SYSTEM_CLOCK_GATE_REG (0x005C)



SYSTEM_CLK_EN Set this bit to enable the system clock. (R/W)

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Register 15.20. SYSTEM_SYSCLK_CONF_REG (0x0060)

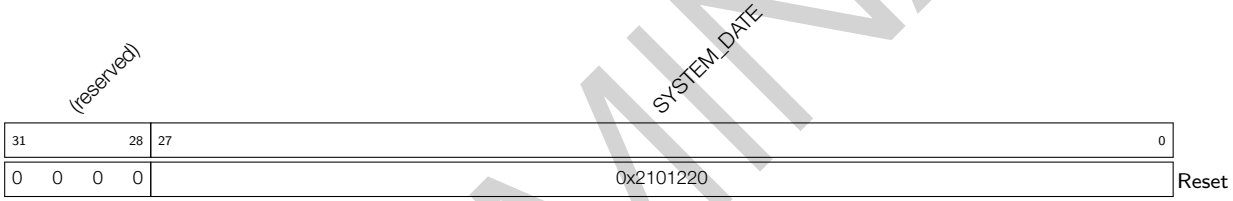


SYSTEM_PRE_DIV_CNT This field is used to set the count of prescaler of XTAL_CLK. For details, please refer to Table 6-4 in Chapter 6 *Reset and Clock*. (R/W)

SYSTEM_SOC_CLK_SEL This field is used to select SOC clock. For details, please refer to Table 6-2 in Chapter 6 *Reset and Clock*. (R/W)

SYSTEM_CLK_XTAL_FREQ This field is used to read XTAL frequency in MHz. (RO)

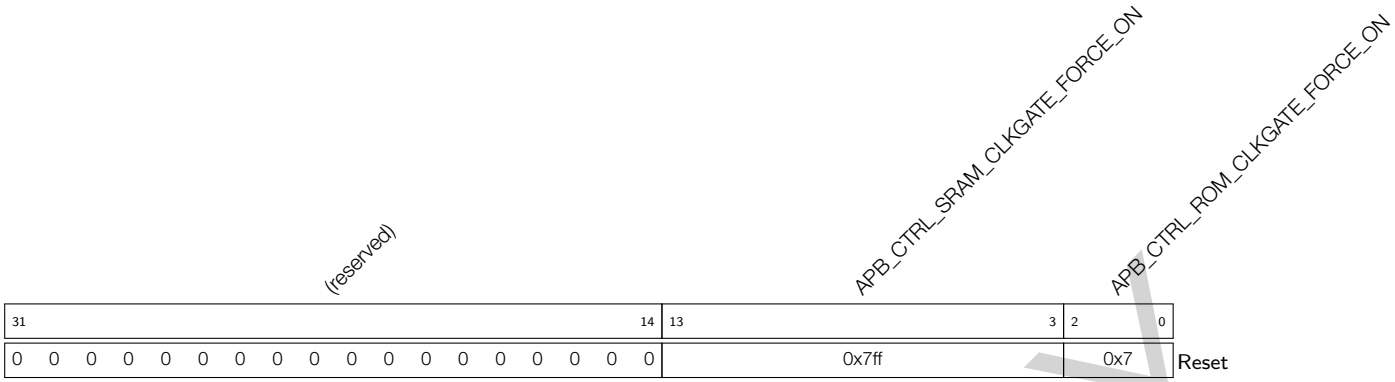
Register 15.21. SYSTEM_DATE_REG (0x0FFC)



SYSTEM_DATE Version control register. (R/W)

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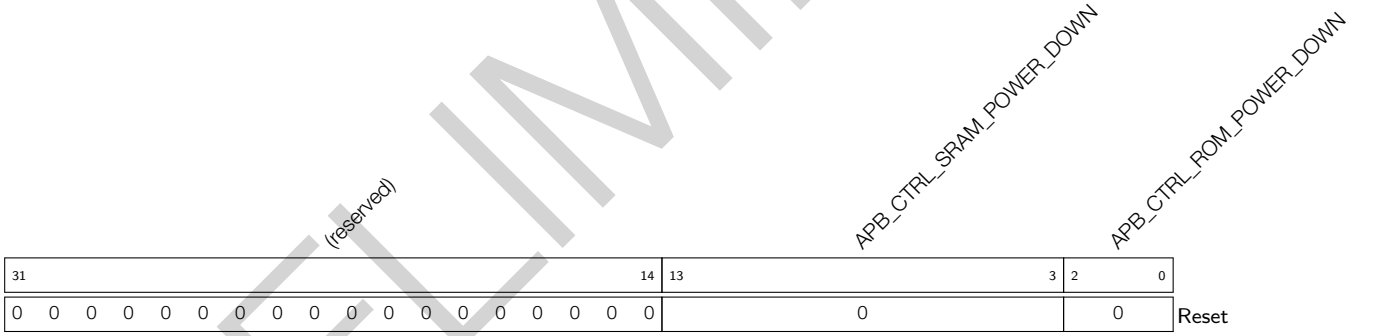
Register 15.22. APB_CTRL_CLKGATE_FORCE_ON_REG (0x00A8)



APB_CTRL_ROM_CLKGATE_FORCE_ON Set 1 to configure the ROM clock gate to be always on; Set 0 to configure the clock gate to turn on automatically when ROM is accessed and turn off automatically when ROM is not accessed. (R/W)

APB_CTRL_SRAM_CLKGATE_FORCE_ON Set 1 to configure the SRAM clock gate to be always on; Set 0 to configure the clock gate to turn on automatically when SRAM is accessed and turn off automatically when SRAM is not accessed. (R/W)

Register 15.23. APB_CTRL_MEM_POWER_DOWN_REG (0x00AC)

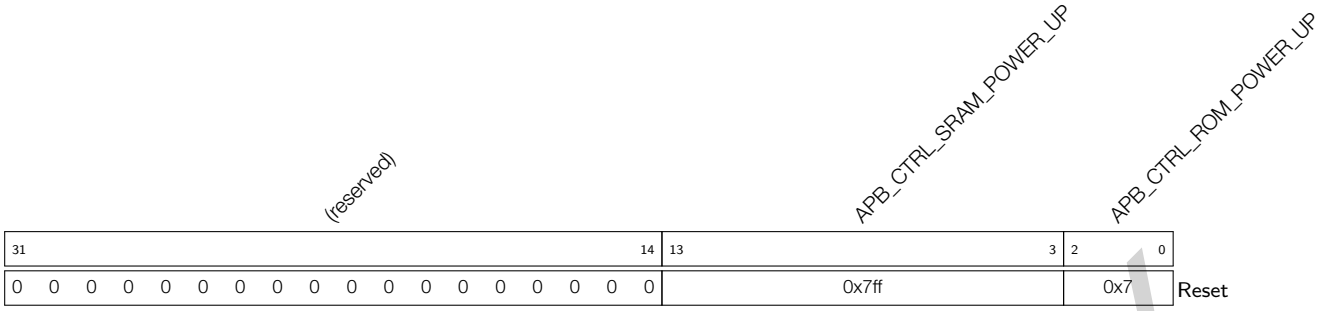


APB_CTRL_ROM_POWER_DOWN Set this field to send the internal ROM into retention state. (R/W)

APB_CTRL_SRAM_POWER_DOWN Set this field to send the internal SRAM into retention state. (R/W)

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Register 15.24. APB_CTRL_MEM_POWER_UP_REG (0x00B0)



APB_CTRL_ROM_POWER_UP Set this field to force the internal ROM to work as normal (do not enter the retention state) when the chip enters light sleep. (R/W)

APB_CTRL_SRAM_POWER_UP Set this field to force the internal SRAM to work as normal (do not enter the retention state) when the chip enters light sleep. (R/W)

PRELIMINARY

16 SHA Accelerator (SHA)

16.1 Introduction

ESP32-S3 integrates an SHA accelerator, which is a hardware device that speeds up SHA algorithm significantly, compared to SHA algorithm implemented solely in software. The SHA accelerator integrated in ESP32-S3 has two working modes, which are Typical SHA and DMA-SHA.

16.2 Features

The following functionality is supported:

- All the hash algorithms introduced in FIPS PUB 180-4 Spec.
  - SHA-1
  - SHA-224
  - SHA-256
  - SHA-384
  - SHA-512
  - SHA-512/224
  - SHA-512/256
  - SHA-512/*t*
- Two working modes
  - Typical SHA
  - DMA-SHA
- interleaved function when working in Typical SHA working mode
- Interrupt function when working in DMA-SHA working mode

16.3 Working Modes

The SHA accelerator integrated in ESP32-S3 has two working modes.

- Typical SHA Working Mode: all the data is written and read via CPU directly.
- DMA-SHA Working Mode: all the data is read via DMA. That is, users can configure the DMA controller to read all the data needed for hash operation, thus releasing CPU for completing other tasks.

Users can start the SHA accelerator with different working modes by configuring registers SHA_START_REG and SHA_DMA_START_REG. For details, please see Table 16-1.

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Table 16-1. SHA Accelerator Working Mode

Working Mode	Configuration Method
Typical SHA	Set SHA_START_REG to 1
DMA-SHA	Set SHA_DMA_START_REG to 1

Users can choose hash algorithms by configuring the SHA_MODE_REG register. For details, please see Table 16-2.

Table 16-2. SHA Hash Algorithm Selection

Hash Algorithm	SHA_MODE_REG Configuration
SHA-1	0
SHA-224	1
SHA-256	2
SHA-384	3
SHA-512	4
SHA-512/224	5
SHA-512/256	6
SHA-512/t	7

Notice:

ESP32-S3's Digital Signature (DS) and HMAC Accelerator (HMAC) modules also call the SHA accelerator. Therefore, users cannot access the SHA accelerator when these modules are working.

16.4 Function Description

SHA accelerator can generate the message digest via two steps: Preprocessing and Hash operation.

16.4.1 Preprocessing

Preprocessing consists of three steps: padding the message, parsing the message into message blocks and setting the initial hash value.

16.4.1.1 Padding the Message

The SHA accelerator can only process message blocks of 512 or 1024 bits, depending on the algorithm. Thus, all the messages should be padded to a multiple of 512 or 1024 bits before the hash task.

Suppose that the length of the message M is m bits. Then M shall be padded as introduced below:

- **SHA-1**, **SHA-224** and **SHA-256**
  1. First, append the bit "1" to the end of the message;
  2. Second, append k zero bits, where k is the smallest, non-negative solution to the equation $m + 1 + k \equiv 448 \ mod \ 512$;
  3. Last, append the 64-bit block of value equal to the number m expressed using a binary representation.

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- **SHA-384**, **SHA-512**, **SHA-512/224**, **SHA-512/256** and **SHA-512/t**

  1. First, append the bit "1" to the end of the message;
  2. Second, append k zero bits, where k is the smallest, non-negative solution to the equation $m + 1 + k \equiv 896 \ mod \ 1024$;
  3. Last, append the 128-bit block of value equal to the number m expressed using a binary representation.

For more details, please refer to Section "5.1 Padding the Message" in FIPS PUB 180-4 Spec.

16.4.1.2 Parsing the Message

The message and its padding must be parsed into N 512-bit or 1024-bit blocks.

- For **SHA-1**, **SHA-224** and **SHA-256**: the message and its padding are parsed into N 512-bit blocks, $M^{(1)}$, $M^{(2)}$, ..., $M^{(N)}$. Since the 512 bits of the input block may be expressed as sixteen 32-bit words, the first 32 bits of message block i are denoted $M_0^{(i)}$, the next 32 bits are $M_1^{(i)}$, and so on up to $M_{15}^{(i)}$.
- For **SHA-384**, **SHA-512**, **SHA-512/224**, **SHA-512/256** and **SHA-512/t**: the message and its padding are parsed into N 1024-bit blocks. Since the 1024 bits of the input block may be expressed as sixteen 64-bit words, the first 64 bits of message block i are denoted $M_0^{(i)}$, the next 64 bits are $M_1^{(i)}$, and so on up to $M_{15}^{(i)}$.

During the task, all the message blocks are written into the SHA_M_n_REG, following the rules below:

- For **SHA-1, SHA-224 and SHA-256**: $M_0^{(i)}$ is stored in SHA_M_0_REG, $M_1^{(i)}$ stored in SHA_M_1_REG, ..., and $M_{15}^{(i)}$ stored in SHA_M_15_REG.
- For **SHA-384, SHA-512, SHA-512/224 and SHA-512/256**: the most significant 32 bits and the least significant 32 bits of $M_0^{(i)}$ are stored in SHA_M_0_REG and SHA_M_1_REG, respectively, ..., the most significant 32 bits and the least significant 32 bits of $M_{15}^{(i)}$ are stored in SHA_M_30_REG and SHA_M_31_REG, respectively.

> **Note:**
> For more information about "message block", please refer to Section "2.1 Glossary of Terms and Acronyms" in FIPS PUB 180-4 Spec.

16.4.1.3 Initial Hash Value

Before hash task begins for each of the secure hash algorithms, the initial Hash value $H^{(0)}$ must be set based on different algorithms, among which the SHA-1, SHA-224, SHA-256, SHA-384, SHA-512, SHA-512/224, and SHA-512/256 algorithms use the initial Hash values (constant C) stored in the hardware.

However, SHA-512/t requires a distinct initial hash value for each operation for a given value of t. Simply put, SHA-512/t is the generic name for a t-bit hash function based on SHA-512 whose output is truncated to t bits. t is any positive integer without a leading zero such that t<512, and t is not 384. The initial hash value for SHA-512/t for a given value of t can be calculated by performing SHA-512 from hexadecimal representation of the string "SHA-512/t". It's not hard to observe that when determining the initial hash values for SHA-512/t algorithms with different t, the only difference lies in the value of t.

Therefore, we have specially developed the following simplified method to calculate the initial hash value for SHA-512/t:

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1. **Generate t_string and t_length**: t_string is a 32-bit data that stores the input message of t. t_length is a 7-bit data that stores the length of the input message. The t_string and t_length are generated in methods described below, depending on the value of t:

   - If $1 <= t <= 9$, then $t\_length = 7'h48$ and t_string is padded in the following format:

$8'h30 + 8'ht_0$	$1'b1$	$23'b0$

     where $t_0 = t$.

     For example, if t = 8, then t_0 = 8 and t_string = $32'h38800000$.

   - If $10 <= t <= 99$, then $t\_length = 7'h50$ and t_string is padded in the following format:

$8'h30 + 8'ht_1$	$8'h30 + 8'ht_0$	$1'b1$	$15'b0$

     where, $t_0 = t\%10$ and $t_1 = t/10$.

     For example, if t = 56, then t_0 = 6, t_1 = 5, and t_string = $32'h35368000$.

   - If $100 <= t < 512$, then $t\_length = 7'h58$ and t_string is padded in the following format:

$8'h30 + 8'ht_2$	$8'h30 + 8'ht_1$	$8'h30 + 8'ht_0$	$1'b1$	$7'b0$

     where, $t_0 = t\%10$, $t_1 = (t/10)\%10$, and $t_2 = t/100$.

     For example, if t = 231, then t_0 = 1, t_1 = 3, t_2 = 2, and t_string = $32'h32333180$.

2. **Initialize relevant registers**: Initialize SHA_T_STRING_REG and SHA_T_LENGTH_REG with the generated t_string and t_length in the previous step.

3. **Obtain initial hash value**: Set the SHA_MODE_REG register to 7. Set the SHA_START_REG register to 1 to start the SHA accelerator. Then poll register SHA_BUSY_REG until the content of this register becomes 0, indicating the calculation of initial hash value is completed.

Please note that the initial value for SHA-512/t can be also calculated according to the Section "5.3.6 SHA-512/t" in FIPS PUB 180-4 Spec, that is performing SHA-512 operation (with its initial hash value set to the result of 8-bitwise XOR operation of C and 0xa5) from the hexadecimal representation of the string "SHA-512/t".

16.4.2 Hash task Process

After the preprocessing, the ESP32-S3 SHA accelerator starts to hash a message M and generates message digest of different lengths, depending on different hash algorithms. As described above, the ESP32-S3 SHA accelerator supports two working modes, which are Typical SHA and DMA-SHA. The operation process for the SHA accelerator under two working modes is described in the following subsections.

16.4.2.1 Typical SHA Mode Process

Usually, the SHA accelerator will process all blocks of a message and produce a message digest before starting the next message digest.

However, ESP32-S3 SHA working in Typical SHA mode also supports optional "interleaved" message digest calculation. Users can insert new calculation (both Typical SHA and DMA-SHA) each time the SHA accelerator completes one message block. To be more specific, users can store the message digest in registers

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SHA_H_*n*_REG after completing each message block, and assign the accelerator with other higher priority tasks. After the inserted calculation completes, users can put the message digest stored back to registers SHA_H_*n*_REG, and resume the accelerator with the previously paused calculation.

Typical SHA Process (except for SHA-512/*t*)

1. Select a hash algorithm.
   - Configure the SHA_MODE_REG register based on Table 16-2.
2. Process the current message block [1].
   - Write the message block in registers SHA_M_*n*_REG.
3. Start the SHA accelerator.
   - If this is the first time to execute this step, set the SHA_START_REG register to 1 to start the SHA accelerator. In this case, the accelerator uses the initial hash value stored in hardware for a given algorithm configured in Step 1 to start the calculation;
   - If this is not the first time to execute this step[2], set the SHA_CONTINUE_REG register to 1 to start the SHA accelerator. In this case, the accelerator uses the hash value stored in the SHA_H_*n*_REG register to start calculation.
4. Check the progress of the current message block.
   - Poll register SHA_BUSY_REG until the content of this register becomes 0, indicating the accelerator has completed the calculation for the current message block and now is in the "idle" status [3].
5. Decide if you have more message blocks to process:
   - If yes, please go back to Step 2.
   - Otherwise, please continue.
6. Obtain the message digest.
   - Read the message digest from registers SHA_H_*n*_REG.

Typical SHA Process (SHA-512/*t*)

1. Select a hash algorithm.
   - Configure the SHA_MODE_REG register to 7 for SHA-512/*t*.
2. Calculate the initial hash value.
   (a) Calculate t_stiring and t_length and initialize SHA_T_STRING_REG and SHA_T_LENGTH_REG with the generated t_string and t_length. For details, please refer to Section 16.4.1.3.
   (b) Set the SHA_START_REG register to 1 to start the SHA accelerator.
   (c) Poll register SHA_BUSY_REG until the content of this register becomes 0, indicating the calculation of initial hash value is completed.
3. Process the current message block[1].
   - Write the message block in registers SHA_M_*n*_REG.
4. Start the SHA accelerator

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- Set the SHA_CONTINUE_REG register to 1. In this case, the accelerator uses the hash value stored in the SHA_H_*n*_REG register to start calculation.

5. Check the progress of the calculation.
   - Poll register SHA_BUSY_REG until the content of this register becomes 0, indicating the accelerator has completed the calculation for the current message block and now is in the "idle" status[3].
6. Decide if you have more message blocks to process:
   - If yes, please go back to Step 3.
   - Otherwise, please continue.
7. Obtain the message digest.
   - Read the message digest from registers SHA_H_*n*_REG.

Note:

1. In this step, the software can also write the next message block (to be processed) in registers SHA_M_*n*_REG, if any, while the hardware starts SHA calculation, to save time.
2. You are resuming the SHA accelerator with the previously paused calculation.
3. Here you can decide if you want to insert other calculations. If yes, please go to the process for interleaved calculations for details.

As mentioned above, ESP32-S3 SHA accelerator supports **"interleaving" calculation under the Typical SHA working mode**.

The process to implement interleaved calculation is described below.

1. Prepare to hand the SHA accelerator over for an interleaved calculation by saving the following data of the previous calculation.
   - The selected hash algorithm stored in the SHA_MODE_REG register.
   - The message digest stored in registers SHA_H_*n*_REG.
2. Perform the interleaved calculation. For the detailed process of the interleaved calculation, please refer to Typical SHA process or DMA-SHA process, depending on the working mode of your interleaved calculation.
3. Prepare to hand the SHA accelerator back to the previously paused calculation by restoring the following data of the previous calculation.
   - Write the previously stored hash algorithm back to register SHA_MODE_REG
   - Write the previously stored message digest back to registers SHA_H_*n*_REG
4. Write the next message block from the previous paused calculation in registers SHA_M_*n*_REG, and set the SHA_CONTINUE_REG register to 1 to restart the SHA accelerator with the previously paused calculation.

16.4.2.2 DMA-SHA Mode Process

ESP32-S3 SHA accelerator does not support "interleaving" message digest calculation when using the DMA, which means you cannot insert new calculation before the whole DMA-SHA process completes. In this case,

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users who need inserted calculation are recommended to divide your message blocks and perform several DMA-SHA calculation, instead of trying to compute all the messages in one go.

In contrast to the Typical SHA working mode, when the SHA accelerator is working under the DMA-SHA mode, all data read are completed via DMA.

Therefore, users are required to configure the DMA controller following the description in Chapter 2 *GDMA Controller (GDMA)*.

DMA-SHA process (except SHA-512/t)

1. Select a hash algorithm.
   - Select a hash algorithm by configuring the SHA_MODE_REG register. For details, please refer to Table 16-2.
2. Configure the SHA_INT_ENA_REG register to enable or disable interrupt (Set 1 to enable).
3. Configure the number of message blocks.
   - Write the number of message blocks M to the SHA_DMA_BLOCK_NUM_REG register.
4. Start the DMA-SHA calculation.
   - If the current DMA-SHA calculation follows a previous calculation, firstly write the message digest from the previous calculation to registers SHA_H_*n*_REG, then write 1 to register SHA_DMA_CONTINUE_REG to start SHA accelerator;
   - Otherwise, write 1 to register SHA_DMA_START_REG to start the accelerator.
5. Wait till the completion of the DMA-SHA calculation, which happens when:
   - The content of SHA_BUSY_REG register becomes 0, or
   - An SHA interrupt occurs. In this case, please clear interrupt by writing 1 to the SHA_INT_CLEAR_REG register.
6. Obtain the message digest:
   - Read the message digest from registers SHA_H_*n*_REG.

DMA-SHA process for SHA-512/t

1. Select a hash algorithm.
   - Select SHA-512/t algorithm by configuring the SHA_MODE_REG register to 7.
2. Configure the SHA_INT_ENA_REG register to enable or disable interrupt (Set 1 to enable).
3. Calculate the initial hash value.
   (a) Calculate t_string and t_length and initialize SHA_T_STRING_REG and SHA_T_LENGTH_REG with the generated t_string and t_length. For details, please refer to Section 16.4.1.3.
   (b) Set the SHA_START_REG register to 1 to start the SHA accelerator.
   (c) Poll register SHA_BUSY_REG until the content of this register becomes 0, indicating the calculation of initial hash value is completed.
4. Configure the number of message blocks.

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- Write the number of message blocks M to the SHA_DMA_BLOCK_NUM_REG register.

5. Start the DMA-SHA calculation.
   - Write 1 to register SHA_DMA_CONTINUE_REG to start the accelerator.
6. Wait till the completion of the DMA-SHA calculation, which happens when:
   - The content of SHA_BUSY_REG register becomes 0, or
   - An SHA interrupt occurs. In this case, please clear interrupt by writing 1 to the SHA_INT_CLEAR_REG register.
7. Obtain the message digest:
   - Read the message digest from registers SHA_H_*n*_REG.

16.4.3 Message Digest

After the hash task completes, the SHA accelerator writes the message digest from the task to registers SHA_H_*n*_REG(*n*: 0~15). The lengths of the generated message digest are different depending on different hash algorithms. For details, see Table 16-6 below:

Table 16-6. The Storage and Length of Message digest from Different Algorithms

Hash Algorithm	Length of Message Digest (in bits)	Storage[1]
SHA-1	160	SHA_H_0_REG ~ SHA_H_4_REG
SHA-224	224	SHA_H_0_REG ~ SHA_H_6_REG
SHA-256	256	SHA_H_0_REG ~ SHA_H_7_REG
SHA-384	384	SHA_H_0_REG ~ SHA_H_11_REG
SHA-512	512	SHA_H_0_REG ~ SHA_H_15_REG
SHA-512/224	224	SHA_H_0_REG ~ SHA_H_6_REG
SHA-512/256	256	SHA_H_0_REG ~ SHA_H_7_REG
SHA-512/*t*[2]	*t*	SHA_H_0_REG ~ SHA_H_*x*_REG

[1] The message digest are stored in registers from most significant bits to the least significant bits, with the first word stored in register SHA_H_0_REG and the second word stored in register SHA_H_1_REG... For details, please see subsection 16.4.1.2.

[2] The registers used for SHA-512/t algorithm depend on the value of t. x+1 indicates the number of 32-bit registers used to store t bits of message digest, so that $x = roundup(t/32)$-1. For example:

- When t = 8, then x = 0, indicating that the 8-bit long message digest is stored in the most significant 8 bits of register SHA_H_0_REG;
- When t = 32, then x = 0, indicating that the 32-bit long message digest is stored in register SHA_H_0_REG;
- When t = 132, then x = 4, indicating that the 132-bit long message digest is stored in registers SHA_H_0_REG, SHA_H_1_REG, SHA_H_2_REG, SHA_H_3_REG, and SHA_H_4_REG.

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16.4.4 Interrupt

SHA accelerator supports interrupt on the completion of message digest calculation when working in the DMA-SHA mode. To enable this function, write 1 to register SHA_INT_ENA_REG. Note that the interrupt should be cleared by software after use via setting the SHA_INT_CLEAR_REG register to 1.

16.5 Register Summary

The addresses in this section are relative to the SHA accelerator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
Control/Status registers			
SHA_CONTINUE_REG	Continues SHA operation (only effective in Typical SHA mode)	0x0014	WO
SHA_BUSY_REG	Indicates if SHA Accelerator is busy or not	0x0018	RO
SHA_DMA_START_REG	Starts the SHA accelerator for DMA-SHA operation	0x001C	WO
SHA_START_REG	Starts the SHA accelerator for Typical SHA operation	0x0010	WO
SHA_DMA_CONTINUE_REG	Continues SHA operation (only effective in DMA-SHA mode)	0x0020	WO
SHA_INT_CLEAR_REG	DMA-SHA interrupt clear register	0x0024	WO
SHA_INT_ENA_REG	DMA-SHA interrupt enable register	0x0028	R/W
Version Register			
SHA_DATE_REG	Version control register	0x002C	R/W
Configuration Registers			
SHA_MODE_REG	Defines the algorithm of SHA accelerator	0x0000	R/W
SHA_T_STRING_REG	String content register for calculating initial Hash Value (only effective for SHA-512/t)	0x0004	R/W
SHA_T_LENGTH_REG	String length register for calculating initial Hash Value (only effective for SHA-512/t)	0x0008	R/W
Memories			
SHA_DMA_BLOCK_NUM_REG	Block number register (only effective for DMA-SHA)	0x000C	R/W
SHA_H_0_REG	Hash value	0x0040	R/W
SHA_H_1_REG	Hash value	0x0044	R/W
SHA_H_2_REG	Hash value	0x0048	R/W
SHA_H_3_REG	Hash value	0x004C	R/W
SHA_H_4_REG	Hash value	0x0050	R/W
SHA_H_5_REG	Hash value	0x0054	R/W
SHA_H_6_REG	Hash value	0x0058	R/W
SHA_H_7_REG	Hash value	0x005C	R/W
SHA_H_8_REG	Hash value	0x0060	R/W
SHA_H_9_REG	Hash value	0x0064	R/W
SHA_H_10_REG	Hash value	0x0068	R/W

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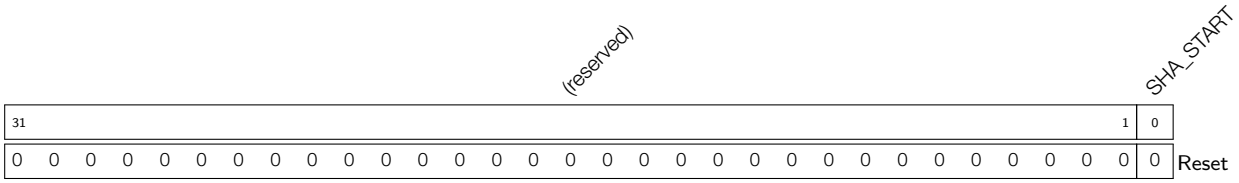
Name	Description	Address	Access
SHA_H_11_REG	Hash value	0x006C	R/W
SHA_H_12_REG	Hash value	0x0070	R/W
SHA_H_13_REG	Hash value	0x0074	R/W
SHA_H_14_REG	Hash value	0x0078	R/W
SHA_H_15_REG	Hash value	0x007C	R/W
SHA_M_0_REG	Message	0x0080	R/W
SHA_M_1_REG	Message	0x0084	R/W
SHA_M_2_REG	Message	0x0088	R/W
SHA_M_3_REG	Message	0x008C	R/W
SHA_M_4_REG	Message	0x0090	R/W
SHA_M_5_REG	Message	0x0094	R/W
SHA_M_6_REG	Message	0x0098	R/W
SHA_M_7_REG	Message	0x009C	R/W
SHA_M_8_REG	Message	0x00A0	R/W
SHA_M_9_REG	Message	0x00A4	R/W
SHA_M_10_REG	Message	0x00A8	R/W
SHA_M_11_REG	Message	0x00AC	R/W
SHA_M_12_REG	Message	0x00B0	R/W
SHA_M_13_REG	Message	0x00B4	R/W
SHA_M_14_REG	Message	0x00B8	R/W
SHA_M_15_REG	Message	0x00BC	R/W
SHA_M_16_REG	Message	0x00C0	R/W
SHA_M_17_REG	Message	0x00C4	R/W
SHA_M_18_REG	Message	0x00C8	R/W
SHA_M_19_REG	Message	0x00CC	R/W
SHA_M_20_REG	Message	0x00D0	R/W
SHA_M_21_REG	Message	0x00D4	R/W
SHA_M_22_REG	Message	0x00D8	R/W
SHA_M_23_REG	Message	0x00DC	R/W
SHA_M_24_REG	Message	0x00E0	R/W
SHA_M_25_REG	Message	0x00E4	R/W
SHA_M_26_REG	Message	0x00E8	R/W
SHA_M_27_REG	Message	0x00EC	R/W
SHA_M_28_REG	Message	0x00F0	R/W
SHA_M_29_REG	Message	0x00F4	R/W
SHA_M_30_REG	Message	0x00F8	R/W
SHA_M_31_REG	Message	0x00FC	R/W

16.6 Registers

The addresses in this section are relative to the SHA accelerator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

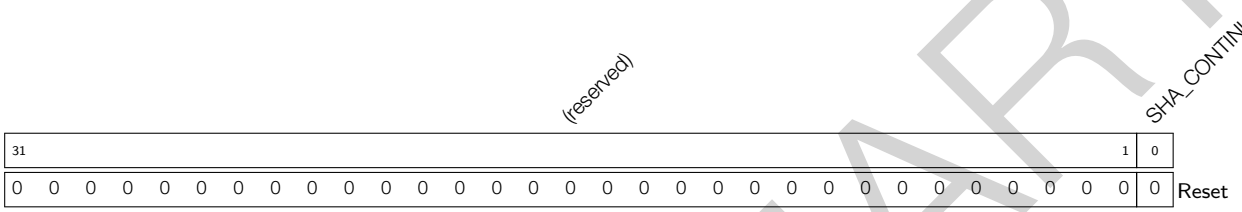
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Register 16.1. SHA_START_REG (0x0010)



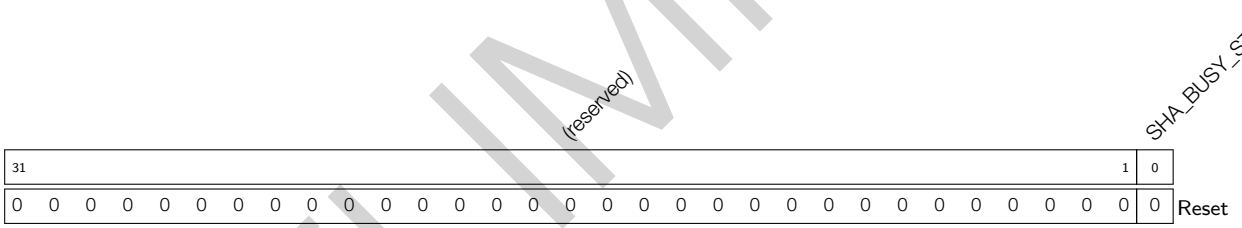
SHA_START Write 1 to start Typical SHA calculation. (WO)

Register 16.2. SHA_CONTINUE_REG (0x0014)



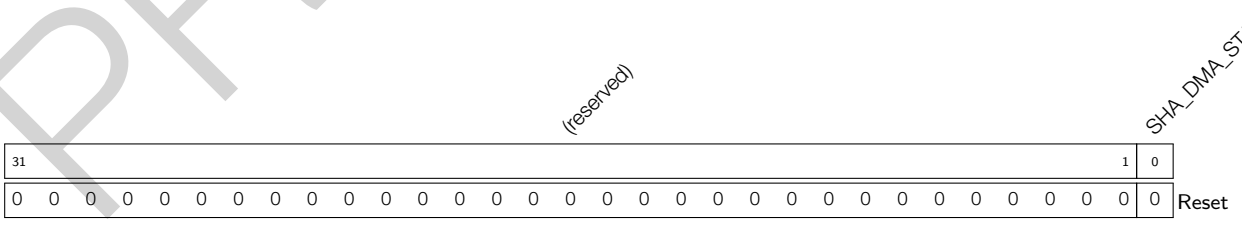
SHA_CONTINUE Write 1 to continue Typical SHA calculation. (WO)

Register 16.3. SHA_BUSY_REG (0x0018)



SHA_BUSY_STATE Indicates the states of SHA accelerator. (RO) 1'h0: idle 1'h1: busy

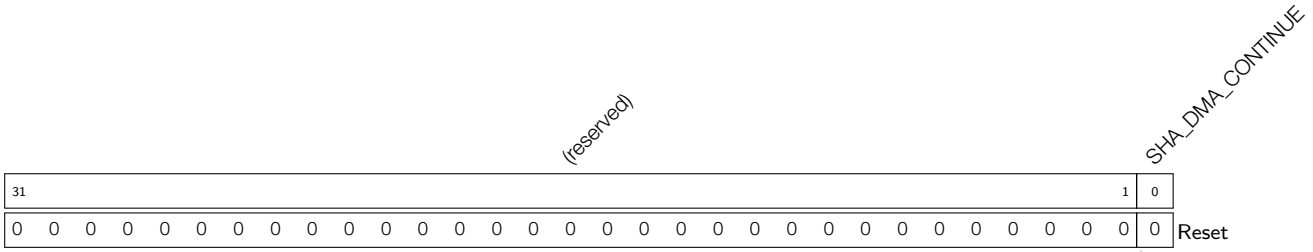
Register 16.4. SHA_DMA_START_REG (0x001C)



SHA_DMA_START Write 1 to start DMA-SHA calculation. (WO)

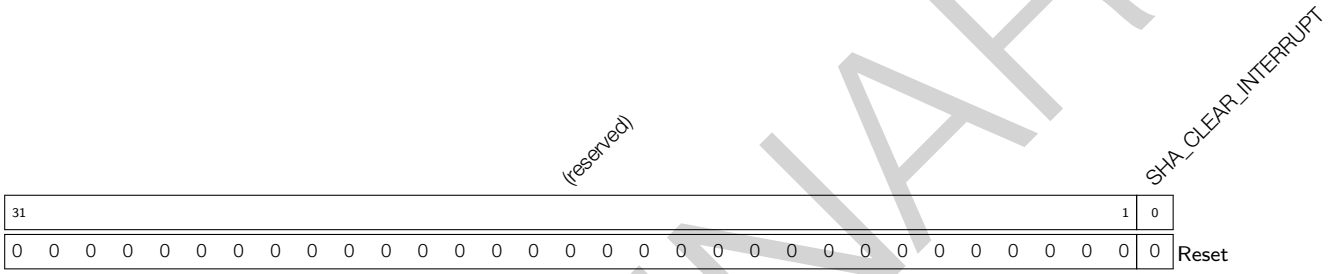
PRELIMINARY

Register 16.5. SHA_DMA_CONTINUE_REG (0x0020)



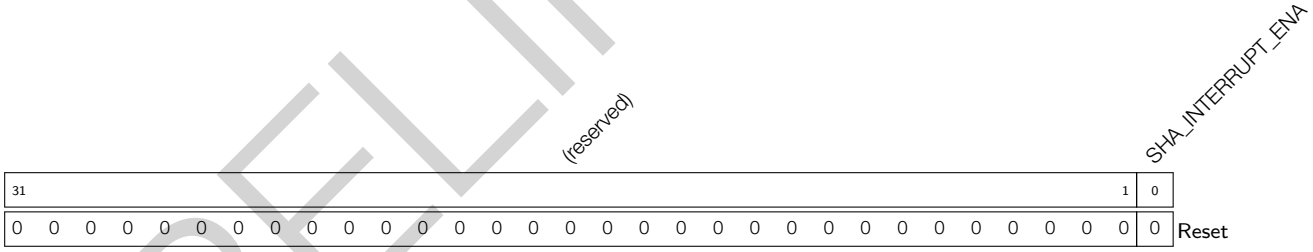
SHA_DMA_CONTINUE Write 1 to continue DMA-SHA calculation. (WO)

Register 16.6. SHA_INT_CLEAR_REG (0x0024)



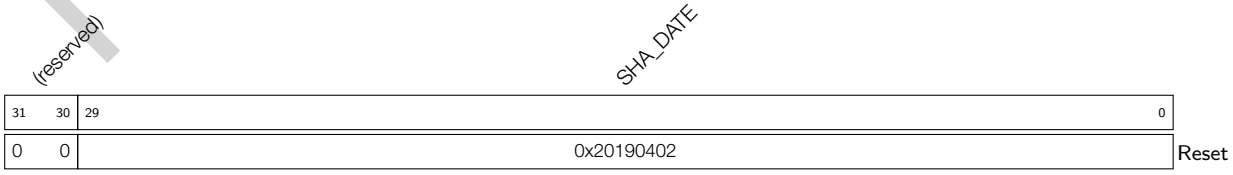
SHA_CLEAR_INTERRUPT Clears DMA-SHA interrupt. (WO)

Register 16.7. SHA_INT_ENA_REG (0x0028)



SHA_INTERRUPT_ENA Enables DMA-SHA interrupt. (R/W)

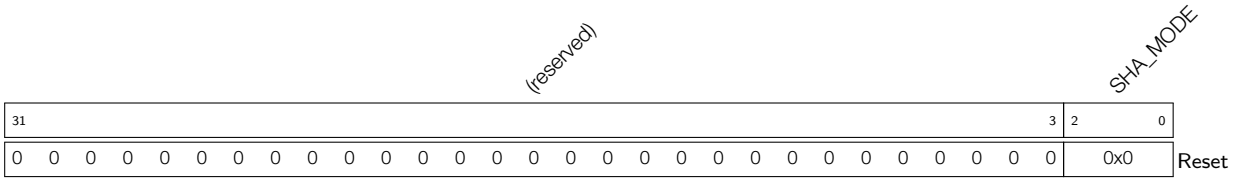
Register 16.8. SHA_DATE_REG (0x002C)



SHA_DATE Version control register. (R/W)

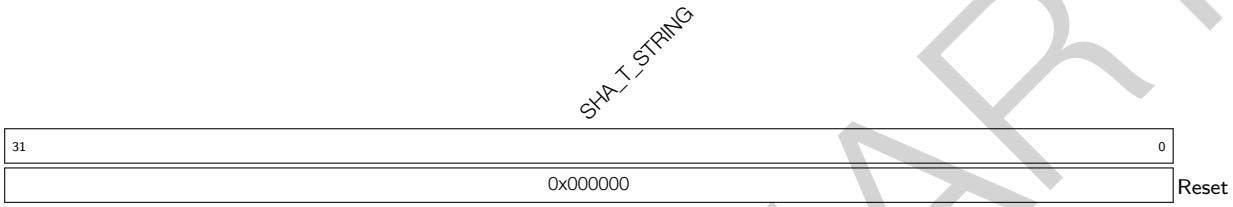
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Register 16.9. SHA_MODE_REG (0x0000)



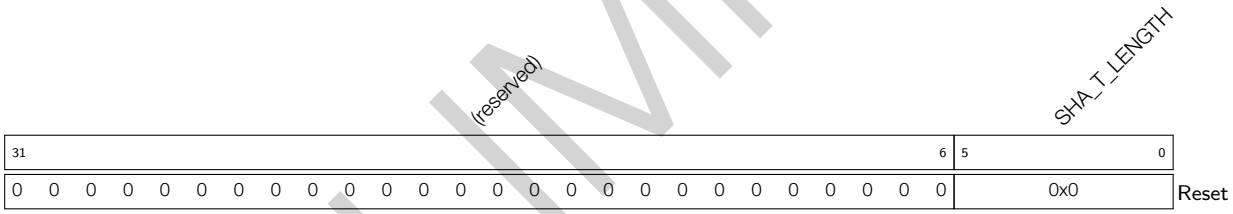
SHA_MODE Defines the SHA algorithm. For details, please see Table 16-2. (R/W)

Register 16.10. SHA_T_STRING_REG (0x0004)



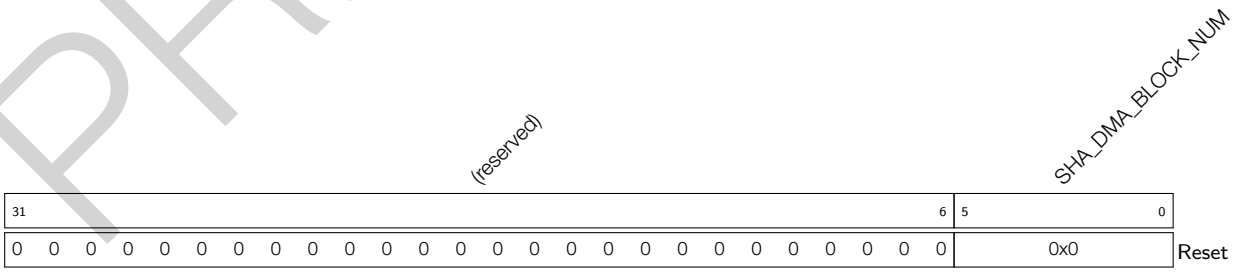
SHA_T_STRING Defines t_string for calculating the initial Hash value for SHA-512/t. (R/W)

Register 16.11. SHA_T_LENGTH_REG (0x0008)



SHA_T_LENGTH Defines t_length for calculating the initial Hash value for SHA-512/t. (R/W)

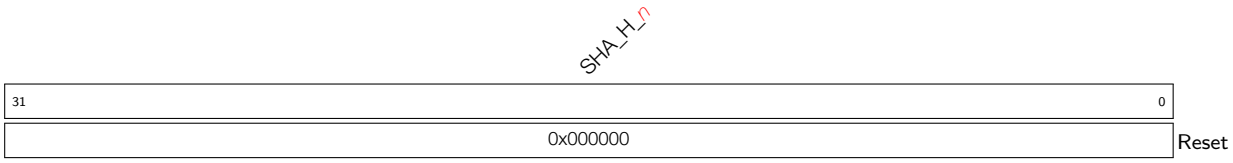
Register 16.12. SHA_DMA_BLOCK_NUM_REG (0x000C)



SHA_DMA_BLOCK_NUM Defines the DMA-SHA block number. (R/W)

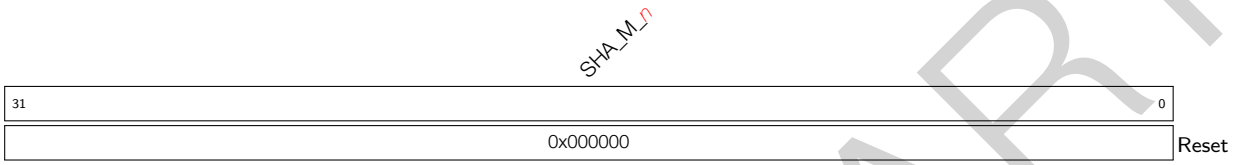
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Register 16.13. SHA_H_*n*_REG (*n*: 0-15) (0x0040+4n*)**



SHA_H_*n* Stores the *n*th 32-bit piece of the Hash value. (R/W)

Register 16.14. SHA_M_*n*_REG (*n*: 0-31) (0x0080+4n*)**



SHA_M_*n* Stores the *n*th 32-bit piece of the message. (R/W)

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17 AES Accelerator (AES)

17.1 Introduction

ESP32-S3 integrates an Advanced Encryption Standard (AES) Accelerator, which is a hardware device that speeds up AES Algorithm significantly, compared to AES algorithms implemented solely in software. The AES Accelerator integrated in ESP32-S3 has two working modes, which are Typical AES and DMA-AES.

17.2 Features

The following functionality is supported:

- Typical AES working mode
  - AES-128/AES-256 encryption and decryption
- DMA-AES working mode
  - AES-128/AES-256 encryption and decryption
  - Block cipher mode
    - ECB (Electronic Codebook)
    - CBC (Cipher Block Chaining)
    - OFB (Output Feedback)
    - CTR (Counter)
    - CFB8 (8-bit Cipher Feedback)
    - CFB128 (128-bit Cipher Feedback)
  - Interrupt on completion of computation

17.3 AES Working Modes

The AES Accelerator integrated in ESP32-S3 has two working modes, which are Typical AES and DMA-AES.

- Typical AES Working Mode:
  - Supports encryption and decryption using cryptographic keys of 128 and 256 bits, specified in NIST FIPS 197.

  In this working mode, the plaintext and ciphertext is written and read via CPU directly.
- DMA-AES Working Mode:
  - Supports encryption and decryption using cryptographic keys of 128 and 256 bits, specified in NIST FIPS 197;
  - Supports block cipher modes ECB/CBC/OFB/CTR/CFB8/CFB128 under NIST SP 800-38A.

  In this working mode, the plaintext and ciphertext is written and read via DMA. An interrupt will be generated when operation completes.

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Users can choose the working mode for AES accelerator by configuring the AES_DMA_ENABLE_REG register according to Table 17-1 below.

Table 17-1. AES Accelerator Working Mode

AES_DMA_ENABLE_REG	Working Mode
0	Typical AES
1	DMA-AES

Users can choose the length of cryptographic keys and encryption / decryption by configuring the AES_MODE_REG register according to Table 17-2 below.

Table 17-2. Key Length and Encryption / Decryption

AES_MODE_REG[2:0]	Key Length and Encryption / Decryption
0	AES-128 encryption
1	reserved
2	AES-256 encryption
3	reserved
4	AES-128 decryption
5	reserved
6	AES-256 decryption
7	reserved

For detailed introduction on these two working modes, please refer to Section 17.4 and Section 17.5 below.

Notice: ESP32-S3's Digital Signature (DS) module will call the AES accelerator. Therefore, users cannot access the AES accelerator when Digital Signature (DS) module is working.

17.4 Typical AES Working Mode

In the Typical AES working mode, users can check the working status of the AES accelerator by inquiring the AES_STATE_REG register and comparing the return value against the Table 17-3 below.

Table 17-3. Working Status under Typical AES Working Mode

AES_STATE_REG	Status	Description
0	IDLE	The AES accelerator is idle or completed operation.
1	WORK	The AES accelerator is in the middle of an operation.

17.4.1 Key, Plaintext, and Ciphertext

The encryption or decryption key is stored in AES_KEY_*n*_REG, which is a set of eight 32-bit registers.

- For AES-128 encryption/decryption, the 128-bit key is stored in AES_KEY_0_REG ~ AES_KEY_3_REG.
- For AES-256 encryption/decryption, the 256-bit key is stored in AES_KEY_0_REG ~ AES_KEY_7_REG.

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The plaintext and ciphertext are stored in AES_TEXT_IN_*m*_REG and AES_TEXT_OUT_*m*_REG, which are two sets of four 32-bit registers.

- For AES-128/AES-256 encryption, the AES_TEXT_IN_*m*_REG registers are initialized with plaintext. Then, the AES Accelerator stores the ciphertext into AES_TEXT_OUT_*m*_REG after operation.
- For AES-128/AES-256 decryption, the AES_TEXT_IN_*m*_REG registers are initialized with ciphertext. Then, the AES Accelerator stores the plaintext into AES_TEXT_OUT_*m*_REG after operation.

17.4.2 Endianness

Text Endianness

In Typical AES working mode, the AES Accelerator uses cryptographic keys to encrypt and decrypt data in blocks of 128 bits. When filling data into AES_TEXT_IN_*m*_REG register or reading result from AES_TEXT_OUT_*m*_REG registers, users should follow the text endianness type specified in Table 17-4.

Table 17-4. Text Endianness Type for Typical AES

Plaintext/Ciphertext					
State[1]		c[2]			
		0	1	2	3
r	0	AES_TEXT_*x*_0_REG[7:0]	AES_TEXT_*x*_1_REG[7:0]	AES_TEXT_*x*_2_REG[7:0]	AES_TEXT_*x*_3_REG[7:0]
	1	AES_TEXT_*x*_0_REG[15:8]	AES_TEXT_*x*_1_REG[15:8]	AES_TEXT_*x*_2_REG[15:8]	AES_TEXT_*x*_3_REG[15:8]
	2	AES_TEXT_*x*_0_REG[23:16]	AES_TEXT_*x*_1_REG[23:16]	AES_TEXT_*x*_2_REG[23:16]	AES_TEXT_*x*_3_REG[23:16]
	3	AES_TEXT_*x*_0_REG[31:24]	AES_TEXT_*x*_1_REG[31:24]	AES_TEXT_*x*_2_REG[31:24]	AES_TEXT_*x*_3_REG[31:24]

[1] The definition of "State (including c and r)" is described in Section 3.4 The State in NIST FIPS 197.

[2] Where *x* = IN or OUT.

Key Endianness

In Typical AES working mode, When filling key into AES_KEY_*m*_REG registers, users should follow the key endianness type specified in Table 17-5 and Table 17-6.

Table 17-5. Key Endianness Type for AES-128 Encryption and Decryption

Bit[1]	w[0]	w[1]	w[2]	w[3][2]
[31:24]	AES_KEY_0_REG[7:0]	AES_KEY_1_REG[7:0]	AES_KEY_2_REG[7:0]	AES_KEY_3_REG[7:0]
[23:16]	AES_KEY_0_REG[15:8]	AES_KEY_1_REG[15:8]	AES_KEY_2_REG[15:8]	AES_KEY_3_REG[15:8]
[15:8]	AES_KEY_0_REG[23:16]	AES_KEY_1_REG[23:16]	AES_KEY_2_REG[23:16]	AES_KEY_3_REG[23:16]
[7:0]	AES_KEY_0_REG[31:24]	AES_KEY_1_REG[31:24]	AES_KEY_2_REG[31:24]	AES_KEY_3_REG[31:24]

[1] Column "Bit" specifies the bytes of each word stored in w[0] ~ w[3].

[2] w[0] ~ w[3] are "the first Nk words of the expanded key" as specified in Section 5.2 Key Expansion in NIST FIPS 197.

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Table 17-6. Key Endianness Type for AES-256 Encryption and Decryption

Bit[1]	w[0]	w[1]	w[2]	w[3]	w[4]	w[5]	w[6]	w[7][2]
[31:24]	AES_KEY_0_REG[7:0]	AES_KEY_1_REG[7:0]	AES_KEY_2_REG[7:0]	AES_KEY_3_REG[7:0]	AES_KEY_4_REG[7:0]	AES_KEY_5_REG[7:0]	AES_KEY_6_REG[7:0]	AES_KEY_7_REG[7:0]
[23:16]	AES_KEY_0_REG[15:8]	AES_KEY_1_REG[15:8]	AES_KEY_2_REG[15:8]	AES_KEY_3_REG[15:8]	AES_KEY_4_REG[15:8]	AES_KEY_5_REG[15:8]	AES_KEY_6_REG[15:8]	AES_KEY_7_REG[15:8]
[15:8]	AES_KEY_0_REG[23:16]	AES_KEY_1_REG[23:16]	AES_KEY_2_REG[23:16]	AES_KEY_3_REG[23:16]	AES_KEY_4_REG[23:16]	AES_KEY_5_REG[23:16]	AES_KEY_6_REG[23:16]	AES_KEY_7_REG[23:16]
[7:0]	AES_KEY_0_REG[31:24]	AES_KEY_1_REG[31:24]	AES_KEY_2_REG[31:24]	AES_KEY_3_REG[31:24]	AES_KEY_4_REG[31:24]	AES_KEY_5_REG[31:24]	AES_KEY_6_REG[31:24]	AES_KEY_7_REG[31:24]

[1] Column “Bit” specifies the bytes of each word stored in w[0] ~ w[7].

[2] w[0] ~ w[7] are “the first Nk words of the expanded key” as specified in Chapter 5.2 Key Expansion in NIST FIPS 197.

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17.4.3 Operation Process

Single Operation

1. Write 0 to the AES_DMA_ENABLE_REG register.
2. Initialize registers AES_MODE_REG, AES_KEY_*n*_REG, AES_TEXT_IN_*m*_REG.
3. Start operation by writing 1 to the AES_TRIGGER_REG register.
4. Wait till the content of the AES_STATE_REG register becomes 0, which indicates the operation is completed.
5. Read results from the AES_TEXT_OUT_*m*_REG register.

Consecutive Operations

In consecutive operations, primarily the input AES_TEXT_IN_*m*_REG and output AES_TEXT_OUT_*m*_REG registers are being written and read, while the content of AES_DMA_ENABLE_REG, AES_MODE_REG, AES_KEY_*n*_REG is kept unchanged. Therefore, the initialization can be simplified during the consecutive operation.

1. Write 0 to the AES_DMA_ENABLE_REG register before starting the first operation.
2. Initialize registers AES_MODE_REG and AES_KEY_*n*_REG before starting the first operation.
3. Update the content of AES_TEXT_IN_*m*_REG.
4. Start operation by writing 1 to the AES_TRIGGER_REG register.
5. Wait till the content of the AES_STATE_REG register becomes 0, which indicates the operation completes.
6. Read results from the AES_TEXT_OUT_*m*_REG register, and return to Step 3 to continue the next operation.

17.5 DMA-AES Working Mode

In the DMA-AES working mode, the AES accelerator supports six block cipher modes including ECB/CBC/OFB/CTR/CFB8/CFB128. Users can choose the block cipher mode by configuring the AES_BLOCK_MODE_REG register according to Table 17-7 below.

Table 17-7. Block Cipher Mode

AES_BLOCK_MODE_REG[2:0]	Block Cipher Mode
0	ECB (Electronic Codebook)
1	CBC (Cipher Block Chaining)
2	OFB (Output Feedback)
3	CTR (Counter)
4	CFB8 (8-bit Cipher Feedback)
5	CFB128 (128-bit Cipher Feedback)
6	reserved
7	reserved

Users can check the working status of the AES accelerator by inquiring the AES_STATE_REG register and comparing the return value against the Table 17-8 below.

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Table 17-8. Working Status under DMA-AES Working mode

AES_STATE_REG[1:0]	Status	Description
0	IDLE	The AES accelerator is idle.
1	WORK	The AES accelerator is in the middle of an operation.
2	DONE	The AES accelerator completed operations.

When working in the DMA-AES working mode, the AES accelerator supports interrupt on the completion of computation. To enable this function, write 1 to the AES_INT_ENA_REG register. By default, the interrupt function is disabled. Also, note that the interrupt should be cleared by software after use.

17.5.1 Key, Plaintext, and Ciphertext

Block Operation

During the block operations, the AES Accelerator reads source data from DMA, and write result data to DMA after the computation.

- For encryption, DMA reads plaintext from memory, then passes it to AES as source data. After computation, AES passes ciphertext as result data back to DMA to write into memory.
- For decryption, DMA reads ciphertext from memory, then passes it to AES as source data. After computation, AES passes plaintext as result data back to DMA to write into memory.

During block operations, the lengths of the source data and result data are the same. The total computation time is reduced because the DMA data operation and AES computation can happen concurrently.

The length of source data for AES Accelerator under DMA-AES working mode must be 128 bits or the integral multiples of 128 bits. Otherwise, trailing zeros will be added to the original source data, so the length of source data equals to the nearest integral multiples of 128 bits. Please see details in Table 17-9 below.

Table 17-9. TEXT-PADDING

Function : TEXT-PADDING( )
Input : X, bit string. **Output** : Y = **TEXT-PADDING**(X), whose length is the nearest integral multiples of 128 bits.
Steps Let us assume that X is a data-stream that can be split into n parts as following: $X = X_1 \| \| X_2 \| \| \cdots \| \| X_{n-1} \| \| X_n$ Here, the lengths of $X_1, X_2, \cdots, X_{n-1}$ all equal to 128 bits, and the length of X_n is t (0<=t<=127). If $t = 0$, then **TEXT-PADDING**(X) = X; If $0 < t <= 127$, define a 128-bit block, X_n^*, and let $X_n^* = X_n \| \| 0^{128-t}$, then **TEXT-PADDING**($X$) = $X_1 \| \| X_2 \| \| \cdots \| \| X_{n-1} \| \| X_n^*$ = $X \| \| 0^{128-t}$

17.5.2 Endianness

Under the DMA-AES working mode, the transmission of source data and result data for AES Accelerator is solely controlled by DMA. Therefore, the AES Accelerator cannot control the Endianness of the source data and result

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data, but does have requirement on how these data should be stored in memory and on the length of the data.

For example, let us assume DMA needs to write the following data into memory at address 0x0280.

- Data represented in hexadecimal:
  - 0102030405060708090A0B0C0D0E0F101112131415161718191A1B1C1D1E1F20
- Data Length:
  - Equals to 2 blocks.

Then, this data will be stored in memory as shown in Table 17-10 below.

Table 17-10. Text Endianness for DMA-AES

Address	Byte	Address	Byte	Address	Byte	Address	Byte
0x0280	0x01	0x0281	0x02	0x0282	0x03	0x0283	0x04
0x0284	0x05	0x0285	0x06	0x0286	0x07	0x0287	0x08
0x0288	0x09	0x0289	0x0A	0x028A	0x0B	0x028B	0x0C
0x028C	0x0D	0x028D	0x0E	0x028E	0x0F	0x028F	0x10
0x0290	0x11	0x0291	0x12	0x0292	0x13	0x0293	0x14
0x0294	0x15	0x0295	0x16	0x0296	0x17	0x0297	0x18
0x0298	0x19	0x0299	0x1A	0x029A	0x1B	0x029B	0x1C
0x029C	0x1D	0x029D	0x1E	0x029E	0x1F	0x029F	0x20

DMA can access both internal memory and PSRAM outside ESP32-S3. When you use DMA to access external PSRAM, please use base addresses that meet the requirements for DMA. When you use DMA to access internal memory, base addresses do not have such requirements. Details can be found in Chapter 2 *GDMA Controller (GDMA)*.

17.5.3 Standard Incrementing Function

AES accelerator provides two Standard Incrementing Functions for the CTR block operation, which are INC_{32} and INC_{128} Standard Incrementing Functions. By setting the AES_INC_SEL_REG register to 0 or 1, users can choose the INC_{32} or INC_{128} functions respectively. For details on the Standard Incrementing Function, please see Chapter B.1 The Standard Incrementing Function in NIST SP 800-38A.

17.5.4 Block Number

Register AES_BLOCK_NUM_REG stores the Block Number of plaintext P or ciphertext C. The length of this register equals to length(**TEXT-PADDING**(P))/128 or length(**TEXT-PADDING**(C))/128. The AES Accelerator only uses this register when working in the DMA-AES mode.

17.5.5 Initialization Vector

AES_IV_MEM is a 16-byte memory, which is only available for AES Accelerator working in block operations. For CBC/OFB/CFB8/CFB128 operations, the AES_IV_MEM memory stores the Initialization Vector (IV). For the CTR operation, the AES_IV_MEM memory stores the Initial Counter Block (ICB).

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Both IV and ICB are 128-bit strings, which can be divided into Byte0, Byte1, Byte2 ⋯ Byte15 (from left to right). AES_IV_MEM stores data following the Endianness pattern presented in Table 17-10, i.e. the most significant (i.e., left-most) byte Byte0 is stored at the lowest address while the least significant (i.e., right-most) byte Byte15 at the highest address.

For more details on IV and ICB, please refer to NIST SP 800-38A.

17.5.6 Block Operation Process

1. Select one of DMA channels to connect with AES, configure the DMA chained list, and then start DMA. For details, please refer to Chapter 2 *GDMA Controller (GDMA)*.
2. Initialize the AES accelerator-related registers:
   - Write 1 to the AES_DMA_ENABLE_REG register.
   - Configure the AES_INT_ENA_REG register to enable or disable the interrupt function.
   - Initialize registers AES_MODE_REG and AES_KEY_*n*_REG.
   - Select block cipher mode by configuring the AES_BLOCK_MODE_REG register. For details, see Table 17-7.
   - Initialize the AES_BLOCK_NUM_REG register. For details, see Section 17.5.4.
   - Initialize the AES_INC_SEL_REG register (only needed when AES Accelerator is working under CTR block operation).
   - Initialize the AES_IV_MEM memory (This is always needed except for ECB block operation).
3. Start operation by writing 1 to the AES_TRIGGER_REG register.
4. Wait for the completion of computation, which happens when the content of AES_STATE_REG becomes 2 or the AES interrupt occurs.
5. Check if DMA completes data transmission from AES to memory. At this time, DMA had already written the result data in memory, which can be accessed directly. For details on DMA, please refer to Chapter 2 *GDMA Controller (GDMA)*.
6. Clear interrupt by writing 1 to the AES_INT_CLR_REG register, if any AES interrupt occurred during the computation.
7. Release the AES Accelerator by writing 0 to the AES_DMA_EXIT_REG register. After this, the content of the AES_STATE_REG register becomes 0. Note that, you can release DMA earlier, but only after Step 4 is completed.

17.6 Memory Summary

The addresses in this section are relative to the AES accelerator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Size (byte)	Starting Address	Ending Address	Access
AES_IV_MEM	Memory IV	16 bytes	0x0050	0x005F	R/W

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17.7 Register Summary

The addresses in this section are relative to the AES accelerator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

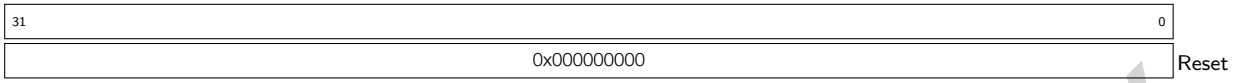
Name	Description	Address	Access
Key Registers			
AES_KEY_0_REG	AES key register 0	0x0000	R/W
AES_KEY_1_REG	AES key register 1	0x0004	R/W
AES_KEY_2_REG	AES key register 2	0x0008	R/W
AES_KEY_3_REG	AES key register 3	0x000C	R/W
AES_KEY_4_REG	AES key register 4	0x0010	R/W
AES_KEY_5_REG	AES key register 5	0x0014	R/W
AES_KEY_6_REG	AES key register 6	0x0018	R/W
AES_KEY_7_REG	AES key register 7	0x001C	R/W
TEXT_IN Registers			
AES_TEXT_IN_0_REG	Source data register 0	0x0020	R/W
AES_TEXT_IN_1_REG	Source data register 1	0x0024	R/W
AES_TEXT_IN_2_REG	Source data register 2	0x0028	R/W
AES_TEXT_IN_3_REG	Source data register 3	0x002C	R/W
TEXT_OUT Registers			
AES_TEXT_OUT_0_REG	Result data register 0	0x0030	RO
AES_TEXT_OUT_1_REG	Result data register 1	0x0034	RO
AES_TEXT_OUT_2_REG	Result data register 2	0x0038	RO
AES_TEXT_OUT_3_REG	Result data register 3	0x003C	RO
Configuration Registers			
AES_MODE_REG	Defines key length and encryption / decryption	0x0040	R/W
AES_DMA_ENABLE_REG	Selects the working mode of the AES accelerator	0x0090	R/W
AES_BLOCK_MODE_REG	Defines the block cipher mode	0x0094	R/W
AES_BLOCK_NUM_REG	Block number configuration register	0x0098	R/W
AES_INC_SEL_REG	Standard incrementing function register	0x009C	R/W
Controlling / Status Registers			
AES_TRIGGER_REG	Operation start controlling register	0x0048	WO
AES_STATE_REG	Operation status register	0x004C	RO
AES_DMA_EXIT_REG	Operation exit controlling register	0x00B8	WO
Interruption Registers			
AES_INT_CLR_REG	DMA-AES interrupt clear register	0x00AC	WO
AES_INT_ENA_REG	DMA-AES interrupt enable register	0x00B0	R/W

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17.8 Registers

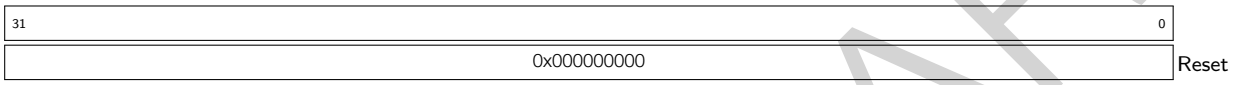
The addresses in this section are relative to the AES accelerator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 17.1. AES_KEY_*n*_REG (*n*: 0-7) (0x0000+4n*)**



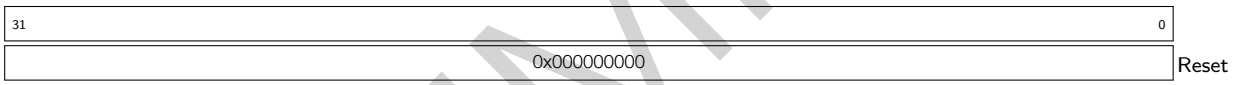
AES_KEY_*n*_REG (*n*: 0-7) Stores AES keys. (R/W)

Register 17.2. AES_TEXT_IN_*m*_REG (*m*: 0-3) (0x0020+4m*)**



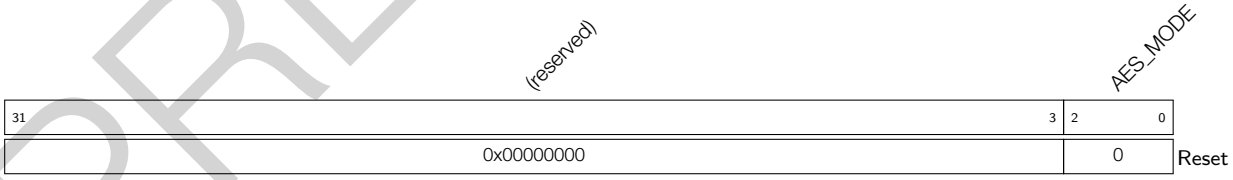
AES_TEXT_IN_*m*_REG (*m*: 0-3) Stores the source data when the AES Accelerator operates in the Typical AES working mode. (R/W)

Register 17.3. AES_TEXT_OUT_*m*_REG (*m*: 0-3) (0x0030+4m*)**



AES_TEXT_OUT_*m*_REG (*m*: 0-3) Stores the result data when the AES Accelerator operates in the Typical AES working mode. (RO)

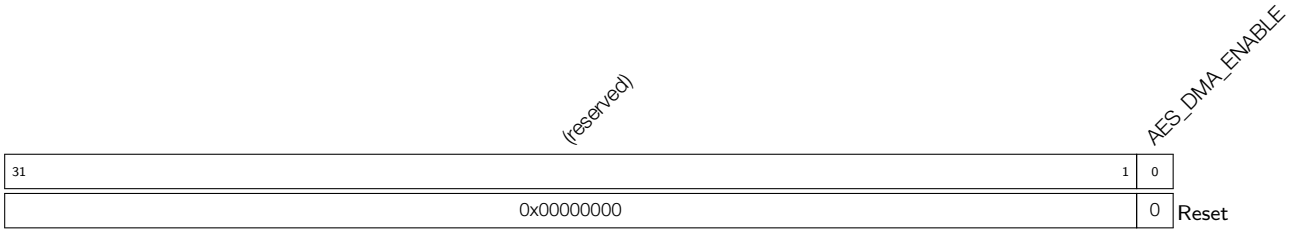
Register 17.4. AES_MODE_REG (0x0040)



AES_MODE Defines the key length and encryption / decryption of the AES Accelerator. For details, see Table 17-2. (R/W)

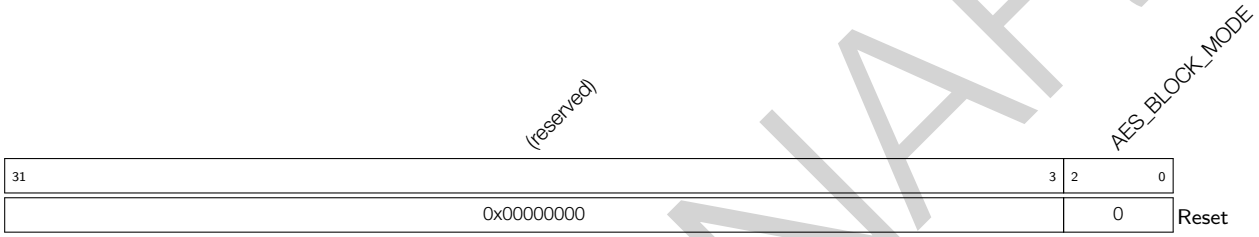
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Register 17.5. AES_DMA_ENABLE_REG (0x0090)



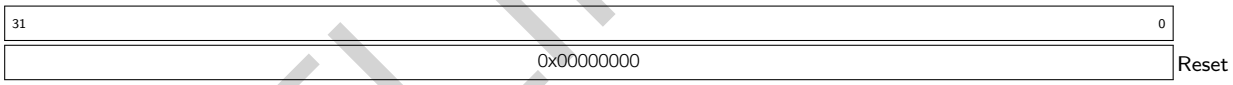
AES_DMA_ENABLE Defines the working mode of the AES Accelerator. 0: Typical AES, 1: DMA-AES. For details, see Table 17-1. (R/W)

Register 17.6. AES_BLOCK_MODE_REG (0x0094)



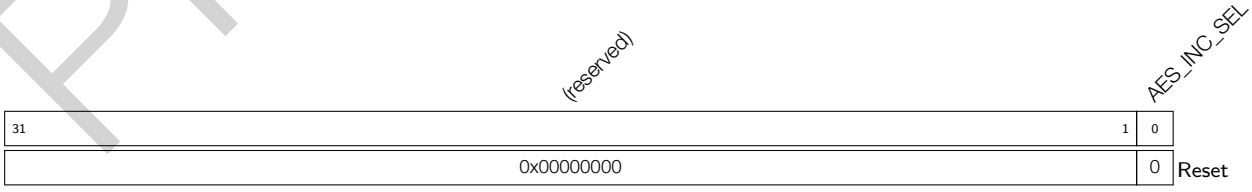
AES_BLOCK_MODE Defines the block cipher mode of the AES Accelerator operating under the DMA-AES working mode. For details, see Table 17-7. (R/W)

Register 17.7. AES_BLOCK_NUM_REG (0x0098)



AES_BLOCK_NUM Stores the Block Number of plaintext or ciphertext when the AES Accelerator operates under the DMA-AES working mode. For details, see Section 17.5.4. (R/W)

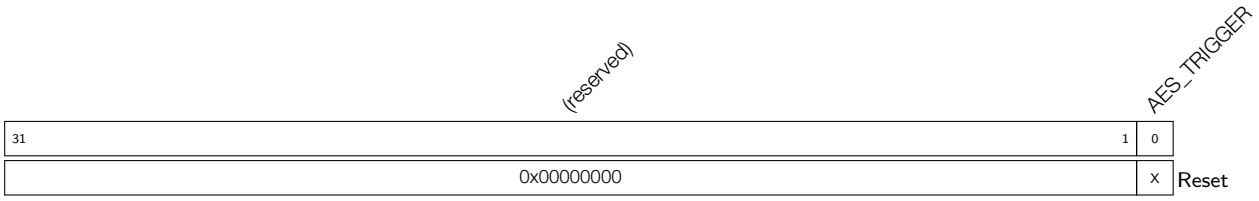
Register 17.8. AES_INC_SEL_REG (0x009C)



AES_INC_SEL Defines the Standard Incrementing Function for CTR block operation. Set this bit to 0 or 1 to choose INC_{32} or INC_{128}. (R/W)

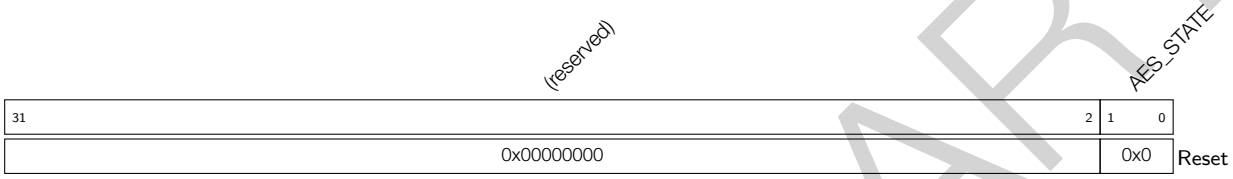
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Register 17.9. AES_TRIGGER_REG (0x0048)



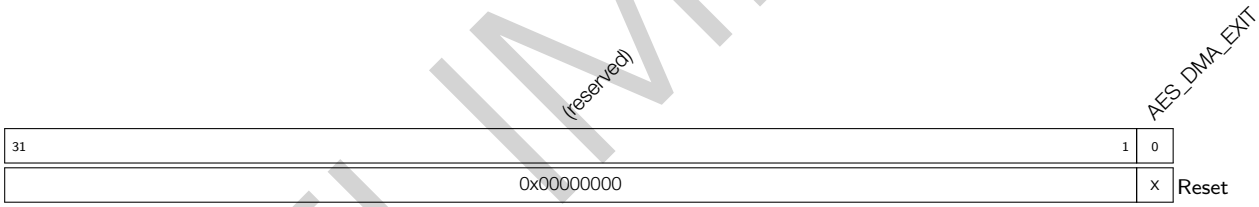
AES_TRIGGER Set this bit to 1 to start AES operation. (WO)

Register 17.10. AES_STATE_REG (0x004C)



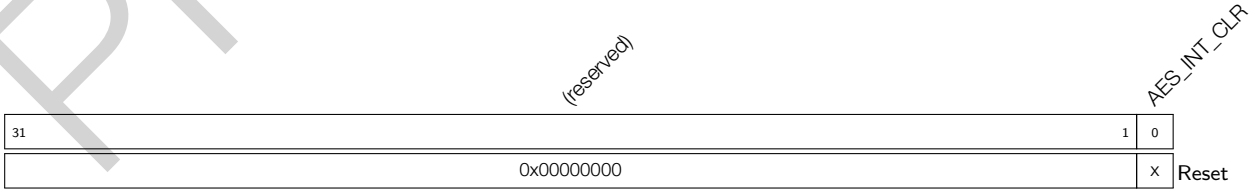
AES_STATE Stores the working status of the AES Accelerator. For details, see Table 17-3 for Typical AES working mode and Table 17-8 for DMA AES working mode. (RO)

Register 17.11. AES_DMA_EXIT_REG (0x00B8)



AES_DMA_EXIT Set this bit to 1 to exit AES operation. This register is only effective for DMA-AES operation. (WO)

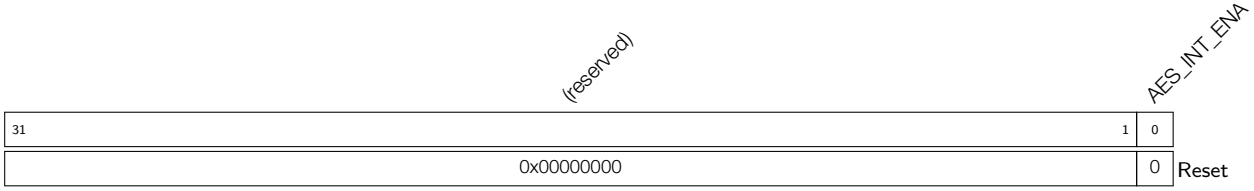
Register 17.12. AES_INT_CLR_REG (0x00AC)



AES_INT_CLR Set this bit to 1 to clear AES interrupt. (WO)

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Register 17.13. AES_INT_ENA_REG (0x00B0)



AES_INT_ENA Set this bit to 1 to enable AES interrupt and 0 to disable interrupt. (R/W)

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18 RSA Accelerator (RSA)

18.1 Introduction

The RSA Accelerator provides hardware support for high precision computation used in various RSA asymmetric cipher algorithms by significantly reducing their software complexity. Compared with RSA algorithms implemented solely in software, this hardware accelerator can speed up RSA algorithms significantly. Besides, the RSA Accelerator also supports operands of different lengths, which provides more flexibility during the computation.

18.2 Features

The following functionality is supported:

- Large-number modular exponentiation with two optional acceleration options
- Large-number modular multiplication
- Large-number multiplication
- Operands of different lengths
- Interrupt on completion of computation

18.3 Functional Description

The RSA Accelerator is activated by setting the SYSTEM_CRYPTO_RSA_CLK_EN bit in the SYSTEM_PERIP_CLK_EN1_REG register and clearing the SYSTEM_RSA_MEM_PD bit in the SYSTEM_RSA_PD_CTRL_REG register. This releases the RSA Accelerator from reset.

The RSA Accelerator is only available after the RSA-related memories are initialized. The content of the RSA_CLEAN_REG register is 0 during initialization and will become 1 after the initialization is done. Therefore, it is advised to wait until RSA_CLEAN_REG becomes 1 before using the RSA Accelerator.

The RSA_INTERRUPT_ENA_REG register is used to control the interrupt triggered on completion of computation. Write 1 or 0 to this register to enable or disable interrupt. By default, the interrupt function of the RSA Accelerator is enabled.

Notice:

ESP32-S3's Digital Signature (DS) module also calls the RSA accelerator. Therefore, users cannot access the RSA accelerator when Digital Signature (DS) is working.

18.3.1 Large Number Modular Exponentiation

Large-number modular exponentiation performs $Z = X^Y \bmod M$. The computation is based on Montgomery multiplication. Therefore, aside from the X, Y, and M arguments, two additional ones are needed — $\overline{r}$ and M', which need to be calculated in advance by software.

RSA Accelerator supports operands of length $N = 32 \times x$, where $x \in \{1, 2, 3, \ldots, 128\}$. The bit lengths of arguments Z, X, Y, M, and $\overline{r}$ can be arbitrary N, but all numbers in a calculation must be of the same length.

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The bit length of M' must be 32.

To represent the numbers used as operands, let us define a base-b positional notation, as follows:

$$b = 2^{32}$$

Using this notation, each number is represented by a sequence of base-b digits:

$$n = \frac{N}{32}$$
$$Z = (Z_{n-1}Z_{n-2}\cdots Z_0)_b$$
$$X = (X_{n-1}X_{n-2}\cdots X_0)_b$$
$$Y = (Y_{n-1}Y_{n-2}\cdots Y_0)_b$$
$$M = (M_{n-1}M_{n-2}\cdots M_0)_b$$
$$\overline{r} = (\overline{r}_{n-1}\overline{r}_{n-2}\cdots \overline{r}_0)_b$$

Each of the n values in $Z_{n-1}\cdots Z_0$, $X_{n-1}\cdots X_0$, $Y_{n-1}\cdots Y_0$, $M_{n-1}\cdots M_0$, $\overline{r}_{n-1}\cdots \overline{r}_0$ represents one base-b digit (a 32-bit word).

Z_{n-1}, X_{n-1}, Y_{n-1}, M_{n-1} and $\overline{r}_{n-1}$ are the most significant bits of Z, X, Y, M, while Z_0, X_0, Y_0, M_0 and $\overline{r}_0$ are the least significant bits.

If we define $R = b^n$, the additional arguments can be calculated as $\overline{r} = R^2 \bmod M$.

The following equation in the form compatible with the extended binary GCD algorithm can be written as

$$M^{-1} \times M + 1 = R \times R^{-1}$$
$$M' = M^{-1} \bmod b$$

Large-number modular exponentiation can be implemented as follows:

1. Write 1 or 0 to the RSA_INTERRUPT_ENA_REG register to enable or disable the interrupt function.
2. Configure relevant registers:
   (a) Write $(\frac{N}{32} - 1)$ to the RSA_MODE_REG register.
   (b) Write M' to the RSA_M_PRIME_REG register.
   (c) Configure registers related to the acceleration options, which are described later in Section 18.3.4.
3. Write X_i, Y_i, M_i and $\overline{r}_i$ for $i \in \{0, 1, \ldots, n-1\}$ to memory blocks RSA_X_MEM, RSA_Y_MEM, RSA_M_MEM and RSA_Z_MEM. The capacity of each memory block is 128 words. Each word of each memory block can store one base-b digit. The memory blocks use the little endian format for storage, i.e. the least significant digit of each number is in the lowest address.

   Users need to write data to each memory block only according to the length of the number; data beyond this length are ignored.
4. Write 1 to the RSA_MODEXP_START_REG register to start computation.
5. Wait for the completion of computation, which happens when the content of RSA_IDLE_REG becomes 1 or the RSA interrupt occurs.

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6. Read the result Z_i for $i \in \{0, 1, \ldots, n-1\}$ from RSA_Z_MEM.
7. Write 1 to RSA_CLEAR_INTERRUPT_REG to clear the interrupt, if you have enabled the interrupt function.

After the computation, the RSA_MODE_REG register, memory blocks RSA_Y_MEM and RSA_M_MEM, as well as the RSA_M_PRIME_REG remain unchanged. However, X_i in RSA_X_MEM and $\overline{r}_i$ in RSA_Z_MEM computation are overwritten, and only these overwritten memory blocks need to be re-initialized before starting another computation.

18.3.2 Large Number Modular Multiplication

Large-number modular multiplication performs $Z = X \times Y \bmod M$. This computation is based on Montgomery multiplication. Therefore, similar to the large number modular exponentiation, two additional arguments are needed – $\overline{r}$ and M', which need to be calculated in advance by software.

The RSA Accelerator supports large-number modular multiplication with operands of 128 different lengths.

The computation can be executed as follows:

1. Write 1 or 0 to the RSA_INTERRUPT_ENA_REG register to enable or disable the interrupt function.
2. Configure relevant registers:
   (a) Write $(\frac{N}{32} - 1)$ to the RSA_MODE_REG register.
   (b) Write M' to the RSA_M_PRIME_REG register.
3. Write X_i, Y_i, M_i, and $\overline{r}_i$ for $i \in \{0, 1, \ldots, n-1\}$ to memory blocks RSA_X_MEM, RSA_Y_MEM, RSA_M_MEM and RSA_Z_MEM. The capacity of each memory block is 128 words. Each word of each memory block can store one base-b digit. The memory blocks use the little endian format for storage, i.e. the least significant digit of each number is in the lowest address.

   Users need to write data to each memory block only according to the length of the number; data beyond this length are ignored.
4. Write 1 to the RSA_MODMULT_START_REG register.
5. Wait for the completion of computation, which happens when the content of RSA_IDLE_REG becomes 1 or the RSA interrupt occurs.
6. Read the result Z_i for $i \in \{0, 1, \ldots, n-1\}$ from RSA_Z_MEM.
7. Write 1 to RSA_CLEAR_INTERRUPT_REG to clear the interrupt, if you have enabled the interrupt function.

After the computation, the length of operands in RSA_MODE_REG, the X_i in memory RSA_X_MEM, the Y_i in memory RSA_Y_MEM, the M_i in memory RSA_M_MEM, and the M' in memory RSA_M_PRIME_REG remain unchanged. However, the $\overline{r}_i$ in memory RSA_Z_MEM has already been overwritten, and only this overwritten memory block needs to be re-initialized before starting another computation.

18.3.3 Large Number Multiplication

Large-number multiplication performs $Z = X \times Y$. The length of result Z is twice that of operand X and operand Y. Therefore, the RSA Accelerator only supports Large Number Multiplication with operand length $N = 32 \times x$, where $x \in \{1, 2, 3, \ldots, 64\}$. The length $\hat{N}$ of result Z is $2 \times N$.

The computation can be executed as follows:

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1. Write 1 or 0 to the RSA_INTERRUPT_ENA_REG register to enable or disable the interrupt function.
2. Write $(\frac{\hat{N}}{32} - 1)$, i.e. $(\frac{N}{16} - 1)$ to the RSA_MODE_REG register.
3. Write X_i and Y_i for $\in \{0, 1, \ldots, n-1\}$ to memory blocks RSA_X_MEM and RSA_Z_MEM. The capacity of each memory block is 64 words. Each word of each memory block can store one base-b digit. The memory blocks use the little endian format for storage, i.e. the least significant digit of each number is in the lowest address. n is $\frac{N}{32}$.

   Write X_i for $i \in \{0, 1, \ldots, n-1\}$ to the address of the i words of the RSA_X_MEM memory block. Note that Y_i for $i \in \{0, 1, \ldots, n-1\}$ will not be written to the address of the i words of the RSA_Z_MEM register, but the address of the $n+i$ words, i.e. the base address of the RSA_Z_MEM memory plus the address offset $4 \times (n+i)$.

   Users need to write data to each memory block only according to the length of the number; data beyond this length are ignored.
4. Write 1 to the RSA_MULT_START_REG register.
5. Wait for the completion of computation, which happens when the content of RSA_IDLE_REG becomes 1 or the RSA interrupt occurs.
6. Read the result Z_i for $i \in \{0, 1, \ldots, \hat{n}-1\}$ from the RSA_Z_MEM register. $\hat{n}$ is $2 \times n$.
7. Write 1 to RSA_CLEAR_INTERRUPT_REG to clear the interrupt, if you have enabled the interrupt function.

After the computation, the length of operands in RSA_MODE_REG and the X_i in memory RSA_X_MEM remain unchanged. However, the Y_i in memory RSA_Z_MEM has already been overwritten, and only this overwritten memory block needs to be re-initialized before starting another computation.

18.3.4 Options for Acceleration

The ESP32-S3 RSA accelerator also provides SEARCH and CONSTANT_TIME options that can be configured to accelerate the large-number modular exponentiation. By default, both options are configured for no acceleration. Users can choose to use one or two of these options to accelerate the computation.

To be more specific, when neither of these two options are configured for acceleration, the time required to calculate $Z = X^Y \bmod M$ is solely determined by the lengths of operands. When either or both of these two options are configured for acceleration, the time required is also correlated with the 0/1 distribution of Y.

To better illustrate how these two options work, first assume Y is represented in binaries as

$$Y = (\widetilde{Y}_{N-1}\widetilde{Y}_{N-2}\cdots\widetilde{Y}_{t+1}\widetilde{Y}_t\widetilde{Y}_{t-1}\cdots\widetilde{Y}_0)_2$$

where,

- N is the length of Y,
- $\widetilde{Y}_t$ is 1,
- $\widetilde{Y}_{N-1}$, $\widetilde{Y}_{N-2}$, ..., $\widetilde{Y}_{t+1}$ are all equal to 0,
- and $\widetilde{Y}_{t-1}$, $\widetilde{Y}_{t-2}$, ..., $\widetilde{Y}_0$ are either 0 or 1 but exactly m bits should be equal to 0 and t-m bits 1, i.e. the Hamming weight of $\widetilde{Y}_{t-1}\widetilde{Y}_{t-2}, \cdots, \widetilde{Y}_0$ is $t - m$.

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When either of these two options is configured for acceleration:

- SEARCH Option (Configuring RSA_SEARCH_ENABLE to 1 for acceleration)
  - The accelerator ignores the bit positions of $\widetilde{Y}_i$, where $i > \alpha$. Search position α is set by configuring the RSA_SEARCH_POS_REG register. The maximum value of α is N-1, which leads to the same result when this option is not used for acceleration. The best acceleration performance can be achieved by setting α to t, in which case, all the $\widetilde{Y}_{N-1}$, $\widetilde{Y}_{N-2}$, ..., $\widetilde{Y}_{t+1}$ of 0s are ignored during the calculation. Note that if you set α to be less than t, then the result of the modular exponentiation $Z = X^Y \bmod M$ will be incorrect.
- CONSTANT_TIME Option (Configuring RSA_CONSTANT_TIME_REG to 0 for acceleration)
  - The accelerator speeds up the calculation by simplifying the calculation concerning the 0 bits of Y. Therefore, the higher the proportion of bits 0 against bits 1, the better the acceleration performance is.

We provide an example to demonstrate the performance of the RSA Accelerator under different combinations of SEARCH and CONSTANT_TIME configuration. Here we perform $Z = X^Y \bmod M$ with N = 3072 and Y = 65537. Table 18-1 below demonstrates the time costs under different combinations of SEARCH and CONSTANT_TIME configuration. Here, we should also mention that, α is set to 16 when the SEARCH option is enabled.

Table 18-1. Acceleration Performance

SEARCH Option	CONSTANT_TIME Option	Time Cost (ms)
No acceleration	No acceleration	752.81
Accelerated	No acceleration	4.52
No acceleration	Acceleration	2.406
Acceleration	Acceleration	2.33

It's obvious that:

- The time cost is the biggest when none of these two options is configured for acceleration.
- The time cost is the smallest when both of these two options are configured for acceleration.
- The time cost can be dramatically reduced when either or both option(s) are configured for acceleration.

18.4 Memory Summary

The addresses in this section are relative to the RSA accelerator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Table 18-2. RSA Accelerator Memory Blocks

Name	Description	Size (byte)	Starting Address	Ending Address	Access
RSA_M_MEM	Memory M	512	0x0000	0x01FF	WO
RSA_Z_MEM	Memory Z	512	0x0200	0x03FF	R/W
RSA_Y_MEM	Memory Y	512	0x0400	0x05FF	WO
RSA_X_MEM	Memory X	512	0x0600	0x07FF	WO

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18.5 Register Summary

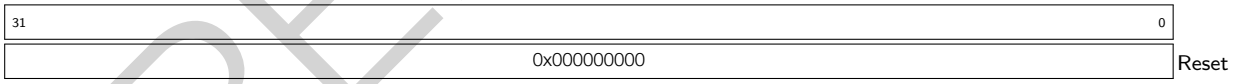
The addresses in this section are relative to the RSA accelerator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
Configuration Registers			
RSA_M_PRIME_REG	Register to store M'	0x0800	R/W
RSA_MODE_REG	RSA length mode	0x0804	R/W
RSA_CONSTANT_TIME_REG	The constant_time option	0x0820	R/W
RSA_SEARCH_ENABLE_REG	The search option	0x0824	R/W
RSA_SEARCH_POS_REG	The search position	0x0828	R/W
Status/Control Registers			
RSA_CLEAN_REG	RSA clean register	0x0808	RO
RSA_MODEXP_START_REG	Modular exponentiation starting bit	0x080C	WO
RSA_MODMULT_START_REG	Modular multiplication starting bit	0x0810	WO
RSA_MULT_START_REG	Normal multiplication starting bit	0x0814	WO
RSA_IDLE_REG	RSA idle register	0x0818	RO
Interrupt Registers			
RSA_CLEAR_INTERRUPT_REG	RSA clear interrupt register	0x081C	WO
RSA_INTERRUPT_ENA_REG	RSA interrupt enable register	0x082C	R/W
Version Register			
RSA_DATE_REG	Version control register	0x0830	R/W

18.6 Registers

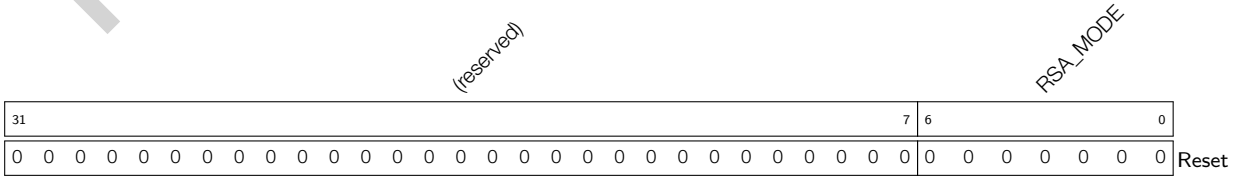
The addresses in this section are relative to the RSA accelerator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 18.1. RSA_M_PRIME_REG (0x0800)



RSA_M_PRIME_REG Stores M'.(R/W)

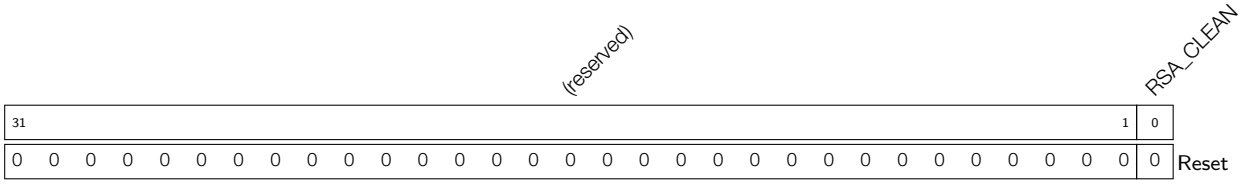
Register 18.2. RSA_MODE_REG (0x0804)



RSA_MODE Stores the mode of modular exponentiation. (R/W)

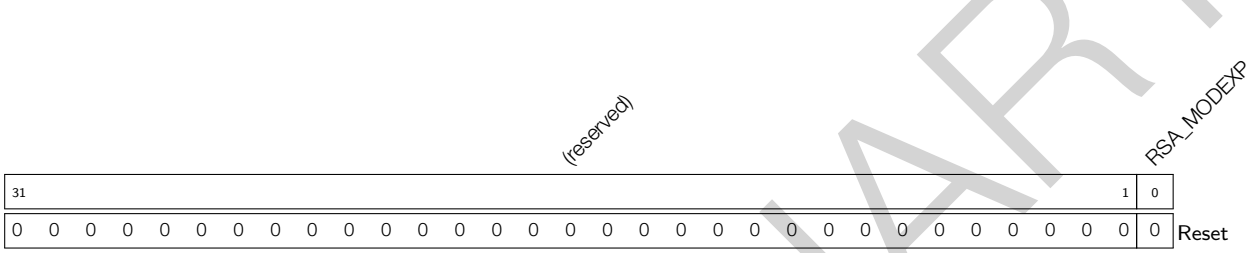
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Register 18.3. RSA_CLEAN_REG (0x0808)



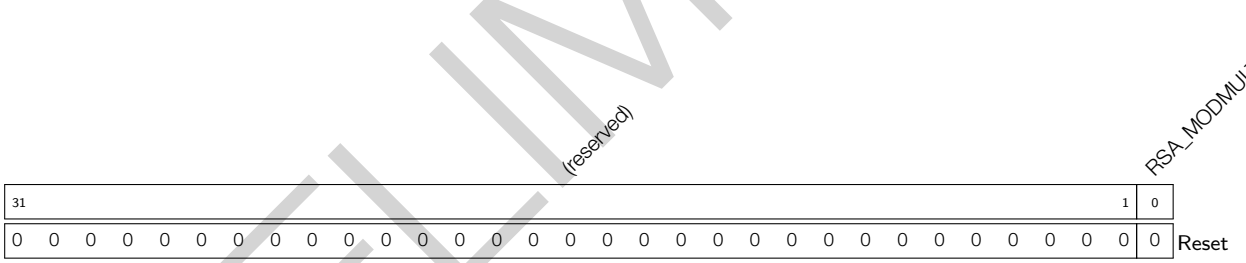
RSA_CLEAN The content of this bit is 1 when memories complete initialization. (RO)

Register 18.4. RSA_MODEXP_START_REG (0x080C)



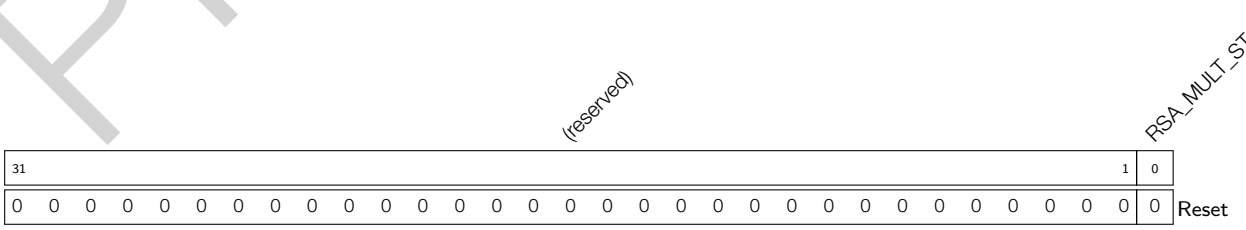
RSA_MODEXP_START Set this bit to 1 to start the modular exponentiation. (WO)

Register 18.5. RSA_MODMULT_START_REG (0x0810)



RSA_MODMULT_START Set this bit to 1 to start the modular multiplication. (WO)

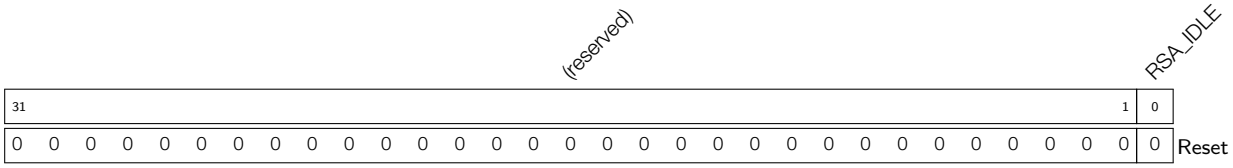
Register 18.6. RSA_MULT_START_REG (0x0814)



RSA_MULT_START Set this bit to 1 to start the multiplication. (WO)

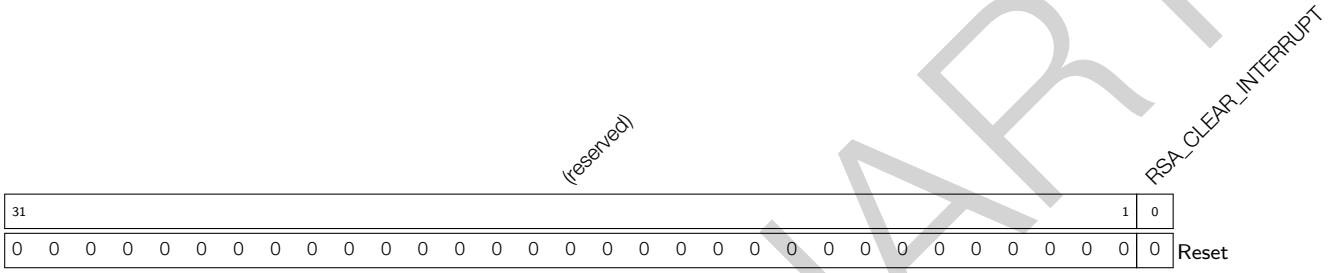
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Register 18.7. RSA_IDLE_REG (0x0818)



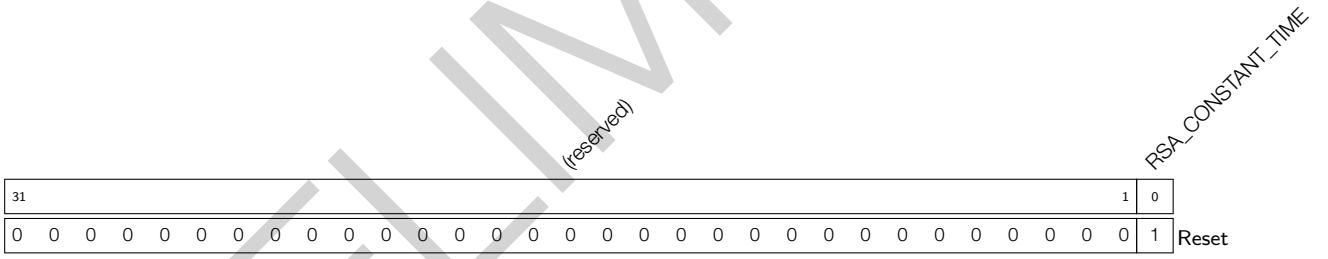
RSA_IDLE The content of this bit is 1 when the RSA accelerator is idle. (RO)

Register 18.8. RSA_CLEAR_INTERRUPT_REG (0x081C)



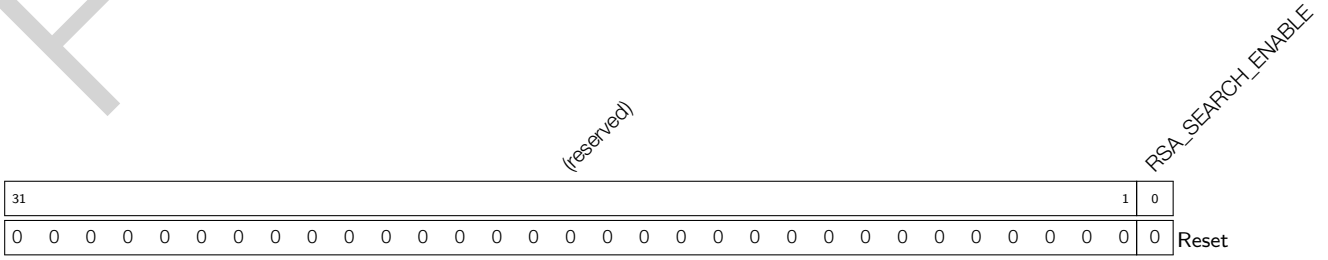
RSA_CLEAR_INTERRUPT Set this bit to 1 to clear the RSA interrupts. (WO)

Register 18.9. RSA_CONSTANT_TIME_REG (0x0820)



RSA_CONSTANT_TIME_REG Controls the constant_time option. 0: acceleration. 1: no acceleration (by default). (R/W)

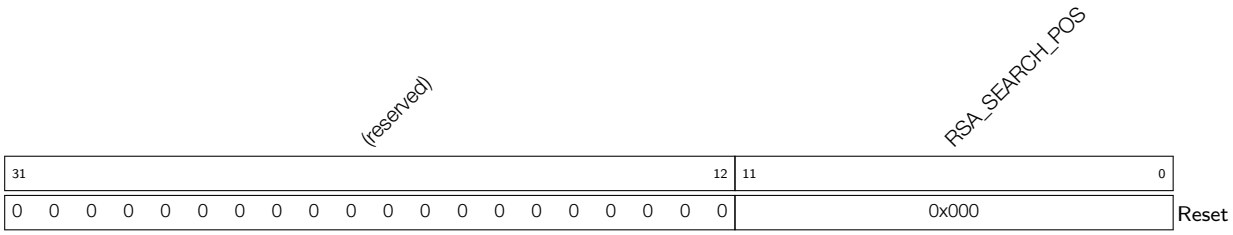
Register 18.10. RSA_SEARCH_ENABLE_REG (0x0824)



RSA_SEARCH_ENABLE Controls the search option. 0: no acceleration (by default). 1: acceleration. (R/W)

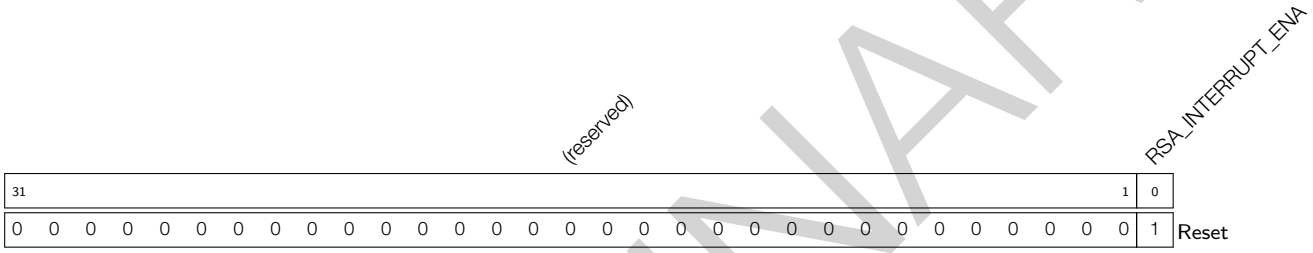
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Register 18.11. RSA_SEARCH_POS_REG (0x0828)



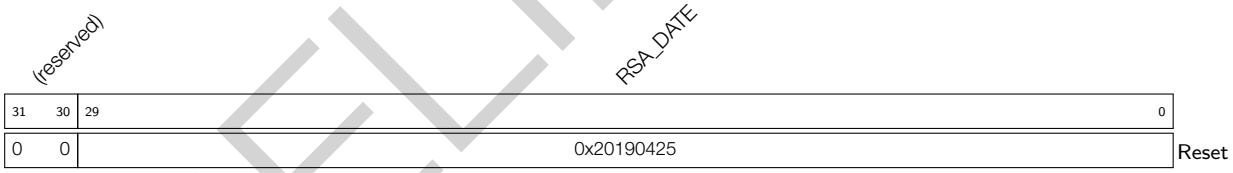
RSA_SEARCH_POS Is used to configure the starting address when the acceleration option of search is used. (R/W)

Register 18.12. RSA_INTERRUPT_ENA_REG (0x082C)



RSA_INTERRUPT_ENA Set this bit to 1 to enable the RSA interrupt. This option is enabled by default. (R/W)

Register 18.13. RSA_DATE_REG (0x0830)



RSA_DATE Version control register. (R/W)

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19 HMAC Accelerator (HMAC)

The Hash-based Message Authentication Code (HMAC) module computes Message Authentication Codes (MACs) using Hash algorithm and keys as described in RFC 2104. The underlying hash algorithm is SHA-256, and the 256-bit HMAC key is stored in an eFuse key block and can be set as read-protected for users.

19.1 Main Features

- Standard HMAC-SHA-256 algorithm
- Hash result only accessible by configurable hardware peripheral (in downstream mode)
- Compatible to challenge-response authentication algorithm
- Generates required keys for the Digital Signature (DS) peripheral (in downstream mode)
- Re-enables soft-disabled JTAG (in downstream mode)

19.2 Functional Description

The HMAC module operates in two modes: upstream mode and downstream mode. In upstream mode, the HMAC message is provided by the user and the calculation result is read back by the user; in downstream mode, the HMAC module is used as a Key Derivation Function (KDF) for other internal hardware. For instance, the JTAG can be temporarily disabled by burning odd number bits of EFUSE_SOFT_DIS_JTAG in eFuse. In this case, users can temporarily re-enable JTAG using the HMAC module in downstream mode.

After the reset signal being released, the HMAC module will check whether the DS key exists in the eFuse. If the key exists, the HMAC module will enter downstream digital signature mode and finish the DS key calculation automatically.

19.2.1 Upstream Mode

Common use cases for the upstream mode are challenge-response protocols supporting HMAC-SHA-256 algorithm. In upstream mode, the user should provide the related HMAC information and read back its calculation results.

Assume the two entities in the challenge-response protocol are A and B respectively, and the entities share the same secret KEY. The data message they expect to exchange is M. The general process of this protocol is as follows:

- A calculates a unique random number M
- A sends M to B
- B calculates the HMAC value (through M and KEY) and sends the result to A
- A also calculates the HMAC value (through M and KEY) internally
- A compares these two values. If they are the same, then the identity of B is authenticated

To calculate the HMAC value (the following steps should be done by the user):

1. Initialize the HMAC module, and enter upstream mode.
2. Write the correctly padded message to the HMAC, one block at a time.

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3. Read back the result from HMAC.

For details of this process, please see Section 19.2.6.

19.2.2 Downstream JTAG Enable Mode

There are two parameters in the eFuse memory to disable JTAG debugging, namely EFUSE_DIS_PAD_JTAG and EFUSE_SOFT_DIS_JTAG. Set EFUSE_DIS_PAD_JTAG to 1 can disable JTAG permanently, and set odd numbers of 1 to EFUSE_SOFT_DIS_JTAG can disable JTAG temporarily. For more details, please see Chapter 4 *eFuse Controller*.

To re-enable the temporarily disabled JTAG, users can follow the steps below:

1. Enable the HMAC module and enter downstream JTAG enable mode.
2. Write 1 to the HMAC_SOFT_JTAG_CTRL_REG register to enter JTAG re-enable compare mode.
3. Write the 256-bit HMAC value which is calculated locally from the 32-byte 0x00 using HMAC-SHA-256 algorithm and the pre-generated key to register HMAC_WR_JTAG_REG, in big-endian order of word.
4. If the HMAC internally calculated value matches the value that user programmed, then JTAG is re-enabled. Otherwise, JTAG remains disabled.
5. JTAG remains in the status as in step 4 until the user writes 1 to register HMAC_SET_INVALIDATE_JTAG_REG or restart JTAG.

For detailed steps of this process, please see Section 19.2.6.

19.2.3 Downstream Digital Signature Mode

The Digital Signature (DS) module encrypts its parameters using AES-CBC algorithm. The HMAC module is used as a Key Derivation Function (KDF) to derive the AES key to decrypt these parameters.

Before starting the DS module, the user needs to obtain the key for it first through HMAC calculation. For more information, please see Chapter 20 *Digital Signature (DS)*. After the clock of HMAC be enabled and reset of HMAC be released, the HMAC module will check to see if there is a functional key in eFuses for the DS module. If yes, HMAC will enter downstream digital signature mode and finish DS key calculation automatically.

19.2.4 HMAC eFuse Configuration

The HMAC module provides three different functionalities: re-enabling JTAG and serving as DS KDF in downstream mode as well as pure HMAC calculation in upstream mode. Table 19-1 lists the register value corresponding to each purpose, which should be written to register HMAC_SET_PARA_PURPOSE_REG by the user (see Section 19.2.6).

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Table 19-1. HMAC Purposes and Configuration Values

Purpose	Mode	Value	Description
JTAG Re-enable	Downstream	6	EFUSE_KEY_PURPOSE_HMAC_DOWN_JTAG
DS Key Derivation	Downstream	7	EFUSE_KEY_PURPOSE_HMAC_DOWN_DIGITAL_SIGNATURE
HMAC Calculation	Upstream	8	EFUSE_KEY_PURPOSE_HMAC_UP
Both JTAG Re-enable and DS KDF	Downstream	5	EFUSE_KEY_PURPOSE_HMAC_DOWN_ALL

Before enabling HMAC to do calculations, user should make sure the key to be used has been burned in eFuse. You can burn a key to eFuse as follows:

1. Prepare a secret 256-bit HMAC key and burn the key to an empty eFuse block y (there are six blocks for storing a key in eFuse. The numbers of those blocks range from 4 to 9, so y = 4,5,..,9. Hence, if we are talking about key0, we mean eFuse block4), and then program the purpose to EFUSE_KEY_PURPOSE_$(y-4)$. Take upstream mode as an example: after programming the key, the user should program EFUSE_KEY_PURPOSE_HMAC_UP (corresponding value is 8) to EFUSE_KEY_PURPOSE_$(y-4)$. Please see Chapter 4 *eFuse Controller* on how to program eFuse keys.
2. Configure this eFuse key block to be read protected, so that users cannot read its value. A copy of this key should be kept by any party who needs to verify this device.

19.2.5 HMAC Initialization

The eFuse key blocks (with correctly programmed purpose values) must be coordinated with the HMAC modes, or HMAC will terminate calculation.

Configure HMAC modes

The correct purpose (see Table 19-1) has to be written to register HMAC_SET_PARA_PURPOSE_REG by the user.

Select eFuse Key Blocks

The eFuse controller provides six key blocks, i.e., KEY0 ~ 5. To select a particular KEYn for a certain HMAC calculation, write the key number n to register HMAC_SET_PARA_KEY_REG.

Note that the purpose of the key has also been programmed to eFuse memory. Only when the configured HMAC purpose matches the defined purpose of KEYn, will the HMAC module execute the configured calculation. Otherwise, it will return a matching error and stop the current calculation. For example, suppose a user selects KEY3 for HMAC calculation, and the value programmed to KEY_PURPOSE_3 is 6 (EFUSE_KEY_PURPOSE_HMAC_DOWN_JTAG). Based on Table 19-1, KEY3 can be used to re-enable JTAG. If the value written to register HMAC_SET_PARA_PURPOSE_REG is also 6, then the HMAC module will start the process to re-enable JTAG.

19.2.6 HMAC Process (Detailed)

The process to call HMAC in ESP32-S3 is as follows:

1. Enable HMAC module

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(a) Set the peripheral clock bits for HMAC and SHA peripherals in SYSTEM_PEIRP_CLK_EN1_REG, and clear the corresponding peripheral reset bits in SYSTEM_PEIRP_RST_EN1_REG. For registers information, please see Chapter 3 *System and Memory*.

(b) Write 1 to register HMAC_SET_START_REG.

2. Configure HMAC keys and key purposes

(a) Write the key purpose m to register HMAC_SET_PARA_PURPOSE_REG. The possible key purpose values are shown in Table 19-1. For more information, please refer to Section 19.2.4.

(b) Select KEYn in eFuse memory as the key by writing n (0 ~ 5) to register HMAC_SET_PARA_KEY_REG. For more information, please refer to Section 19.2.5.

(c) Write 1 to register HMAC_SET_PARA_FINISH_REG to complete the configuration.

(d) Read register HMAC_QUERY_ERROR_REG. If its value is 1, it means the purpose of the selected block does not match the configured key purpose and the calculation will not proceed. If its value is 0, it means the purpose of the selected block matches the configured key purpose, and then the calculation can proceed.

(e) When the value of HMAC_SET_PARA_PURPOSE_REG is not 8, it means the HMAC module is in downstream mode, proceed with Step 3. When the value is 8, it means the HMAC module is in upstream mode, proceed with Step 4.

3. Downstream mode

(a) Poll Status register HMAC_QUERY_BUSY_REG. When the value of this register is 0, HMAC calculation in downstream mode is completed.

(b) In downstream mode, the calculation result is used by either the JTAG or DS module in the hardware. To clear the result and make further usage of the dependent hardware (JTAG or DS), write 1 to either register HMAC_SET_INVALIDATE_JTAG_REG to clear the result generated by JTAG key; or to register HMAC_SET_INVALIDATE_DS_REG to clear the result generated by DS key.

(c) Downstream mode operation completed.

4. Transmit message block Block_n ($n >= 1$) in upstream mode

(a) Poll Status register HMAC_QUERY_BUSY_REG. When the value of this register is 0, go to step 4(b).

(b) Write the 512-bit Block_n to register HMAC_WDATA0~15_REG. Write 1 to register HMAC_SET_MESSAGE_ONE_REG, to trigger the processing of this message block.

(c) Poll Status register HMAC_QUERY_BUSY_REG. When the value of this register is 0, go to step 4(d).

(d) Different message blocks will be generated, depending on whether the size of the to-be-processed message is a multiple of 512 bits.

- If the bit length of the message is a multiple of 512 bits, there are three possible options:

  i. If Block_n+1 exists, write 1 to register HMAC_SET_MESSAGE_ING_REG to make $n = n + 1$, and then jump to step 4(b).

  ii. If Block_n is the last block of the message and the user wants to apply SHA padding in hardware, write 1 to register HMAC_SET_MESSAGE_END_REG, and then jump to step 6.

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iii. If Block_n is the last block of the padded message and the user has applied SHA padding in software, write 1 to register HMAC_SET_MESSAGE_PAD_REG, and then jump to step 5.

- If the bit length of the message is not a multiple of 512 bits, there are three possible options as follows. Note that in this case, the user should apply SHA padding to the message, after which the padded message length should be a multiple of 512 bits.

  i. If Block_n is the only message block, $n = 1$, and Block_1 has included all padding bits, write 1 to register HMAC_ONE_BLOCK_REG, and then jump to step 6.

  ii. If Block_n is the second to last padded block, write 1 to register HMAC_SET_MESSAGE_PAD_REG, and then jump to step 5.

  iii. If Block_n is neither the last nor the second to last message block, write 1 to register HMAC_SET_MESSAGE_ING_REG and define $n = n + 1$, and then jump to step 4.(b).

5. Apply SHA padding to message

   (a) After applying SHA padding to the last message block as described in Section 19.3.1, write this block to register HMAC_WDATA0~15_REG, and then write 1 to register HMAC_SET_MESSAGE_ONE_REG. Then the HMAC module will calculate this message block.

   (b) Jump to step 6.

6. Read hash result in upstream mode

   (a) Poll Status register HMAC_QUERY_BUSY_REG. When the value of this register is 0, go to the next step.

   (b) Read hash result from register HMAC_RDATA0~7_REG.

   (c) Write 1 to register HMAC_SET_RESULT_FINISH_REG to finish calculation.

   (d) Upstream mode operation is completed.

Note:
The SHA accelerator can be called directly, or used internally by the DS module and the HMAC module. However, they can not share the hardware resources simultaneously. Therefore, SHA module can not be called by the CPU nor DS module when the HMAC module is in use.

19.3 HMAC Algorithm Details

19.3.1 Padding Bits

The HMAC module uses SHA-256 as hash algorithm. If the input message is not a multiple of 512 bits, a SHA-256 padding algorithm must be applied in software. The SHA-256 padding algorithm is the same as described in Section *Padding the Message* of *FIPS PUB 180-4*.

As shown in Figure 19-1, suppose the length of the unpadded message is m bits. Padding steps are as follows:

1. Append one bit of value "1" to the end of the unpadded message;
2. Append k bits of value "0", where k is the smallest non-negative number which satisfies $m + 1 + k \equiv 448 (mod 512)$;

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3. Append a 64-bit integer value as a binary block. This block includes the length of the unpadded message as a big-endian binary integer value m.

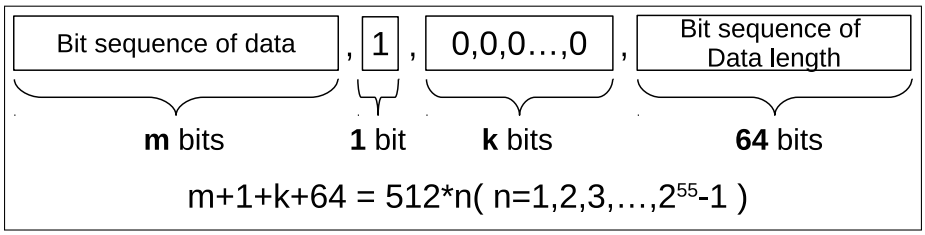


Figure 19-1. HMAC SHA-256 Padding Diagram

In downstream mode, there is no need to input any message or apply padding. In upstream mode, if the length of the unpadded message is a multiple of 512 bits, the user can choose to configure hardware to apply the SHA padding. If the length is not a multiple of 512 bits, the user must apply the SHA padding manually. For detailed steps, please see Section 19.2.6.

19.3.2 HMAC Algorithm Structure

The structure of the implemented algorithm in the HMAC module is shown in Figure 19-2. This is the standard HMAC algorithm as described in RFC 2104.

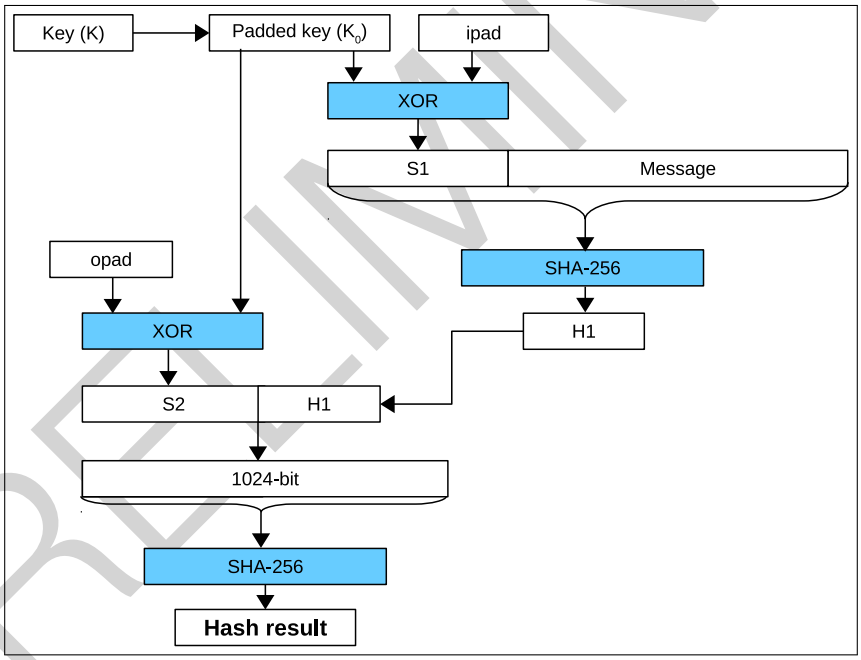


Figure 19-2. HMAC Structure Schematic Diagram

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In Figure 19-2:

1. ipad is a 512-bit message block composed of 64 bytes of 0x36.
2. opad is a 512-bit message block composed of 64 bytes of 0x5c.

The HMAC module appends a 256-bit 0 sequence after the bit sequence of the 256-bit key K in order to get a 512-bit K_0. Then, the HMAC module XORs K_0 with ipad to get the 512-bit S1. Afterwards, the HMAC module appends the input message (multiple of 512 bits) after the 512-bit S1, and exercises the SHA-256 algorithm to get the 256-bit H1.

The HMAC module appends the 256-bit SHA-256 hash result H1 to the 512-bit S2 value, which is calculated using the XOR operation of K_0 and opad. A 768-bit sequence will be generated. Then, the HMAC module uses the SHA padding algorithm described in Section 19.3.1 to pad the 768-bit sequence to a 1024-bit sequence, and applies the SHA-256 algorithm to get the final hash result (256-bit).

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19.4 Register Summary

The addresses in this section are relative to HMAC Accelerator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
Status/Control Register			
HMAC_SET_START_REG	HMAC start control register	0x040	WO
HMAC_SET_PARA_PURPOSE_REG	HMAC parameter purpose register	0x044	WO
HMAC_SET_PARA_KEY_REG	HMAC pamameter key register	0x048	WO
HMAC_SET_PARA_FINISH_REG	Finish initial configuration	0x04C	WO
HMAC_SET_MESSAGE_ONE_REG	HMAC message control register	0x050	WO
HMAC_SET_MESSAGE_ING_REG	HMAC message continue register	0x054	WO
HMAC_SET_MESSAGE_END_REG	HMAC message end register	0x058	WO
HMAC_SET_RESULT_FINISH_REG	HMAC result reading finish register	0x05C	WO
HMAC_SET_INVALIDATE_JTAG_REG	Invalidate JTAG result register	0x060	WO
HMAC_SET_INVALIDATE_DS_REG	Invalidate digital signature result register	0x064	WO
HMAC_QUERY_ERROR_REG	Stores matching results between keys generated by users and corresponding purposes	0x068	RO
HMAC_QUERY_BUSY_REG	Busy state of HMAC module	0x06C	RO
HMAC Message Block			
HMAC_WR_MESSAGE_0_REG	Message register 0	0x080	WO
HMAC_WR_MESSAGE_1_REG	Message register 1	0x084	WO
HMAC_WR_MESSAGE_2_REG	Message register 2	0x088	WO
HMAC_WR_MESSAGE_3_REG	Message register 3	0x08C	WO
HMAC_WR_MESSAGE_4_REG	Message register 4	0x090	WO
HMAC_WR_MESSAGE_5_REG	Message register 5	0x094	WO
HMAC_WR_MESSAGE_6_REG	Message register 6	0x098	WO
HMAC_WR_MESSAGE_7_REG	Message register 7	0x09C	WO
HMAC_WR_MESSAGE_8_REG	Message register 8	0x0A0	WO
HMAC_WR_MESSAGE_9_REG	Message register 9	0x0A4	WO
HMAC_WR_MESSAGE_10_REG	Message register 10	0x0A8	WO
HMAC_WR_MESSAGE_11_REG	Message register 11	0x0AC	WO
HMAC_WR_MESSAGE_12_REG	Message register 12	0x0B0	WO
HMAC_WR_MESSAGE_13_REG	Message register 13	0x0B4	WO
HMAC_WR_MESSAGE_14_REG	Message register 14	0x0B8	WO
HMAC_WR_MESSAGE_15_REG	Message register 15	0x0BC	WO
HMAC Upstream Result			
HMAC_RD_RESULT_0_REG	Hash result register 0	0x0C0	RO
HMAC_RD_RESULT_1_REG	Hash result register 1	0x0C4	RO
HMAC_RD_RESULT_2_REG	Hash result register 2	0x0C8	RO
HMAC_RD_RESULT_3_REG	Hash result register 3	0x0CC	RO
HMAC_RD_RESULT_4_REG	Hash result register 4	0x0D0	RO
HMAC_RD_RESULT_5_REG	Hash result register 5	0x0D4	RO
HMAC_RD_RESULT_6_REG	Hash result register 6	0x0D8	RO

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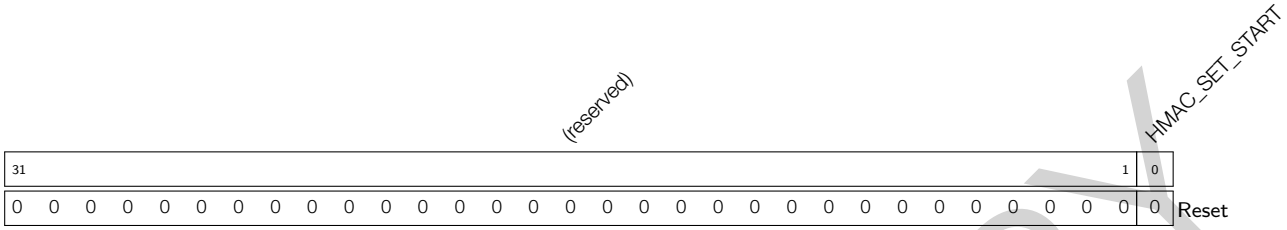
Name	Description	Address	Access
HMAC_RD_RESULT_7_REG	Hash result register 7	0x0DC	RO
configuration Register			
HMAC_SET_MESSAGE_PAD_REG	Software padding register	0x0F0	WO
HMAC_ONE_BLOCK_REG	One block message register	0x0F4	WO
HMAC_SOFT_JTAG_CTRL_REG	Re-enable JTAG register 0	0x0F8	WO
HMAC_WR_JTAG_REG	Re-enable JTAG register 1	0x0FC	WO
Version Register			
HMAC_DATE_REG	Version control register	0x1FC	R/W

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19.5 Registers

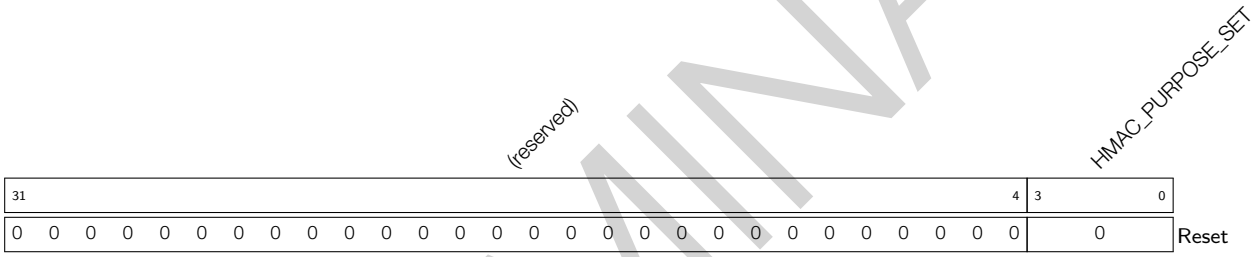
The addresses in this section are relative to HMAC Accelerator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 19.1. HMAC_SET_START_REG (0x040)



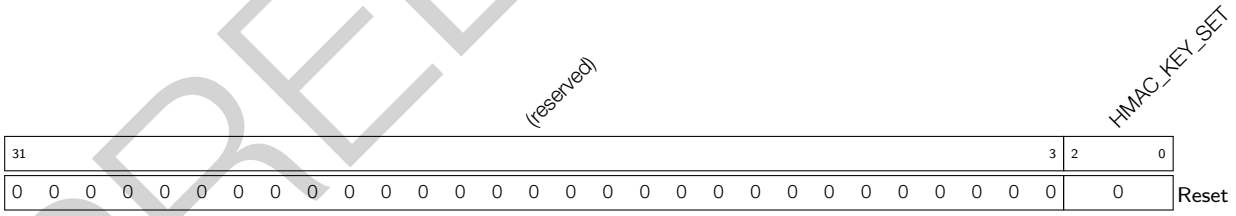
HMAC_SET_START Set this bit to start hmac operation. (WO)

Register 19.2. HMAC_SET_PARA_PURPOSE_REG (0x044)



HMAC_PURPOSE_SET Set HMAC parameter purpose, please see Table 19-1. (WO)

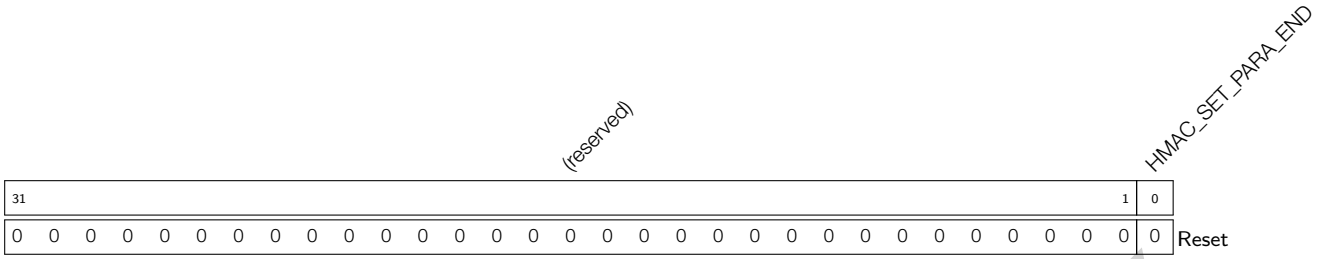
Register 19.3. HMAC_SET_PARA_KEY_REG (0x048)



HMAC_KEY_SET Set HMAC parameter key. There are six keys with index 0 ~ 5. Write the index of the selected key to this field. (WO)

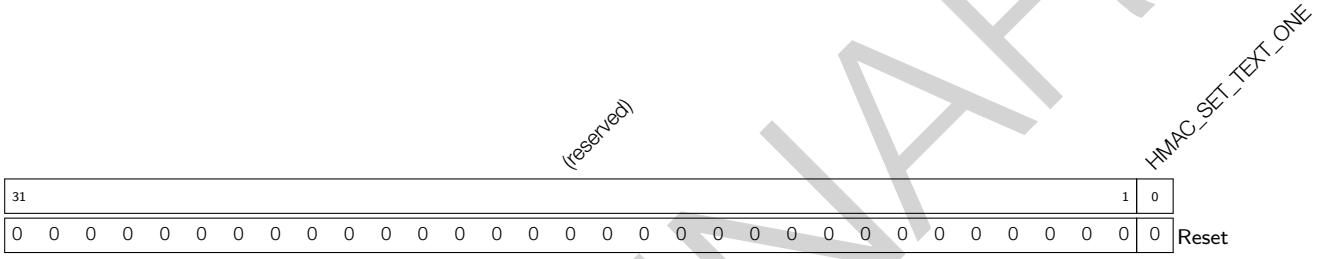
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Register 19.4. HMAC_SET_PARA_FINISH_REG (0x04C)



HMAC_SET_PARA_END Set this bit to finish HMAC configuration. (WO)

Register 19.5. HMAC_SET_MESSAGE_ONE_REG (0x050)



HMAC_SET_TEXT_ONE Call SHA to calculate one message block. (WO)

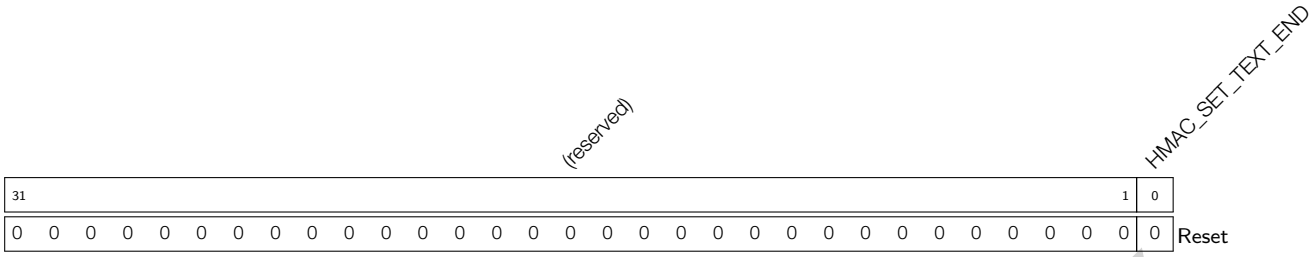
Register 19.6. HMAC_SET_MESSAGE_ING_REG (0x054)



HMAC_SET_TEXT_ING Set this bit to show there are still some message blocks to be processed. (WO)

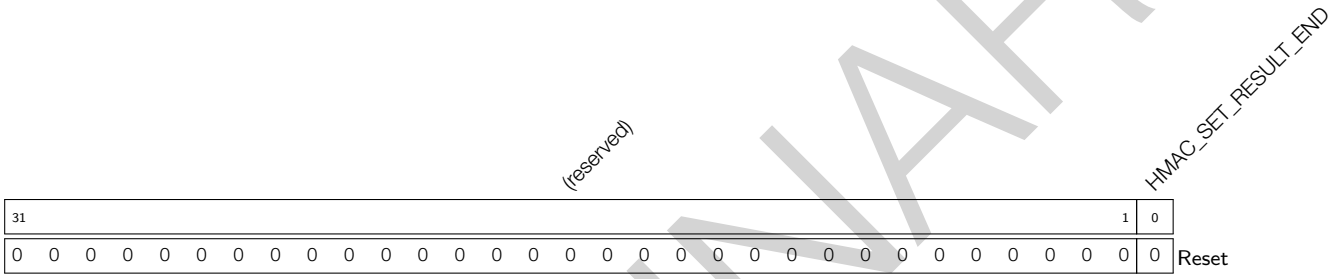
PRELIMINARY

Register 19.7. HMAC_SET_MESSAGE_END_REG (0x058)



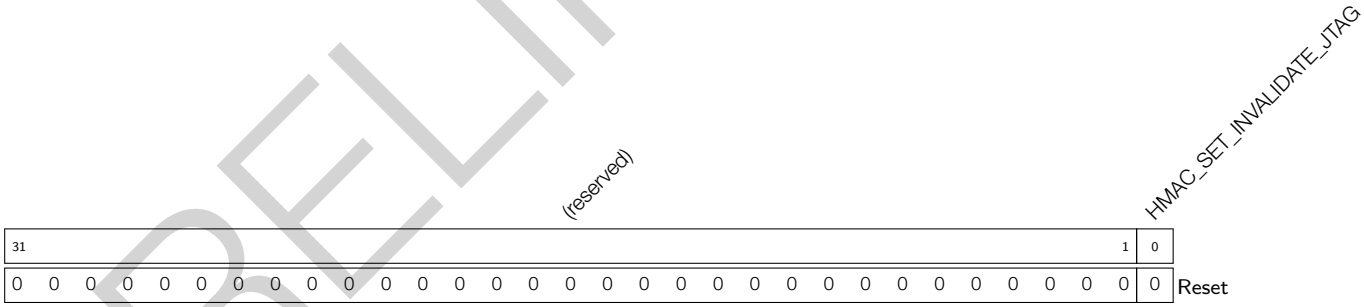
HMAC_SET_TEXT_END Set this bit to start hardware padding. (WO)

Register 19.8. HMAC_SET_RESULT_FINISH_REG (0x05C)



HMAC_SET_RESULT_END After read result from upstream, then let HMAC back to idle. (WO)

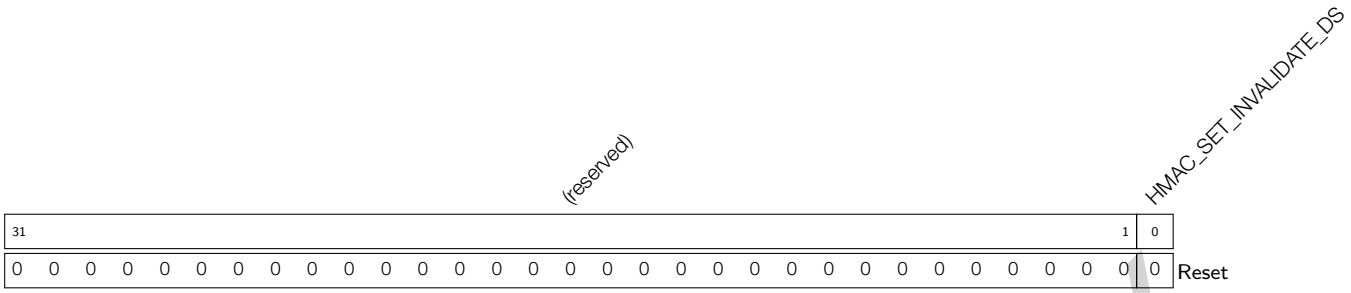
Register 19.9. HMAC_SET_INVALIDATE_JTAG_REG (0x060)



HMAC_SET_INVALIDATE_JTAG Set this bit to clear calculation results when re-enabling JTAG in downstream mode. (WO)

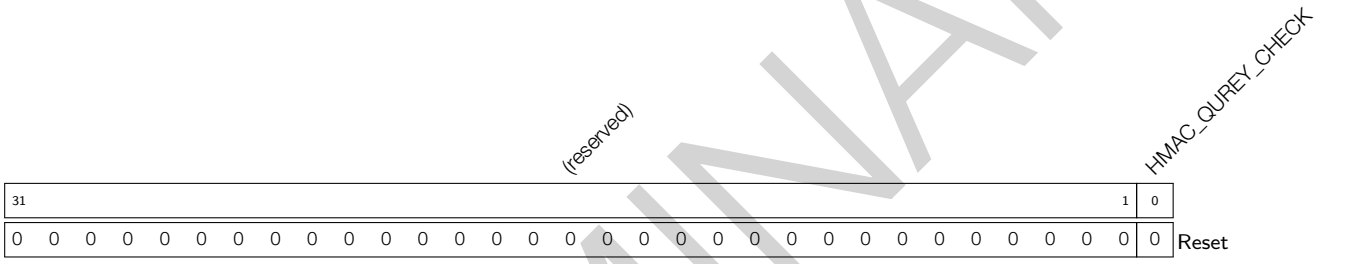
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Register 19.10. HMAC_SET_INVALIDATE_DS_REG (0x064)



HMAC_SET_INVALIDATE_DS Set this bit to clear calculation results of the DS module in downstream mode. (WO)

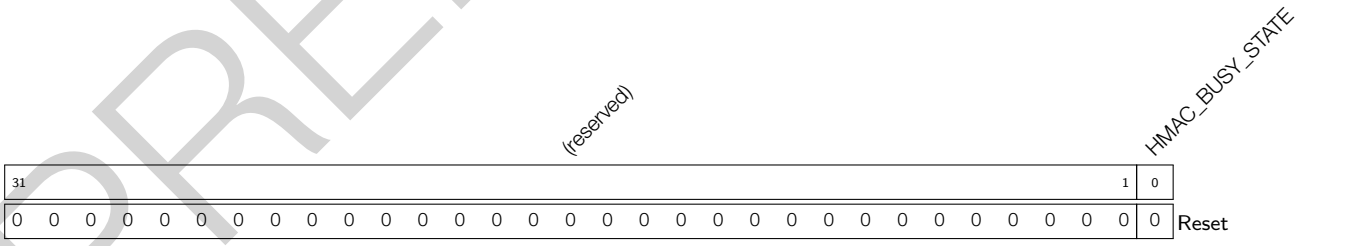
Register 19.11. HMAC_QUERY_ERROR_REG (0x068)



HMAC_QUREY_CHECK Indicates whether a HMAC key matches the purpose.

- 0: HMAC key and purpose match.
- 1: error. (RO)

Register 19.12. HMAC_QUERY_BUSY_REG (0x06C)

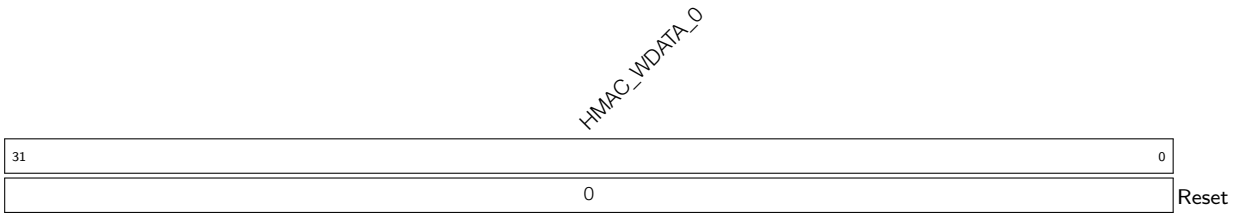


HMAC_BUSY_STATE Indicates whether HMAC is in busy state.

- 1'b0: idle.
- 1'b1: HMAC is still working for calculation. (RO)

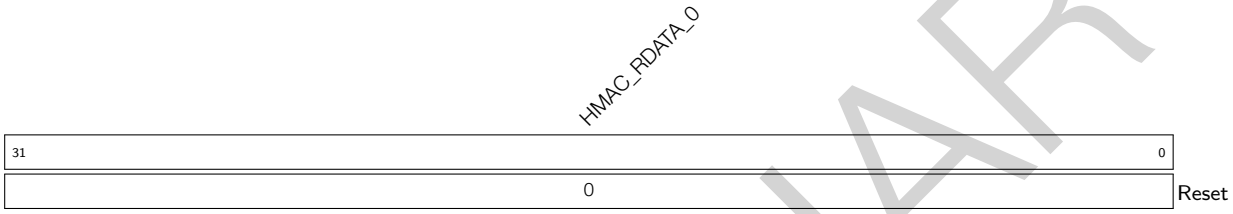
PRELIMINARY

Register 19.13. HMAC_WR_MESSAGE_*n*_REG (*n*: 0-15) (0x080+4n*)**



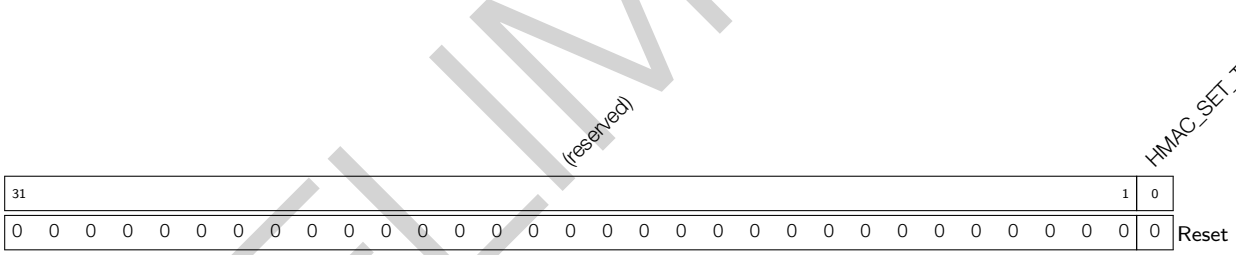
HMAC_WDATA_*n* Store the *n*th 32-bit of message. (WO)

Register 19.14. HMAC_RD_RESULT_*n*_REG (*n*: 0-7) (0x0C0+4n*)**



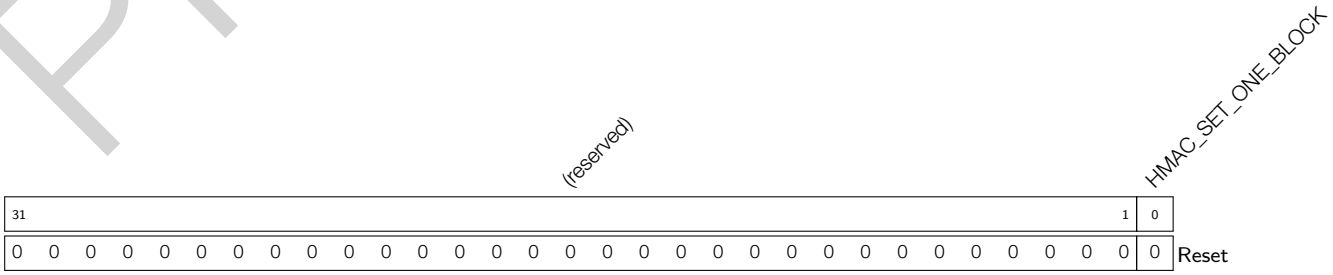
HMAC_RDATA_*n* Read the *n*th 32-bit of hash result. (RO)

Register 19.15. HMAC_SET_MESSAGE_PAD_REG (0x0F0)



HMAC_SET_TEXT_PAD Set this bit to start software padding. (WO)

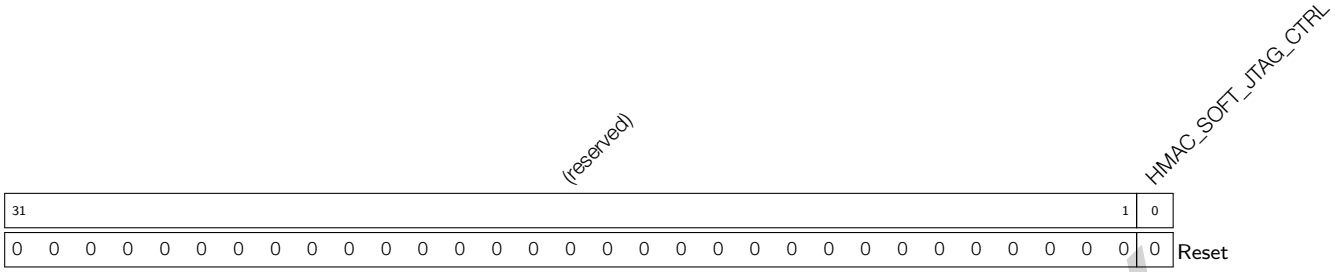
Register 19.16. HMAC_ONE_BLOCK_REG (0x0F4)



HMAC_SET_ONE_BLOCK Set this bit to show that no padding is required. (WO)

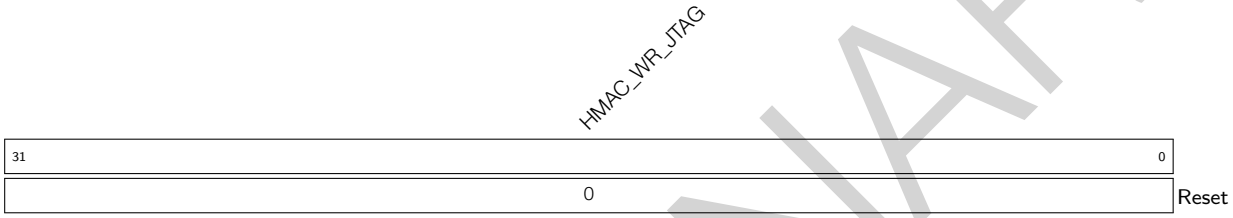
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Register 19.17. HMAC_SOFT_JTAG_CTRL_REG (0x0F8)



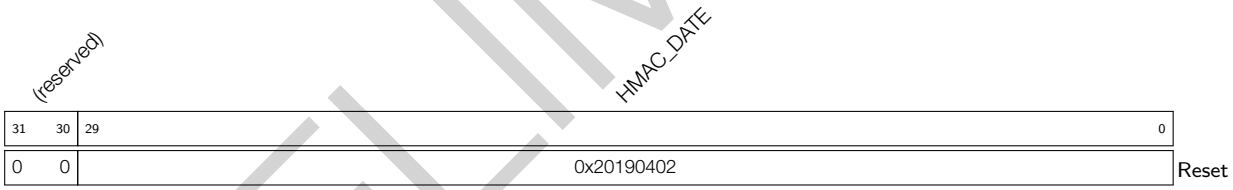
HMAC_SOFT_JTAG_CTRL Set this bit to turn on JTAG verification. (WO)

Register 19.18. HMAC_WR_JTAG_REG (0x0FC)



HMAC_WR_JTAG 32-bit of key to be compared. (WO)

Register 19.19. HMAC_DATE_REG (0x1FC)



HMAC_DATE Version control register.(R/W)

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20 Digital Signature (DS)

20.1 Overview

A Digital Signature is used to verify the authenticity and integrity of a message using a cryptographic algorithm. This can be used to validate a device's identity to a server, or to check the integrity of a message.

The ESP32-S3 includes a Digital Signature (DS) module providing hardware acceleration of messages' signatures based on RSA. It uses pre-encrypted parameters to calculate a signature. The parameters are encrypted using HMAC as a key-derivation function. In turn, the HMAC uses eFuses as an input key. The whole process happens in hardware so that neither the decryption key for the RSA parameters nor the input key for the HMAC key derivation function can be seen by the users while calculating the signature.

20.2 Features

- RSA Digital Signatures with key length up to 4096 bits
- Encrypted private key data, only decryptable by DS peripheral
- SHA-256 digest to protect private key data against tampering by an attacker

20.3 Functional Description

20.3.1 Overview

The DS peripheral calculates RSA signature as $Z = X^Y \bmod M$ where Z is the signature, X is the input message, Y and M are the RSA private key parameters.

Private key parameters are stored in flash or other memory as ciphertext. They are decrypted using a key (DS_KEY) which can only be read by the DS peripheral via the HMAC peripheral. The required inputs ($HMAC\_KEY$) to generate the key are only stored in eFuse and can only be accessed by the HMAC peripheral. The DS peripheral hardware can decrypt the private key, and the private key in plaintext is never accessed by the software. For more detailed information about eFuse and HMAC peripherals, please refer to Chapter 4 *eFuse Controller* and 19 *HMAC Accelerator (HMAC)* peripheral.

The input message X will be sent directly to the DS peripheral by the software, each time a signature is needed. After the RSA signature operation, the signature Z is read back by the software.

For better understanding, we define some symbols and functions here, which are only applicable to this chapter:

- 1^s A bit string consist of s bits that stores "1".
- $[x]_s$ A bit string of s bits, in which s should be the integral multiple of 8 bits. If x is a number ($x < 2^s$), it is represented in little endian byte order in the bit string. x may be a variable value such as $[Y]_{4096}$ or as a hexadecimal constant such as $[0x0C]_8$. If necessary, the value $[x]_t$ can be right-padded with $(s - t)$ number of 0 to reach s bits in length, and finally get $[x]_s$. For example, $[0x05]_8 = 00000101$, $[0x05]_{16} = 0000010100000000$, $[0x0005]_{16} = 0000000000000101$, $[0x13]_8 = 00010011$, $[0x13]_{16} = 0001001100000000$, $[0x0013]_{16} = 0000000000010011$.
- $||$ A bit string concatenation operator for joining multiple bit strings into a longer bit string.

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20.3.2 Private Key Operands

Private key operands Y (private key exponent) and M (key modulus) are generated by the user. They have a particular RSA key length (up to 4096 bits). Two additional private key operands are needed: $\overline{r}$ and M'. These two operands are derived from Y and M.

Operands Y, M, $\overline{r}$ and M' are encrypted by the user along with an authentication digest and stored as a single ciphertext C. C is inputted to the DS peripheral in this encrypted format, decrypted by the hardware, and then used for RSA signature calculation. Detailed description of how to generate C is provided in Section 20.3.3.

The DS peripheral supports RSA signature calculation $Z = X^Y \bmod M$, in which the length of operands should be $N = 32 \times x$ where $x \in \{1, 2, 3, \ldots, 128\}$. The bit lengths of arguments Z, X, Y, M and $\overline{r}$ should be an arbitrary value in N, and all of them in a calculation must be of the same length, while the bit length of M' should always be 32. For more detailed information about RSA calculation, please refer to Section 18.3.1 *Large Number Modular Exponentiation* in Chapter 18 *RSA Accelerator (RSA)*.

20.3.3 Software Prerequisites

The left side of Figure 20-1 lists preparations required by the software before the hardware starts RSA signature calculation, while the right side lists the hardware workflow during the entire calculation procedure.

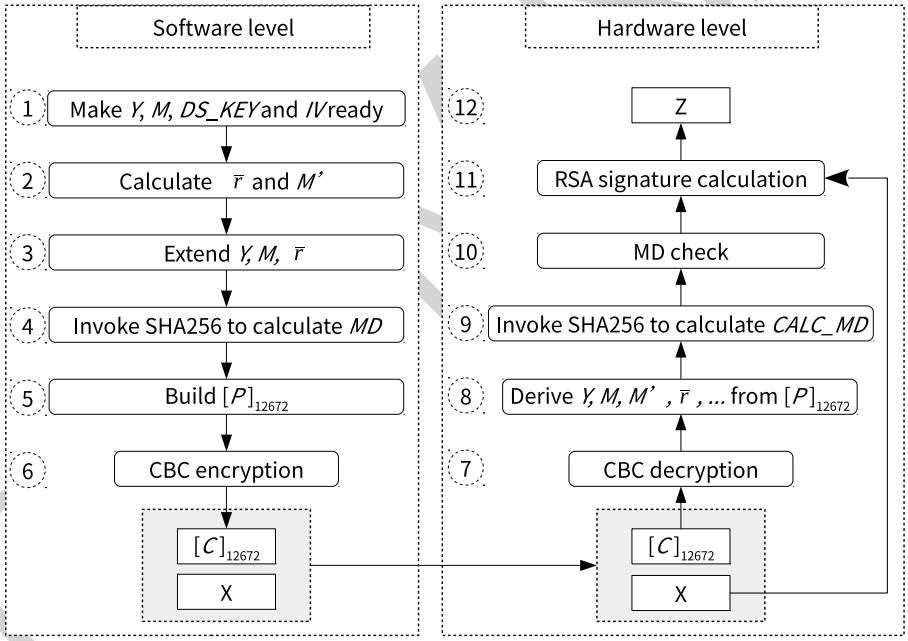


Figure 20-1. Software Preparations and Hardware Working Process

Note:

1. The software preparation (left side in the Figure 20-1) is a one-time operation before any signature is calculated, while the hardware calculation (right side in the Figure 1-1) repeats for every signature calculation.

Users need to follow the steps shown in the left part of Figure 20-1 to calculate C. Detailed instructions are as follows:

- **Step 1**: Prepare operands Y and M whose lengths should meet the requirements in Section 20.3.2.

Define $[L]_{32} = \frac{N}{32}$ (i.e., for RSA 4096, $[L]_{32}$ == [0x80]$_{32}$). Prepare $[HMAC\_KEY]_{256}$ and calculate $[DS\_KEY]_{256}$ based on DS_KEY = HMAC-SHA256 ($[HMAC\_KEY]_{256}$, 1^{256}). Generate a random $[IV]_{128}$ which should meet the requirements of the AES-CBC block encryption algorithm. For more information on AES, please refer to Chapter 17 *AES Accelerator (AES)*.

- **Step 2**: Calculate $\overline{r}$ and M' based on M.
- **Step 3**: Extend Y, M and $\overline{r}$, in order to get $[Y]_{4096}$, $[M]_{4096}$ and $[\overline{r}]_{4096}$, respectively. This step is only required for Y, M and $\overline{r}$ whose length are less than 4096 bits, since their largest length are 4096 bits.
- **Step 4** Calculate MD authentication code using the SHA-256:
  $[MD]_{256}$ = SHA256 ($[Y]_{4096}||[M]_{4096}||[\overline{r}]_{4096}||[M']_{32}||[L]_{32}||[IV]_{128}$)
- **Step 5**: Build $[P]_{12672}$ = ($[Y]_{4096}||[M]_{4096}||[\overline{r}]_{4096}||[MD]_{256}||[M']_{32}||[L]_{32}||[\beta]_{64}$), where $[\beta]_{64}$ is a PKCS#7 padding value, i.e., a 64-bit string [0x0808080808080808]$_{64}$ composed of 8 bytes (value = 0x80). The purpose of $[\beta]_{64}$ is to make the bit length of P a multiple of 128.
- **Step 6**: Calculate C = $[C]_{12672}$ = AES-CBC-ENC ($[P]_{12672}$, $[DS\_KEY]_{256}$, $[IV]_{128}$), where C is the ciphertext with length of 12672 bits.

20.3.4 DS Operation at the Hardware Level

The hardware operation is triggered each time a digital signature needs to be calculated. The inputs are the pre-generated private key ciphertext C, a unique message X, and IV.

The DS operation at the hardware level can be divided into the following three stages:

1. **Decryption: Step 7 and 8 in Figure 20-1**

   The decryption process is the inverse of Step 6 in figure 20-1. The DS peripheral will call AES accelerator to decrypt C in CBC block mode and get the resulted plaintext. The decryption process can be represented by P = AES-CBC-DEC (C, DS_KEY, IV), where IV (i.e., $[IV]_{128}$) is defined by users. $[DS\_KEY]_{256}$ is provided by HMAC module, derived from $HMAC\_KEY$ stored in eFuse. $[DS\_KEY]_{256}$, as well as $[HMAC\_KEY]_{256}$ are not readable by users.

   With P, the DS peripheral can derive $[Y]_{4096}$, $[M]_{4096}$, $[\overline{r}]_{4096}$, $[M']_{32}$, $[L]_{32}$, MD authentication code, and the padding value $[\beta]_{64}$. This process is the inverse of Step 5.

2. **Check: Step 9 and 10 in Figure 20-1**

   The DS peripheral will perform two checks: MD check and padding check. Padding check is not shown in Figure 20-1, as it happens at the same time with MD check.

   - MD check: The DS peripheral calls SHA-256 to calculate the MD authentication code $[CALC\_MD]_{256}$ from $[Y]_{4096}||[M]_{4096}||[\overline{r}]_{4096}||[M']_{32}||[L]_{32}||[IV]_{128}$). Then, $[CALC\_MD]_{256}$ is compared against the pre-calculated MD authentication code $[MD]_{256}$ from step 4. Only when the two match, MD check passes.
   - Padding check: The DS peripheral checks if $[\beta]_{64}$ complies with the aforementioned PKCS#7 format. Only when $[\beta]_{64}$ complies with the format, padding check passes.

   The DS peripheral will only perform subsequent operations if MD check passes. If padding check fails, an error bit is set in the query register, but it does not affect the subsequent operations, i.e., it is up to the user to proceed or not.

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3. **Calculation: Step 11 and 12 in Figure 20-1**

   The DS peripheral treats X (input by users) and Y, M, $\overline{r}$ (compiled) as big numbers. With M', all operands to perform X^Y mod M are in place. The operand length is defined by L. The DS peripheral will get the signed result Z by calling RSA to perform $Z = X^Y$ mod M.

20.3.5 DS Operation at the Software Level

The following software steps should be followed each time a Digital Signature needs to be calculated. The inputs are the pre-generated private key ciphertext C, a unique message X, and IV. These software steps trigger the hardware steps described in Section 20.3.4.

We assume that the software has called the HMAC peripheral and HMAC on the hardware has calculated DS_KEY based on $HMAC\_KEY$.

1. **Prerequisites**: Prepare operands C, X, IV according to Section 20.3.3.
2. **Activate the DS peripheral**: Write 1 to DS_SET_START_REG.
3. **Check if DS_KEY is ready**: Poll DS_QUERY_BUSY_REG until the software reads 0.

   If the software does not read 0 in DS_QUERY_BUSY_REG after approximately 1 ms, it indicates a problem with HMAC initialization. In such a case, the software can read register DS_QUERY_KEY_WRONG_REG to get more information:

   - If the software reads 0 in DS_QUERY_KEY_WRONG_REG, it indicates that the HMAC peripheral has not been activated.
   - If the software reads any value from 1 to 15 in DS_QUERY_KEY_WRONG_REG, it indicates that HMAC was activated, but the DS peripheral did not successfully receive the DS_KEY value from the HMAC peripheral. This may indicate that the HMAC operation has been interrupted due to a software concurrency problem.
4. **Configure register**: Write IV block to register DS_IV_*m*_REG (*m*: 0-3). For more information on the IV block, please refer to Chapter 17 *AES Accelerator (AES)*.
5. **Write X to memory block DS_X_MEM**: Write X_i ($i \in \{0, 1, \ldots, n-1\}$), where $n = \frac{N}{32}$, to memory block DS_X_MEM whose capacity is 128 words. Each word can store one base-b digit. The memory block uses the little endian format for storage, i.e., the least significant digit of the operand is in the lowest address. Words in DS_X_MEM block after the configured length of X (N bits, as described in Section 20.3.2) are ignored.
6. **Write C to memory block DS_C_MEM**: Write C_i ($i \in \{0, 1, \ldots, 395\}$) to memory block DS_C_MEM whose capacity is 396 words. Each word can store one base-b digit.
7. **Start DS operation**: Write 1 to register DS_SET_ME_REG.
8. **Wait for the operation to be completed**: Poll register DS_QUERY_BUSY_REG until the software reads 0.
9. **Query check result**: Read register DS_QUERY_CHECK_REG and determine the subsequent operations based on the return value.

   - If the value is 0, it indicates that both padding check and MD check pass. Users can continue to get the signed result Z.

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- If the value is 1, it indicates that the padding check passes but MD check fails. The signed result Z is invalid. The operation will resume directly from Step 11.
- If the value is 2, it indicates that the padding check fails but MD check passes. Users can continue to get the signed result Z. But please note that the data encapsulation format does not complie with the aforementioned PKCS#7 format, which may not be what you want.
- If the value is 3, it indicates that both padding check and MD check fail. In this case, some fatal errors may occurred and the signed result Z is invalid. The operation will resume directly from Step 11.

10. **Read the signed result**: Read the signed result Z_i ($i \in \{0, 1, \ldots, n-1\}$), where $n = \frac{N}{32}$, from memory block DS_Z_MEM. The memory block stores Z in little-endian byte order.
11. **Exit the operation**: Write 1 to DS_SET_FINISH_REG, then poll DS_QUERY_BUSY_REG until the software reads 0.

After the operation, all the input/output registers and memory blocks are cleared.

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20.4 Memory Summary

The addresses in this section are relative to the [Digital Signature] base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Size (byte)	Starting Address	Ending Address	Access
DS_C_MEM	Memory block C	1584	0x0000	0x062F	WO
DS_X_MEM	Memory block X	512	0x0800	0x09FF	WO
DS_Z_MEM	Memory block Z	512	0x0A00	0x0BFF	RO

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20.5 Register Summary

The addresses in this section are relative to the Digital Signature base address provided in Table 3-3 in Chapter 3 *System and Memory*.

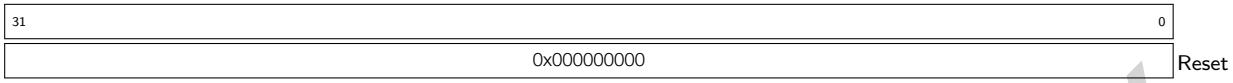
Name	Description	Address	Access
Configuration Registers			
DS_IV_0_REG	IV block data	0x0630	WO
DS_IV_1_REG	IV block data	0x0634	WO
DS_IV_2_REG	IV block data	0x0638	WO
DS_IV_3_REG	IV block data	0x063C	WO
Status/Control Registers			
DS_SET_START_REG	Activates the DS peripheral	0x0E00	WO
DS_SET_ME_REG	Starts DS operation	0x0E04	WO
DS_SET_FINISH_REG	Ends DS operation	0x0E08	WO
DS_QUERY_BUSY_REG	Status of the DS peripheral	0x0E0C	RO
DS_QUERY_KEY_WRONG_REG	Checks the reason why DS_KEY is not ready	0x0E10	RO
DS_QUERY_CHECK_REG	Queries DS check result	0x0814	RO
Version Register			
DS_DATE_REG	Version control register	0x0820	W/R

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20.6 Registers

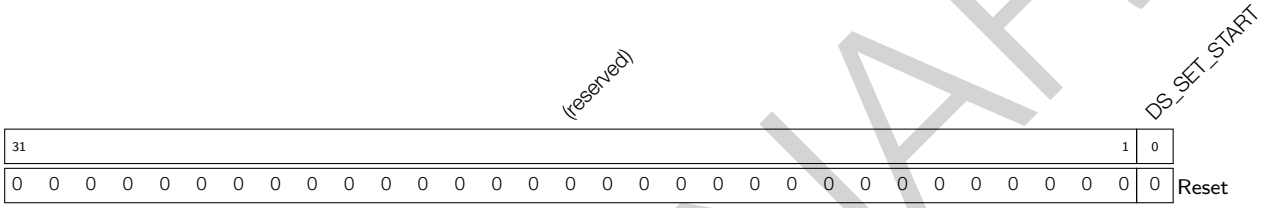
The addresses in this section are relative to the Digital Signature base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 20.1. DS_IV_*m*_REG (*m*: 0-3) (0x0630+4m*)**



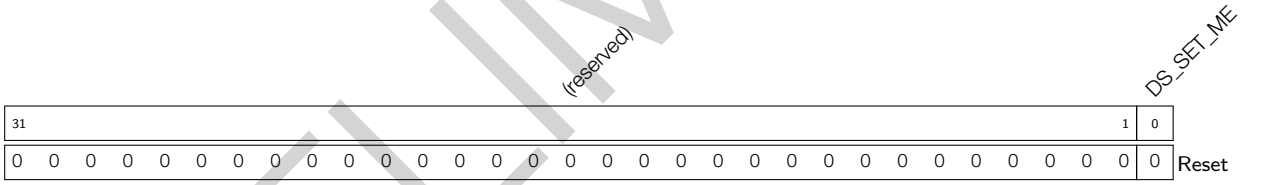
DS_IV_*m*_REG (*m*: 0-3) IV block data. (WO)

Register 20.2. DS_SET_START_REG (0x0E00)



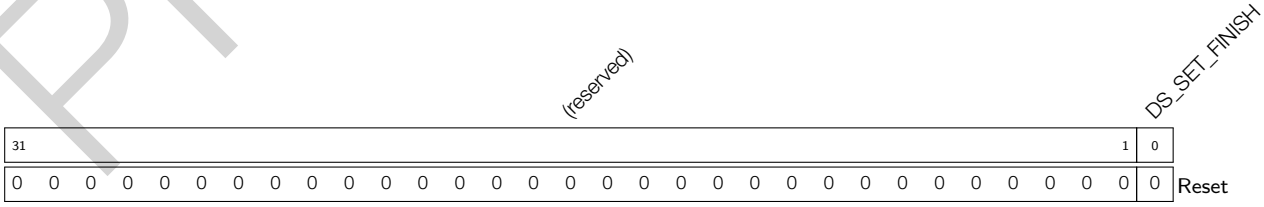
DS_SET_START Write 1 to this register to activate the DS peripheral. (WO)

Register 20.3. DS_SET_ME_REG (0x0E04)



DS_SET_ME Write 1 to this register to start DS operation. (WO)

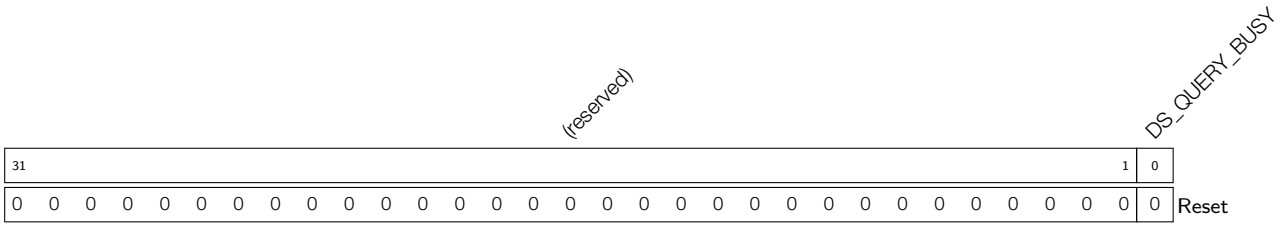
Register 20.4. DS_SET_FINISH_REG (0x0E08)



DS_SET_FINISH Write 1 to this register to end DS operation. (WO)

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Register 20.5. DS_QUERY_BUSY_REG (0x0E0C)



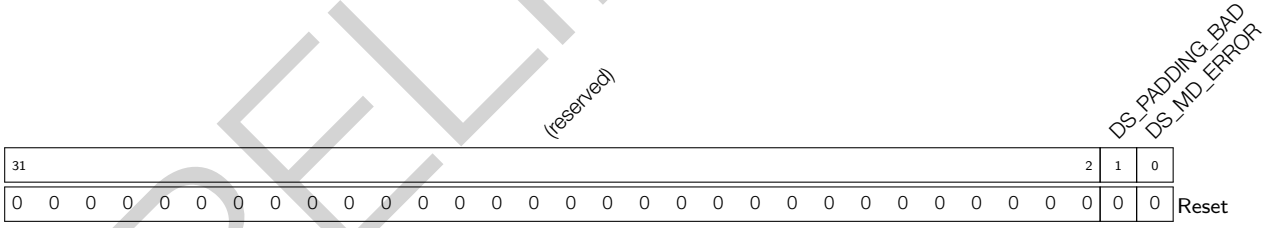
DS_QUERY_BUSY 1: The DS peripheral is busy; 0: The DS peripheral is idle. (RO)

Register 20.6. DS_QUERY_KEY_WRONG_REG (0x0E10)



DS_QUERY_KEY_WRONG 1-15: HMAC was activated, but the DS peripheral did not successfully receive the DS_KEY from the HMAC peripheral. (The biggest value is 15); 0: HMAC is not activated. (RO)

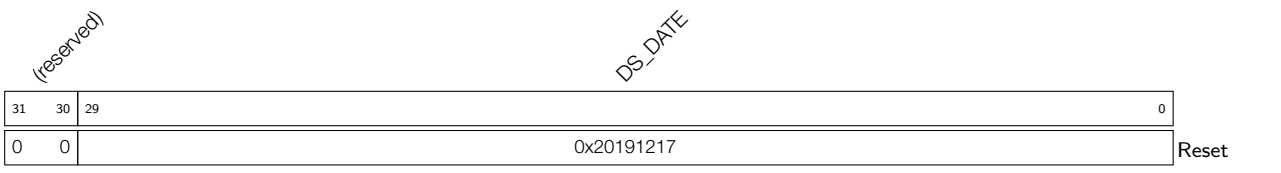
Register 20.7. DS_QUERY_CHECK_REG (0x0E14)



DS_PADDING_BAD 1: The padding check fails; 0: The padding check passes. (RO)

DS_MD_ERROR 1: The MD check fails; 0: The MD check passes. (RO)

Register 20.8. DS_DATE_REG (0x0E20)



DS_DATE Version control register. (R/W)

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21 External Memory Encryption and Decryption (XTS_AES)

21.1 Overview

The ESP32-S3 integrates an External Memory Encryption and Decryption module that complies with the XTS_AES standard algorithm specified in IEEE Std 1619-2007, providing security for users' application code and data stored in the external memory (flash and RAM). Users can store proprietary firmware and sensitive data (e.g., credentials for gaining access to a private network) to the external flash, or store general data to the external RAM.

21.2 Features

- General XTS_AES algorithm, compliant with IEEE Std 1619-2007
- Software-based manual encryption
- High-speed auto encryption, without software's participation
- High-speed auto decryption, without software's participation
- Encryption and decryption functions jointly determined by registers configuration, eFuse parameters, and boot mode

21.3 Module Structure

The External Memory Encryption and Decryption module consists of three blocks, namely the Manual Encryption block, Auto Encryption block, and Auto Decryption block. The module architecture is shown in Figure 21-1.

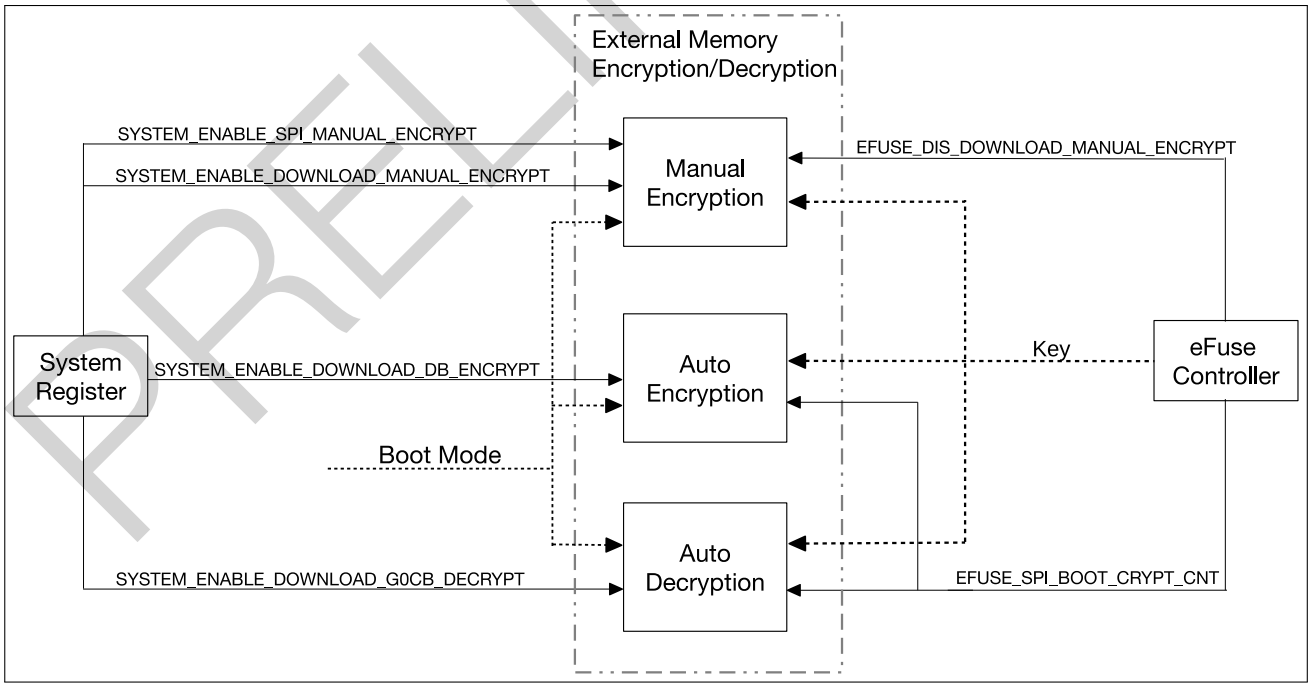


Figure 21-1. External Memory Encryption and Decryption Operation Settings

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The Manual Encryption block can encrypt instructions/data which will then be written to the external flash as ciphertext via SPI1.

When the CPU writes data to the external RAM through cache, the Auto Encryption block will automatically encrypt the data first, then the data will be written to the external RAM as ciphertext.

When the CPU reads from the external flash or external RAM through cache, the Auto Decryption block will automatically decrypt the ciphertext to retrieve instructions and data.

In the System Registers (SYSREG) peripheral, the following four bits in register SYSTEM_EXTERNAL_DEVICE_ENCRYPT_DECRYPT_CONTROL_REG are relevant to the external memory encryption and decryption:

- SYSTEM_ENABLE_DOWNLOAD_MANUAL_ENCRYPT
- SYSTEM_ENABLE_DOWNLOAD_G0CB_DECRYPT
- SYSTEM_ENABLE_DOWNLOAD_DB_ENCRYPT
- SYSTEM_ENABLE_SPI_MANUAL_ENCRYPT

The XTS_AES module also fetches two parameters from the peripheral 4 *eFuse Controller*, which are: EFUSE_DIS_DOWNLOAD_MANUAL_ENCRYPT and EFUSE_SPI_BOOT_CRYPT_CNT.

21.4 Functional Description

21.4.1 XTS Algorithm

The manual encryption and auto encryption/decryption all use the same algorithm, i.e., XTS algorithm. During implementation, the XTS algorithm is characterized by a "data unit" of 1024 bits, which is defined in the Section *XTS-AES encryption procedure* of *XTS-AES Tweakable Block Cipher* Standard. For more information about XTS-AES algorithm, please refer to IEEE Std 1619-2007.

21.4.2 Key

The Manual Encryption block, Auto Encryption block and Auto Decryption block share the same Key when implementing XTS algorithm. The Key is provided by the eFuse hardware and cannot be accessed by users.

The Key can be either 256-bit or 512-bit long. The value and length of the Key are determined by eFuse parameters. For easier description, now define:

- Block$_A$: the BLOCK in BLOCK4 ~ BLOCK9 whose key purpose is EFUSE_KEY_PURPOSE_XTS_AES_256_KEY_1. If Block$_A$ is true, then the 256-bit Key_A is stored in it.
- Block$_B$: the BLOCK in BLOCK4 ~ BLOCK9 whose key purpose is EFUSE_KEY_PURPOSE_XTS_AES_256_KEY_2. If Block$_B$ is true, then the 256-bit Key_B is stored in it.
- Block$_C$: the BLOCK in BLOCK4 ~ BLOCK9 whose key purpose is EFUSE_KEY_PURPOSE_XTS_AES_128_KEY. If Block$_C$ is true, then the 256-bit Key_C is stored in it.

There are five possibilities of how the Key is generated depending on whether Block$_A$, Block$_B$ and Block$_C$ exists or not, as shown in Table 21-1. In each case, the Key can be uniquely determined by Block$_A$, Block$_B$ or Block$_C$.

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Table 21-1. Key generated based on Key_A, Key_B and Key_C

Block$_A$	Block$_B$	Block$_C$	Key	Key Length (bit)
Yes	Yes	Don't care	$Key_A \| \| Key_B$	512
Yes	No	Don't care	$Key_A \| \| 0^{256}$	512
No	Yes	Don't care	$0^{256} \| \| Key_B$	512
No	No	Yes	Key_C	256
No	No	No	0^{256}	256

Notes:

"YES" indicates that the block exists; "NO" indicates that the block does not exist; "0^{256}" indicates a bit string that consists of 256-bit zeros; "||" is a bonding operator for joining one bit string to another.

For more information of key purposes, please refer to Table 4-2 *Secure Key Purpose Values* in Chapter 4 *eFuse Controller*.

21.4.3 Target Memory Space

The target memory space refers to a continuous address space in the external memory where the first encrypted ciphertext is stored. The target memory space can be uniquely determined by three relevant parameters: type, size and base address, whose definitions are listed below.

- Type: the $type$ of the target memory space, either external flash or external RAM. Value 0 indicates external flash, while 1 indicates external RAM.
- Size: the $size$ of the target memory space, indicating the number bytes encrypted in one encryption operation, which supports 16, 32 or 64 bytes.
- Base address: the $base\_addr$ of the target memory space. It is a 30-bit physical address, with range of 0x0000_0000 ~ 0x3FFF_FFFF. It should be aligned to $size$, i.e., $base\_addr \% size == 0$.

For example, if there are 16 bytes of instruction data need to be encrypted and written to address 0x130 ~ 0x13F in the external flash, then the target space is 0x130 ~ 0x13F, type is 0 (external flash), size is 16 (bytes), and base address is 0x130.

The encryption of any length (must be multiples of 16 bytes) of plaintext instruction/data can be completed separately in multiple operations, and each operation has individual target memory space and the relevant parameters.

For Auto Encryption/Decryption blocks, these parameters are automatically defined by hardware. For Manual Encryption block, these parameters should be configured manually by users.

Note:

The "tweak" defined in Chapter *5.1 Data units and tweaks* of IEEE Std 1619-2007 is a 128-bit non-negative integer ($tweak$), which can be generated according to $tweak = type * 2^{30}$ + ($base\_addr$ & 0x3FFFFF80). The lowest 7 bits and the highest 97 bits in $tweak$ are always zero.

21.4.4 Data Padding

For Auto Encryption/Decryption blocks, data padding is automatically completed by hardware. For Manual Encryption block, data padding should be completed manually by users. The Manual Encryption block has a

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registers block which consists of 16 registers, i.e., XTS_AES_PLAIN_n_REG (n: 0-15), that are dedicated to data padding and can store up to 512 bits of plaintext instructions/data.

Actually, the Manual Encryption block does not care where the plaintext comes from, but only where the ciphertext will be stored. Because of the strict correspondence between plaintext and ciphertext, in order to better describe how the plaintext is stored in the register block, we assume that the plaintext is stored in the target memory space in the first place and replaced by ciphertext after encryption. Therefore, the following description no longer has the concept of "plaintext", but uses "target memory space" instead. Please note that the plaintext can come from everywhere in actual use, but users should understand how the plaintext is stored in the register block.

How mapping works between target memory space and registers:

Assume a word in the target memory space is stored in $address$, define $offset = address\%64$, $n = \frac{offset}{4}$, then the word will be stored in register XTS_AES_PLAIN_n_REG.

For example, if the $size$ of the target memory space is 64, then all the 16 registers will be used for data storage. The mapping between $offset$ and registers is shown in Table 21-2.

Table 21-2. Mapping Between Offsets and Registers

$offset$	Register	$offset$	Register
0x00	XTS_AES_PLAIN_0_REG	0x20	XTS_AES_PLAIN_8_REG
0x04	XTS_AES_PLAIN_1_REG	0x24	XTS_AES_PLAIN_9_REG
0x08	XTS_AES_PLAIN_2_REG	0x28	XTS_AES_PLAIN_10_REG
0x0C	XTS_AES_PLAIN_3_REG	0x2C	XTS_AES_PLAIN_11_REG
0x10	XTS_AES_PLAIN_4_REG	0x30	XTS_AES_PLAIN_12_REG
0x14	XTS_AES_PLAIN_5_REG	0x34	XTS_AES_PLAIN_13_REG
0x18	XTS_AES_PLAIN_6_REG	0x38	XTS_AES_PLAIN_14_REG
0x1C	XTS_AES_PLAIN_7_REG	0x3C	XTS_AES_PLAIN_15_REG

21.4.5 Manual Encryption Block

The Manual Encryption block is a peripheral module. It is equipped with registers and can be accessed by the CPU directly. Registers embedded in this block, the System Registers (SYSREG) peripheral, eFuse parameters, and boot mode jointly configure and use this module. Please note that the Manual Encryption block can only encrypt for storage in the external flash.

The Manual Encryption block is operational only under certain conditions. The operating conditions are:

- In SPI Boot mode

  If bit SYSTEM_ENABLE_SPI_MANUAL_ENCRYPT in register SYSTEM_EXTERNAL_DEVICE_ENCRYPT_DECRYPT_CONTROL_REG is 1, the Manual Encryption block can be enabled. Otherwise, it is not operational.

- In Download Boot mode

  If bit SYSTEM_ENABLE_DOWNLOAD_MANUAL_ENCRYPT in register SYSTEM_EXTERNAL_DEVICE_ENCRYPT_DECRYPT_CONTROL_REG is 1 and the eFuse parameter

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EFUSE_DIS_DOWNLOAD_MANUAL_ENCRYPT is 0, the Manual Encryption block can be enabled. Otherwise, it is not operational.

Note:

- Even though the CPU can skip cache and get the encrypted instruction/data directly by reading the external memory, users can by no means access Key.

21.4.6 Auto Encryption Block

The Auto Encryption block is not a conventional peripheral, so it does not have any registers and cannot be accessed by the CPU directly. The System Registers (SYSREG) peripheral, eFuse parameters, and boot mode jointly configure and use this block.

The Auto Encryption block is operational only under certain conditions. The operating conditions are:

- In SPI Boot mode

  If the first bit or the third bit in parameter SPI_BOOT_CRYPT_CNT (3 bits) is set to 1, then the Auto Encryption block can be enabled. Otherwise, it is not operational.

- In Download Boot mode

  If bit SYSTEM_ENABLE_DOWNLOAD_DB_ENCRYPT in register SYSTEM_EXTERNAL_DEVICE_ENCRYPT_DECRYPT_CONTROL_REG is 1, the Auto Encryption block can be enabled. Otherwise, it is not operational.

Note:

- When the Auto Encryption block is enabled, it will automatically encrypt data if the CPU writes data to the external RAM, and then the encrypted ciphertext will be written to the external RAM. The entire encryption process does not need software participation and is transparent to the cache. Users can by no means obtain the encryption Key during the process.
- When the Auto Encryption block is disabled, it will ignore the CPU's access request to cache and do not process the data. Therefore, the data will be written to the external RAM as plaintext directly.

21.4.7 Auto Decryption Block

The Auto Decryption block is not a conventional peripheral, so it does not have any registers and cannot be accessed by the CPU directly. The System Registers (SYSREG) peripheral, eFuse parameters, and boot mode jointly configure and use this block.

The Auto Decryption block is operational only under certain conditions. The operating conditions are:

- In SPI Boot mode

  If the first bit or the third bit in parameter SPI_BOOT_CRYPT_CNT (3 bits) is set to 1, then the Auto Decryption block can be enabled. Otherwise, it is not operational.

- In Download Boot mode

  If bit SYSTEM_ENABLE_DOWNLOAD_G0CB_DECRYPT in register SYSTEM_EXTERNAL_DEVICE_ENCRYPT_DECRYPT_CONTROL_REG is 1, the Auto Decryption block

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can be enabled. Otherwise, it is not operational.

Note:

- When the Auto Decryption block is enabled, it will automatically decrypt the ciphertext if the CPU reads instructions/data from the external memory via cache to retrieve the instructions/data. The entire decryption process does not need software participation and is transparent to the cache. Users can by no means obtain the decryption Key during the process.
- When the Auto Decryption block is disabled, it does not have any effect on the contents stored in the external memory, no matter they are encrypted or not. Therefore, what the CPU reads via cache is the original information stored in the external memory.

21.5 Software Process

When the Manual Encryption block operates, software needs to be involved in the process. The steps are as follows:

1. Configure XTS_AES:
   - Set register XTS_AES_DESTINATION_REG to $type$ = 0.
   - Set register XTS_AES_PHYSICAL_ADDRESS_REG to $base\_addr$.
   - Set register XTS_AES_LINESIZE_REG to $\frac{size}{32}$.

   For definitions of $type$, $base\_addr$ and $size$, please refer to Section 21.4.3.
2. Pad plaintext data to the registers block XTS_AES_PLAIN_*n*_REG (*n*: 0-15). For detailed information, please refer to Section 21.4.4.
   Please pad data to registers according to your actual needs, and the unused ones could be set to arbitrary values.
3. Wait for Manual Encrypt block to be idle. Poll register XTS_AES_STATE_REG until the software reads 0.
4. Trigger manual encryption by writing 1 to register XTS_AES_TRIGGER_REG.
5. Wait for the encryption process. Poll register XTS_AES_STATE_REG until the software reads 2.
   Step 1 to 5 are the steps of encrypting plaintext instructions with the Manual Encryption block using the Key.
6. Grant the ciphertext access to SPI1. Write 1 to register XTS_AES_RELEASE_REG to grant SPI1 the access to the encrypted ciphertext. After this, the value of register XTS_AES_STATE_REG will become 3.
7. Call SPI1 to write the ciphertext in the external flash (see Chapter 3 *SPI Controller (SPI) [to be added later]*).
8. Destroy the ciphertext. Write 1 to register XTS_AES_DESTROY_REG. After this, the value of register XTS_AES_STATE_REG will become 0.

Repeat above steps to meet plaintext instructions/data encryption demands.

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21.6 Register Summary

The addresses in this section are relative to the External Memory Encryption and Decryption base address provided in Table 3-3 in Chapter 3 *System and Memory*.

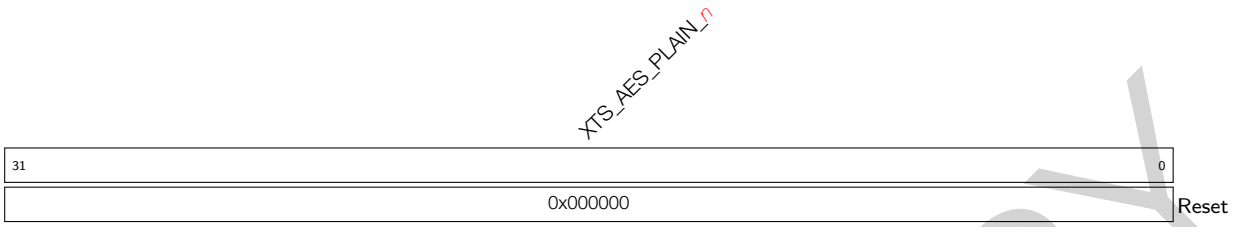
Name	Description	Address	Access
Plaintext Register Heap			
XTS_AES_PLAIN_0_REG	Plaintext register 0	0x0000	R/W
XTS_AES_PLAIN_1_REG	Plaintext register 1	0x0004	R/W
XTS_AES_PLAIN_2_REG	Plaintext register 2	0x0008	R/W
XTS_AES_PLAIN_3_REG	Plaintext register 3	0x000C	R/W
XTS_AES_PLAIN_4_REG	Plaintext register 4	0x0010	R/W
XTS_AES_PLAIN_5_REG	Plaintext register 5	0x0014	R/W
XTS_AES_PLAIN_6_REG	Plaintext register 6	0x0018	R/W
XTS_AES_PLAIN_7_REG	Plaintext register 7	0x001C	R/W
XTS_AES_PLAIN_8_REG	Plaintext register 8	0x0020	R/W
XTS_AES_PLAIN_9_REG	Plaintext register 9	0x0024	R/W
XTS_AES_PLAIN_10_REG	Plaintext register 10	0x0028	R/W
XTS_AES_PLAIN_11_REG	Plaintext register 11	0x002C	R/W
XTS_AES_PLAIN_12_REG	Plaintext register 12	0x0030	R/W
XTS_AES_PLAIN_13_REG	Plaintext register 13	0x0034	R/W
XTS_AES_PLAIN_14_REG	Plaintext register 14	0x0038	R/W
XTS_AES_PLAIN_15_REG	Plaintext register 15	0x003C	R/W
Configuration Registers			
XTS_AES_LINESIZE_REG	Configures the size of target memory space	0x0040	R/W
XTS_AES_DESTINATION_REG	Configures the type of the external memory	0x0044	R/W
XTS_AES_PHYSICAL_ADDRESS_REG	Physical address	0x0048	R/W
Contro/Status Registers			
XTS_AES_TRIGGER_REG	Activates AES algorithm	0x004C	WO
XTS_AES_RELEASE_REG	Release control	0x0050	WO
XTS_AES_DESTROY_REG	Destroys control	0x0054	WO
XTS_AES_STATE_REG	Status register	0x0058	RO
Version Register			
XTS_AES_DATE_REG	Version control register	0x005C	RO

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21.7 Registers

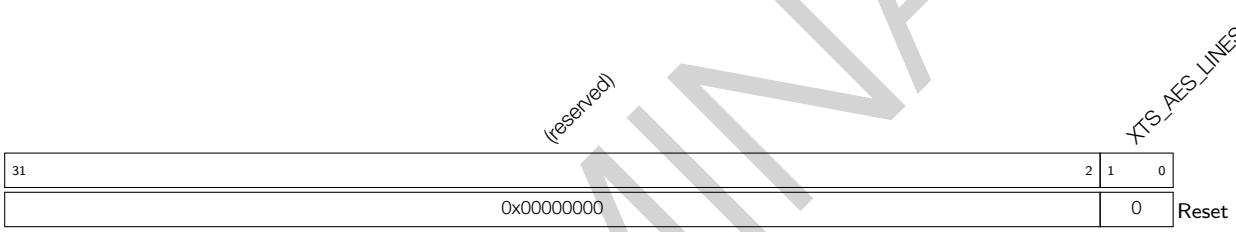
The addresses in this section are relative to the External Memory Encryption and Decryption base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 21.1. XTS_AES_PLAIN_*n*_REG (*n*: 0-15) (0x0000+4*n)



XTS_AES_PLAIN_*n* Stores *n*th 32-bit piece of plain text. (R/W)

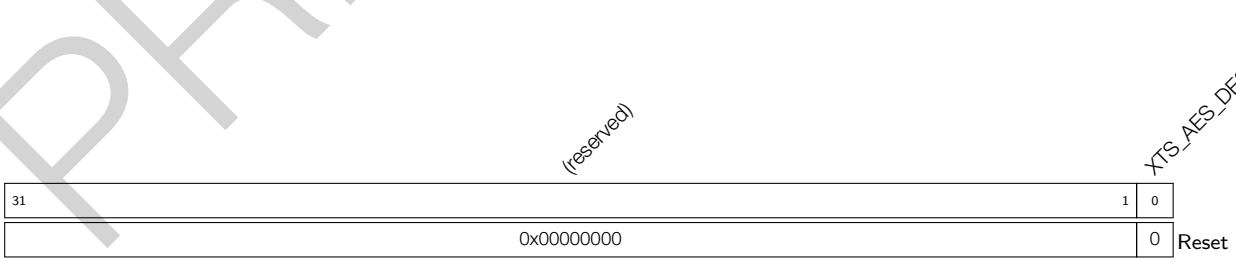
Register 21.2. XTS_AES_LINESIZE_REG (0x0040)



XTS_AES_LINESIZE Configures the data size of one encryption.

- 0: 16 bytes;
- 1: 32 bytes;
- 2: 64 bytes. (R/W)

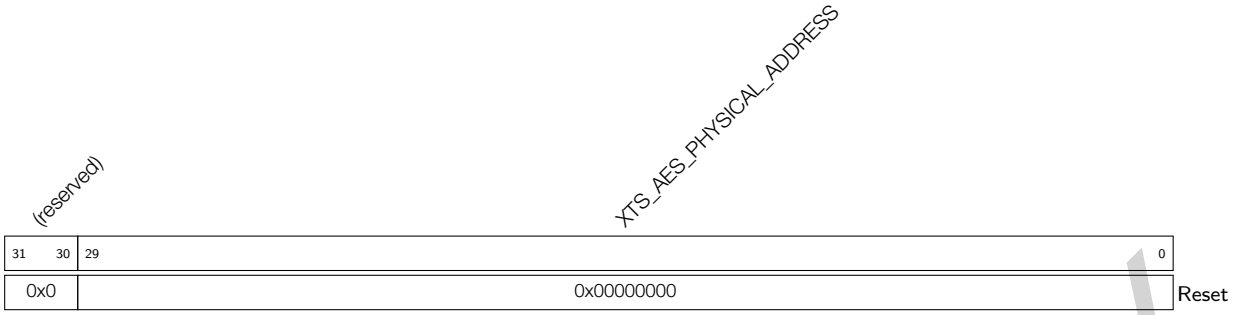
Register 21.3. XTS_AES_DESTINATION_REG (0x0044)



XTS_AES_DESTINATION Configures the type of the external memory. Currently, it must be set to 0, as the Manual Encryption block only supports flash encryption. Errors may occur if users write 1. 0: flash; 1: external RAM. (R/W)

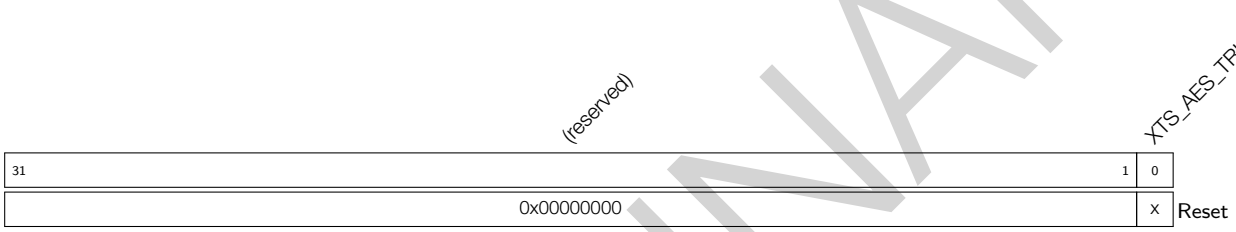
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Register 21.4. XTS_AES_PHYSICAL_ADDRESS_REG (0x0048)



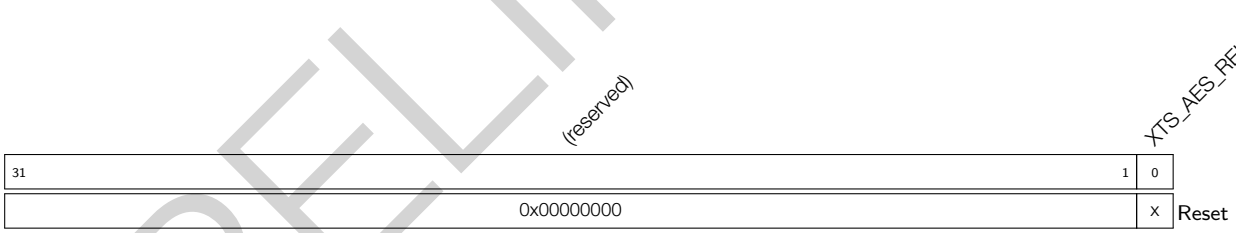
XTS_AES_PHYSICAL_ADDRESS Physical address. (R/W)

Register 21.5. XTS_AES_TRIGGER_REG (0x004C)



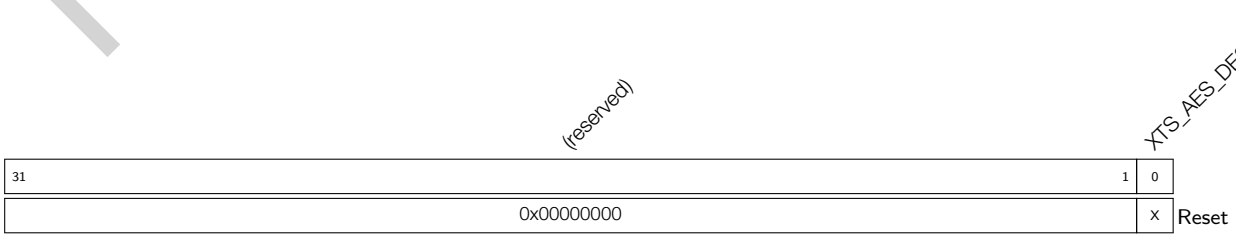
XTS_AES_TRIGGER Write 1 to enable manual encryption. (WO)

Register 21.6. XTS_AES_RELEASE_REG (0x0050)



XTS_AES_RELEASE Write 1 to grant SPI1 access to encrypted result. (WO)

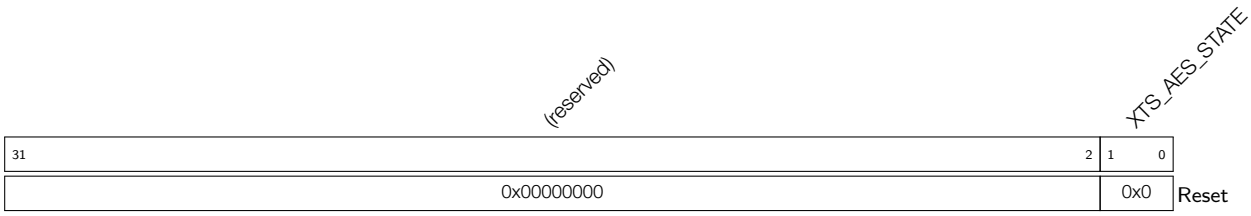
Register 21.7. XTS_AES_DESTROY_REG (0x0054)



XTS_AES_DESTROY Write 1 to destroy encrypted result. (WO)

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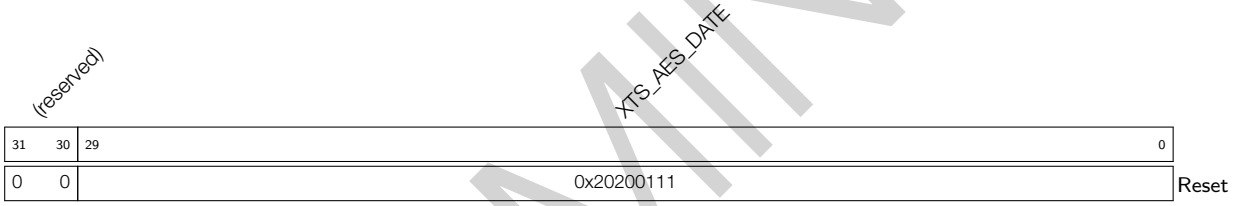
Register 21.8. XTS_AES_STATE_REG (0x0058)



XTS_AES_STATE Indicates the status of the Manual Encryption block. (RO)

- 0x0 (XTS_AES_IDLE): idle;
- 0x1 (XTS_AES_BUSY): busy with encryption;
- 0x2 (XTS_AES_DONE): encryption is completed, but the encrypted result is not accessible to SPI;
- 0x3 (XTS_AES_RELEASE): encrypted result is accessible to SPI.

Register 21.9. XTS_AES_DATE_REG (0x005C)



XTS_AES_DATE Version control register. (R/W)

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22 Clock Glitch Detection

22.1 Overview

The Clock Glitch Detection module on ESP32-S3 detects glitches in external crystal XTAL_CLK signals, and generates a system reset signal (see Chapter 6 *Reset and Clock*) when detecting glitches to reset the whole digital circuit including RTC. By doing so, it prevents attackers from injecting glitches on external crystal XTAL_CLK clock to compromise ESP32-S3 and thus strengthens chip security.

22.2 Functional Description

22.2.1 Clock Glitch Detection

The Clock Glitch Detection module on ESP32-S3 monitors input clock signals from XTAL_CLK. If it detects a glitch, namely a clock pulse (a or b in the figure below) with a width shorter than 3 ns, input clock signals from XTAL_CLK are blocked.

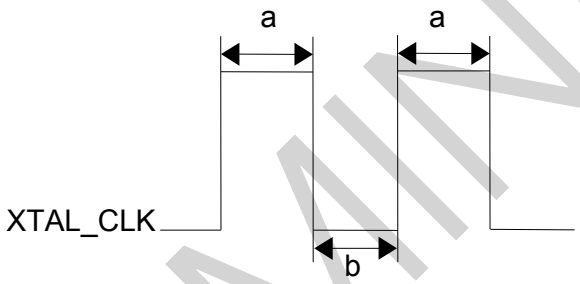


Figure 22-1. XTAL_CLK Pulse Width

22.2.2 Reset

Once detecting a glitch on XTAL_CLK that affects the circuit's normal operation, the Clock Glitch Detection module triggers a system reset if RTC_CNTL_GLITCH_RST_EN bit is enabled. By default, this bit is set to enable a reset.

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23 Random Number Generator (RNG)

23.1 Introduction

The ESP32-S3 contains a true random number generator, which generates 32-bit random numbers that can be used for cryptographical operations, among other things.

23.2 Features

The random number generator in ESP32-S3 generates true random numbers, which means random number generated from a physical process, rather than by means of an algorithm. No number generated within the specified range is more or less likely to appear than any other number.

23.3 Functional Description

Every 32-bit value that the system reads from the RNG_DATA_REG register of the random number generator is a true random number. These true random numbers are generated based on the thermal noise in the system and the asynchronous clock mismatch.

Thermal noise comes from the high-speed ADC or SAR ADC or both. Whenever the high-speed ADC or SAR ADC is enabled, bit streams will be generated and fed into the random number generator through an XOR logic gate as random seeds.

When the RTC20M_CLK clock is enabled for the digital core, the random number generator will also sample RTC20M_CLK (20 MHz) as a random bit seed. RTC20M_CLK is an asynchronous clock source and it increases the RNG entropy by introducing circuit metastability. However, to ensure maximum entropy, it's recommended to always enable an ADC source as well.

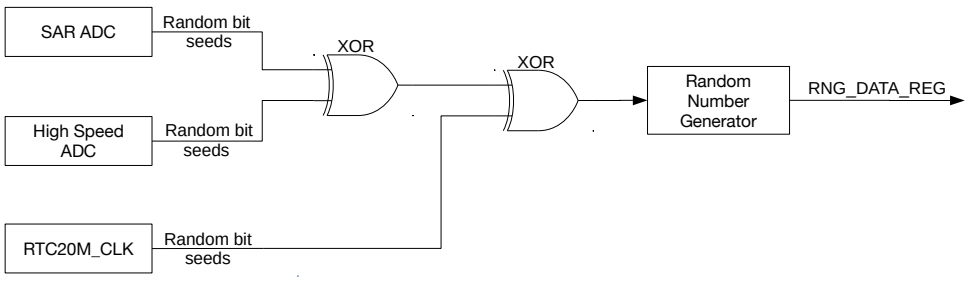


Figure 23-1. Noise Source

When there is noise coming from the SAR ADC, the random number generator is fed with a 2-bit entropy in one clock cycle of RTC20M_CLK (20 MHz), which is generated from an internal RC oscillator (see Chapter 6 *Reset and Clock* for details). Thus, it is advisable to read the RNG_DATA_REG register at a maximum rate of 500 kHz to obtain the maximum entropy.

When there is noise coming from the high-speed ADC, the random number generator is fed with a 2-bit entropy in one APB clock cycle, which is normally 80 MHz. Thus, it is advisable to read the RNG_DATA_REG register at a maximum rate of 5 MHz to obtain the maximum entropy.

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23.4 Programming Procedure

When using the random number generator, make sure at least either the SAR ADC, high-speed ADC, or RTC20M_CLK is enabled. Otherwise, pseudo-random numbers will be returned.

- SAR ADC can be enabled by using the DIG ADC controller. For details, please refer to Chapter 4 *On-Chip Sensors and Analog Signal Processing [to be added later]*.
- High-speed ADC is enabled automatically when the Wi-Fi or Bluetooth modules is enabled.
- RTC20M_CLK is enabled by setting the RTC_CNTL_DIG_CLK20M_EN bit in the RTC_CNTL_CLK_CONF_REG register.

Note:
Note that, when the Wi-Fi module is enabled, the value read from the high-speed ADC can be saturated in some extreme cases, which lowers the entropy. Thus, it is advisable to also enable the SAR ADC as the noise source for the random number generator for such cases.

When using the random number generator, read the RNG_DATA_REG register multiple times until sufficient random numbers have been generated. Ensure the rate at which the register is read does not exceed the frequencies described in section 23.3 above.

23.5 Register Summary

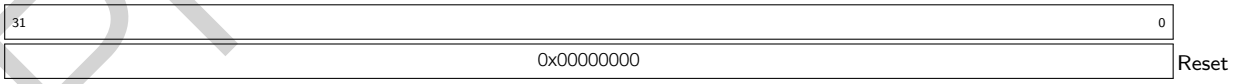
The address in the following table is relative to the random number generator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
RNG_DATA_REG	Random number data	0x0110	RO

23.6 Register

The address in this section is relative to the random number generator base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 23.1. RNG_DATA_REG (0x0110)



RNG_DATA Random number source. (RO)

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24 UART Controller (UART)

24.1 Overview

In embedded system applications, data are required to be transferred in a simple way with minimal system resources. This can be achieved by a Universal Asynchronous Receiver/Transmitter (UART), which flexibly exchanges data with other peripheral devices in full-duplex mode. ESP32-S3 has three UART controllers compatible with various UART devices. They support Infrared Data Association (IrDA) and RS485 transmission.

Each of the three UART controllers has a group of registers that function identically. In this chapter, the three UART controllers are referred to as UART*n*, in which *n* denotes 0, 1, or 2.

A UART is a character-oriented data link for asynchronous communication between devices. Such communication does not provide any clock signal to send data. Therefore, in order to communicate successfully, the transmitter and the receiver must operate at the same baud rate with the same stop bit and parity bit.

A UART data frame usually begins with one start bit, followed by data bits, one parity bit (optional) and one or more stop bits. UART controllers on ESP32-S3 support various lengths of data bits and stop bits. These controllers also support software and hardware flow control as well as GDMA for seamless high-speed data transfer. This allows developers to use multiple UART ports at minimal software cost.

24.2 Features

Each UART controller has the following features:

- Three clock sources that can be divided
- Programmable baud rate
- 1024 x 8-bit RAM shared by TX FIFOs and RX FIFOs of the three UART controllers
- Full-duplex asynchronous communication
- Automatic baud rate detection of input signals
- Data bits ranging from 5 to 8
- Stop bits of 1, 1.5, 2 or 3 bits
- Parity bit
- Special character AT_CMD detection
- RS485 protocol
- IrDA protocol
- High-speed data communication using GDMA
- UART as wake-up source
- Software and hardware flow control

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24.3 UART Structure

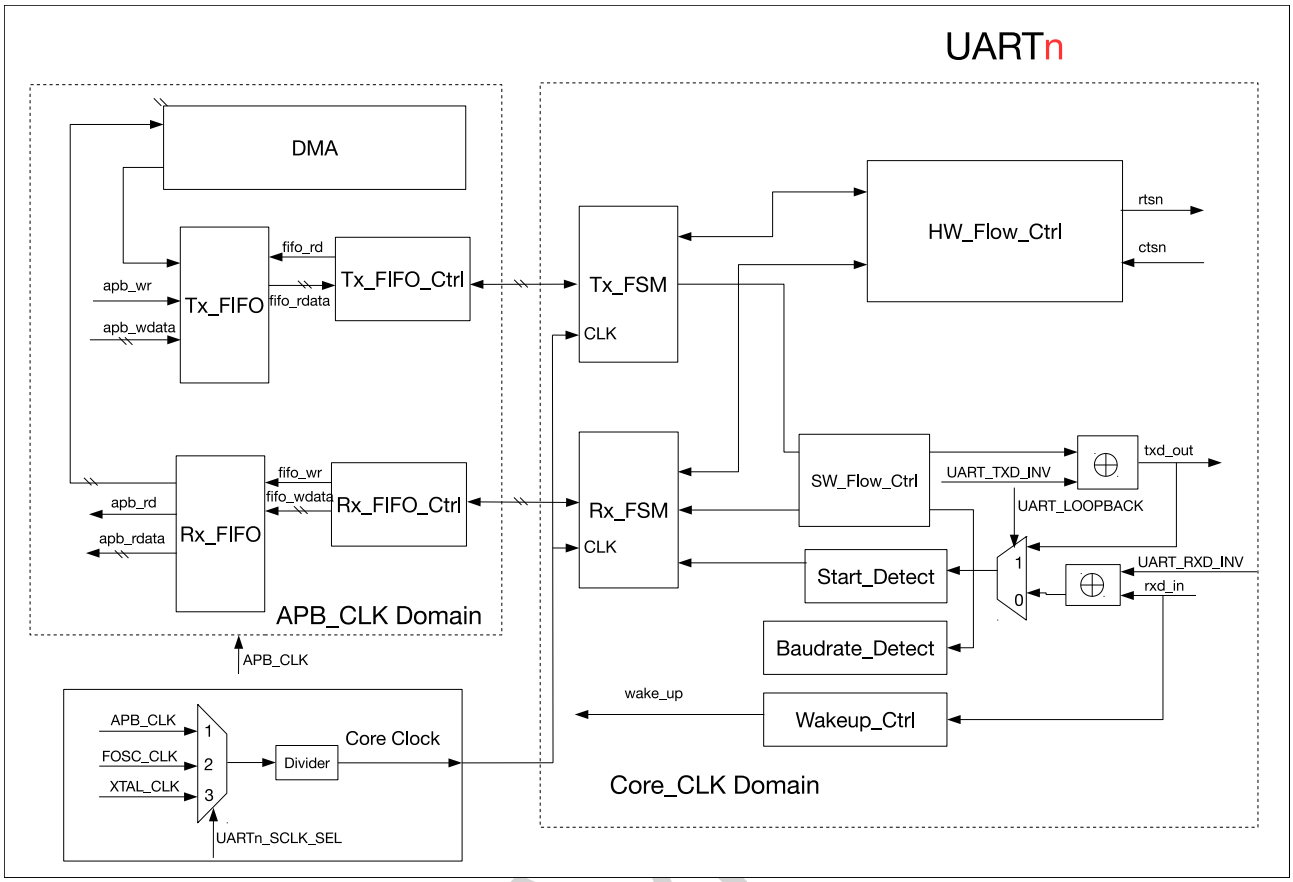


Figure 24-1. UART Structure

Figure 24-1 shows the basic structure of a UART controller. A UART controller works in two clock domains, namely APB_CLK domain and Core Clock domain (the UART Core's clock domain). The UART Core has three clock sources: 80 MHz APB_CLK, FOSC_CLK and external crystal clock XTAL_CLK (for details, please refer to Chapter 6 *Reset and Clock*), which are selected by configuring UART_SCLK_SEL. The selected clock source is divided by a divider to generate clock signals that drive the UART Core.

A UART controller is broken down into two parts: a transmitter and a receiver.

The transmitter contains a FIFO, called TX FIFO (or Tx_FIFO), which buffers data to be sent. Software can write data to the Tx_FIFO either via the APB bus, or using GDMA. Tx_FIFO_Ctrl controls writing and reading the Tx_FIFO. When Tx_FIFO is not empty, Tx_FSM reads data bits in the data frame via Tx_FIFO_Ctrl, and converts them into a bitstream. The levels of output signal txd_out can be inverted by configuring UART_TXD_INV field.

The receiver also contains a FIFO, called RX FIFO (or Rx_FIFO), which buffers received data. The levels of input signal rxd_in can be inverted by configuring UART_RXD_INV field. Baudrate_Detect measures the baud rate of input signal rxd_in by detecting its minimum pulse width. Start_Detect detects the start bit in a data frame. If the start bit is detected, Rx_FSM stores data bits in the data frame into Rx_FIFO by Rx_FIFO_Ctrl. Software can read data from Rx_FIFO via the APB bus, or receive data using GDMA.

HW_Flow_Ctrl controls rxd_in and txd_out data flows by standard UART RTS and CTS flow control signals (rtsn_out and ctsn_in). SW_Flow_Ctrl controls data flows by automatically adding special characters to outgoing

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data and detecting special characters in incoming data.

When a UART controller is in Light-sleep mode (see Chapter 5 *Low-Power Management (RTC_CNTL) [to be added later]* for more details), Wakeup_Ctrl counts up rising edges of rxd_in. When the number reaches UART_ACTIVE_THRESHOLD + 2, a wake_up signal is generated and sent to RTC, which then wakes up the ESP32-S3 chip.

24.4 Functional Description

24.4.1 Clock and Reset

UART controllers are asynchronous. their configuration registers, TX FIFOs, and RX FIFOs are in APB_CLK domain, while the module controlling transmission and reception (i.e. UART Core) is in Core Clock domain. The latter can be sourced out of three clocks, namely APB_CLK, FOSC_CLK and external crystal clock XTAL_CLK, which can be selected by configuring UART_SCLK_SEL. The selected clock source can be divided. This divider supports fractional division, and the divisor is equal to:

$$UART\_SCLK\_DIV\_NUM + \frac{UART\_SCLK\_DIV\_B}{UART\_SCLK\_DIV\_A}$$

The divisor ranges from 1 ~ 256.

When the frequency of the UART Core's clock is higher than the frequency needed to generate baud rate, the UART Core can be clocked at a lower frequency by the divider, in order to reduce power consumption. Usually, the UART Core's clock frequency is lower than the APB_CLK's frequency, and can be divided by the largest divisor value when higher than the frequency needed to generate baud rate. The frequency of the UART Core's clock can also be at most twice higher than the APB_CLK. The clock for the UART transmitter and the UART receiver can be controlled independently. To enable the clock for the UART transmitter, UART_TX_SCLK_EN shall be set; to enable the clock for the UART receiver, UART_RX_SCLK_EN shall be set.

Section 24.5 explains the procedure to ensure that the configured register values are synchronized between APB_CLK domain and Core Clock domain.

Section 24.5.2.1 explains the procedure to reset the whole UART controller. Note that it is not recommended to only reset the APB clock domain module or UART Core.

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24.4.2 UART RAM

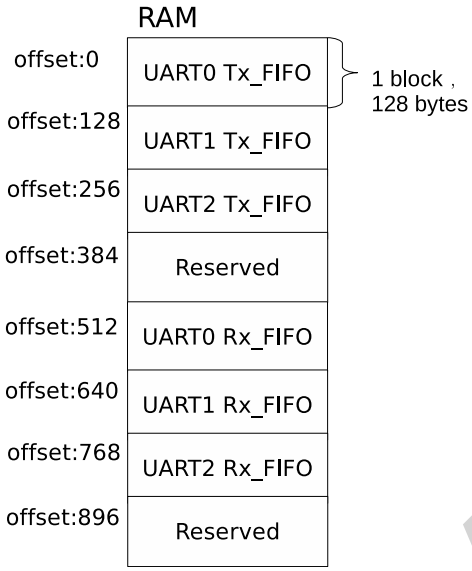


Figure 24-2. UART Controllers Sharing RAM

All three UART controllers on ESP32-S3 share 1024 × 8 bits of RAM. As Figure 24-2 illustrates, the RAM is divided into 8 blocks, each has 128 × 8 bits. Figure 24-2 shows how many RAM blocks are allocated by default to TX and RX FIFOs for each of the three UART controllers. UART*n* Tx_FIFO can be expanded by configuring UART_TX_SIZE, while UART*n* Rx_FIFO can be expanded by configuring UART_RX_SIZE. Some limits are imposed:

- UART0 Tx_FIFO can be increased up to 8 blocks (the whole RAM);
- UART1 Tx_FIFO can be increased up to 7 blocks (from offset 128 to the end address);
- UART2 Tx_FIFO can be increased up to 6 blocks (from offset 256 to the end address);
- UART0 Rx_FIFO can be increased up to 4 blocks (from offset 512 to the end address);
- UART1 Rx_FIFO can be increased up to 3 blocks (from offset 640 to the end address);
- UART2 Rx_FIFO can be increased up to 2 blocks (from offset 768 to the end address).

Please note that starting addresses of all FIFOs are fixed, so expanding one FIFO may take up the default space of other FIFOs. For example, by setting UART_TX_SIZE of UART0 to 2, the size of UART0 Tx_FIFO is increased by 128 bytes (from offset 0 to offset 255). In this case, UART0 Tx_FIFO takes up the default space for UART1 Tx_FIFO, and UART1's transmitting function cannot be used as a result.

When neither of the three UART controllers is active, RAM can enter low-power mode by setting UART_MEM_FORCE_PD.

UART*n* Tx_FIFO is reset by setting UART_TXFIFO_RST. UART*n* Rx_FIFO is reset by setting UART_RXFIFO_RST.

The "empty" signal threshold for Tx_FIFO is configured by setting UART_TXFIFO_EMPTY_THRHD. When data stored in Tx_FIFO is less than UART_TXFIFO_EMPTY_THRHD, a UART_TXFIFO_EMPTY_INT interrupt is generated. The "full" signal threshold for Rx_FIFO is configured by setting UART_RXFIFO_FULL_THRHD. When data stored in Rx_FIFO is equal to or greater than UART_RXFIFO_FULL_THRHD, a UART_RXFIFO_FULL_INT

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interrupt is generated. In addition, when Rx_FIFO receives more data than its capacity, a UART_RXFIFO_OVF_INT interrupt is generated.

TX FIFO and RX FIFO can be accessed via the APB bus or GDMA. Access via the APB bus is performed through register UART_FIFO_REG. You can put data into TX FIFO by writing UART_RXFIFO_RD_BYTE, and get data in RX FIFO by reading this exact same field. For access via GDMA, please refer to Section 24.4.10.

24.4.3 Baud Rate Generation and Detection

24.4.3.1 Baud Rate Generation

Before a UART controller sends or receives data, the baud rate should be configured by setting corresponding registers. The baud rate generator of a UART controller functions by dividing the input clock source. It can divide the clock source by a fractional amount. The divisor is configured by UART_CLKDIV_REG: UART_CLKDIV for the integer part, and UART_CLKDIV_FRAG for the fractional part. When using the 80 MHz input clock, the UART controller supports a maximum baud rate of 5 Mbaud.

The divisor of the baud rate is equal to

$$UART\_CLKDIV + \frac{UART\_CLKDIV\_FRAG}{16}$$

meaning that the final baud rate is equal to

$$\frac{INPUT\_FREQ}{UART\_CLKDIV + \frac{UART\_CLKDIV\_FRAG}{16}}$$

where INPUT_FREQ is the frequency of UART Core's source clock. For example, if UART_CLKDIV = 694 and UART_CLKDIV_FRAG = 7 then the divisor value is

$$694 + \frac{7}{16} = 694.4375$$

When UART_CLKDIV_FRAG is 0, the baud rate generator is an integer clock divider where an output pulse is generated every UART_CLKDIV input pulses.

When UART_CLKDIV_FRAG is not 0, the divider is fractional and the output baud rate clock pulses are not strictly uniform. As shown in Figure 24-3, for every 16 output pulses, the frequency of some pulses is INPUT_FREQ/(UART_CLKDIV + 1), and the frequency of the other pulses is INPUT_FREQ/UART_CLKDIV. A total of UART_CLKDIV_FRAG output pulses are generated by dividing (UART_CLKDIV + 1) input pulses, and the remaining (16 - UART_CLKDIV_FRAG) output pulses are generated by dividing UART_CLKDIV input pulses.

The output pulses are interleaved as shown in Figure 24-3 below, to make the output timing more uniform:

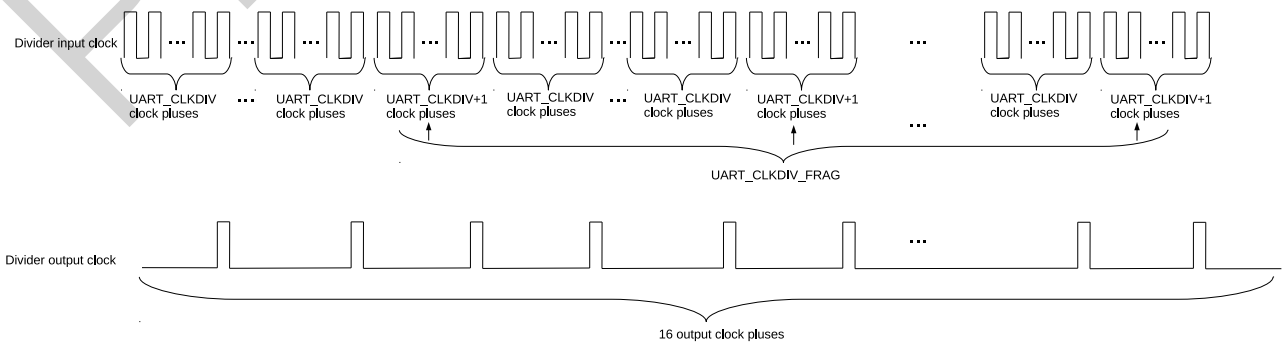


Figure 24-3. UART Controllers Division

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To support IrDA (see Section 24.4.6 for details), the fractional clock divider for IrDA data transmission generates clock signals divided by 16 × UART_CLKDIV_REG. This divider works similarly as the one elaborated above: it takes UART_CLKDIV/16 as the integer value and the lowest four bits of UART_CLKDIV as the fractional value.

24.4.3.2 Baud Rate Detection

Automatic baud rate detection (Autobaud) on UARTs is enabled by setting UART_AUTOBAUD_EN. The Baudrate_Detect module shown in Figure 24-1 filters any noise whose pulse width is shorter than UART_GLITCH_FILT.

Before communication starts, the transmitter can send random data to the receiver for baud rate detection. UART_LOWPULSE_MIN_CNT stores the minimum low pulse width, UART_HIGHPULSE_MIN_CNT stores the minimum high pulse width, UART_POSEDGE_MIN_CNT stores the minimum pulse width between two rising edges, and UART_NEGEDGE_MIN_CNT stores the minimum pulse width between two falling edges. These four fields are read by software to determine the transmitter's baud rate.

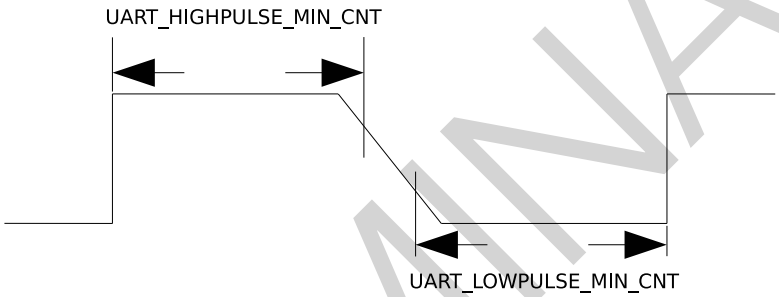


Figure 24-4. The Timing Diagram of Weak UART Signals Along Falling Edges

Baud rate can be determined in the following three ways:

1. Normally, to avoid sampling erroneous data along rising or falling edges in metastable state, which results in inaccuracy of UART_LOWPULSE_MIN_CNT or UART_HIGHPULSE_MIN_CNT, use a weighted average of these two values to eliminate errors. In this case, baud rate is calculated as follows:

$$B_{\text{uart}} = \frac{f_{\text{clk}}}{(\text{UART\_LOWPULSE\_MIN\_CNT} + \text{UART\_HIGHPULSE\_MIN\_CNT} + 2)/2}$$

2. If UART signals are weak along falling edges as shown in Figure 24-4, which leads to inaccurate average of UART_LOWPULSE_MIN_CNT and UART_HIGHPULSE_MIN_CNT, use UART_POSEDGE_MIN_CNT to determine the transmitter's baud rate as follows:

$$B_{\text{uart}} = \frac{f_{\text{clk}}}{(\text{UART\_POSEDGE\_MIN\_CNT} + 1)/2}$$

3. If UART signals are weak along rising edges, use UART_NEGEDGE_MIN_CNT to determine the transmitter's baud rate as follows:

$$B_{\text{uart}} = \frac{f_{\text{clk}}}{(\text{UART\_NEGEDGE\_MIN\_CNT} + 1)/2}$$

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24.4.4 UART Data Frame

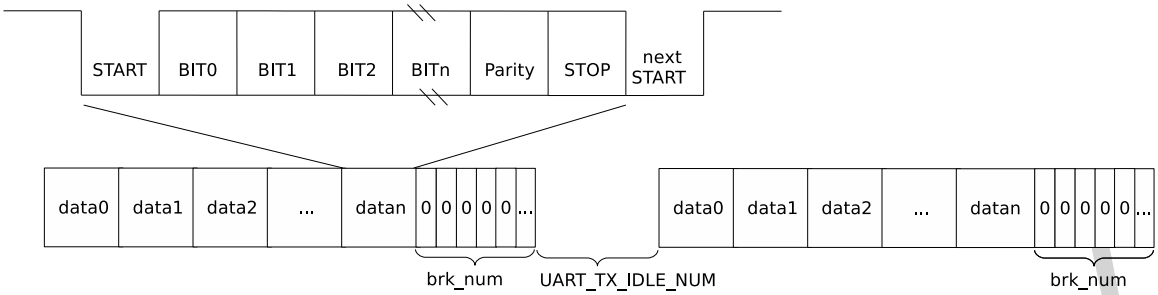


Figure 24-5. Structure of UART Data Frame

Figure 24-5 shows the basic structure of a data frame. A frame starts with one START bit, and ends with STOP bits which can be 1, 1.5, 2 or 3 bits long, configured by UART_STOP_BIT_NUM, UART_DL1_EN and UART_DL0_EN. The START bit is logical low, whereas STOP bits are logical high.

The actual data length can be anywhere between 5 ~ 8 bits, configured by UART_BIT_NUM. When UART_PARITY_EN is set, a parity bit is added after data bits. UART_PARITY is used to choose even parity or odd parity. When the receiver detects a parity bit error in data received, a UART_PARITY_ERR_INT interrupt is generated, and the erroneous data are still stored into the RX FIFO. When the receiver detects a data frame error, a UART_FRM_ERR_INT interrupt is generated, and the erroneous data by default is stored into the RX FIFO.

If all data in Tx_FIFO have been sent, a UART_TX_DONE_INT interrupt is generated. After this, if the UART_TXD_BRK bit is set then the transmitter will send several low level bits, namely delimiters, to separate data packets. The number of low level bits is configured by UART_TX_BRK_NUM. Once the transmitter has sent all delimiters, a UART_TX_BRK_DONE_INT interrupt is generated. The minimum interval between data frames can be configured using UART_TX_IDLE_NUM. If the transmitter stays idle for UART_TX_IDLE_NUM or more time (in the unit of bit time, i.e. the time it takes to transfer one bit), a UART_TX_BRK_IDLE_DONE_INT interrupt is generated.

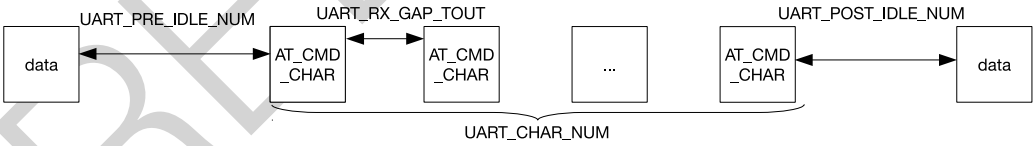


Figure 24-6. AT_CMD Character Structure

Figure 24-6 is the structure of a special character AT_CMD. If the receiver constantly receives AT_CMD_CHAR and the following conditions are met, a UART_AT_CMD_CHAR_DET_INT interrupt is generated. The specific value of AT_CMD_CHAR can be read from UART*n*_AT_CMD_CHAR.

- The interval between the first AT_CMD_CHAR and the last non-AT_CMD_CHAR character is at least UART_PRE_IDLE_NUM cycles.
- The interval between two AT_CMD_CHAR characters is less than UART_RX_GAP_TOUT cycles.
- The number of AT_CMD_CHAR characters is equal to or greater than UART_CHAR_NUM.

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- The interval between the last AT_CMD_CHAR character and next non-AT_CMD_CHAR character is at least UART_POST_IDLE_NUM cycles.

24.4.5 RS485

All three UART controllers support RS485 protocol. This protocol uses differential signals to transmit data, so it can communicate over longer distances at higher bit rates than RS232. RS485 has two-wire half-duplex mode and four-wire full-duplex modes. UART controllers support two-wire half-duplex transmission and bus snooping. In a two-wire RS485 multidrop network, there can be 32 slaves at most.

24.4.5.1 Driver Control

As shown in Figure 24-7, in a two-wire multidrop network, an external RS485 transceiver is needed for differential to single-ended conversion. A RS485 transceiver contains a driver and a receiver. When a UART controller is not in transmitter mode, the connection to the differential line can be broken by disabling the driver. When the DE (Driver Enable) signal is 1, the driver is enabled; when DE is 0, the driver is disabled.

The UART receiver converts differential signals to single-ended signals via an external receiver. RE is the enable control signal for the receiver. When RE is 0, the receiver is enabled; when RE is 1, the receiver is disabled. If RE is configured as 0, the UART controller is allowed to snoop data on the bus, including data sent by itself.

DE can be controlled by either software or hardware. To reduce the cost of software, DE is controlled by hardware in our design. As shown in Figure 24-7, DE is connected to dtrn_out of UART (please refer to Section 24.4.9.1 for more details).

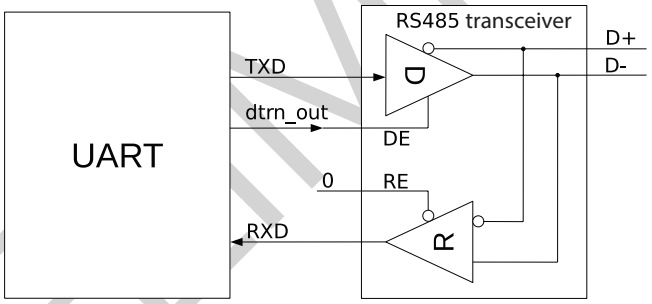


Figure 24-7. Driver Control Diagram in RS485 Mode

24.4.5.2 Turnaround Delay

By default, all three UART controllers work in receiver mode. When a UART controller is switched from transmitter mode to receiver mode, the RS485 protocol requires a turnaround delay of one cycle after the stop bit. The UART transmitter supports adding a turnaround delay of one cycle not only before the start bit but also after the stop bit. When UART_DL0_EN is set, a turnaround delay of one cycle is added before the start bit; when UART_DL1_EN is set, a turnaround delay of one cycle is added after the stop bit.

24.4.5.3 Bus Snooping

In a two-wire multidrop network, UART controllers support bus snooping if RE of the external RS485 transceiver is 0. By default, a UART controller is not allowed to transmit and receive data simultaneously. If UART_RS485TX_RX_EN is set and the external RS485 transceiver is configured as in Figure 24-7, a UART

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controller may receive data in transmitter mode and snoop the bus. If UART_RS485RXBY_TX_EN is set, a UART controller may transmit data in receiver mode.

All three UART controllers can snoop data sent by themselves. In transmitter mode, when a UART controller monitors a collision between data sent and data received, a UART_RS485_CLASH_INT interrupt is generated; when it monitors a data frame error, a UART_RS485_FRM_ERR_INT interrupt is generated; when it monitors a polarity error, a UART_RS485_PARITY_ERR_INT is generated.

24.4.6 IrDA

IrDA protocol consists of three layers, namely the physical layer, the link access protocol, and the link management protocol. The three UART controllers implement IrDA's physical layer. In IrDA encoding, a UART controller supports data rates up to 115.2 kbit/s (SIR, or serial infrared mode). As shown in Figure 24-8, the IrDA encoder converts a NRZ (non-return to zero code) signal to a RZI (return to zero code) signal and sends it to the external driver and infrared LED. This encoder uses modulated signals whose pulse width is 3/16 bits to indicate logic "0", and low levels to indicate logic "1". The IrDA decoder receives signals from the infrared receiver and converts them to NRZ signals. In most cases, the receiver is high when it is idle, and the encoder output polarity is the opposite of the decoder input polarity. If a low pulse is detected, it indicates that a start bit has been received.

When IrDA function is enabled, one bit is divided into 16 clock cycles. If the bit to be sent is zero, then the 9th, 10th and 11th clock cycle are high.

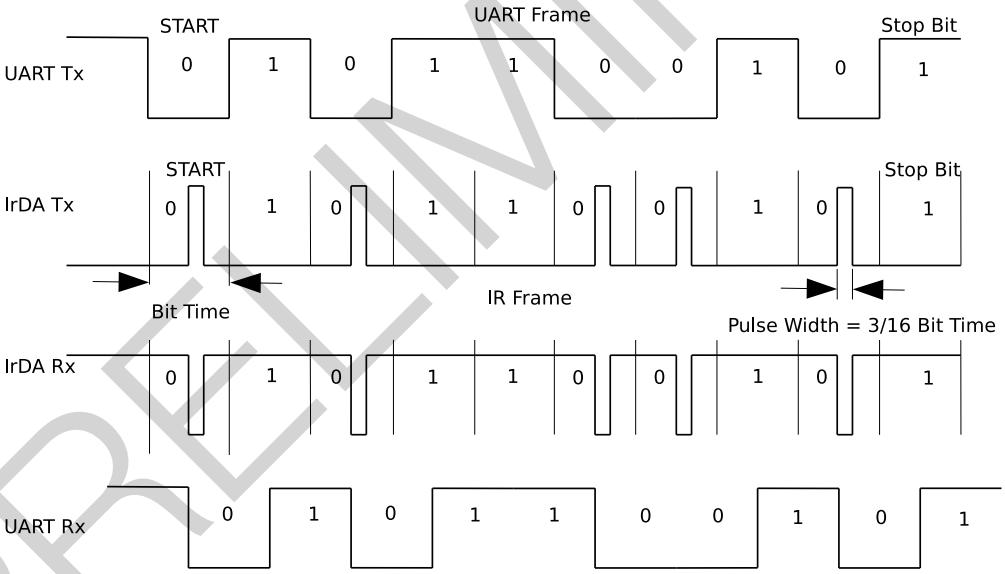


Figure 24-8. The Timing Diagram of Encoding and Decoding in SIR mode

The IrDA transceiver is half-duplex, meaning that it cannot send and receive data simultaneously. As shown in Figure 24-9, IrDA function is enabled by setting UART_IRDA_EN. When UART_IRDA_TX_EN is set (high), the IrDA transceiver is enabled to send data and not allowed to receive data; when UART_IRDA_TX_EN is reset (low), the IrDA transceiver is enabled to receive data and not allowed to send data.

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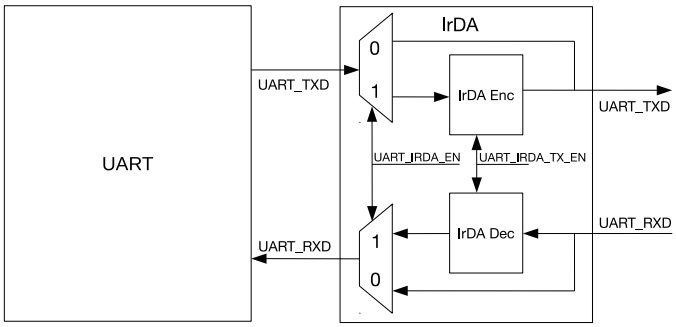


Figure 24-9. IrDA Encoding and Decoding Diagram

24.4.7 Wake-up

UART0 and UART1 can be set as a wake-up source for Light-sleep mode. To be specific Wakeup_Ctrl counts up the rising edges of rxd_in, and when this count becomes greater than UART_ACTIVE_THRESHOLD + 2, a wake_up signal is generated and sent to RTC, which then wakes ESP32-S3 up.

24.4.8 Loopback Test

UART*n* supports loopback testing, which can be enabled by setting UART_LOOPBACK. When loopback testing is enabled, UART output signal txd_out is connected to its input signal rxd_in, rtsn_out is connected to ctsn_in, and dtrn_out is connected to dsrn_out. Data are then sent out through txd_out. If the data received match the data sent, it indicates that UART*n* controller is working properly.

24.4.9 Flow Control

UART controllers have two ways to control data flow, namely hardware flow control and software flow control. Hardware flow control is achieved using output signal rtsn_out and input signal dsrn_in. Software flow control is achieved by inserting special characters (XON or XOFF) in data flow sent and detecting special characters in data flow received.

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24.4.9.1 Hardware Flow Control

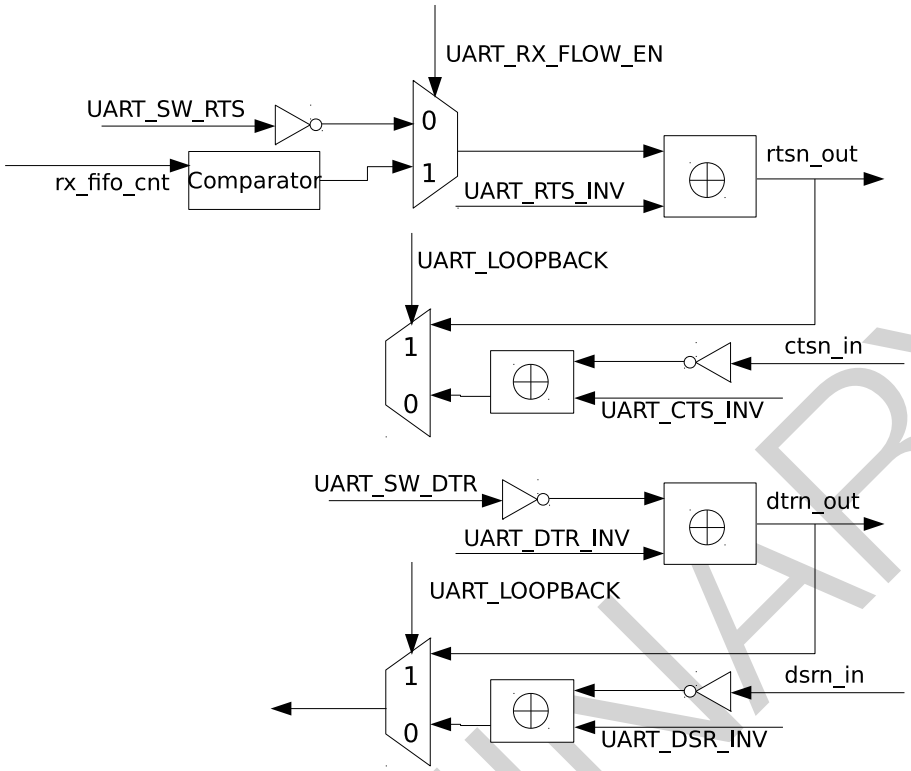


Figure 24-10. Hardware Flow Control Diagram

Figure 24-10 shows hardware flow control of a UART controller. Hardware flow control uses output signal rtsn_out and input signal dsrn_in. Figure 24-11 illustrates how these signals are connected between UART on ESP32-S3 (hereinafter referred to as IU0) and the external UART (hereinafter referred to as EU0).

When rtsn_out of IU0 is low, EU0 is allowed to send data; when rtsn_out of IU0 is high, EU0 is notified to stop sending data until rtsn_out of IU0 returns to low. The output signal rtsn_out can be controlled in two ways.

- Software control: Enter this mode by clearing UART_RX_FLOW_EN to 0. In this mode, the level of rtsn_out is changed by configuring UART_SW_RTS.
- Hardware control: Enter this mode by setting UART_RX_FLOW_EN to 1. In this mode, rtsn_out is pulled high when data in Rx_FIFO exceeds UART_RX_FLOW_THRHD.

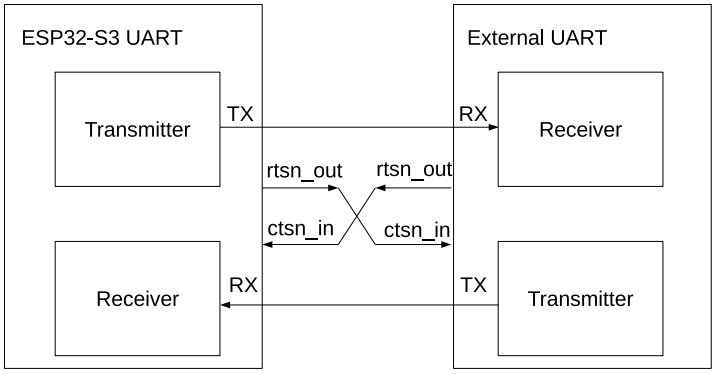


Figure 24-11. Connection between Hardware Flow Control Signals

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When ctsn_in of IU0 is low, IU0 is allowed to send data; when ctsn_in is high, IU0 is not allowed to send data. When IU0 detects an edge change on ctsn_in, a UART_CTS_CHG_INT interrupt is generated.

If dtrn_out of IU0 is high, it indicates that IU0 is ready to transmit data. dtrn_out is generated by configuring the UART_SW_DTR field. When the IU0 transmitter detects a edge change on dsrn_in, a UART_DSR_CHG_INT interrupt is generated. After this interrupt is detected, software can obtain the level of input signal dsrn_in by reading UART_DSRN. If dsrn_in is high, it indicates that EU0 is ready to transmit data.

In a two-wire RS485 multidrop network enabled by setting UART_RS485_EN, dtrn_out is generated by hardware and used for transmit/receive turnaround. When data transmission starts, dtrn_out is pulled high and the external driver is enabled; when data transmission completes, dtrn_out is pulled low and the external driver is disabled. Please note that when there is turnaround delay of one cycle added after the stop bit, dtrn_out is pulled low after the delay.

24.4.9.2 Software Flow Control

Instead of CTS/RTS lines, software flow control uses XON/XOFF characters to start or stop data transmission. Such flow control can be enabled by setting UART_SW_FLOW_CON_EN to 1.

When choosing software flow control, the hardware automatically detects if XON and XOFF characters are used in data flow, and generates a UART_SW_XOFF_INT or a UART_SW_XON_INT interrupt accordingly. When XOFF character is detected, the transmitter stops data transmission once the current byte has been transmitted; when XON character is detected, the transmitter starts data transmission. In addition, software can force the transmitter to stop sending data or to start sending data by setting respectively UART_FORCE_XOFF or UART_FORCE_XON.

Software determines whether to insert flow control characters according to the remaining room in the RX FIFO. When UART_SEND_XOFF is set, the transmitter sends an XOFF character configured by UART_XOFF_CHAR after the current byte in transmission; when UART_SEND_XON is set, the transmitter sends an XON character configured by UART_XON_CHAR after the current byte in transmission. If the RX FIFO of a UART controller stores more data than UART_XOFF_THRESHOLD, UART_SEND_XOFF is set by hardware. As a result, the transmitter sends an XOFF character configured by UART_XOFF_CHAR after the current byte in transmission. If the RX FIFO of a UART controller stores less data than UART_XON_THRESHOLD, UART_SEND_XON is set by hardware. As a result, the transmitter sends an XON character configured by UART_XON_CHAR after the current byte in transmission.

24.4.10 GDMA Mode

All three UART controllers on ESP32-S3 share one TX/RX GDMA (general direct memory access) channel via UHCI. In GDMA mode, UART controllers support the decoding and encoding of HCI data packets. The UHCI_UART*n*_CE field determines which UART controller occupies the GDMA TX/RX channel.

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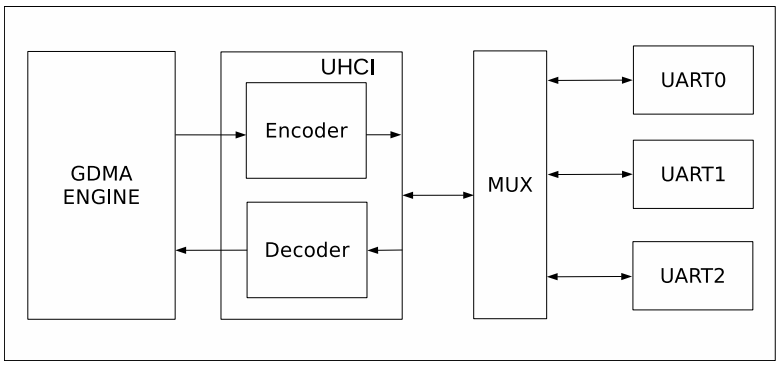


Figure 24-12. Data Transfer in GDMA Mode

Figure 24-12 shows how data are transferred using GDMA. Before GDMA receives data, software prepares an inlink (i.e. a linked list of receive descriptors. For details, see Chapter 2 GDMA Controller (GDMA)). GDMA_INLINK_ADDR_CH*n* points to the first receive descriptor in the inlink. After GDMA_INLINK_START_CH*n* is set, UHCI passes data that UART has received to the decoder. The decoded data are then stored into the RAM pointed by the inlink under the control of GDMA.

Before GDMA sends data, software prepares an outlink and data to be sent. GDMA_OUTLINK_ADDR_CH*n* points to the first transmit descriptor in the outlink. After GDMA_OUTLINK_START_CH*n* is set, GDMA reads data from the RAM pointed by outlink. The data are then encoded by the encoder, and sent sequentially by the UART transmitter.

HCI data packets have separators at the beginning and the end, with data bits in the middle (separators + data bits + separators). The encoder inserts separators in front of and after data bits, and replaces data bits identical to separators with special characters (i.e. escape characters). The decoder removes separators in front of and after data bits, and replaces escape characters with separators. There can be more than one continuous separator at the beginning and the end of a data packet. The separator is configured by UHCI_SEPER_CHAR, 0xC0 by default. The escape characters are configured by UHCI_ESC_SEQ0_CHAR0 (0xDB by default) and UHCI_ESC_SEQ0_CHAR1 (0xDD by default). When all data have been sent, a GDMA_OUT_TOTAL_EOF_CH*n*_INT interrupt is generated. When all data have been received, a GDMA_IN_SUC_EOF_CH*n*_INT is generated.

24.4.11 UART Interrupts

- UART_AT_CMD_CHAR_DET_INT: Triggered when the receiver detects an AT_CMD character.
- UART_RS485_CLASH_INT: Triggered when a collision is detected between the transmitter and the receiver in RS485 mode.
- UART_RS485_FRM_ERR_INT: Triggered when an error is detected in the data frame sent by the transmitter in RS485 mode.
- UART_RS485_PARITY_ERR_INT: Triggered when an error is detected in the parity bit sent by the transmitter in RS485 mode.
- UART_TX_DONE_INT: Triggered when all data in the TX FIFO have been sent.
- UART_TX_BRK_IDLE_DONE_INT: Triggered when the transmitter stays idle after sending the last data bit. The minimum amount of time marking the transmitter state as idle is determined by the configurable threshold value.

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- UART_TX_BRK_DONE_INT: Triggered when the transmitter has sent all NULL characters following the complete transmission of data from the TX FIFO.
- UART_GLITCH_DET_INT: Triggered when the receiver detects a glitch in the middle of the start bit.
- UART_SW_XOFF_INT: Triggered when UART_SW_FLOW_CON_EN is set and the receiver receives a XOFF character.
- UART_SW_XON_INT: Triggered when UART_SW_FLOW_CON_EN is set and the receiver receives a XON character.
- UART_RXFIFO_TOUT_INT: Triggered when the receiver takes more time than UART_RX_TOUT_THRHD to receive one byte.
- UART_BRK_DET_INT: Triggered when the receiver detects a NULL character after stop bits.
- UART_CTS_CHG_INT: Triggered when the receiver detects an edge change on CTSn signals.
- UART_DSR_CHG_INT: Triggered when the receiver detects an edge change on DSRn signals.
- UART_RXFIFO_OVF_INT: Triggered when the receiver receives more data than the capacity of the RX FIFO.
- UART_FRM_ERR_INT: Triggered when the receiver detects a data frame error.
- UART_PARITY_ERR_INT: Triggered when the receiver detects a parity error.
- UART_TXFIFO_EMPTY_INT: Triggered when the TX FIFO stores less data than what UART_TXFIFO_EMPTY_THRHD specifies.
- UART_RXFIFO_FULL_INT: Triggered when the receiver receives more data than what UART_RXFIFO_FULL_THRHD specifies.
- UART_WAKEUP_INT: Triggered when UART is woken up.

24.4.12 UHCI Interrupts

- UHCI_APP_CTRL1_INT: Triggered when software sets UHCI_APP_CTRL1_INT_RAW.
- UHCI_APP_CTRL0_INT: Triggered when software sets UHCI_APP_CTRL0_INT_RAW.
- UHCI_OUTLINK_EOF_ERR_INT: Triggered when an EOF error is detected in a transmit descriptor.
- UHCI_SEND_A_REG_Q_INT: Triggered when UHCI has sent a series of short packets using always_send.
- UHCI_SEND_S_REG_Q_INT: Triggered when UHCI has sent a series of short packets using single_send.
- UHCI_TX_HUNG_INT: Triggered when UHCI takes too long to read RAM using a GDMA transmit channel.
- UHCI_RX_HUNG_INT: Triggered when UHCI takes too long to receive data using a GDMA receive channel.
- UHCI_TX_START_INT: Triggered when GDMA detects a separator character.
- UHCI_RX_START_INT: Triggered when a separator character has been sent.

24.5 Programming Procedures

24.5.1 Register Type

All UART registers are in APB_CLK domain. According to whether clock domain crossing and synchronization are required, UART registers that can be configured by software are classified into three types, namely

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synchronous registers, static registers, and immediate registers. Synchronous registers are read in Core Clock domain, and take effect after synchronization. Static registers are also read in Core Clock domain, but would not change dynamically. Therefore, for static registers, clock domain crossing is not required, and software can turn on and off the clock for the UART transmitter or receiver to ensure that the configuration sampled in Core Clock domain is correct. Immediate registers are read in APB_CLK domain, and take effect after being configured via the APB bus.

24.5.1.1 Synchronous Registers

Since synchronous registers are read in core clock domain, but written in APB_CLK domain, they implement the clock domain crossing design to ensure that their values sampled in Core Clock domain are correct. These registers as listed in Table 24-1 are configured as follows:

- Enable register synchronization by clearing UART_UPDATE_CTRL to 0;
- Wait for UART_REG_UPDATE to become 0, which indicates the completion of last synchronization;
- Configure synchronous registers;
- Synchronize the configured values to Core Clock domain by writing 1 to UART_REG_UPDATE.

Table 24-1. UART*n* Synchronous Registers

Register	Field
UART_CLKDIV_REG	UART_CLKDIV_FRAG[3:0]
	UART_CLKDIV[11:0]
UART_CONF0_REG	UART_AUTOBAUD_EN
	UART_ERR_WR_MASK
	UART_TXD_INV
	UART_RXD_INV
	UART_IRDA_EN
	UART_TX_FLOW_EN
	UART_LOOPBACK
	UART_IRDA_RX_INV
	UART_IRDA_TX_EN
	UART_IRDA_WCTL
	UART_IRDA_TX_EN
	UART_IRDA_DPLX
	UART_STOP_BIT_NUM
	UART_BIT_NUM
	UART_PARITY_EN
	UART_PARITY

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Table 24-1 – cont'd from previous page

Register	Field
UART_FLOW_CONF_REG	UART_SEND_XOFF
	UART_SEND_XON
	UART_FORCE_XOFF
	UART_FORCE_XON
	UART_XONOFF_DEL
	UART_SW_FLOW_CON_EN
UART_RS485_CONF_REG	UART_RS485_TX_DLY_NUM[3:0]
	UART_RS485_RX_DLY_NUM
	UART_RS485RXBY_TX_EN
	UART_RS485TX_RX_EN
	UART_DL1_EN
	UART_DL0_EN
	UART_RS485_EN

24.5.1.2 Static Registers

Static registers, though also read in Core Clock domain, would not change dynamically when UART controllers are at work, so they do not implement the clock domain crossing design. These registers must be configured when the UART transmitter or receiver is not at work. In this case, software can turn off the clock for the UART transmitter or receiver, so that static registers are not sampled in their metastable state. When software turns on the clock, the configured values are stable to be correctly sampled. Static registers as listed in Table 24-2 are configured as follows:

- Turn off the clock for the UART transmitter by clearing UART_TX_SCLK_EN, or the clock for the UART receiver by clearing UART_RX_SCLK_EN, depending on which one (transmitter or receiver) is not at work;
- Configure static registers;
- Turn on the clock for the UART transmitter by writing 1 to UART_TX_SCLK_EN, or the clock for the UART receiver by writing 1 to UART_RX_SCLK_EN.

Table 24-2. UART*n* Static Registers

Register	Field
UART_RX_FILT_REG	UART_GLITCH_FILT_EN
	UART_GLITCH_FILT[7:0]
UART_SLEEP_CONF_REG	UART_ACTIVE_THRESHOLD[9:0]
UART_SWFC_CONF0_REG	UART_XOFF_CHAR[7:0]
UART_SWFC_CONF1_REG	UART_XON_CHAR[7:0]
UART_IDLE_CONF_REG	UART_TX_IDLE_NUM[9:0]
UART_AT_CMD_PRECNT_REG	UART_PRE_IDLE_NUM[15:0]
UART_AT_CMD_POSTCNT_REG	UART_POST_IDLE_NUM[15:0]
UART_AT_CMD_GAPTOUT_REG	UART_RX_GAP_TOUT[15:0]
UART_AT_CMD_CHAR_REG	UART_CHAR_NUM[7:0]
	UART_AT_CMD_CHAR[7:0]

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24.5.1.3 Immediate Registers

Except those listed in Table 24-1 and Table 24-2, registers that can be configured by software are immediate registers read in APB_CLK domain, such as interrupt and FIFO configuration registers.

24.5.2 Detailed Steps

Figure 24-13 illustrates the process to program UART controllers, namely initializing the UART, configuring the registers, enabling the transmitter and/or receiver, and finishing data transmission.

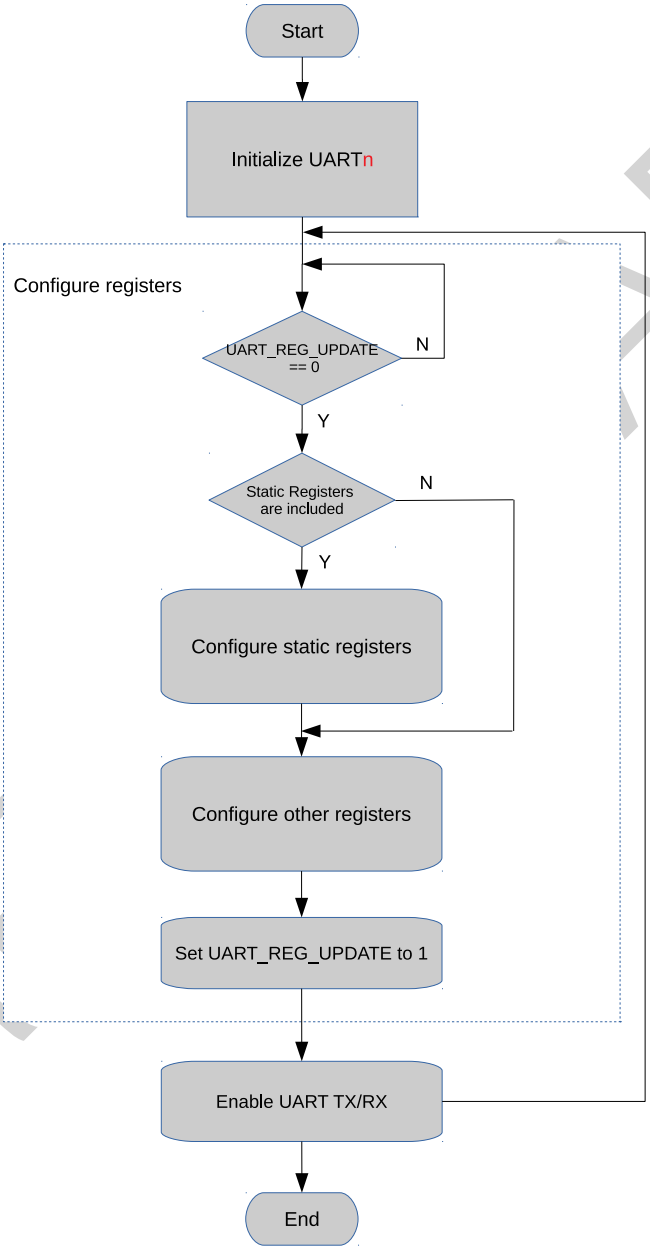


Figure 24-13. UART Programming Procedures

24.5.2.1 Initializing UART*n*

Initializing UART*n* requires two steps: resetting UART*n* and enabling register synchronization.

To reset UART*n*:

- enable the clock for UART RAM by setting SYSTEM_UART_MEM_CLK_EN to 1;
- enable APB_CLK for UART*n* by setting SYSTEM_UART*n*_CLK_EN to 1;
- clear SYSTEM_UART*n*_RST;
- write 1 to UART_RST_CORE;
- write 1 to SYSTEM_UART*n*_RST;
- clear SYSTEM_UART*n*_RST;
- clear UART_RST_CORE.

To enable register synchronization, clear UART_UPDATE_CTRL.

24.5.2.2 Configuring UART*n* Communication

To configure UART*n* communication:

- wait for UART_REG_UPDATE to become 0, which indicates the completion of last synchronization;
- configure static registers (if any) following Section 24.5.1.2;
- select the clock source via UART_SCLK_SEL;
- configure divisor of the divider via UART_SCLK_DIV_NUM, UART_SCLK_DIV_A, and UART_SCLK_DIV_B;
- configure the baud rate for transmission via UART_CLKDIV and UART_CLKDIV_FRAG;
- configure data length via UART_BIT_NUM;
- configure odd or even parity check via UART_PARITY_EN and UART_PARITY;
- optional steps depending on application ...
- synchronize the configured values to Core Clock domain by writing 1 to UART_REG_UPDATE.

24.5.2.3 Enabling UART*n*

To enable UART*n* transmitter:

- configure the TX FIFO's empty threshold via UART_TXFIFO_EMPTY_THRHD;
- disable UART_TXFIFO_EMPTY_INT interrupt by clearing UART_TXFIFO_EMPTY_INT_ENA;
- write data to be sent to UART_RXFIFO_RD_BYTE;
- clear UART_TXFIFO_EMPTY_INT interrupt by setting UART_TXFIFO_EMPTY_INT_CLR;
- enable UART_TXFIFO_EMPTY_INT interrupt by setting UART_TXFIFO_EMPTY_INT_ENA;
- detect UART_TXFIFO_EMPTY_INT and wait for the completion of data transmission.

To enable UART*n* receiver:

- configure RXFIFO's full threshold via UART_RXFIFO_FULL_THRHD;
- enable UART_RXFIFO_FULL_INT interrupt by setting UART_RXFIFO_FULL_INT_ENA;
- detect UART_TXFIFO_FULL_INT and wait until the RXFIFO is full;

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- read data from RXFIFO via UART_RXFIFO_RD_BYTE, and obtain the number of bytes received in RXFIFO via UART_RXFIFO_CNT.

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24.6 Register Summary

24.6.1 UART Register Summary

The addresses in this section are relative to UART Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
FIFO Configuration			
UART_FIFO_REG	FIFO data register	0x0000	RO
UART_MEM_CONF_REG	UART threshold and allocation configuration	0x0060	R/W
UART Interrupt Register			
UART_INT_RAW_REG	Raw interrupt status	0x0004	R/WTC/SS
UART_INT_ST_REG	Masked interrupt status	0x0008	RO
UART_INT_ENA_REG	Interrupt enable bits	0x000C	R/W
UART_INT_CLR_REG	Interrupt clear bits	0x0010	WT
Configuration Register			
UART_CLKDIV_REG	Clock divider configuration	0x0014	R/W
UART_RX_FILT_REG	RX filter configuration	0x0018	R/W
UART_CONF0_REG	Configuration register 0	0x0020	R/W
UART_CONF1_REG	Configuration register 1	0x0024	R/W
UART_FLOW_CONF_REG	Software flow control configuration	0x0034	varies
UART_SLEEP_CONF_REG	Sleep mode configuration	0x0038	R/W
UART_SWFC_CONF0_REG	Software flow control character configuration	0x003C	R/W
UART_SWFC_CONF1_REG	Software flow control character configuration	0x0040	R/W
UART_TXBRK_CONF_REG	TX break character configuration	0x0044	R/W
UART_IDLE_CONF_REG	Frame end idle time configuration	0x0048	R/W
UART_RS485_CONF_REG	RS485 mode configuration	0x004C	R/W
UART_CLK_CONF_REG	UART core clock configuration	0x0078	R/W
Status Register			
UART_STATUS_REG	UART status register	0x001C	RO
UART_MEM_TX_STATUS_REG	TX FIFO write and read offset address	0x0064	RO
UART_MEM_RX_STATUS_REG	RX FIFO write and read offset address	0x0068	RO
UART_FSM_STATUS_REG	UART transmitter and receiver status	0x006C	RO
Autobaud Register			
UART_LOWPULSE_REG	Autobaud minimum low pulse duration register	0x0028	RO
UART_HIGHPULSE_REG	Autobaud minimum high pulse duration register	0x002C	RO
UART_RXD_CNT_REG	Autobaud edge change count register	0x0030	RO
UART_POSPULSE_REG	Autobaud high pulse register	0x0070	RO
UART_NEGPULSE_REG	Autobaud low pulse register	0x0074	RO
AT Escape Sequence Selection Configuration			
UART_AT_CMD_PRECNT_REG	Pre-sequence timing configuration	0x0050	R/W
UART_AT_CMD_POSTCNT_REG	Post-sequence timing configuration	0x0054	R/W
UART_AT_CMD_GAPTOUT_REG	Timeout configuration	0x0058	R/W
UART_AT_CMD_CHAR_REG	AT escape sequence detection configuration	0x005C	R/W

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Name	Description	Address	Access
Version Register			
UART_DATE_REG	UART version control register	0x007C	R/W
UART_ID_REG	UART ID register	0x0080	varies

24.6.2 UHCI Register Summary

The addresses in this section are relative to UHCI Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
Configuration Register			
UHCI_CONF0_REG	UHCI configuration register	0x0000	R/W
UHCI_CONF1_REG	UHCI configuration register	0x0018	varies
UHCI_ESCAPE_CONF_REG	Escape character configuration	0x0024	R/W
UHCI_HUNG_CONF_REG	Timeout configuration	0x0028	R/W
UHCI_ACK_NUM_REG	UHCI ACK number configuration	0x002C	varies
UHCI_QUICK_SENT_REG	UHCI quick_sent configuration register	0x0034	varies
UHCI_REG_Q0_WORD0_REG	Q0_WORD0 quick_sent register	0x0038	R/W
UHCI_REG_Q0_WORD1_REG	Q0_WORD1 quick_sent register	0x003C	R/W
UHCI_REG_Q1_WORD0_REG	Q1_WORD0 quick_sent register	0x0040	R/W
UHCI_REG_Q1_WORD1_REG	Q1_WORD1 quick_sent register	0x0044	R/W
UHCI_REG_Q2_WORD0_REG	Q2_WORD0 quick_sent register	0x0048	R/W
UHCI_REG_Q2_WORD1_REG	Q2_WORD1 quick_sent register	0x004C	R/W
UHCI_REG_Q3_WORD0_REG	Q3_WORD0 quick_sent register	0x0050	R/W
UHCI_REG_Q3_WORD1_REG	Q3_WORD1 quick_sent register	0x0054	R/W
UHCI_REG_Q4_WORD0_REG	Q4_WORD0 quick_sent register	0x0058	R/W
UHCI_REG_Q4_WORD1_REG	Q4_WORD1 quick_sent register	0x005C	R/W
UHCI_REG_Q5_WORD0_REG	Q5_WORD0 quick_sent register	0x0060	R/W
UHCI_REG_Q5_WORD1_REG	Q5_WORD1 quick_sent register	0x0064	R/W
UHCI_REG_Q6_WORD0_REG	Q6_WORD0 quick_sent register	0x0068	R/W
UHCI_REG_Q6_WORD1_REG	Q6_WORD1 quick_sent register	0x006C	R/W
UHCI_ESC_CONF0_REG	Escape sequence configuration register 0	0x0070	R/W
UHCI_ESC_CONF1_REG	Escape sequence configuration register 1	0x0074	R/W
UHCI_ESC_CONF2_REG	Escape sequence configuration register 2	0x0078	R/W
UHCI_ESC_CONF3_REG	Escape sequence configuration register 3	0x007C	R/W
UHCI_PKT_THRES_REG	Configuration register for packet length	0x0080	R/W
UHCI Interrupt Register			
UHCI_INT_RAW_REG	Raw interrupt status	0x0004	varies
UHCI_INT_ST_REG	Masked interrupt status	0x0008	RO
UHCI_INT_ENA_REG	Interrupt enable bits	0x000C	R/W
UHCI_INT_CLR_REG	Interrupt clear bits	0x0010	WT
UHCI_APP_INT_SET_REG	Software interrupt trigger source	0x0014	WT
UHCI Status Register			
UHCI_STATE0_REG	UHCI receive status	0x001C	RO

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Name	Description	Address	Access
UHCI_STATE1_REG	UHCI transmit status	0x0020	RO
UHCI_RX_HEAD_REG	UHCI packet header register	0x0030	RO
Version Register			
UHCI_DATE_REG	UHCI version control register	0x0084	R/W

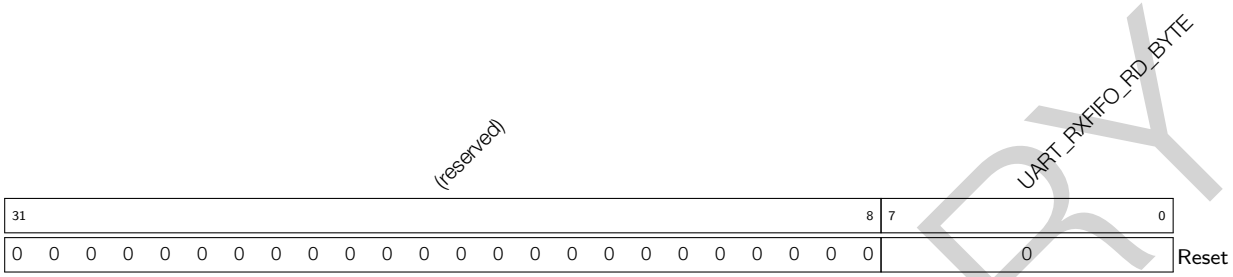
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24.7 Registers

24.7.1 UART Registers

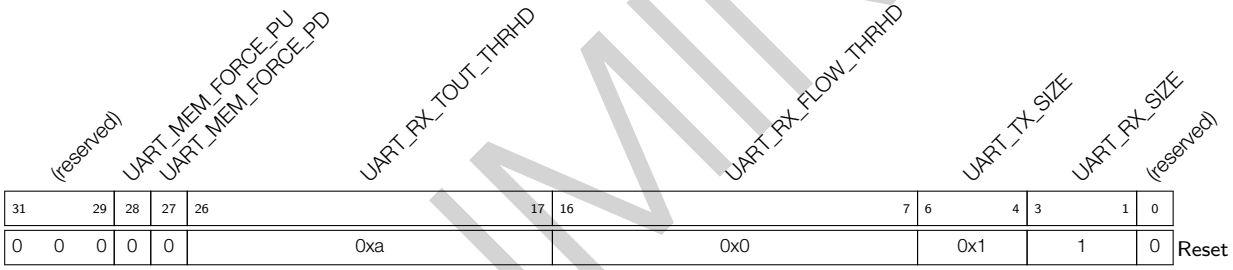
The addresses in this section are relative to UART Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 24.1. UART_FIFO_REG (0x0000)



UART_RXFIFO_RD_BYTE UART*n* accesses FIFO via this field. (RO)

Register 24.2. UART_MEM_CONF_REG (0x0060)



UART_RX_SIZE This field is used to configure the amount of RAM allocated for RX FIFO. The default number is 128 bytes. (R/W)

UART_TX_SIZE This field is used to configure the amount of RAM allocated for TX FIFO. The default number is 128 bytes. (R/W)

UART_RX_FLOW_THRHD This field is used to configure the maximum amount of data bytes that can be received when hardware flow control works. (R/W)

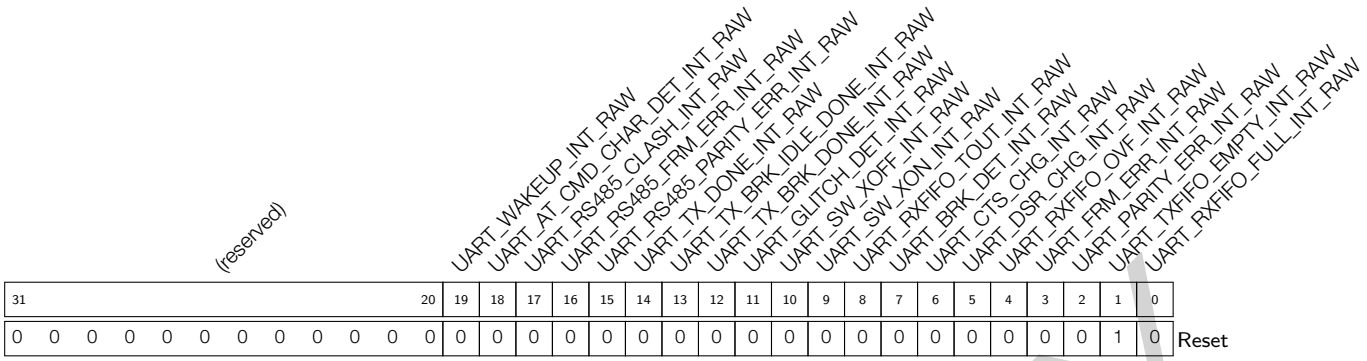
UART_RX_TOUT_THRHD This field is used to configure the threshold time that receiver takes to receive one byte, in the unit of bit time (the time it takes to transfer one bit). The UART_RXFIFO_TOUT_INT interrupt will be triggered when the receiver takes more time to receive one byte with UART RX_TOUT_EN set to 1. (R/W)

UART_MEM_FORCE_PD Set this bit to force power down UART RAM. (R/W)

UART_MEM_FORCE_PU Set this bit to force power up UART RAM. (R/W)

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Register 24.3. UART_INT_RAW_REG (0x0004)



UART_RXFIFO_FULL_INT_RAW This interrupt raw bit turns to high level when the receiver receives more data than what UART_RXFIFO_FULL_THRHD specifies. (R/WTC/SS)

UART_TXFIFO_EMPTY_INT_RAW This interrupt raw bit turns to high level when the amount of data in TX FIFO is less than what UART_TXFIFO_EMPTY_THRHD specifies. (R/WTC/SS)

UART_PARITY_ERR_INT_RAW This interrupt raw bit turns to high level when the receiver detects a parity error in the data. (R/WTC/SS)

UART_FRM_ERR_INT_RAW This interrupt raw bit turns to high level when the receiver detects a data frame error. (R/WTC/SS)

UART_RXFIFO_OVF_INT_RAW This interrupt raw bit turns to high level when the receiver receives more data than the capacity of RX FIFO. (R/WTC/SS)

UART_DSR_CHG_INT_RAW This interrupt raw bit turns to high level when the receiver detects the edge change of DSRn signal. (R/WTC/SS)

UART_CTS_CHG_INT_RAW This interrupt raw bit turns to high level when the receiver detects the edge change of CTSn signal. (R/WTC/SS)

UART_BRK_DET_INT_RAW This interrupt raw bit turns to high level when the receiver detects a 0 after the stop bit. (R/WTC/SS)

UART_RXFIFO_TOUT_INT_RAW This interrupt raw bit turns to high level when the receiver takes more time than UART_RX_TOUT_THRHD to receive a byte. (R/WTC/SS)

UART_SW_XON_INT_RAW This interrupt raw bit turns to high level when the receiver receives an XON character and UART_SW_FLOW_CON_EN is set to 1. (R/WTC/SS)

UART_SW_XOFF_INT_RAW This interrupt raw bit turns to high level when the receiver receives an XOFF character and UART_SW_FLOW_CON_EN is set to 1. (R/WTC/SS)

UART_GLITCH_DET_INT_RAW This interrupt raw bit turns to high level when the receiver detects a glitch in the middle of a start bit. (R/WTC/SS)

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Register 24.3. UART_INT_RAW_REG (0x0004)

Continued from the previous page...

UART_TX_BRK_DONE_INT_RAW This interrupt raw bit turns to high level when the transmitter completes sending NULL characters, after all data in TX FIFO are sent. (R/WTC/SS)

UART_TX_BRK_IDLE_DONE_INT_RAW This interrupt raw bit turns to high level when the transmitter has kept the shortest duration after sending the last data. (R/WTC/SS)

UART_TX_DONE_INT_RAW This interrupt raw bit turns to high level when the transmitter has sent out all data in FIFO. (R/WTC/SS)

UART_RS485_PARITY_ERR_INT_RAW This interrupt raw bit turns to high level when the receiver detects a parity error from the echo of the transmitter in RS485 mode. (R/WTC/SS)

UART_RS485_FRM_ERR_INT_RAW This interrupt raw bit turns to high level when the receiver detects a data frame error from the echo of the transmitter in RS485 mode. (R/WTC/SS)

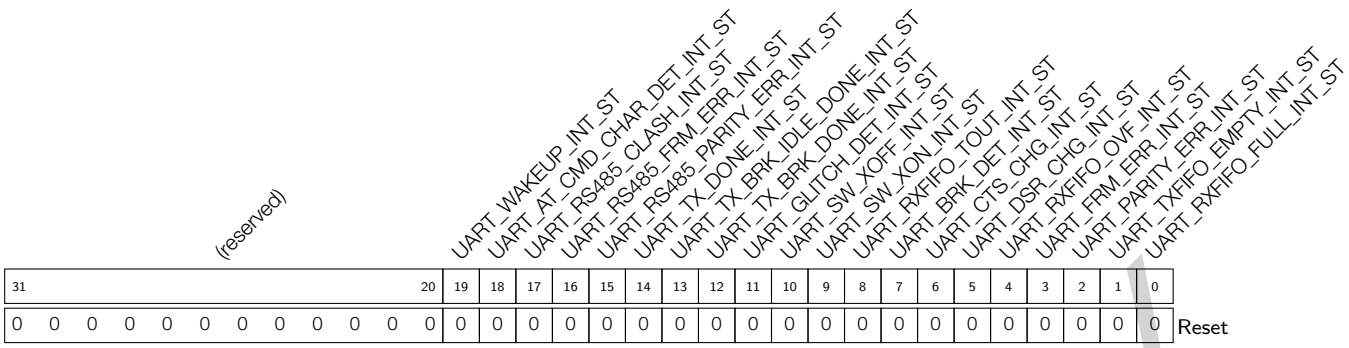
UART_RS485_CLASH_INT_RAW This interrupt raw bit turns to high level when a collision is detected between the transmitter and the receiver in RS485 mode. (R/WTC/SS)

UART_AT_CMD_CHAR_DET_INT_RAW This interrupt raw bit turns to high level when the receiver detects the configured UART_AT_CMD_CHAR. (R/WTC/SS)

UART_WAKEUP_INT_RAW This interrupt raw bit turns to high level when the input RXD edge changes more times than what UART_ACTIVE_THRESHOLD specifies in Light-sleep mode. (R/WTC/SS)

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Register 24.4. UART_INT_ST_REG (0x0008)



UART_RXFIFO_FULL_INT_ST This is the status bit for UART_RXFIFO_FULL_INT when UART_RXFIFO_FULL_INT_ENA is set to 1. (RO)

UART_TXFIFO_EMPTY_INT_ST This is the status bit for UART_TXFIFO_EMPTY_INT when UART_TXFIFO_EMPTY_INT_ENA is set to 1. (RO)

UART_PARITY_ERR_INT_ST This is the status bit for UART_PARITY_ERR_INT when UART_PARITY_ERR_INT_ENA is set to 1. (RO)

UART_FRM_ERR_INT_ST This is the status bit for UART_FRM_ERR_INT when UART_FRM_ERR_INT_ENA is set to 1. (RO)

UART_RXFIFO_OVF_INT_ST This is the status bit for UART_RXFIFO_OVF_INT when UART_RXFIFO_OVF_INT_ENA is set to 1. (RO)

UART_DSR_CHG_INT_ST This is the status bit for UART_DSR_CHG_INT when UART_DSR_CHG_INT_ENA is set to 1. (RO)

UART_CTS_CHG_INT_ST This is the status bit for UART_CTS_CHG_INT when UART_CTS_CHG_INT_ENA is set to 1. (RO)

UART_BRK_DET_INT_ST This is the status bit for UART_BRK_DET_INT when UART_BRK_DET_INT_ENA is set to 1. (RO)

UART_RXFIFO_TOUT_INT_ST This is the status bit for UART_RXFIFO_TOUT_INT when UART_RXFIFO_TOUT_INT_ENA is set to 1. (RO)

UART_SW_XON_INT_ST This is the status bit for UART_SW_XON_INT when UART_SW_XON_INT_ENA is set to 1. (RO)

UART_SW_XOFF_INT_ST This is the status bit for UART_SW_XOFF_INT when UART_SW_XOFF_INT_ENA is set to 1. (RO)

UART_GLITCH_DET_INT_ST This is the status bit for UART_GLITCH_DET_INT when UART_GLITCH_DET_INT_ENA is set to 1. (RO)

UART_TX_BRK_DONE_INT_ST This is the status bit for UART_TX_BRK_DONE_INT when UART_TX_BRK_DONE_INT_ENA is set to 1. (RO)

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Register 24.4. UART_INT_ST_REG (0x0008)

Continued from the previous page...

UART_TX_BRK_IDLE_DONE_INT_ST This is the status bit for UART_TX_BRK_IDLE_DONE_INT when UART_TX_BRK_IDLE_DONE_INT_ENA is set to 1. (RO)

UART_TX_DONE_INT_ST This is the status bit for UART_TX_DONE_INT when UART_TX_DONE_INT_ENA is set to 1. (RO)

UART_RS485_PARITY_ERR_INT_ST This is the status bit for UART_RS485_PARITY_ERR_INT when UART_RS485_PARITY_INT_ENA is set to 1. (RO)

UART_RS485_FRM_ERR_INT_ST This is the status bit for UART_RS485_FRM_ERR_INT when UART_RS485_FRM_ERR_INT_ENA is set to 1. (RO)

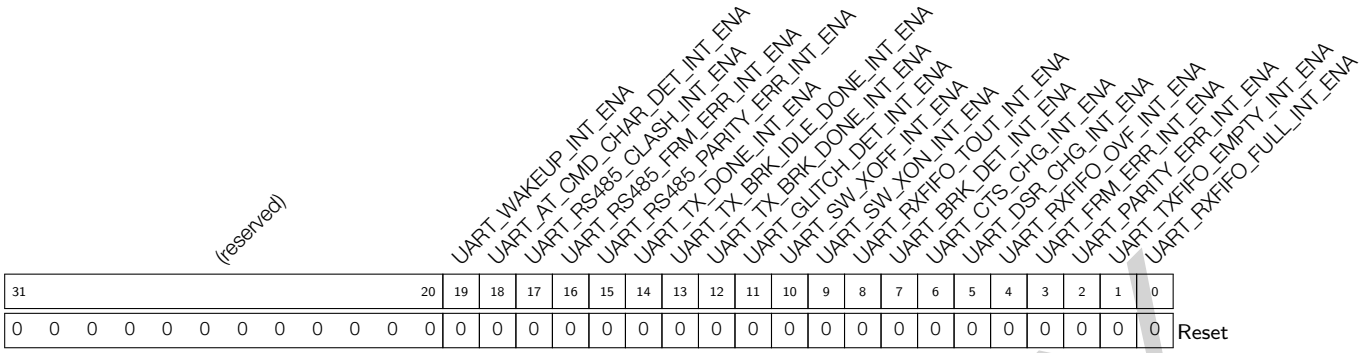
UART_RS485_CLASH_INT_ST This is the status bit for UART_RS485_CLASH_INT when UART_RS485_CLASH_INT_ENA is set to 1. (RO)

UART_AT_CMD_CHAR_DET_INT_ST This is the status bit for UART_AT_CMD_CHAR_DET_INT when UART_AT_CMD_CHAR_DET_INT_ENA is set to 1. (RO)

UART_WAKEUP_INT_ST This is the status bit for UART_WAKEUP_INT when UART_WAKEUP_INT_ENA is set to 1. (RO)

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Register 24.5. UART_INT_ENA_REG (0x000C)



UART_RXFIFO_FULL_INT_ENA This is the enable bit for UART_RXFIFO_FULL_INT. (R/W)

UART_TXFIFO_EMPTY_INT_ENA This is the enable bit for UART_TXFIFO_EMPTY_INT. (R/W)

UART_PARITY_ERR_INT_ENA This is the enable bit for UART_PARITY_ERR_INT. (R/W)

UART_FRM_ERR_INT_ENA This is the enable bit for UART_FRM_ERR_INT. (R/W)

UART_RXFIFO_OVF_INT_ENA This is the enable bit for UART_RXFIFO_OVF_INT. (R/W)

UART_DSR_CHG_INT_ENA This is the enable bit for UART_DSR_CHG_INT. (R/W)

UART_CTS_CHG_INT_ENA This is the enable bit for UART_CTS_CHG_INT. (R/W)

UART_BRK_DET_INT_ENA This is the enable bit for UART_BRK_DET_INT. (R/W)

UART_RXFIFO_TOUT_INT_ENA This is the enable bit for UART_RXFIFO_TOUT_INT. (R/W)

UART_SW_XON_INT_ENA This is the enable bit for UART_SW_XON_INT. (R/W)

UART_SW_XOFF_INT_ENA This is the enable bit for UART_SW_XOFF_INT. (R/W)

UART_GLITCH_DET_INT_ENA This is the enable bit for UART_GLITCH_DET_INT. (R/W)

UART_TX_BRK_DONE_INT_ENA This is the enable bit for UART_TX_BRK_DONE_INT. (R/W)

UART_TX_BRK_IDLE_DONE_INT_ENA This is the enable bit for UART_TX_BRK_IDLE_DONE_INT. (R/W)

UART_TX_DONE_INT_ENA This is the enable bit for UART_TX_DONE_INT. (R/W)

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Register 24.5. UART_INT_ENA_REG (0x000C)

Continued from the previous page...

UART_RS485_PARITY_ERR_INT_ENA This is the enable bit for UART_RS485_PARITY_ERR_INT. (R/W)

UART_RS485_FRM_ERR_INT_ENA This is the enable bit for UART_RS485_PARITY_ERR_INT. (R/W)

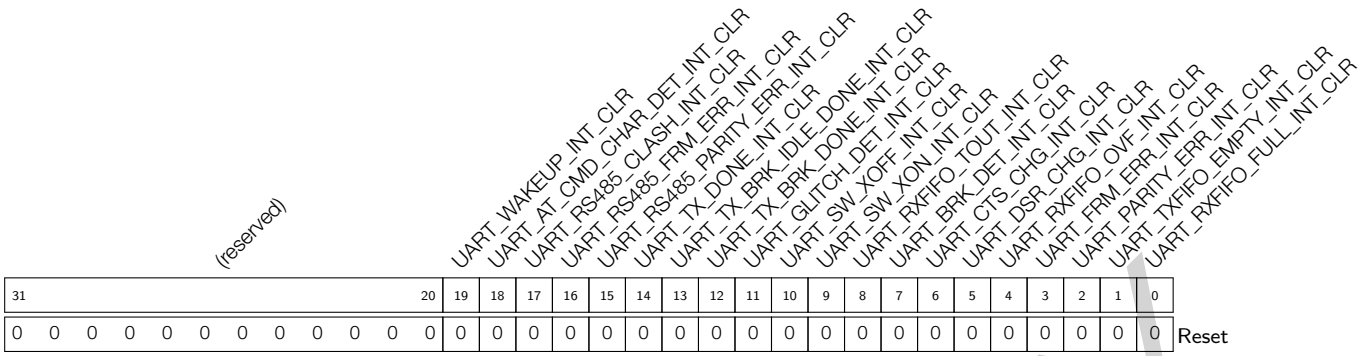
UART_RS485_CLASH_INT_ENA This is the enable bit for UART_RS485_CLASH_INT. (R/W)

UART_AT_CMD_CHAR_DET_INT_ENA This is the enable bit for UART_AT_CMD_CHAR_DET_INT. (R/W)

UART_WAKEUP_INT_ENA This is the enable bit for UART_WAKEUP_INT. (R/W)

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Register 24.6. UART_INT_CLR_REG (0x0010)



UART_RXFIFO_FULL_INT_CLR Set this bit to clear the UART_THE RXFIFO_FULL_INT interrupt. (WT)

UART_TXFIFO_EMPTY_INT_CLR Set this bit to clear the UART_TXFIFO_EMPTY_INT interrupt. (WT)

UART_PARITY_ERR_INT_CLR Set this bit to clear the UART_PARITY_ERR_INT interrupt. (WT)

UART_FRM_ERR_INT_CLR Set this bit to clear the UART_FRM_ERR_INT interrupt. (WT)

UART_RXFIFO_OVF_INT_CLR Set this bit to clear the UART_UART_RXFIFO_OVF_INT interrupt. (WT)

UART_DSR_CHG_INT_CLR Set this bit to clear the UART_DSR_CHG_INT interrupt. (WT)

UART_CTS_CHG_INT_CLR Set this bit to clear the UART_CTS_CHG_INT interrupt. (WT)

UART_BRK_DET_INT_CLR Set this bit to clear the UART_BRK_DET_INT interrupt. (WT)

UART_RXFIFO_TOUT_INT_CLR Set this bit to clear the UART_RXFIFO_TOUT_INT interrupt. (WT)

UART_SW_XON_INT_CLR Set this bit to clear the UART_SW_XON_INT interrupt. (WT)

UART_SW_XOFF_INT_CLR Set this bit to clear the UART_SW_XOFF_INT interrupt. (WT)

UART_GLITCH_DET_INT_CLR Set this bit to clear the UART_GLITCH_DET_INT interrupt. (WT)

UART_TX_BRK_DONE_INT_CLR Set this bit to clear the UART_TX_BRK_DONE_INT interrupt. (WT)

UART_TX_BRK_IDLE_DONE_INT_CLR Set this bit to clear the UART_TX_BRK_IDLE_DONE_INT interrupt. (WT)

UART_TX_DONE_INT_CLR Set this bit to clear the UART_TX_DONE_INT interrupt. (WT)

UART_RS485_PARITY_ERR_INT_CLR Set this bit to clear the UART_RS485_PARITY_ERR_INT interrupt. (WT)

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Register 24.6. UART_INT_CLR_REG (0x0010)

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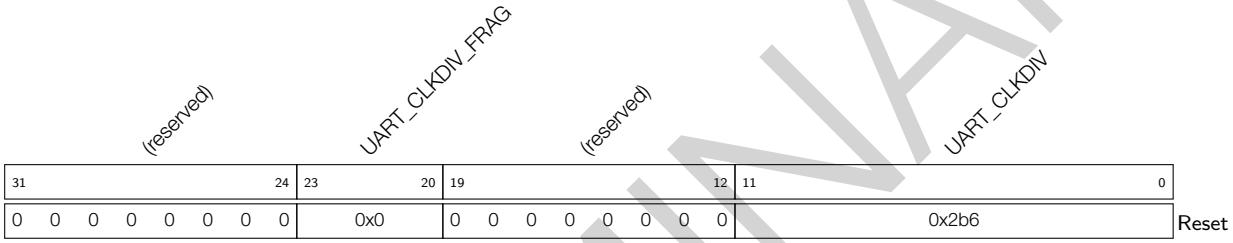
UART_RS485_FRM_ERR_INT_CLR Set this bit to clear the UART_RS485_FRM_ERR_INT interrupt. (WT)

UART_RS485_CLASH_INT_CLR Set this bit to clear the UART_RS485_CLASH_INT interrupt. (WT)

UART_AT_CMD_CHAR_DET_INT_CLR Set this bit to clear the UART_AT_CMD_CHAR_DET_INT interrupt. (WT)

UART_WAKEUP_INT_CLR Set this bit to clear the UART_WAKEUP_INT interrupt. (WT)

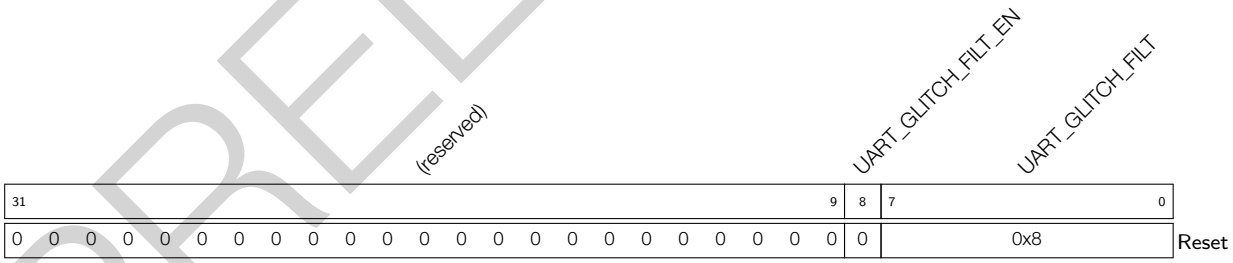
Register 24.7. UART_CLKDIV_REG (0x0014)



UART_CLKDIV The integral part of the frequency divisor. (R/W)

UART_CLKDIV_FRAG The fractional part of the frequency divisor. (R/W)

Register 24.8. UART_RX_FILT_REG (0x0018)

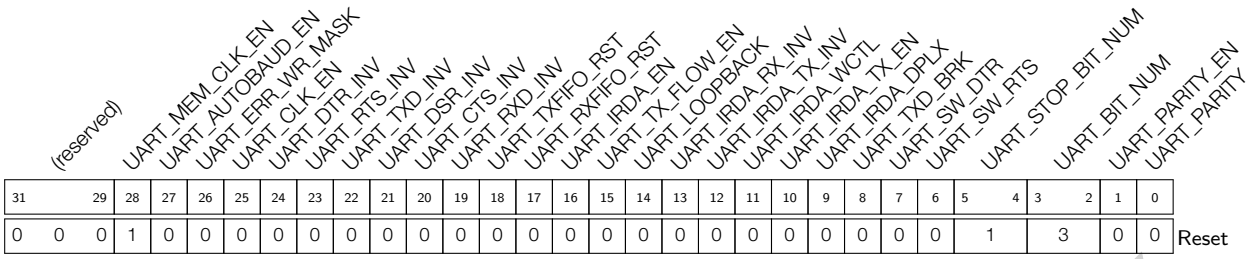


UART_GLITCH_FILT When input pulse width is lower than this value, the pulse is ignored. (R/W)

UART_GLITCH_FILT_EN Set this bit to enable RX signal filter. (R/W)

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Register 24.9. UART_CONF0_REG (0x0020)



UART_PARITY This bit is used to configure the parity check mode. (R/W)

UART_PARITY_EN Set this bit to enable UART parity check. (R/W)

UART_BIT_NUM This field is used to set the length of data. (R/W)

UART_STOP_BIT_NUM This field is used to set the length of stop bit. (R/W)

UART_SW_RTS This bit is used to configure the software RTS signal which is used in software flow control. (R/W)

UART_SW_DTR This bit is used to configure the software DTR signal which is used in software flow control. (R/W)

UART_TXD_BRK Set this bit to enable the transmitter to send NULL characters when the process of sending data is done. (R/W)

UART_IRDA_DPLX Set this bit to enable IrDA loopback mode. (R/W)

UART_IRDA_TX_EN This is the start enable bit for IrDA transmitter. (R/W)

UART_IRDA_WCTL 0: Set IrDA transmitter's 11th bit to 0; 1: The IrDA transmitter's 11th bit is the same as 10th bit. (R/W)

UART_IRDA_TX_INV Set this bit to invert the level of IrDA transmitter. (R/W)

UART_IRDA_RX_INV Set this bit to invert the level of IrDA receiver. (R/W)

UART_LOOPBACK Set this bit to enable UART loopback test mode. (R/W)

UART_TX_FLOW_EN Set this bit to enable flow control function for transmitter. (R/W)

UART_IRDA_EN Set this bit to enable IrDA protocol. (R/W)

UART_RXFIFO_RST Set this bit to reset the UART RX FIFO. (R/W)

UART_TXFIFO_RST Set this bit to reset the UART TX FIFO. (R/W)

UART_RXD_INV Set this bit to invert the level value of UART RXD signal. (R/W)

UART_CTS_INV Set this bit to invert the level value of UART CTS signal. (R/W)

UART_DSR_INV Set this bit to invert the level value of UART DSR signal. (R/W)

Continued on the next page...

PRELIMINARY

Register 24.9. UART_CONF0_REG (0x0020)

Continued from the previous page...

UART_TXD_INV Set this bit to invert the level value of UART TXD signal. (R/W)

UART_RTS_INV Set this bit to invert the level value of UART RTS signal. (R/W)

UART_DTR_INV Set this bit to invert the level value of UART DTR signal. (R/W)

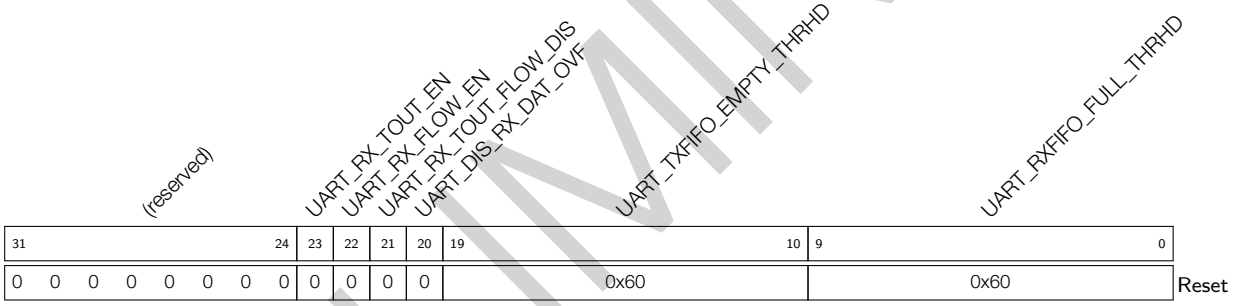
UART_CLK_EN 0: Support clock only when application writes registers; 1: Force clock on for registers. (R/W)

UART_ERR_WR_MASK 0: Receiver stores the data even if the received data is wrong; 1: Receiver stops storing data into FIFO when data is wrong. (R/W)

UART_AUTOBAUD_EN This is the enable bit for baud rate detection. (R/W)

UART_MEM_CLK_EN The signal to enable UART RAM clock gating. (R/W)

Register 24.10. UART_CONF1_REG (0x0024)



UART_RXFIFO_FULL_THRHD An UART_RXFIFO_FULL_INT interrupt is generated when the receiver receives more data than the value of this field. (R/W)

UART_TXFIFO_EMPTY_THRHD An UART_TXFIFO_EMPTY_INT interrupt is generated when the number of data bytes in TX FIFO is less than the value of this field. (R/W)

UART_DIS_RX_DAT_OVF Disable UART RX data overflow detection. (R/W)

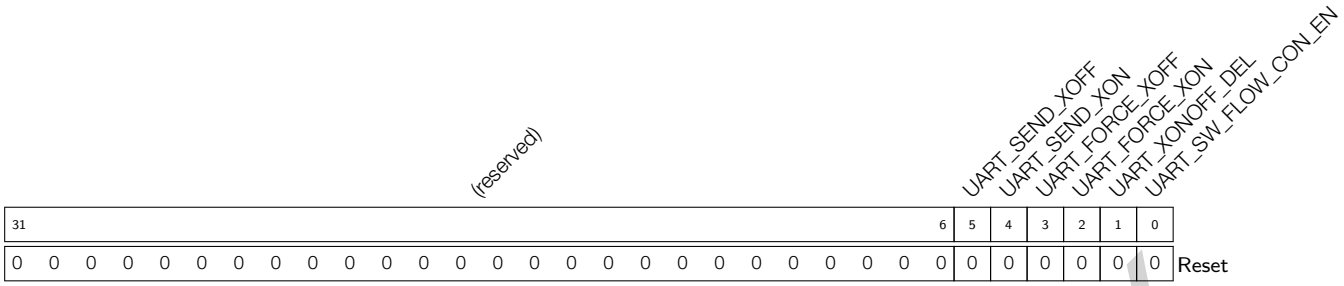
UART_RX_TOUT_FLOW_DIS Set this bit to stop accumulating idle_cnt when hardware flow control works. (R/W)

UART_RX_FLOW_EN This is the flow enable bit for UART receiver. (R/W)

UART_RX_TOUT_EN This is the enable bit for UART receiver's timeout function. (R/W)

PRELIMINARY

Register 24.11. UART_FLOW_CONF_REG (0x0034)



UART_SW_FLOW_CON_EN Set this bit to enable software flow control. When UART receives flow control characters XON or XOFF, which can be configured by UART_XON_CHAR or UART_XOFF_CHAR respectively, UART_SW_XON_INT or UART_SW_XOFF_INT interrupts can be triggered if enabled. (R/W)

UART_XONOFF_DEL Set this bit to remove flow control characters from the received data. (R/W)

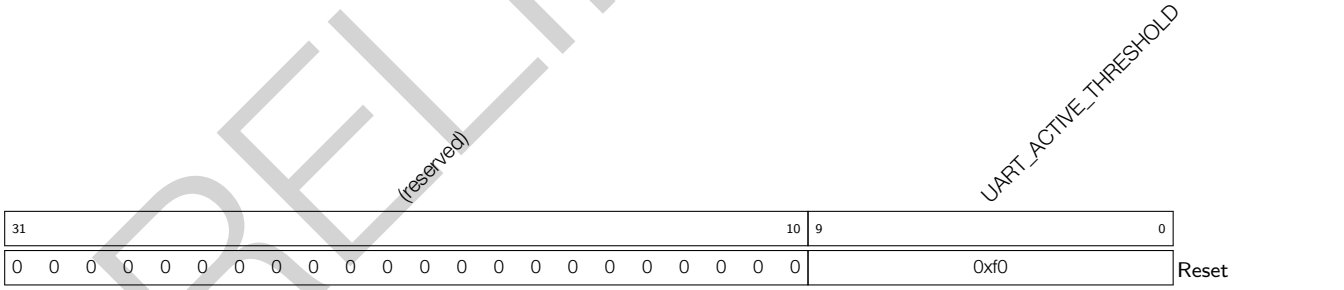
UART_FORCE_XON Set this bit to force the transmitter to send data. (R/W)

UART_FORCE_XOFF Set this bit to stop the transmitter from sending data. (R/W)

UART_SEND_XON Set this bit to send an XON character. This bit is cleared by hardware automatically. (R/W/SS/SC)

UART_SEND_XOFF Set this bit to send an XOFF character. This bit is cleared by hardware automatically. (R/W/SS/SC)

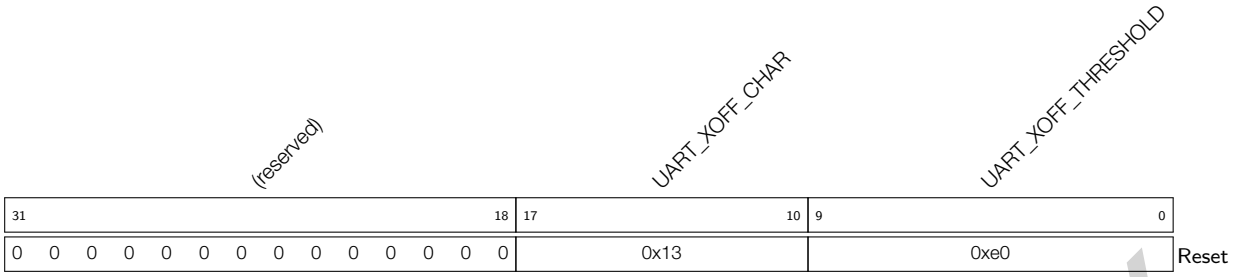
Register 24.12. UART_SLEEP_CONF_REG (0x0038)



UART_ACTIVE_THRESHOLD UART is activated from Light-sleep mode when the input RXD edge changes more times than the value of this field. (R/W)

PRELIMINARY

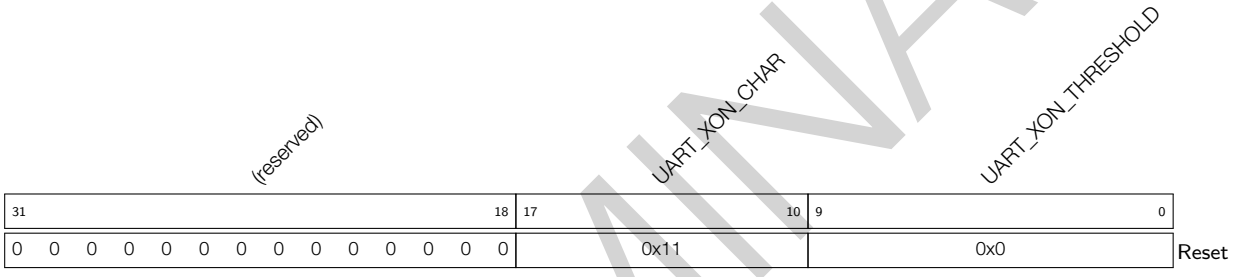
Register 24.13. UART_SWFC_CONF0_REG (0x003C)



UART_XOFF_THRESHOLD When the number of data bytes in RX FIFO is more than the value of this field with UART_SW_FLOW_CON_EN set to 1, the transmitter sends an XOFF character. (R/W)

UART_XOFF_CHAR This field stores the XOFF flow control character. (R/W)

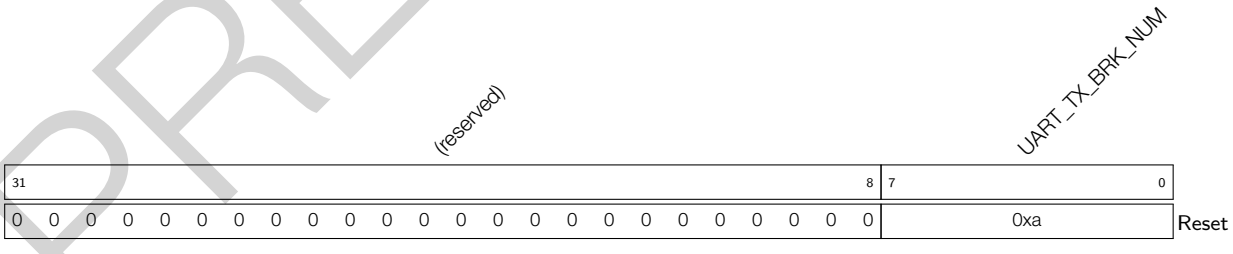
Register 24.14. UART_SWFC_CONF1_REG (0x0040)



UART_XON_THRESHOLD When the number of data bytes in RX FIFO is less than the value of this field with UART_SW_FLOW_CON_EN set to 1, the transmitter sends an XON character. (R/W)

UART_XON_CHAR This field stores the XON flow control character. (R/W)

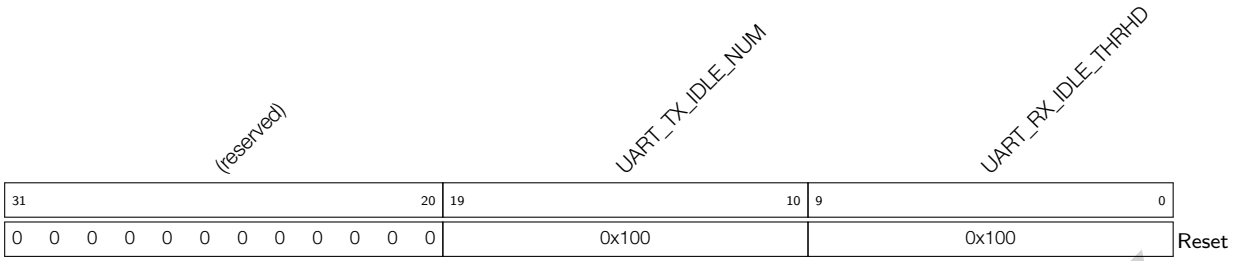
Register 24.15. UART_TXBRK_CONF_REG (0x0044)



UART_TX_BRK_NUM This field is used to configure the number of 0 to be sent after the process of sending data is done. It is active when UART_TXD_BRK is set to 1. (R/W)

PRELIMINARY

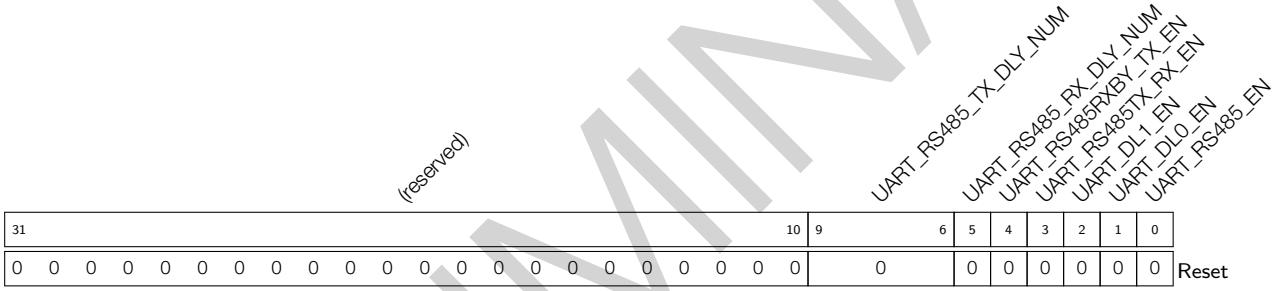
Register 24.16. UART_IDLE_CONF_REG (0x0048)



UART_RX_IDLE_THRHD A frame end signal is generated when the receiver takes more time to receive one byte data than the value of this field, in the unit of bit time (the time it takes to transfer one bit). (R/W)

UART_TX_IDLE_NUM This field is used to configure the duration time between transfers, in the unit of bit time (the time it takes to transfer one bit). (R/W)

Register 24.17. UART_RS485_CONF_REG (0x004C)



UART_RS485_EN Set this bit to choose RS485 mode. (R/W)

UART_DL0_EN Set this bit to delay the stop bit by 1 bit. (R/W)

UART_DL1_EN Set this bit to delay the stop bit by 1 bit. (R/W)

UART_RS485TX_RX_EN Set this bit to enable receiver could receive data when the transmitter is transmitting data in RS485 mode. (R/W)

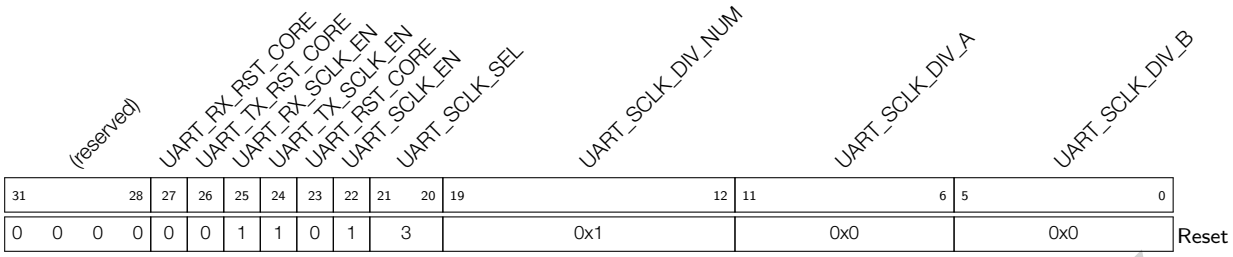
UART_RS485RXBY_TX_EN 1: enable RS485 transmitter to send data when RS485 receiver line is busy. (R/W)

UART_RS485_RX_DLY_NUM This bit is used to delay the receiver's internal data signal. (R/W)

UART_RS485_TX_DLY_NUM This field is used to delay the transmitter's internal data signal. (R/W)

PRELIMINARY

Register 24.18. UART_CLK_CONF_REG (0x0078)



UART_SCLK_DIV_B The denominator of the frequency divisor. (R/W)

UART_SCLK_DIV_A The numerator of the frequency divisor. (R/W)

UART_SCLK_DIV_NUM The integral part of the frequency divisor. (R/W)

UART_SCLK_SEL Selects UART clock source. 1: APB_CLK; 2: FOSC_CLK; 3: XTAL_CLK. (R/W)

UART_SCLK_EN Set this bit to enable UART TX/RX clock. (R/W)

UART_RST_CORE Write 1 and then write 0 to this bit, to reset UART TX/RX. (R/W)

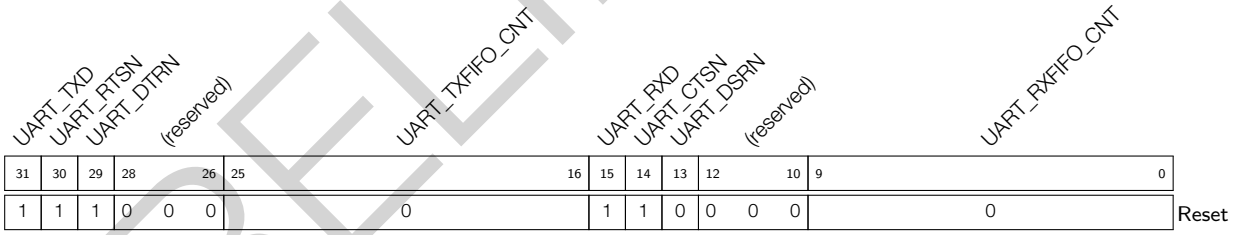
UART_TX_SCLK_EN Set this bit to enable UART TX clock. (R/W)

UART_RX_SCLK_EN Set this bit to enable UART RX clock. (R/W)

UART_TX_RST_CORE Write 1 and then write 0 to this bit, to reset UART TX. (R/W)

UART_RX_RST_CORE Write 1 and then write 0 to this bit, to reset UART RX. (R/W)

Register 24.19. UART_STATUS_REG (0x001C)



UART_RXFIFO_CNT Stores the number of valid data bytes in RX FIFO. (RO)

UART_DSRN This bit represents the level of the internal UART DSR signal. (RO)

UART_CTSN This bit represents the level of the internal UART CTS signal. (RO)

UART_RXD This bit represents the level of the internal UART RXD signal. (RO)

UART_TXFIFO_CNT Stores the number of data bytes in TX FIFO. (RO)

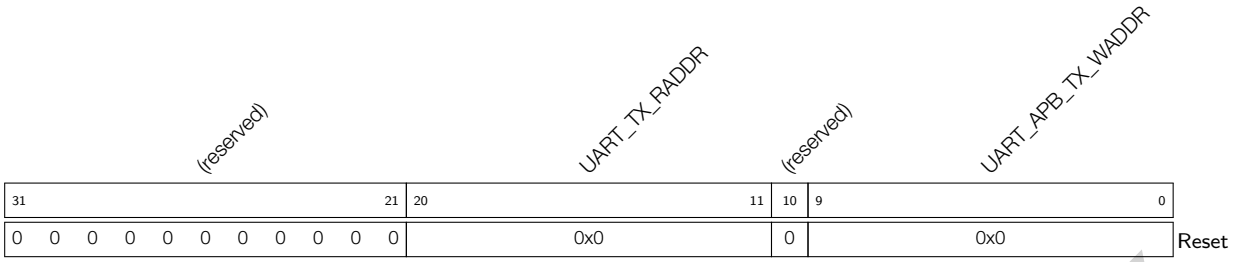
UART_DTRN This bit represents the level of the internal UART DTR signal. (RO)

UART_RTSN This bit represents the level of the internal UART RTS signal. (RO)

UART_TXD This bit represents the level of the internal UART TXD signal. (RO)

PRELIMINARY

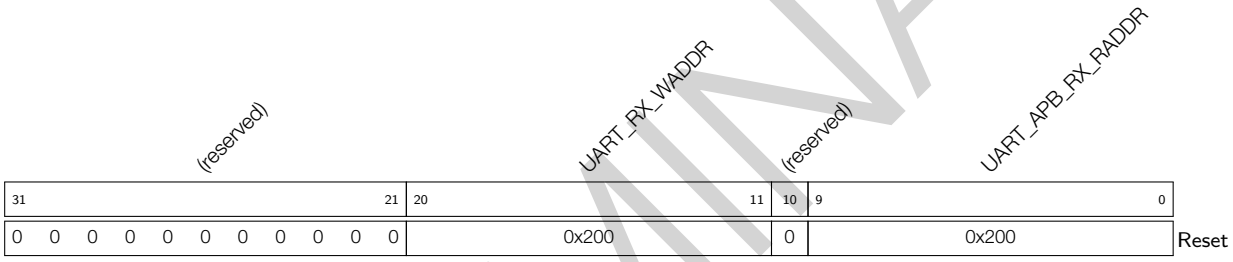
Register 24.20. UART_MEM_TX_STATUS_REG (0x0064)



UART_APB_TX_WADDR This field stores the offset address in TX FIFO when software writes TX FIFO via APB. (RO)

UART_TX_RADDR This field stores the offset address in TX FIFO when TX FSM reads data via Tx_FIFO_Ctrl. (RO)

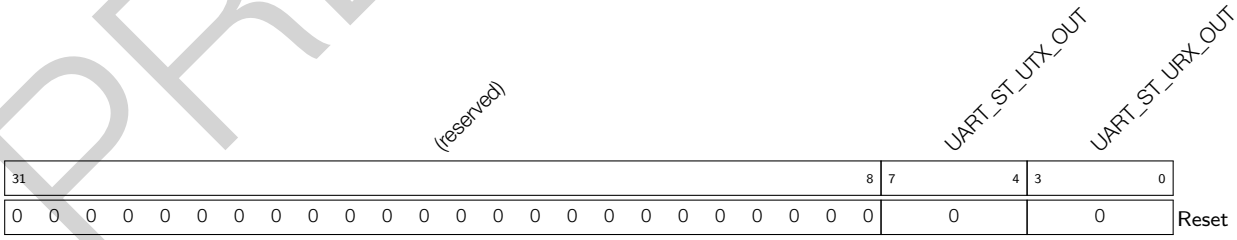
Register 24.21. UART_MEM_RX_STATUS_REG (0x0068)



UART_APB_RX_RADDR This field stores the offset address in RX FIFO when software reads data from RX FIFO via APB. UART0 is 0x200. UART1 is 0x280. UART2 is 0x300. (RO)

UART_RX_WADDR This field stores the offset address in RX FIFO when Rx_FIFO_Ctrl writes RX FIFO. UART0 is 0x200. UART1 is 0x280. UART2 is 0x300. (RO)

Register 24.22. UART_FSM_STATUS_REG (0x006C)

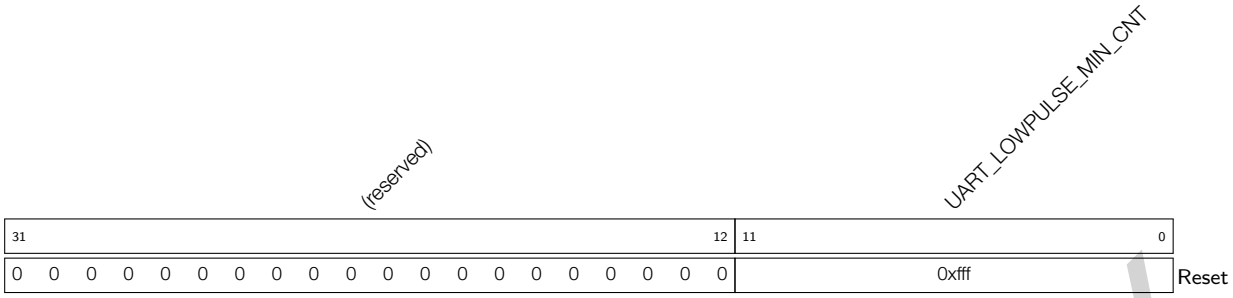


UART_ST_URX_OUT This is the status field of the receiver. (RO)

UART_ST_UTX_OUT This is the status field of the transmitter. (RO)

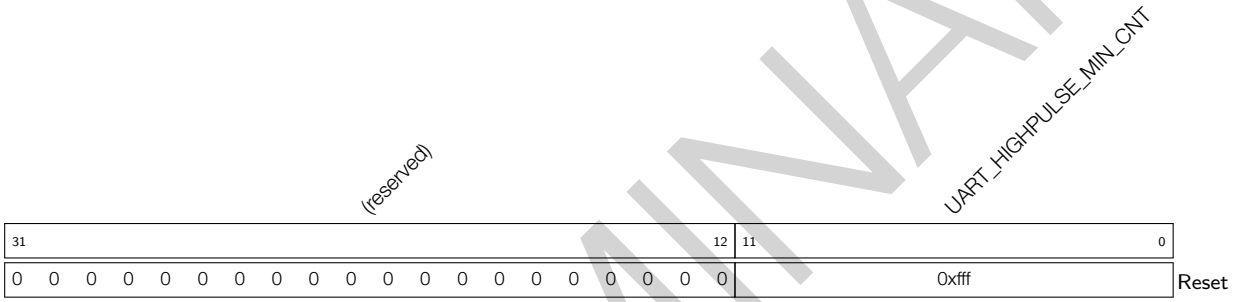
PRELIMINARY

Register 24.23. UART_LOWPULSE_REG (0x0028)



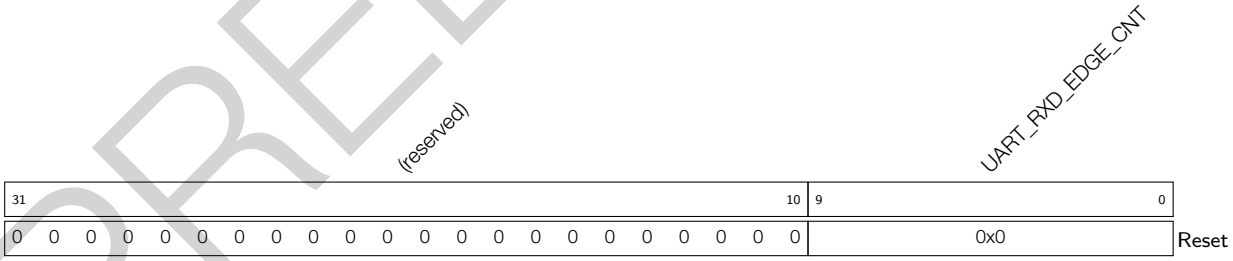
UART_LOWPULSE_MIN_CNT This field stores the value of the minimum duration time of the low level pulse, in the unit of APB_CLK cycles. It is used in baud rate detection. (RO)

Register 24.24. UART_HIGHPULSE_REG (0x002C)



UART_HIGHPULSE_MIN_CNT This field stores the value of the maximum duration time for the high level pulse, in the unit of APB_CLK cycles. It is used in baud rate detection. (RO)

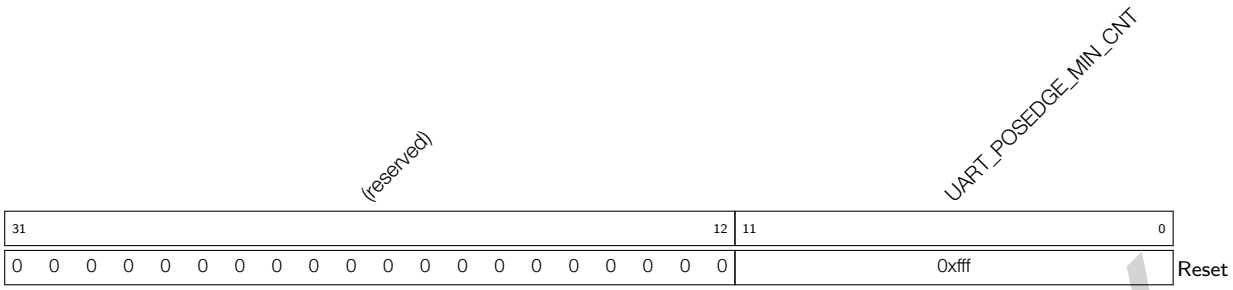
Register 24.25. UART_RXD_CNT_REG (0x0030)



UART_RXD_EDGE_CNT This field stores the count of RXD edge change. It is used in baud rate detection. (RO)

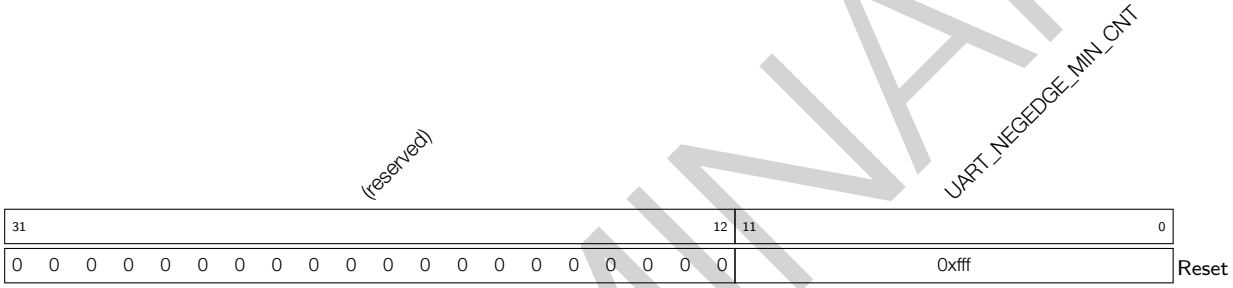
PRELIMINARY

Register 24.26. UART_POSPULSE_REG (0x0070)



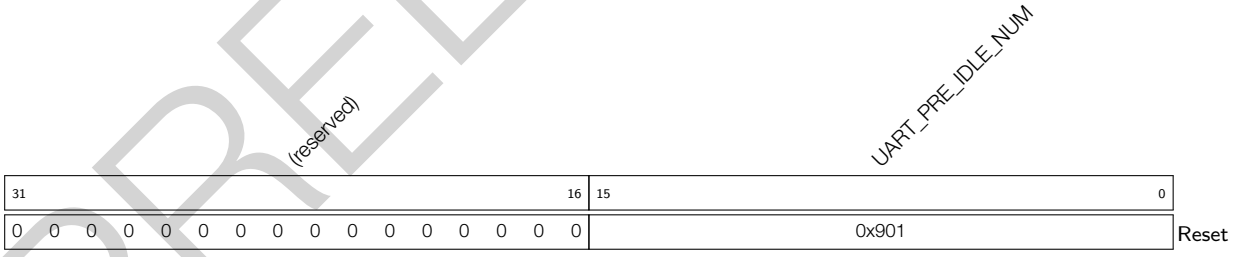
UART_POSEDGE_MIN_CNT This field stores the minimal input clock count between two positive edges. It is used in baud rate detection. (RO)

Register 24.27. UART_NEGPULSE_REG (0x0074)



UART_NEGEDGE_MIN_CNT This field stores the minimal input clock count between two negative edges. It is used in baud rate detection. (RO)

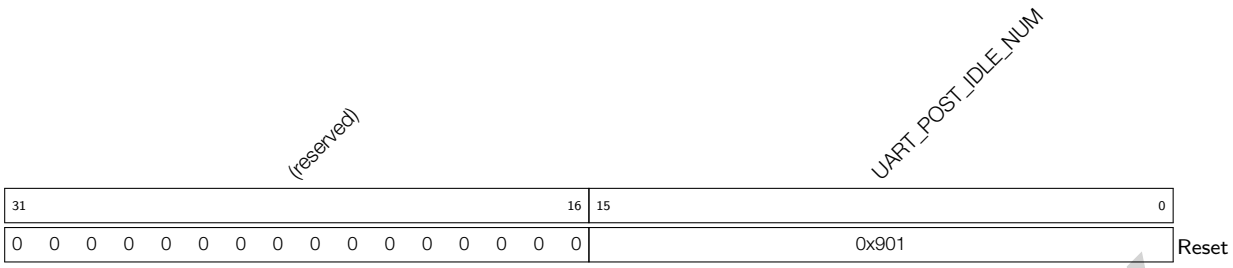
Register 24.28. UART_AT_CMD_PRECNT_REG (0x0050)



UART_PRE_IDLE_NUM This field is used to configure the idle duration time before the first AT_CMD is received by the receiver, in the unit of bit time (the time it takes to transfer one bit). (R/W)

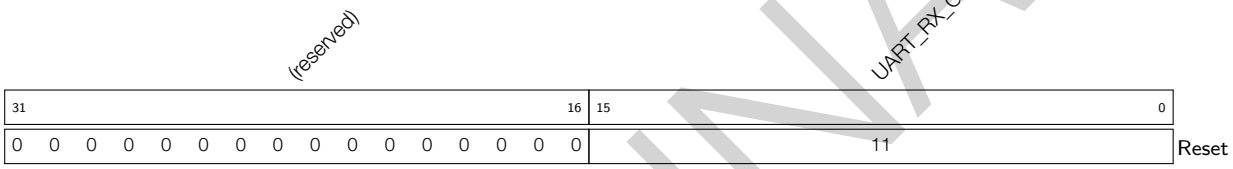
PRELIMINARY

Register 24.29. UART_AT_CMD_POSTCNT_REG (0x0054)



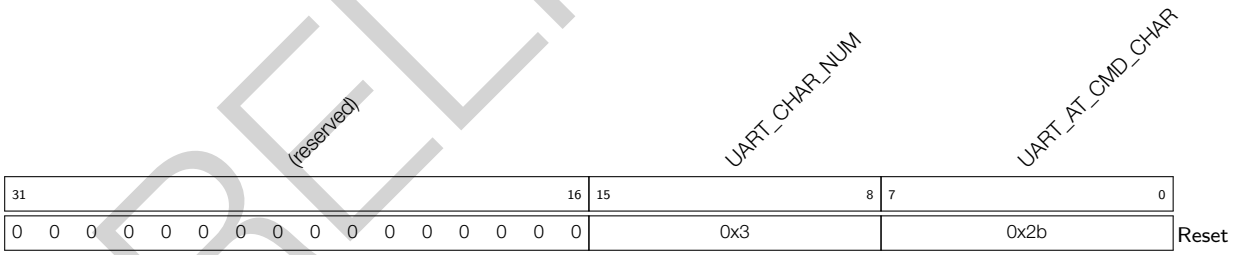
UART_POST_IDLE_NUM This field is used to configure the duration time between the last AT_CMD and the next data byte, in the unit of bit time (the time it takes to transfer one bit). (R/W)

Register 24.30. UART_AT_CMD_GAPTOUT_REG (0x0058)



UART_RX_GAP_TOUT This field is used to configure the duration time between the AT_CMD characters, in the unit of bit time (the time it takes to transfer one bit). (R/W)

Register 24.31. UART_AT_CMD_CHAR_REG (0x005C)

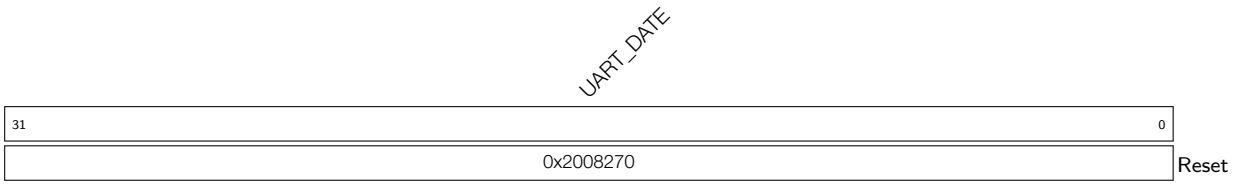


UART_AT_CMD_CHAR This field is used to configure the content of AT_CMD character. (R/W)

UART_CHAR_NUM This field is used to configure the number of continuous AT_CMD characters received by the receiver. (R/W)

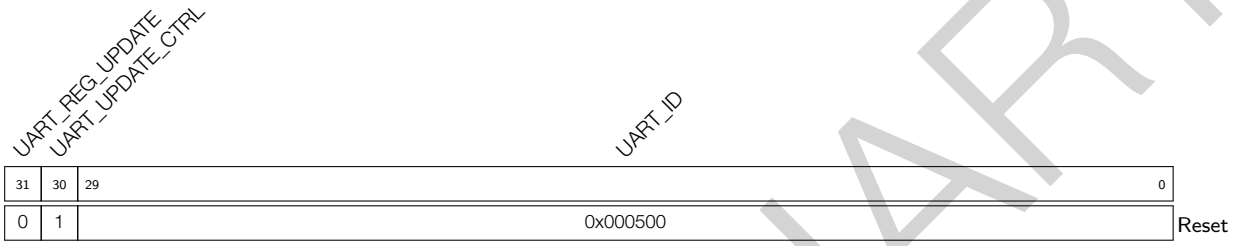
PRELIMINARY

Register 24.32. UART_DATE_REG (0x007C)



UART_DATE This is the version control register. (R/W)

Register 24.33. UART_ID_REG (0x0080)



UART_ID This field is used to configure the UART_ID. (R/W)

UART_UPDATE_CTRL This bit is used to control register synchronization mode. 0: After registers are configured, software needs to write 1 to UART_REG_UPDATE to synchronize registers; 1: Registers are automatically synchronized into UART Core's clock domain. (R/W)

UART_REG_UPDATE When this bit is set to 1 by software, registers are synchronized to UART Core's clock domain. This bit is cleared by hardware after synchronization is done. (R/W/SC)

24.7.2 UHCI Regsiters

The addresses in this section are relative to UHCI Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

PRELIMINARY

Register 24.34. UHCI_CONF0_REG (0x0000)



UHCI_TX_RST Write 1, then write 0 to this bit to reset decode state machine. (R/W)

UHCI_RX_RST Write 1, then write 0 to this bit to reset encode state machine. (R/W)

UHCI_UART0_CE Set this bit to link up UHCI and UART0. (R/W)

UHCI_UART1_CE Set this bit to link up UHCI and UART1. (R/W)

UHCI_UART2_CE Set this bit to link up UHCI and UART2. (R/W)

UHCI_SEPER_EN Set this bit to separate the data frame using a special character. (R/W)

UHCI_HEAD_EN Set this bit to encode the data packet with a formatting header. (R/W)

UHCI_CRC_REC_EN Set this bit to enable UHCI to receive the 16 bit CRC. (R/W)

UHCI_UART_IDLE_EOF_EN If this bit is set to 1, UHCI will end the payload receiving process when UART has been in idle state. (R/W)

UHCI_LEN_EOF_EN If this bit is set to 1, UHCI decoder stops receiving payload data when the number of received data bytes has reached the specified value. The value is payload length indicated by UHCI packet header when UHCI_HEAD_EN is 1 or the value is configuration value when UHCI_HEAD_EN is 0. If this bit is set to 0, UHCI decoder stops receiving payload data when 0xC0 has been received. (R/W)

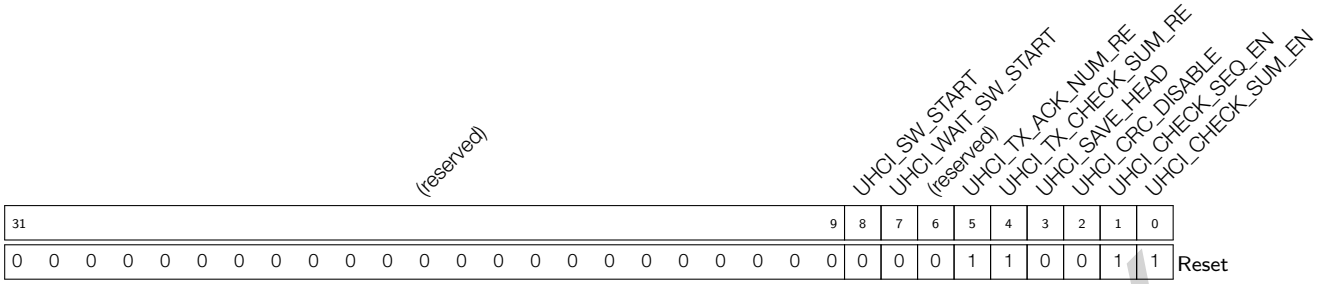
UHCI_ENCODE_CRC_EN Set this bit to enable data integrity check by appending a 16 bit CCITT-CRC to end of the payload. (R/W)

UHCI_CLK_EN 0: Support clock only when application writes registers; 1: Force clock on for registers. (R/W)

UHCI_UART_RX_BRK_EOF_EN If this bit is set to 1, UHCI will end payload receive process when NULL frame is received by UART. (R/W)

PRELIMINARY

Register 24.35. UHCI_CONF1_REG (0x0018)



UHCI_CHECK_SUM_EN This is the enable bit to check header checksum when UHCI receives a data packet. (R/W)

UHCI_CHECK_SEQ_EN This is the enable bit to check sequence number when UHCI receives a data packet. (R/W)

UHCI_CRC_DISABLE Set this bit to support CRC calculation. Data Integrity Check Present bit in UHCI packet frame should be 1. (R/W)

UHCI_SAVE_HEAD Set this bit to save the packet header when UHCI receives a data packet. (R/W)

UHCI_TX_CHECK_SUM_RE Set this bit to encode the data packet with a checksum. (R/W)

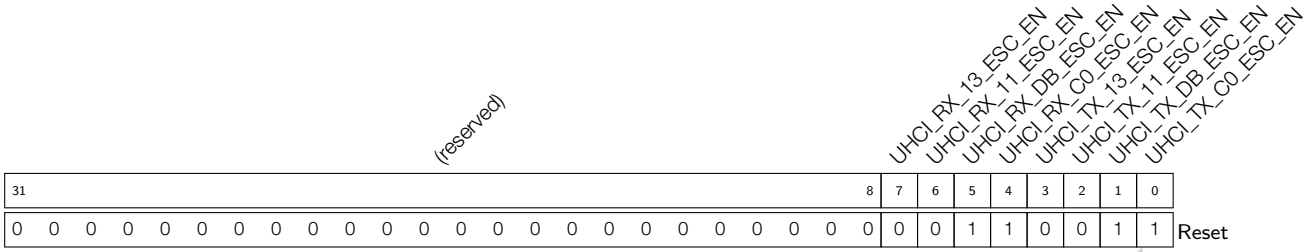
UHCI_TX_ACK_NUM_RE Set this bit to encode the data packet with an acknowledgment when a reliable packet is to be transmitted. (R/W)

UHCI_WAIT_SW_START The UHCI encoder will jump to ST_SW_WAIT status if this bit is set to 1. (R/W)

UHCI_SW_START If current UHCI_ENCODE_STATE is ST_SW_WAIT, the UHCI will start to send data packet out when this bit is set to 1. (R/W/SC)

PRELIMINARY

Register 24.36. UHCI_ESCAPE_CONF_REG (0x0024)



UHCI_TX_C0_ESC_EN Set this bit to to decode character 0xC0 when DMA receives data. (R/W)

UHCI_TX_DB_ESC_EN Set this bit to to decode character 0xDB when DMA receives data. (R/W)

UHCI_TX_11_ESC_EN Set this bit to to decode flow control character 0x11 when DMA receives data. (R/W)

UHCI_TX_13_ESC_EN Set this bit to to decode flow control character 0x13 when DMA receives data. (R/W)

UHCI_RX_C0_ESC_EN Set this bit to replace 0xC0 by special characters when DMA sends data. (R/W)

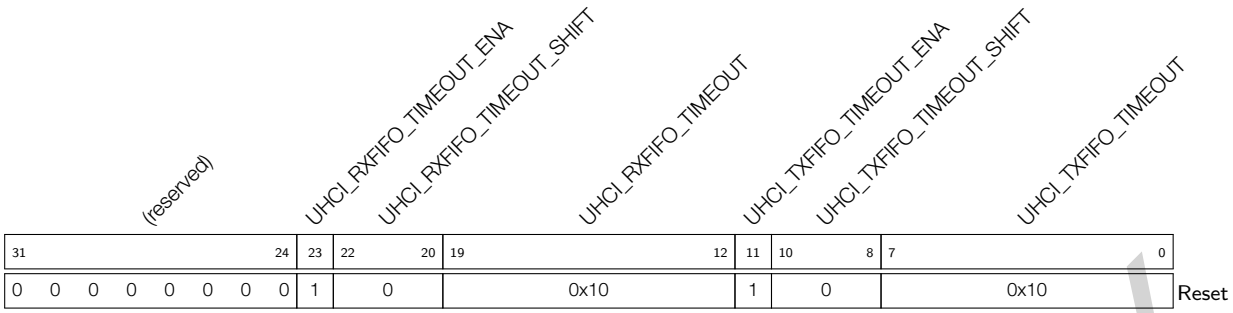
UHCI_RX_DB_ESC_EN Set this bit to replace 0xDB by special characters when DMA sends data. (R/W)

UHCI_RX_11_ESC_EN Set this bit to replace flow control character 0x11 by special characters when DMA sends data. (R/W)

UHCI_RX_13_ESC_EN Set this bit to replace flow control character 0x13 by special characters when DMA sends data. (R/W)

PRELIMINARY

Register 24.37. UHCI_HUNG_CONF_REG (0x0028)



UHCI_TXFIFO_TIMEOUT This field stores the timeout value. UHCI will produce the UHCI_TX_HUNG_INT interrupt when DMA takes more time to receive data. (R/W)

UHCI_TXFIFO_TIMEOUT_SHIFT This field is used to configure the maximum tick count. (R/W)

UHCI_TXFIFO_TIMEOUT_ENA This is the enable bit for TX FIFO receive timeout. (R/W)

UHCI_RXFIFO_TIMEOUT This field stores the timeout value. UHCI will produce the UHCI_RX_HUNG_INT interrupt when DMA takes more time to read data from RAM. (R/W)

UHCI_RXFIFO_TIMEOUT_SHIFT This field is used to configure the maximum tick count. (R/W)

UHCI_RXFIFO_TIMEOUT_ENA This is the enable bit for DMA send timeout. (R/W)

Register 24.38. UHCI_ACK_NUM_REG (0x002C)

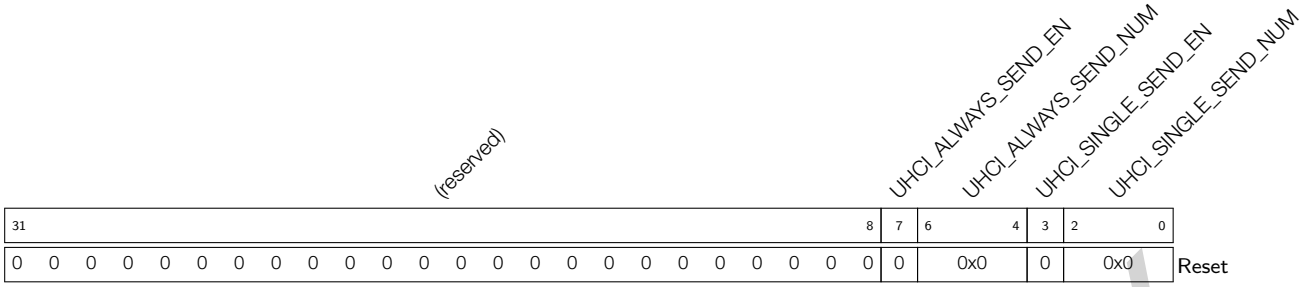


UHCI_ACK_NUM This is the ACK number used in software flow control. (R/W)

UHCI_ACK_NUM_LOAD Set this bit to 1, and the value configured by UHCI_ACK_NUM would be loaded. (WT)

PRELIMINARY

Register 24.39. UHCI_QUICK_SENT_REG (0x0034)



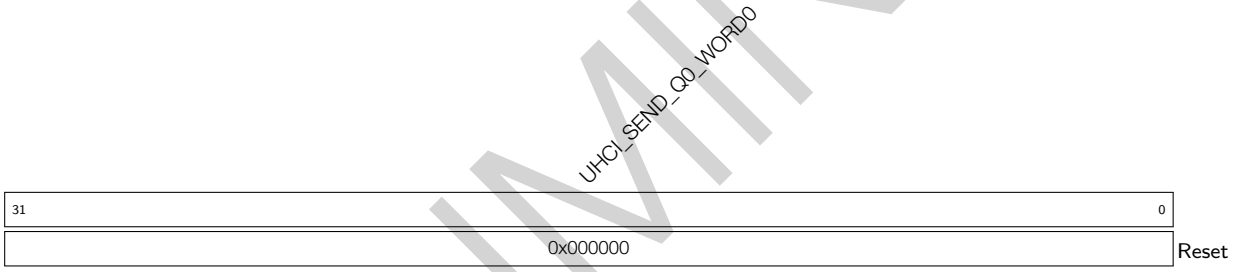
UHCI_SINGLE_SEND_NUM This field is used to specify single_send mode. (R/W)

UHCI_SINGLE_SEND_EN Set this bit to enable single_send mode to send short packets. (R/W/SC)

UHCI_ALWAYS_SEND_NUM This field is used to specify always_send mode. (R/W)

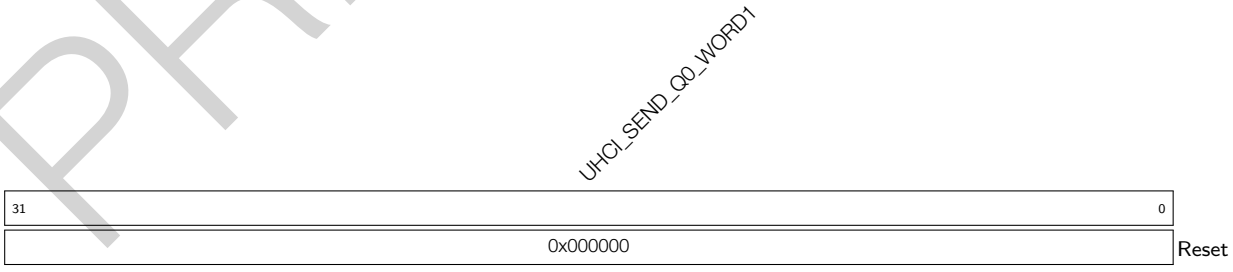
UHCI_ALWAYS_SEND_EN Set this bit to enable always_send mode to send short packets. (R/W)

Register 24.40. UHCI_REG_Q0_WORD0_REG (0x0038)



UHCI_SEND_Q0_WORD0 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

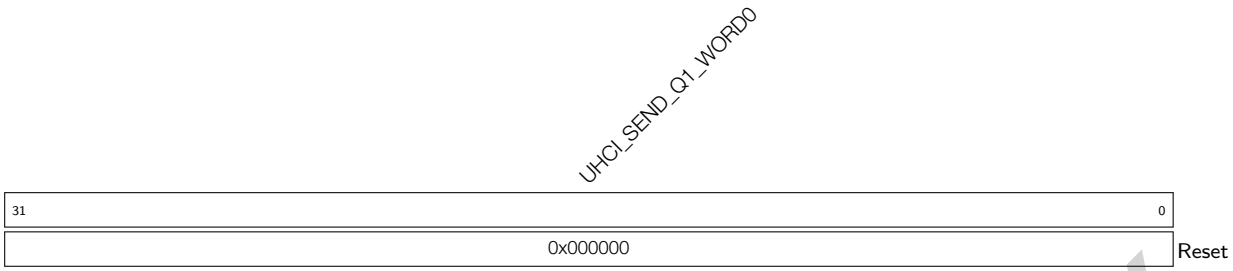
Register 24.41. UHCI_REG_Q0_WORD1_REG (0x003C)



UHCI_SEND_Q0_WORD1 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

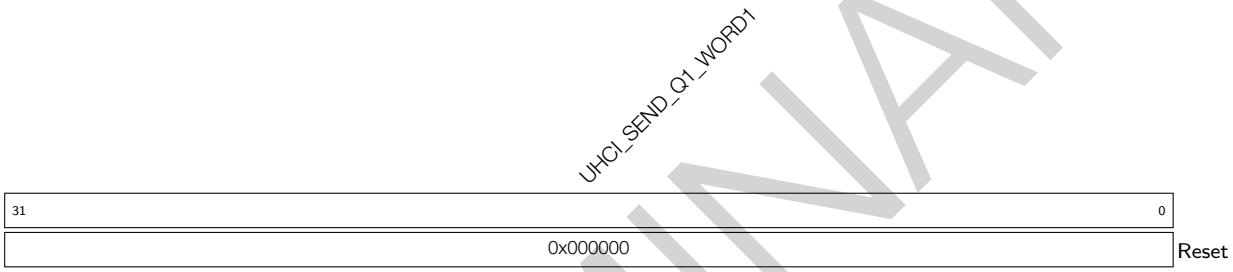
PRELIMINARY

Register 24.42. UHCI_REG_Q1_WORD0_REG (0x0040)



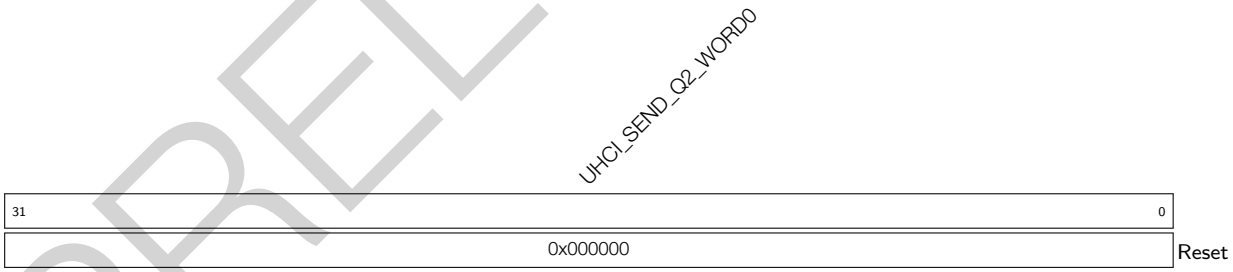
UHCI_SEND_Q1_WORD0 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

Register 24.43. UHCI_REG_Q1_WORD1_REG (0x0044)



UHCI_SEND_Q1_WORD1 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

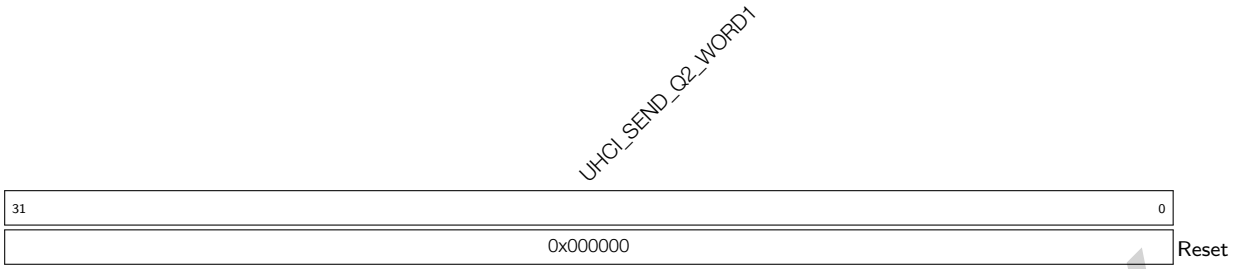
Register 24.44. UHCI_REG_Q2_WORD0_REG (0x0048)



UHCI_SEND_Q2_WORD0 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

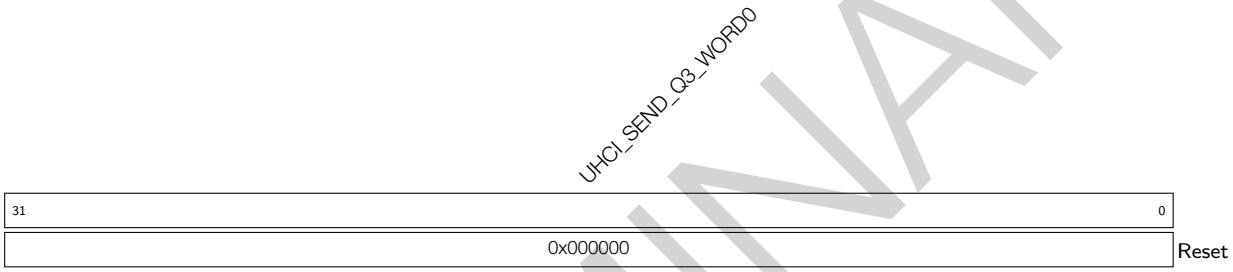
PRELIMINARY

Register 24.45. UHCI_REG_Q2_WORD1_REG (0x004C)



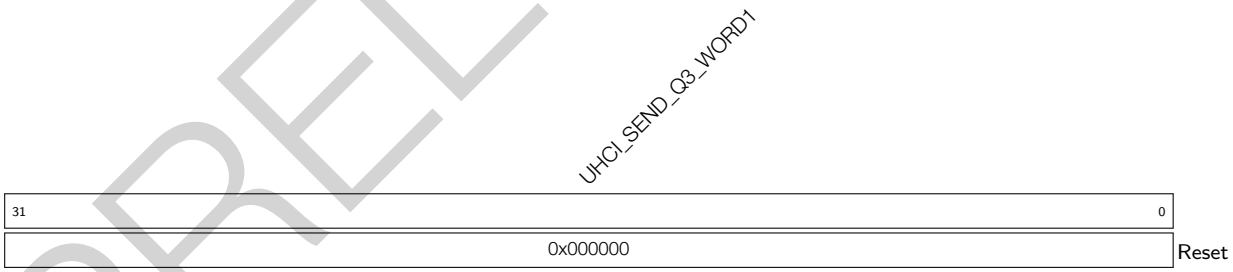
UHCI_SEND_Q2_WORD1 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

Register 24.46. UHCI_REG_Q3_WORD0_REG (0x0050)



UHCI_SEND_Q3_WORD0 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

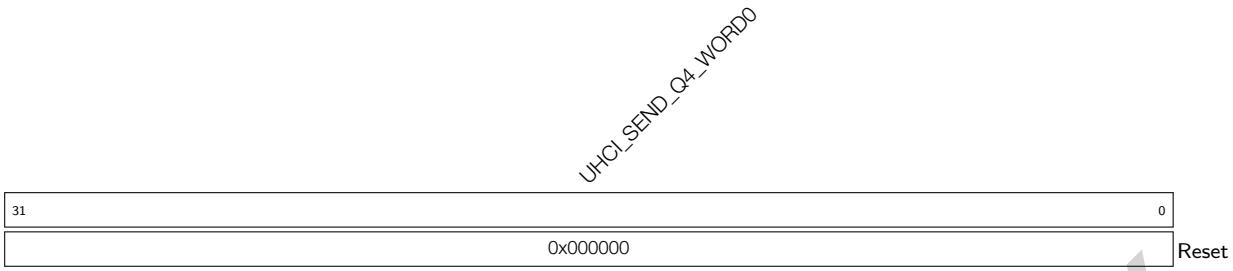
Register 24.47. UHCI_REG_Q3_WORD1_REG (0x0054)



UHCI_SEND_Q3_WORD1 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

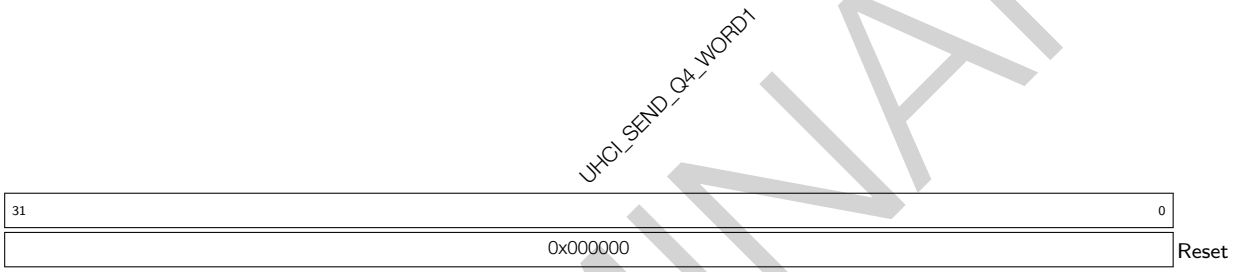
PRELIMINARY

Register 24.48. UHCI_REG_Q4_WORD0_REG (0x0058)



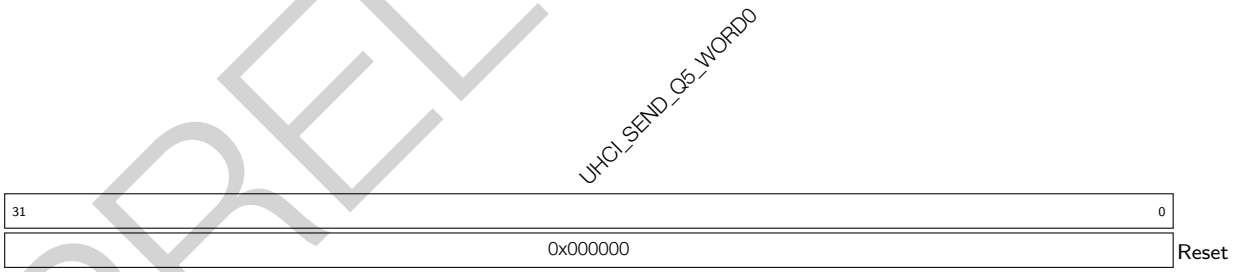
UHCI_SEND_Q4_WORD0 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

Register 24.49. UHCI_REG_Q4_WORD1_REG (0x005C)



UHCI_SEND_Q4_WORD1 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

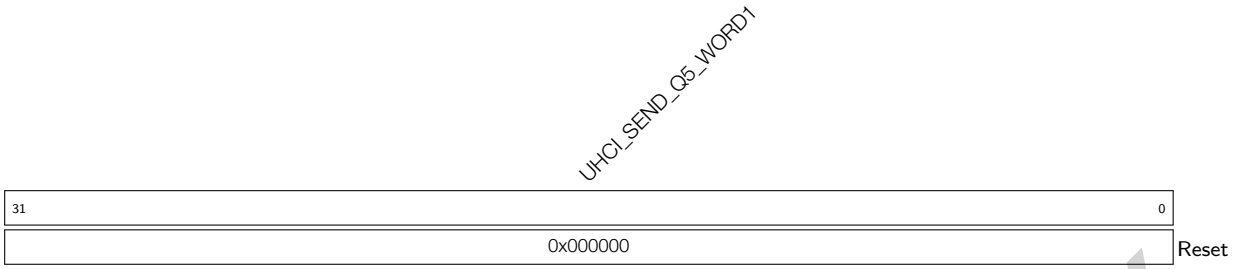
Register 24.50. UHCI_REG_Q5_WORD0_REG (0x0060)



UHCI_SEND_Q5_WORD0 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

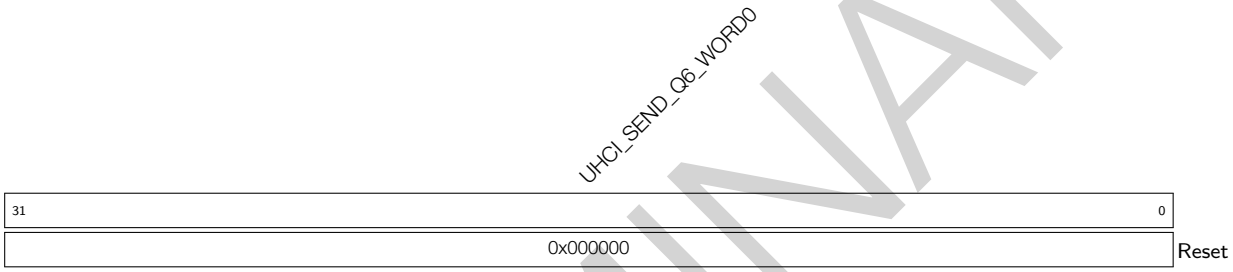
PRELIMINARY

Register 24.51. UHCI_REG_Q5_WORD1_REG (0x0064)



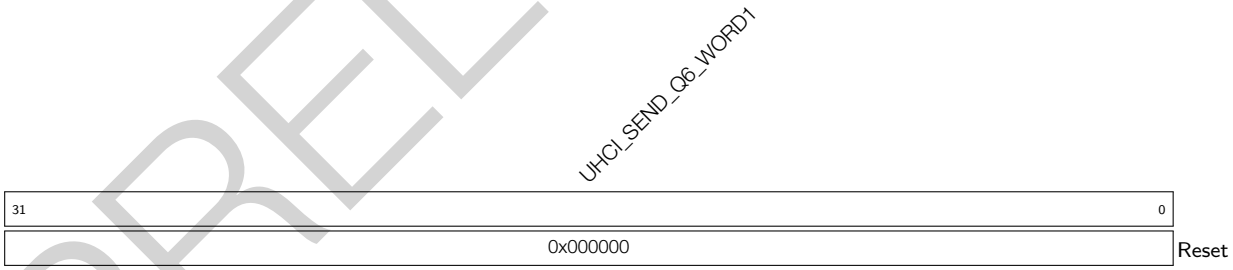
UHCI_SEND_Q5_WORD1 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

Register 24.52. UHCI_REG_Q6_WORD0_REG (0x0068)



UHCI_SEND_Q6_WORD0 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

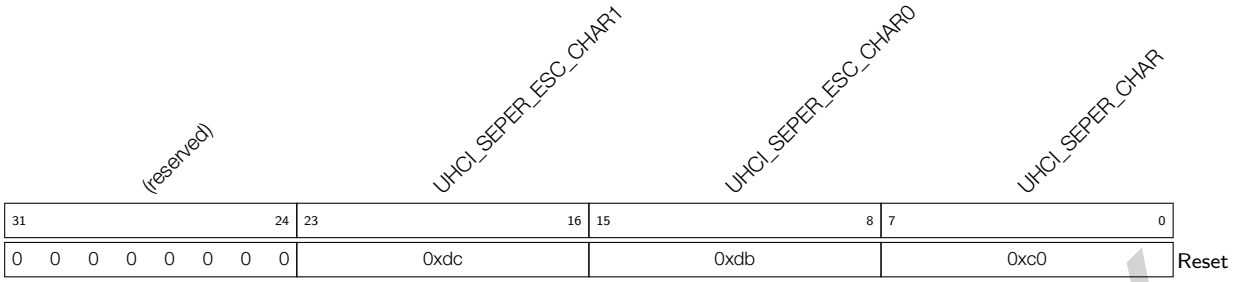
Register 24.53. UHCI_REG_Q6_WORD1_REG (0x006C)



UHCI_SEND_Q6_WORD1 This register is used as a quick_sent register when mode is specified by UHCI_ALWAYS_SEND_NUM or UHCI_SINGLE_SEND_NUM. (R/W)

PRELIMINARY

Register 24.54. UHCI_ESC_CONF0_REG (0x0070)

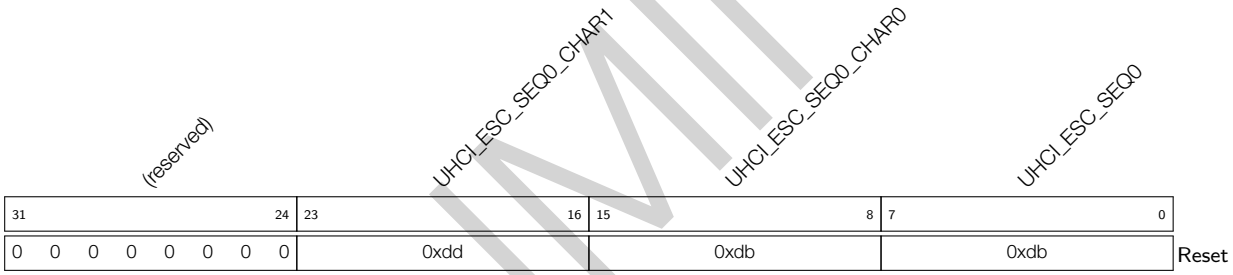


UHCI_SEPER_CHAR This field is used to define separators to encode data packets. The default value is 0xC0. (R/W)

UHCI_SEPER_ESC_CHAR0 This field is used to define the first character of SLIP escape sequence. The default value is 0xDB. (R/W)

UHCI_SEPER_ESC_CHAR1 This field is used to define the second character of SLIP escape sequence. The default value is 0xDC. (R/W)

Register 24.55. UHCI_ESC_CONF1_REG (0x0074)



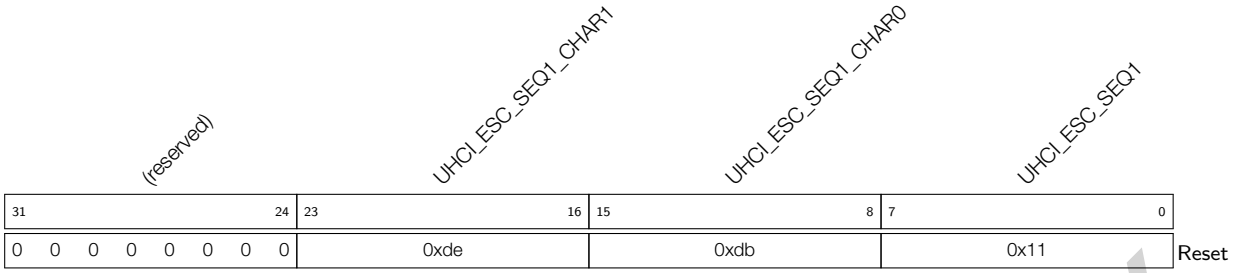
UHCI_ESC_SEQ0 This field is used to define a character that need to be encoded. The default value is 0xDB that used as the first character of SLIP escape sequence. (R/W)

UHCI_ESC_SEQ0_CHAR0 This field is used to define the first character of SLIP escape sequence. The default value is 0xDB. (R/W)

UHCI_ESC_SEQ0_CHAR1 This field is used to define the second character of SLIP escape sequence. The default value is 0xDD. (R/W)

PRELIMINARY

Register 24.56. UHCI_ESC_CONF2_REG (0x0078)

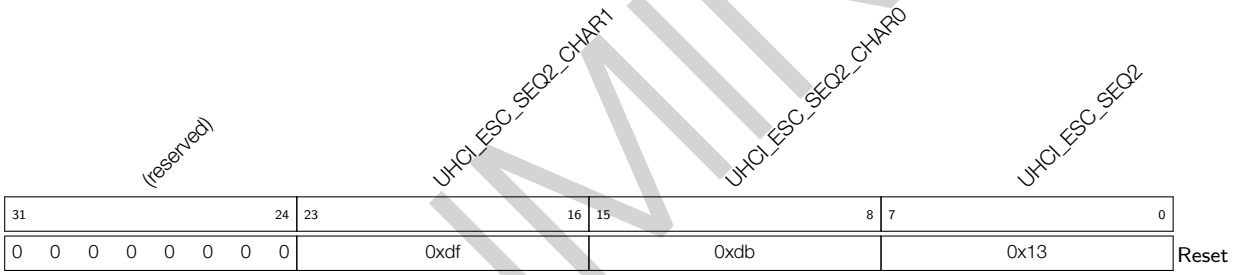


UHCI_ESC_SEQ1 This field is used to define a character that need to be encoded. The default value is 0x11 that used as a flow control character. (R/W)

UHCI_ESC_SEQ1_CHAR0 This field is used to define the first character of SLIP escape sequence. The default value is 0xDB. (R/W)

UHCI_ESC_SEQ1_CHAR1 This field is used to define the second character of SLIP escape sequence. The default value is 0xDE. (R/W)

Register 24.57. UHCI_ESC_CONF3_REG (0x007C)



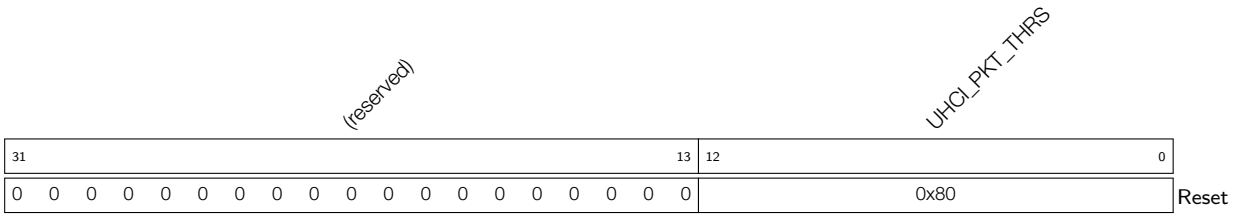
UHCI_ESC_SEQ2 This field is used to define a character that need to be decoded. The default value is 0x13 that used as a flow control character. (R/W)

UHCI_ESC_SEQ2_CHAR0 This field is used to define the first character of SLIP escape sequence. The default value is 0xDB. (R/W)

UHCI_ESC_SEQ2_CHAR1 This field is used to define the second character of SLIP escape sequence. The default value is 0xDF. (R/W)

PRELIMINARY

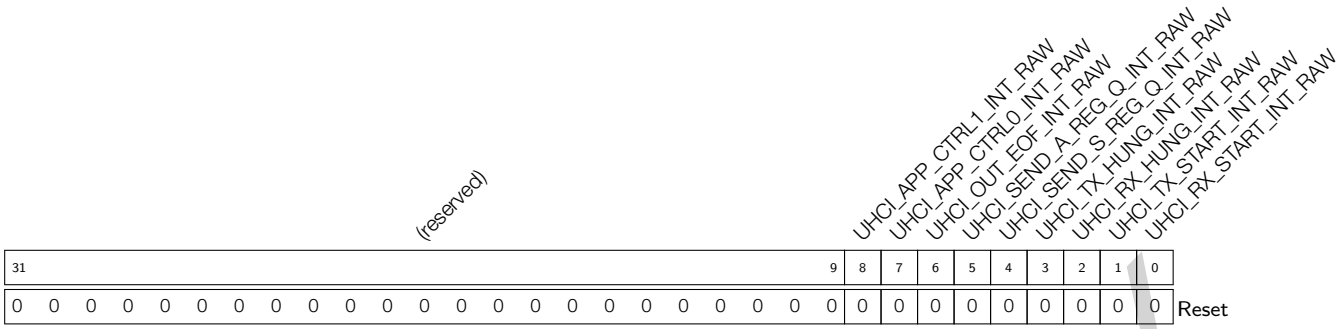
Register 24.58. UHCI_PKT_THRES_REG (0x0080)



UHCI_PKT_THRS This field is used to configure the maximum value of the packet length when UHCI_HEAD_EN is 0. (R/W)

PRELIMINARY

Register 24.59. UHCI_INT_RAW_REG (0x0004)



UHCI_RX_START_INT_RAW This is the interrupt raw bit for UHCI_RX_START_INT interrupt. The interrupt is triggered when a separator has been sent. (R/WTC/SS)

UHCI_TX_START_INT_RAW This is the interrupt raw bit for UHCI_TX_START_INT interrupt. The interrupt is triggered when UHCI detects a separator. (R/WTC/SS)

UHCI_RX_HUNG_INT_RAW This is the interrupt raw bit for UHCI_RX_HUNG_INT interrupt. The interrupt is triggered when UHCI takes more time to receive data than configure value. (R/WTC/SS)

UHCI_TX_HUNG_INT_RAW This is the interrupt raw bit for UHCI_TX_HUNG_INT interrupt. The interrupt is triggered when UHCI takes more time to read data from RAM than the configured value. (R/WTC/SS)

UHCI_SEND_S_REG_Q_INT_RAW This is the interrupt raw bit for UHCI_SEND_S_REG_Q_INT interrupt. The interrupt is triggered when UHCI has sent out a short packet using single_send mode. (R/WTC/SS)

UHCI_SEND_A_REG_Q_INT_RAW This is the interrupt raw bit for UHCI_SEND_A_REG_Q_INT interrupt. The interrupt is triggered when UHCI has sent out a short packet using always_send mode. (R/WTC/SS)

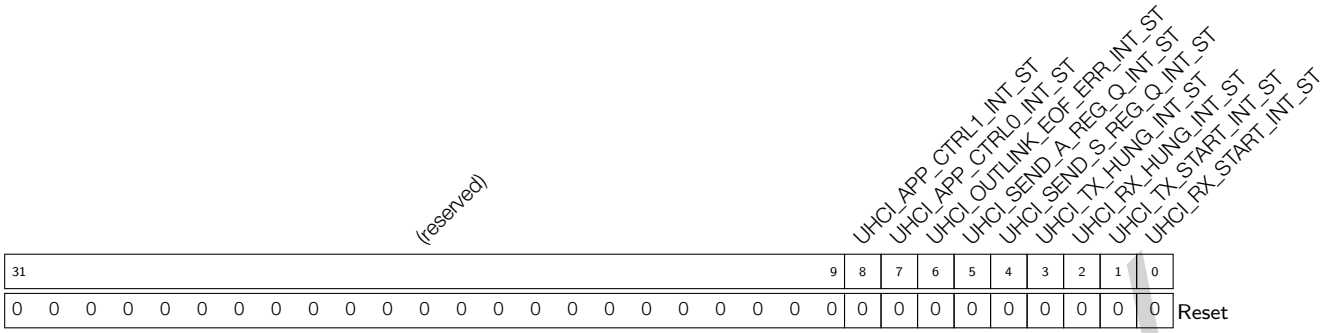
UHCI_OUT_EOF_INT_RAW This is the interrupt raw bit for UHCI_OUT_EOF_INT interrupt. The interrupt is triggered when there are some errors in EOF in the transmit descriptors. (R/WTC/SS)

UHCI_APP_CTRL0_INT_RAW This is the interrupt raw bit for UHCI_APP_CTRL0_INT interrupt. The interrupt is triggered when UHCI_APP_CTRL0_IN_SET is set. (R/W)

UHCI_APP_CTRL1_INT_RAW This is the interrupt raw bit for UHCI_APP_CTRL1_INT interrupt. The interrupt is triggered when UHCI_APP_CTRL1_IN_SET is set. (R/W)

PRELIMINARY

Register 24.60. UHCI_INT_ST_REG (0x0008)



UHCI_RX_START_INT_ST This is the masked interrupt bit for UHCI_RX_START_INT interrupt when UHCI_RX_START_INT_ENA is set to 1. (RO)

UHCI_TX_START_INT_ST This is the masked interrupt bit for UHCI_TX_START_INT interrupt when UHCI_TX_START_INT_ENA is set to 1. (RO)

UHCI_RX_HUNG_INT_ST This is the masked interrupt bit for UHCI_RX_HUNG_INT interrupt when UHCI_RX_HUNG_INT_ENA is set to 1. (RO)

UHCI_TX_HUNG_INT_ST This is the masked interrupt bit for UHCI_TX_HUNG_INT interrupt when UHCI_TX_HUNG_INT_ENA is set to 1. (RO)

UHCI_SEND_S_REG_Q_INT_ST This is the masked interrupt bit for UHCI_SEND_S_REG_Q_INT interrupt when UHCI_SEND_S_REG_Q_INT_ENA is set to 1. (RO)

UHCI_SEND_A_REG_Q_INT_ST This is the masked interrupt bit for UHCI_SEND_A_REG_Q_INT interrupt when UHCI_SEND_A_REG_Q_INT_ENA is set to 1. (RO)

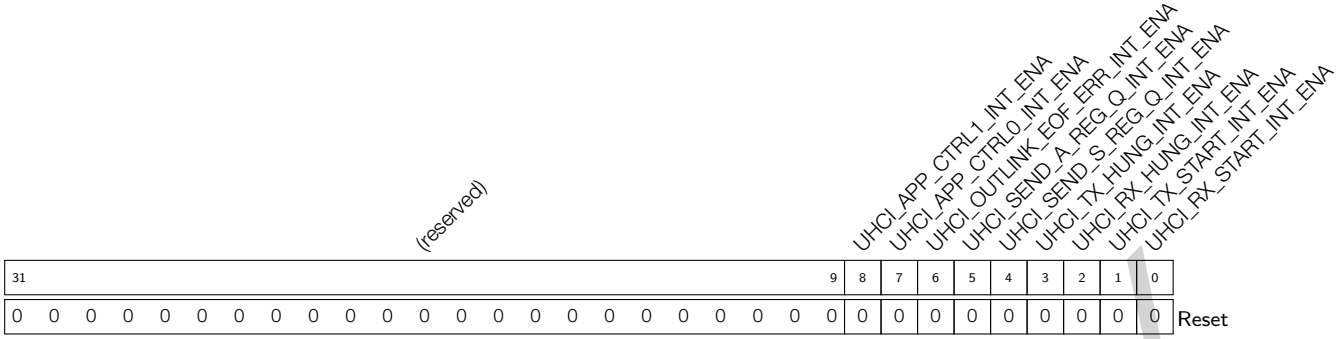
UHCI_OUTLINK_EOF_ERR_INT_ST This is the masked interrupt bit for UHCI_OUTLINK_EOF_ERR_INT interrupt when UHCI_OUTLINK_EOF_ERR_INT_ENA is set to 1. (RO)

UHCI_APP_CTRL0_INT_ST This is the masked interrupt bit for UHCI_APP_CTRL0_INT interrupt when UHCI_APP_CTRL0_INT_ENA is set to 1. (RO)

UHCI_APP_CTRL1_INT_ST This is the masked interrupt bit for UHCI_APP_CTRL1_INT interrupt when UHCI_APP_CTRL1_INT_ENA is set to 1. (RO)

PRELIMINARY

Register 24.61. UHCI_INT_ENA_REG (0x000C)



UHCI_RX_START_INT_ENA This is the interrupt enable bit for UHCI_RX_START_INT interrupt. (R/W)

UHCI_TX_START_INT_ENA This is the interrupt enable bit for UHCI_TX_START_INT interrupt. (R/W)

UHCI_RX_HUNG_INT_ENA This is the interrupt enable bit for UHCI_RX_HUNG_INT interrupt. (R/W)

UHCI_TX_HUNG_INT_ENA This is the interrupt enable bit for UHCI_TX_HUNG_INT interrupt. (R/W)

UHCI_SEND_S_REG_Q_INT_ENA This is the interrupt enable bit for UHCI_SEND_S_REG_Q_INT interrupt. (R/W)

UHCI_SEND_A_REG_Q_INT_ENA This is the interrupt enable bit for UHCI_SEND_A_REG_Q_INT interrupt. (R/W)

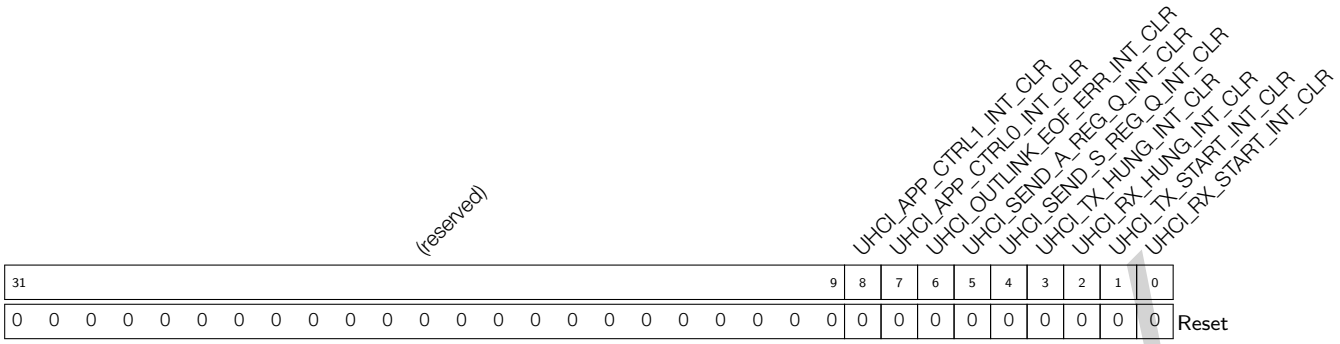
UHCI_OUTLINK_EOF_ERR_INT_ENA This is the interrupt enable bit for UHCI_OUTLINK_EOF_ERR_INT interrupt. (R/W)

UHCI_APP_CTRL0_INT_ENA This is the interrupt enable bit for UHCI_APP_CTRL0_INT interrupt. (R/W)

UHCI_APP_CTRL1_INT_ENA This is the interrupt enable bit for UHCI_APP_CTRL1_INT interrupt. (R/W)

PRELIMINARY

Register 24.62. UHCI_INT_CLR_REG (0x0010)



UHCI_RX_START_INT_CLR Set this bit to clear UHCI_RX_START_INT interrupt. (WT)

UHCI_TX_START_INT_CLR Set this bit to clear UHCI_TX_START_INT interrupt. (WT)

UHCI_RX_HUNG_INT_CLR Set this bit to clear UHCI_RX_HUNG_INT interrupt. (WT)

UHCI_TX_HUNG_INT_CLR Set this bit to clear UHCI_TX_HUNG_INT interrupt. (WT)

UHCI_SEND_S_REG_Q_INT_CLR Set this bit to clear UHCI_SEND_S_REG_Q_INT interrupt. (WT)

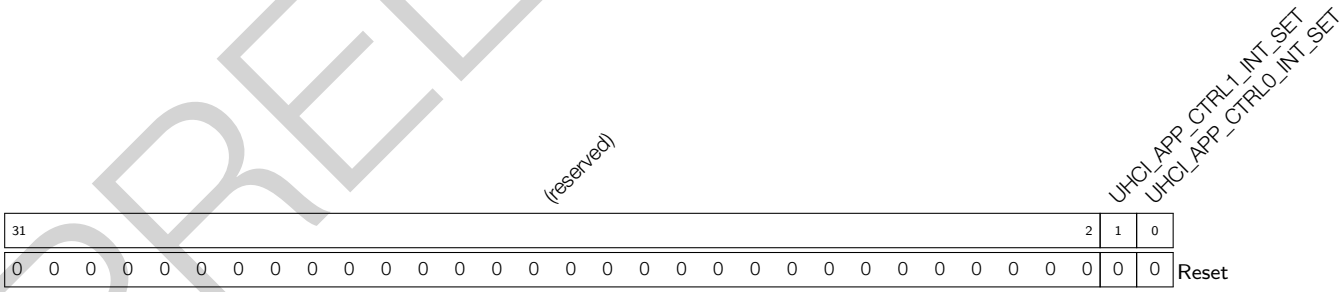
UHCI_SEND_A_REG_Q_INT_CLR Set this bit to clear UHCI_SEND_A_REG_Q_INT interrupt. (WT)

UHCI_OUTLINK_EOF_ERR_INT_CLR Set this bit to clear UHCI_OUTLINK_EOF_ERR_INT interrupt. (WT)

UHCI_APP_CTRL0_INT_CLR Set this bit to clear UHCI_APP_CTRL0_INT interrupt. (WT)

UHCI_APP_CTRL1_INT_CLR Set this bit to clear UHCI_APP_CTRL1_INT interrupt. (WT)

Register 24.63. UHCI_APP_INT_SET_REG (0x0014)

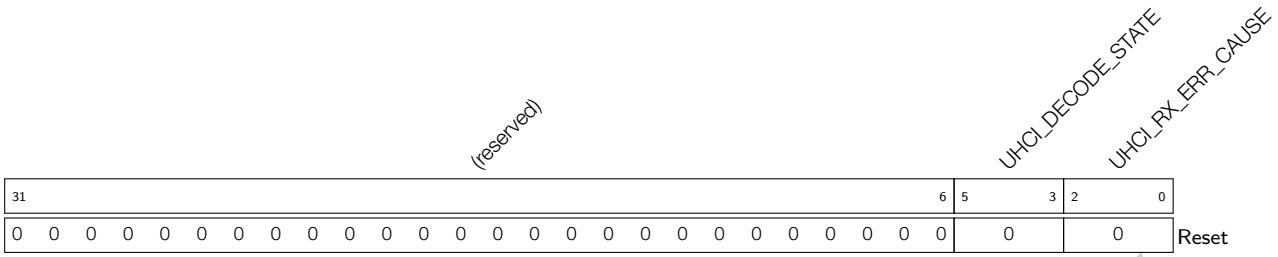


UHCI_APP_CTRL0_INT_SET This bit is software interrupt trigger source of UHCI_APP_CTRL0_INT. (WT)

UHCI_APP_CTRL1_INT_SET This bit is software interrupt trigger source of UHCI_APP_CTRL1_INT. (WT)

PRELIMINARY

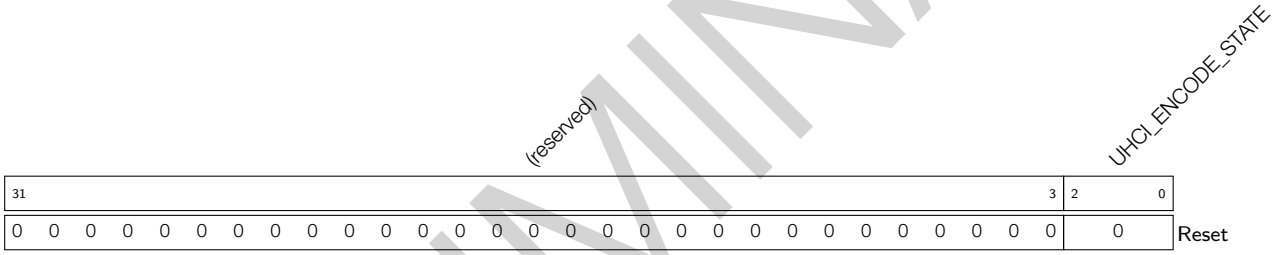
Register 24.64. UHCI_STATE0_REG (0x001C)



UHCI_RX_ERR_CAUSE This field indicates the error type when DMA has received a packet with error. 3'b001: Checksum error in the HCI packet. 3'b010: Sequence number error in the HCI packet. 3'b011: CRC bit error in the HCI packet. 3'b100: 0xC0 is found but the received HCI packet is not end. 3'b101: 0xC0 is not found when the HCI packet has been received. 3'b110: CRC check error. (RO)

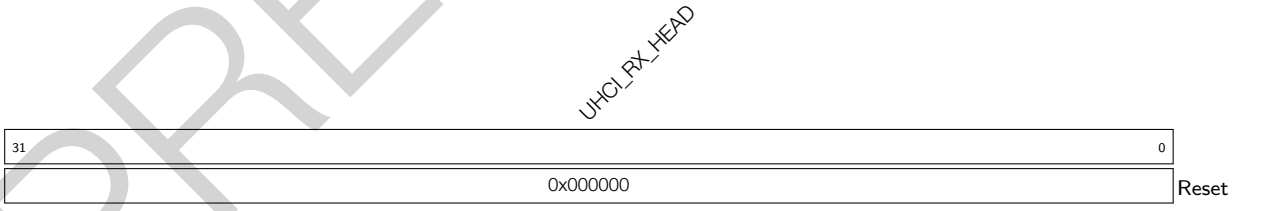
UHCI_DECODE_STATE UHCI decoder status. (RO)

Register 24.65. UHCI_STATE1_REG (0x0020)



UHCI_ENCODE_STATE UHCI encoder status. (RO)

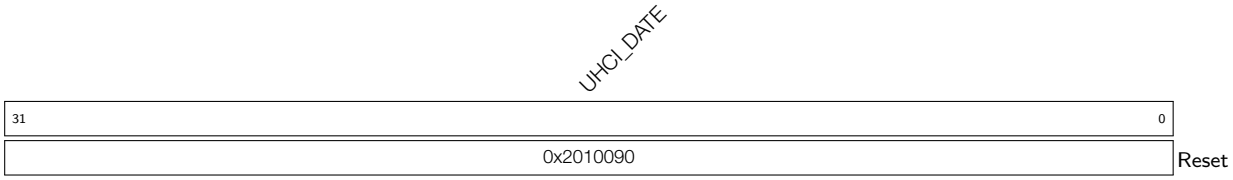
Register 24.66. UHCI_RX_HEAD_REG (0x0030)



UHCI_RX_HEAD This register stores the header of the current received packet. (RO)

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Register 24.67. UHCI_DATE_REG (0x0084)



UHCI_DATE This is the version control register. (R/W)

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25 I2C Controller (I2C)

The I2C (Inter-Integrated Circuit) bus allows ESP32-S3 to communicate with multiple external devices. These external devices can share one bus.

25.1 Overview

The I2C bus has two lines, namely a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL lines are open-drain. The I2C bus can be connected to a single or multiple master devices and a single or multiple slave devices. However, only one master device can access a slave at a time via the bus.

The master initiates communication by generating a START condition: pulling the SDA line low while SCL is high, and sending nine clock pulses via SCL. The first eight pulses are used to transmit a 7-bit address followed by a read/write ($R/\overline{W}$) bit. If the address of an I2C slave matches the 7-bit address transmitted, this matching slave can respond by pulling SDA low on the ninth clock pulse. The master and the slave can send or receive data according to the $R/\overline{W}$ bit. Whether to terminate the data transfer or not is determined by the logic level of the acknowledge (ACK) bit. During data transfer, SDA changes only when SCL is low. Once finishing communication, the master sends a STOP condition: pulling SDA up while SCL is high. If a master both reads and writes data in one transfer, then it should send a RSTART condition, a slave address and a $R/\overline{W}$ bit before changing its operation. The RSTART condition is used to change the transfer direction and the mode of the devices (master mode or slave mode).

25.2 Features

The I2C controller has the following features:

- Master mode and slave mode
- Communication between multiple masters and slaves
- Standard mode (100 Kbit/s)
- Fast mode (400 Kbit/s)
- 7-bit addressing and 10-bit addressing
- Continuous data transfer achieved by pulling SCL low
- Programmable digital noise filtering
- Double addressing mode, which uses slave address and slave memory or register address

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25.3 I2C Architecture

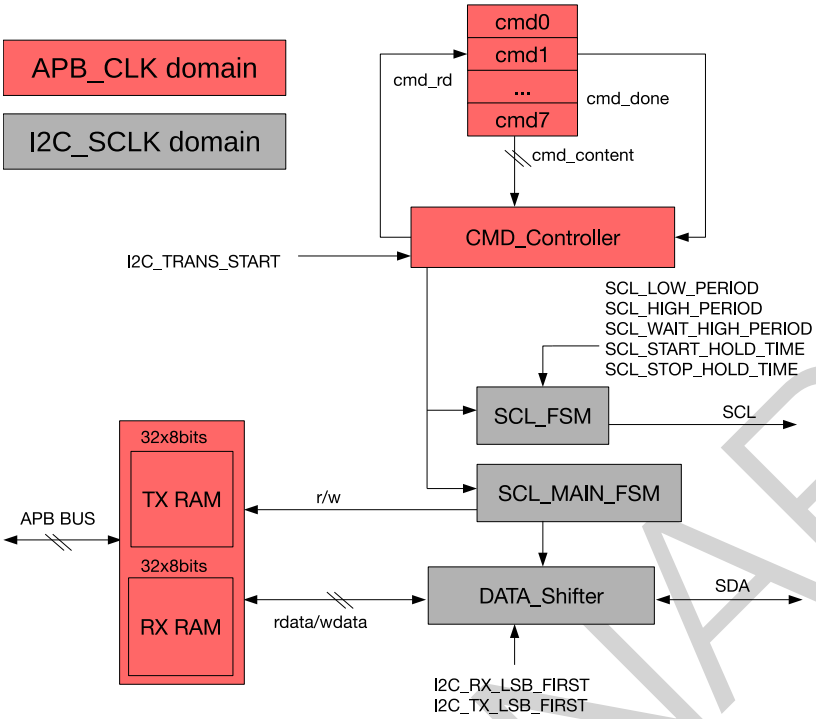


Figure 25-1. I2C Master Architecture

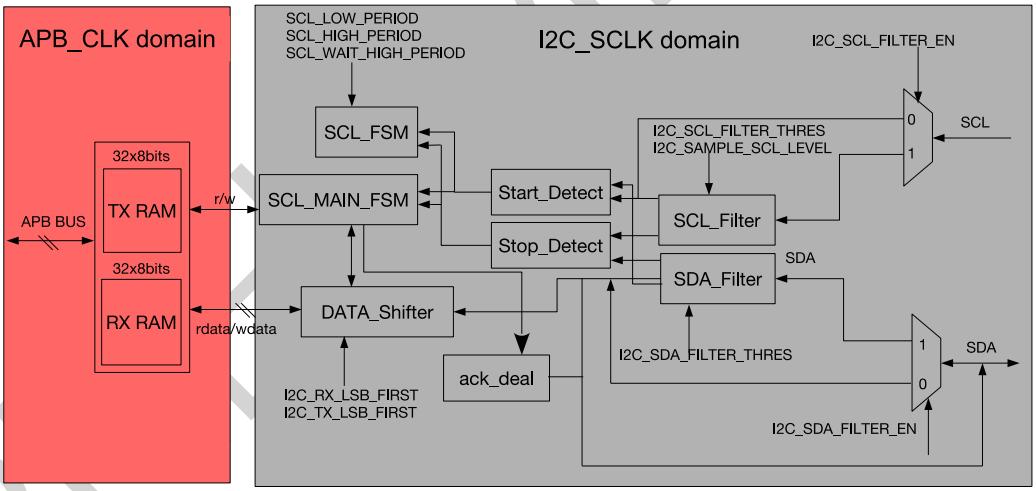


Figure 25-2. I2C Slave Architecture

The I2C controller runs either in master mode or slave mode, which is determined by I2C_MS_MODE. Figure 25-1 shows the architecture of a master, while Figure 25-2 shows that of a slave. The I2C controller has the following main parts:

- transmit and receive memory (TX/RX RAM)
- command controller (CMD_Controller)
- SCL clock controller (SCL_FSM)
- SDA data controller (SCL_MAIN_FSM)

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- serial/parallel data converter (DATA_Shifter)
- filter for SCL (SCL_Filter)
- filter for SDA (SDA_Filter)

Besides, the I2C controller also has a clock module which generates I2C clocks, and a synchronization module which synchronizes the APB bus and the I2C controller.

The clock module is used to select clock sources, turn on and off clocks, and divide clocks. SCL_Filter and SDA_Filter remove noises on SCL input signals and SDA input signals respectively. The synchronization module synchronizes signal transfer between different clock domains.

Figure 25-3 and Figure 25-4 are the timing diagram and corresponding parameters of the I2C protocol. SCL_FSM generates the timing sequence conforming to the I2C protocol.

SCL_MAIN_FSM controls the execution of I2C commands and the sequence of the SDA line. CMD_Controller is used for an I2C master to generate (R)START, STOP, WRITE, READ and END commands. TX RAM and RX RAM store data to be transmitted and data received respectively. DATA_Shifter shifts data between serial and parallel form.

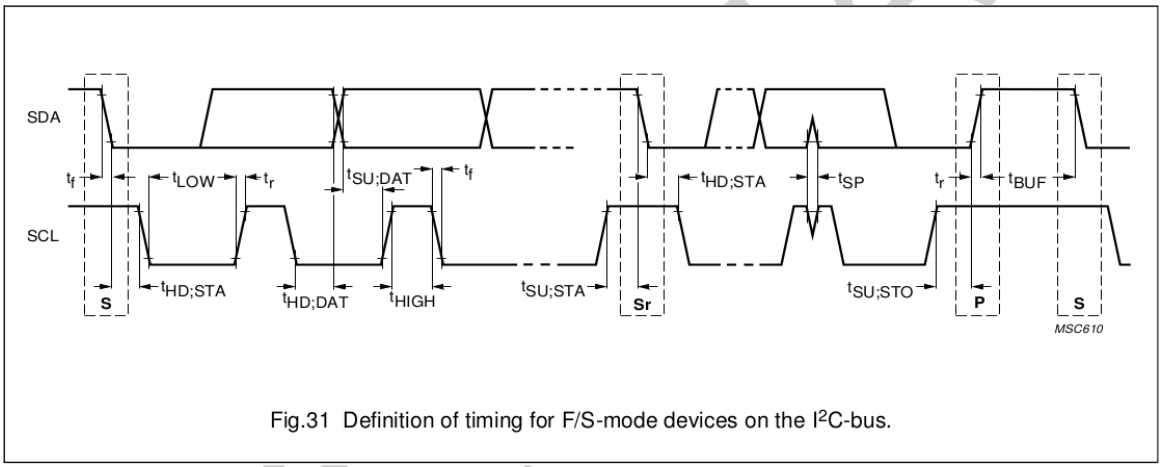


Fig.31 Definition of timing for F/S-mode devices on the I²C-bus.

Figure 25-3. I2C Protocol Timing (Cited from Fig.31 in The I2C-bus specification Version 2.1)

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PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	20 + 0.1C_b(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	20 + 0.1C_b(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs

Figure 25-4. I2C Timing Parameters (Cited from Table 5 in The I2C-bus specification Version 2.1)

25.4 Functional Description

Note that operations may differ between the I2C controller in ESP32-S3 and other masters or slaves on the bus. Please refer to datasheets of individual I2C devices for specific information.

25.4.1 Clock Configuration

Registers, TX RAM, and RX RAM are configured and accessed in the APB_CLK clock domain, whose frequency is 1 ∼ 80 MHz. The main logic of the I2C controller, including SCL_FSM, SCL_MAIN_FSM, SCL_FILTER, SDA_FILTER, and DATA_SHIFTER, are in the I2C_SCLK clock domain.

You can choose the clock source for I2C_SCLK from XTAL_CLK or FOSC_CLK via I2C_SCLK_SEL. When I2C_SCLK_SEL is cleared, the clock source is XTAL_CLK. When I2C_SCLK_SEL is set, the clock source is FOSC_CLK. The clock source is enabled by configuring I2C_SCLK_ACTIVE as high level, and then passes through a fractional divider to generate I2C_SCLK according to the following equation:

$$Divisor = I2C\_SCLK\_DIV\_NUM + 1 + \frac{I2C\_SCLK\_DIV\_A}{I2C\_SCLK\_DIV\_B}$$

The frequency of XTAL_CLK is 40 MHz, while the frequency of FOSC_CLK is 17.5 MHz. Limited by timing parameters, the derived clock I2C_SCLK should operate at a frequency 20 timers larger than SCL's frequency.

25.4.2 SCL and SDA Noise Filtering

SCL_Filter and SDA_Filter modules are identical and are used to filter signal noises on SCL and SDA, respectively. These filters can be enabled or disabled by configuring I2C_SCL_FILTER_EN and I2C_SDA_FILTER_EN.

Take SCL_Filter as an example. When enabled, SCL_Filter samples input signals on the SCL line continuously. These input signals are valid only if they remain unchanged for consecutive I2C_SCL_FILTER_THRES I2C_SCLK

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clock cycles. Given that only valid input signals can pass through the filter, SCL_Filter can remove glitches whose pulse width is shorter than I2C_SCL_FILTER_THRES I2C_SCLK clock cycles, while SDA_Filter can remove glitches whose pulse width is shorter than I2C_SDA_FILTER_THRES I2C_SCLK clock cycles.

25.4.3 SCL Clock Stretching

The I2C controller in slave mode (i.e. slave) can hold the SCL line low in exchange for more time to process data. This function called clock stretching is enabled by setting the I2C_SLAVE_SCL_STRETCH_EN bit. The time period to release the SCL line from stretching is configured by setting the I2C_STRETCH_PROTECT_NUM field, in order to avoid timing sequence errors. The slave will hold the SCL line low when one of the following four events occurs:

1. Address match: The address of the slave matches the address sent by the master via the SDA line, and the $R/\overline{W}$ bit is 1.
2. RAM being full: RX RAM of the slave is full. Note that when the slave receives less than 32 bytes, it is not necessary to enable clock stretching; when the slave receives 32 bytes or more, you may interrupt data transmission to wrapped around RAM via the FIFO threshold, or enable clock stretching for more time to process data. When clock stretching is nabled, I2C_RX_FULL_ACK_LEVEL must be cleared, otherwise there will be unpredictable consequences.
3. RAM being empty: The slave is sending data, but its TX RAM is empty.
4. Sending an ACK: If I2C_SLAVE_BYTE_ACK_CTL_EN is set, the slave pulls SCL low when sending an ACK bit. At this stage, software validates data and configures I2C_SLAVE_BYTE_ACK_LVL to control the level of the ACK bit. Note that when RX RAM of the slave is full, the level of the ACK bit to be sent is determined by I2C_RX_FULL_ACK_LEVEL, instead of I2C_SLAVE_BYTE_ACK_LVL. In this case, I2C_RX_FULL_ACK_LEVEL should also be cleared to ensure proper functioning of clock stretching.

After SCL has been stretched low, the cause of stretching can be read from the I2C_STRETCH_CAUSE bit. Clock stretching is disabled by setting the I2C_SLAVE_SCL_STRETCH_CLR bit.

25.4.4 Generating SCL Pulses in Idle State

Usually when the I2C bus is idle, the SCL line is held high. The I2C controller in ESP32-S3 can be programmed to generate SCL pulses in idle state. This function only works when the I2C controller is configured as master. If the I2C_SCL_RST_SLV_EN bit is set, hardware will send I2C_SCL_RST_SLV_NUM SCL pulses, and then automatically clear this bit. When software reads 0 in I2C_SCL_RST_SLV_EN, set I2C_CONF_UPGATE to stop this function.

25.4.5 Synchronization

I2C registers are configured in APB_CLK domain, whereas the I2C controller is configured in asynchronous I2C_SCLK domain. Therefore, before being used by the I2C controller, register values should be synchronized by first writing configuration registers and then writing 1 to I2C_CONF_UPGATE. Registers that need synchronization are listed in Table 25-1.

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Table 25-1. I2C Synchronous Registers

Register	Parameter	Address
I2C_CTR_REG	I2C_SLV_TX_AUTO_START_EN	0x0004
	I2C_ADDR_10BIT_RW_CHECK_EN	
	I2C_ADDR_BROADCASTING_EN	
	I2C_SDA_FORCE_OUT	
	I2C_SCL_FORCE_OUT	
	I2C_SAMPLE_SCL_LEVEL	
	I2C_RX_FULL_ACK_LEVEL	
	I2C_MS_MODE	
	I2C_TX_LSB_FIRST	
	I2C_RX_LSB_FIRST	
	I2C_ARBITRATION_EN	
I2C_TO_REG	I2C_TIME_OUT_EN	0x000C
	I2C_TIME_OUT_VALUE	
I2C_SLAVE_ADDR_REG	I2C_ADDR_10BIT_EN	0x0010
	I2C_SLAVE_ADDR	
I2C_FIFO_CONF_REG	I2C_FIFO_ADDR_CFG_EN	0x0018
I2C_SCL_SP_CONF_REG	I2C_SDA_PD_EN	0x0080
	I2C_SCL_PD_EN	
	I2C_SCL_RST_SLV_NUM	
	I2C_SCL_RST_SLV_EN	
I2C_SCL_STRETCH_CONF_REG	I2C_SLAVE_BYTE_ACK_CTL_EN	0x0084
	I2C_SLAVE_BYTE_ACK_LVL	
	I2C_SLAVE_SCL_STRETCH_EN	
	I2C_STRETCH_PROTECT_NUM	
I2C_SCL_LOW_PERIOD_REG	I2C_SCL_LOW_PERIOD	0x0000
I2C_SCL_HIGH_PERIOD_REG	I2C_WAIT_HIGH_PERIOD	0x0038
	I2C_HIGH_PERIOD	
I2C_SDA_HOLD_REG	I2C_SDA_HOLD_TIME	0x0030
I2C_SDA_SAMPLE_REG	I2C_SDA_SAMPLE_TIME	0x0034
I2C_SCL_START_HOLD_REG	I2C_SCL_START_HOLD_TIME	0x0040
I2C_SCL_RSTART_SETUP_REG	I2C_SCL_RSTART_SETUP_TIME	0x0044
I2C_SCL_STOP_HOLD_REG	I2C_SCL_STOP_HOLD_TIME	0x0048
I2C_SCL_STOP_SETUP_REG	I2C_SCL_STOP_SETUP_TIME	0x004C
I2C_SCL_ST_TIME_OUT_REG	I2C_SCL_ST_TO_I2C	0x0078
I2C_SCL_MAIN_ST_TIME_OUT_REG	I2C_SCL_MAIN_ST_TO_I2C	0x007C
I2C_FILTER_CFG_REG	I2C_SCL_FILTER_EN	0x0050
	I2C_SCL_FILTER_THRES	
	I2C_SDA_FILTER_EN	
	I2C_SDA_FILTER_THRES	

25.4.6 Open-Drain Output

SCL and SDA output drivers must be configured as open drain. There are two ways to achieve this:

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1. Set I2C_SCL_FORCE_OUT and I2C_SDA_FORCE_OUT, and configure GPIO_PIN*n*_PAD_DRIVER for corresponding SCL and SDA pads as open-drain.
2. Clear I2C_SCL_FORCE_OUT and I2C_SDA_FORCE_OUT.

Because these lines are configured as open-drain, the low-to-high transition time of each line is longer, determined together by the pull-up resistor and line capacitance. The output duty cycle of I2C is limited by the SDA and SCL line's pull-up speed, mainly SCL's speed.

In addition, when I2C_SCL_FORCE_OUT and I2C_SCL_PD_EN are set to 1, SCL can be forced low; when I2C_SDA_FORCE_OUT and I2C_SDA_PD_EN are set to 1, SDA can be forced low.

25.4.7 Timing Parameter Configuration

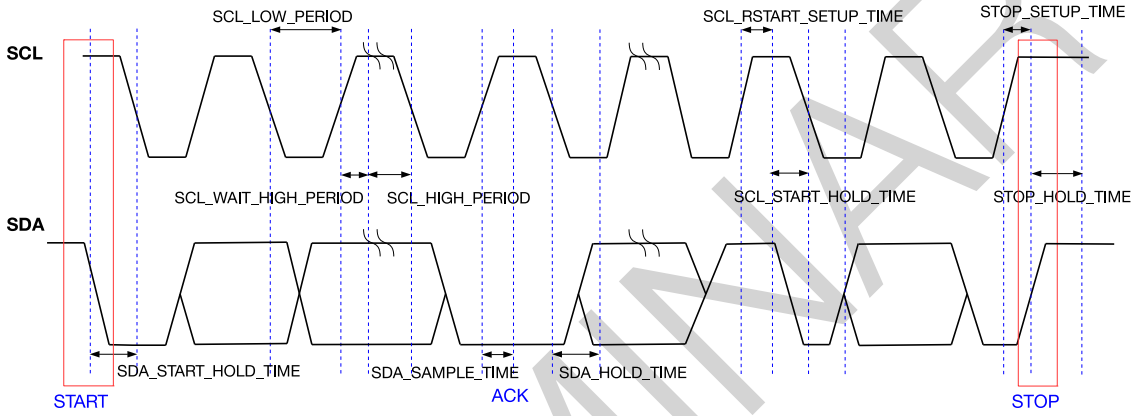


Figure 25-5. I2C Timing Diagram

Figure 25-5 shows the timing diagram of an I2C master. This figure also specifies registers used to configure the START bit, STOP bit, data hold time, data sample time, waiting time on the rising SCL edge, etc. Timing parameters are calculated as follows in I2C_SCLK clock cycles:

1. $t_{LOW} = (I2C\_SCL\_LOW\_PERIOD + 1) \cdot T_{I2C\_SCLK}$
2. $t_{HIGH} = (I2C\_SCL\_HIGH\_PERIOD + 1) \cdot T_{I2C\_SCLK}$
3. $t_{SU:STA} = (I2C\_SCL\_RSTART\_SETUP\_TIME + 1) \cdot T_{I2C\_SCLK}$
4. $t_{HD:STA} = (I2C\_SCL\_START\_HOLD\_TIME + 1) \cdot T_{I2C\_SCLK}$
5. $t_{r} = (I2C\_SCL\_WAIT\_HIGH\_PERIOD + 1) \cdot T_{I2C\_SCLK}$
6. $t_{SU:STO} = (I2C\_SCL\_STOP\_SETUP\_TIME + 1) \cdot T_{I2C\_SCLK}$
7. $t_{BUF} = (I2C\_SCL\_STOP\_HOLD\_TIME + 1) \cdot T_{I2C\_SCLK}$
8. $t_{HD:DAT} = (I2C\_SDA\_HOLD\_TIME + 1) \cdot T_{I2C\_SCLK}$
9. $t_{SU:DAT} = (I2C\_SCL\_LOW\_PERIOD - I2C\_SDA\_HOLD\_TIME) \cdot T_{I2C\_SCLK}$

Timing registers below are divided into two groups, depending on the mode in which these registers are active:

- Master mode only:

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1. I2C_SCL_START_HOLD_TIME: Specifies the interval between pulling SDA low and pulling SCL low when the master generates a START condition. This interval is (I2C_SCL_START_HOLD_TIME +1) in I2C_SCLK cycles. This register is active only when the I2C controller works in master mode.
2. I2C_SCL_LOW_PERIOD: Specifies the low period of SCL. This period lasts (I2C_SCL_LOW_PERIOD +1) in I2C_SCLK cycles. However, it could be extended when SCL is pulled low by peripheral devices or by an END command executed by the I2C controller, or when the clock is stretched. This register is active only when the I2C controller works in master mode.
3. I2C_SCL_WAIT_HIGH_PERIOD: Specifies time for SCL to go high in I2C_SCLK cycles. Please make sure that SCL could be pulled high within this time period. Otherwise, the high period of SCL may be incorrect. This register is active only when the I2C controller works in master mode.
4. I2C_SCL_HIGH_PERIOD: Specifies the high period of SCL in I2C_SCLK cycles. This register is active only when the I2C controller works in master mode. When SCL goes high within (I2C_SCL_WAIT_HIGH_PERIOD + 1) in I2C_SCLK cycles, its frequency is:

$$f_{scl} = \frac{f_{\text{I2C\_SCLK}}}{\text{I2C\_SCL\_LOW\_PERIOD} + \text{I2C\_SCL\_HIGH\_PERIOD} + \text{I2C\_SCL\_WAIT\_HIGH\_PERIOD} + 3}$$

- Master mode and slave mode:
  1. I2C_SDA_SAMPLE_TIME: Specifies the interval between the rising edge of SCL and the level sampling time of SDA. It is advised to set a value in the middle of SCL's high period, so as to correctly sample the level of SCL. This register is active both in master mode and slave mode.
  2. I2C_SDA_HOLD_TIME: Specifies the interval between changing the SDA output level and the falling edge of SCL. This register is active both in master mode and slave mode.

Timing parameters limits corresponding register configuration.

1. $\frac{f_{I2C\_SCLK}}{f_{SCL}} > 20$
2. $3 \times f_{I2C\_SCLK} \leq (I2C\_SDA\_HOLD\_TIME - 4) \times f_{APB\_CLK}$
3. I2C_SDA_HOLD_TIME + I2C_SCL_START_HOLD_TIME > SDA_FILTER_THRES + 3
4. I2C_SCL_WAIT_HIGH_PERIOD < I2C_SDA_SAMPLE_TIME < I2C_SCL_HIGH_PERIOD
5. I2C_SDA_SAMPLE_TIME < I2C_SCL_WAIT_HIGH_PERIOD + I2C_SCL_START_HOLD_TIME + I2C_SCL_RSTART_SETUP_TIME
6. I2C_STRETCH_PROTECT_NUM + I2C_SDA_HOLD_TIME > I2C_SCL_LOW_PERIOD

25.4.8 Timeout Control

The I2C controller has three types of timeout control, namely timeout control for SCL_FSM, for SCL_MAIN_FSM, and for the SCL line. The first two are always enabled, while the third is configurable.

When SCL_FSM remains unchanged for more than $2^{I2C\_SCL\_ST\_TO\_I2C}$ clock cycles, an I2C_SCL_ST_TO_INT interrupt is triggered, and then SCL_FSM goes to idle state. The value of I2C_SCL_ST_TO_I2C should be less than or equal to 22, which means SCL_FSM could remain unchanged for 2^{22} I2C_SCLK clock cycles at most before the interrupt is generated.

When SCL_MAIN_FSM remains unchanged for more than $2^{I2C\_SCL\_MAIN\_ST\_TO\_I2C}$ I2C_SCLK clock cycles, an

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I2C_SCL_MAIN_ST_TO_INT interrupt is triggered, and then SCL_MAIN_FSM goes to idle state. The value of I2C_SCL_MAIN_ST_TO_I2C should be less than or equal to 22, which means SCL_MAIN_FSM could remain unchanged for 2^{22} clock cycles at most before the interrupt is generated.

Timeout control for SCL is enabled by setting I2C_TIME_OUT_EN. When the level of SCL remains unchanged for more than I2C_TIME_OUT_VALUE clock cycles, an I2C_TIME_OUT_INT interrupt is triggered, and then the I2C bus goes to idle state.

25.4.9 Command Configuration

When the I2C controller works in master mode, CMD_Controller reads commands from 8 sequential command registers and controls SCL_FSM and SCL_MAIN_FSM accordingly.

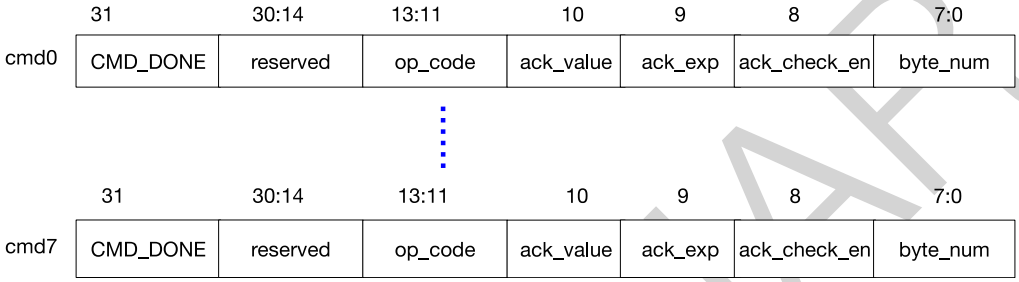


Figure 25-6. Structure of I2C Command Registers

Command registers, whose structure is illustrated in Figure 25-6, are active only when the I2C controller works in master mode. Fields of command registers are:

1. CMD_DONE: Indicates that a command has been executed. After each command has been executed, the CMD_DONE bit in the corresponding command register is set to 1 by hardware. By reading this bit, software can tell if the command has been executed. When writing new commands, this bit must be cleared by software.
2. op_code: Indicates the command. The I2C controller supports five commands:
   - RSTART: op_code = 6. The I2C controller sends a START bit or a RSTART bit defined by the I2C protocol.
   - WRITE: op_code = 1. The I2C controller sends a slave address, a register address (only in double addressing mode) and data to the slave.
   - READ: op_code = 3. The I2C controller reads data from the slave.
   - STOP: op_code = 2. The I2C controller sends a STOP bit defined by the I2C protocol. This code also indicates that the command sequence has been executed, and the CMD_Controller stops reading commands. After restarted by software, the CMD_Controller resumes reading commands from command register 0.
   - END: op_code = 4. The I2C controller pulls the SCL line down and suspends I2C communication. This code also indicates that the command sequence has completed, and the CMD_Controller stops executing commands. Once software refreshes data in command registers and the RAM, the CMD_Controller can be restarted to execute commands from command register 0 again.
3. ack_value: Used to configure the level of the ACK bit sent by the I2C controller during a read operation. This bit is ignored in RSTART, STOP, END and WRITE conditions.

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4. ack_exp: Used to configure the level of the ACK bit expected by the I2C controller during a write operation. This bit is ignored during RSTART, STOP, END and READ conditions.
5. ack_check_en: Used to enable the I2C controller during a write operation to check whether the ACK level sent by the slave matches ack_exp in the command. If this bit is set and the level received does not match ack_exp in the WRITE command, the master will generate an I2C_NACK_INT interrupt and a STOP condition for data transfer. If this bit is cleared, the controller will not check the ACK level sent by the slave. This bit is ignored during RSTART, STOP, END and READ conditions.
6. byte_num: Specifies the length of data (in bytes) to be read or written. Can range from 1 to 255 bytes. This bit is ignored during RSTART, STOP and END conditions.

Each command sequence is executed starting from command register 0 and terminated by a STOP or an END. Therefore, there must be a STOP or an END command in the eight command registers.

A complete data transfer on the I2C bus should be initiated by a START and terminated by a STOP. The transfer process may be completed using multiple sequences, separated by END commands. Each sequence may differ in the direction of data transfer, clock frequency, slave addresses, data length, etc. This allows efficient use of available peripheral RAM and also achieves more flexible I2C communication.

25.4.10 TX/RX RAM Data Storage

Both TX RAM and RX RAM are 32 × 8 bits, and can be accessed in FIFO or non-FIFO mode. If I2C_NONFIFO_EN bit is cleared, both RAMs are accessed in FIFO mode; if I2C_NONFIFO_EN bit is set, both RAMs are accessed in non-FIFO mode.

TX RAM stores data that the I2C controller needs to send. During communication, when the I2C controller needs to send data (except acknowledgement bits), it reads data from TX RAM and sends them sequentially via SDA. When the I2C controller works in master mode, all data must be stored in TX RAM in the order they will be sent to slaves. The data stored in TX RAM include slave addresses, read/write bits, register addresses (only in double addressing mode) and data to be sent. When the I2C controller works in slave mode, TX RAM only stores data to be sent.

TX RAM can be read and written by the CPU. The CPU writes to TX RAM either in FIFO mode or in non-FIFO mode (direct address). In FIFO mode, the CPU writes to TX RAM via the fixed address I2C_DATA_REG, with addresses for writing in TX RAM incremented automatically by hardware. In non-FIFO mode, the CPU accesses TX RAM directly via address fields (I2C Base Address + 0x100) ~(I2C Base Address + 0x17C). Each byte in TX RAM occupies an entire word in the address space. Therefore, the address of the first byte is I2C Base Address + 0x100, the second byte is I2C Base Address + 0x104, the third byte is I2C Base Address + 0x108, and so on. The CPU can only read TX RAM via direct addresses. Addresses for reading TX RAM are the same with addresses for writing TX RAM.

RX RAM stores data the I2C controller receives during communication. When the I2C controller works in slave mode, neither slave addresses sent by the master nor register addresses (only in double addressing mode) will be stored into RX RAM. Values of RX RAM can be read by software after I2C communication completes.

RX RAM can only be read by the CPU. The CPU reads RX RAM either in FIFO mode or in non-FIFO mode (direct address). In FIFO mode, the CPU reads RX RAM via the fixed address I2C_DATA_REG, with addresses for reading RX RAM incremented automatically by hardware. In non-FIFO mode, the CPU accesses TX RAM directly via address fields (I2C Base Address + 0x180) ~(I2C Base Address + 0x1FC). Each byte in RX RAM occupies an entire word in the address space. Therefore, the address of the first byte is I2C Base Address + 0x180, the

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second byte is I2C Base Address + 0x184, the third byte is I2C Base Address + 0x188 and so on.

In FIFO mode, TX RAM of a master may wrap around to send data larger than 32 bytes. Set I2C_FIFO_PRT_EN. If the size of data to be sent is smaller than I2C_TXFIFO_WM_THRHD (master), an I2C_TXFIFO_WM_INT (master) interrupt is generated. After receiving the interrupt, software continues writing to I2C_DATA_REG (master). Please ensure that software writes to or refreshes TX RAM before the master sends data, otherwise it may result in unpredictable consequences.

In FIFO mode, RX RAM of a slave may also wrap around to receive data larger than 32 bytes. Set I2C_FIFO_PRT_EN and clear I2C_RX_FULL_ACK_LEVEL. If data already received (to be overwritten) is larger than I2C_RXFIFO_WM_THRHD (slave), an I2C_RXFIFO_WM_INT (slave) interrupt is generated. After receiving the interrupt, software continues reading from I2C_DATA_REG (slave).

25.4.11 Data Conversion

DATA_Shifter is used for serial/parallel conversion, converting byte data in TX RAM to an outgoing serial bitstream or an incoming serial bitstream to byte data in RX RAM. I2C_RX_LSB_FIRST and I2C_TX_LSB_FIRST can be used to select LSB- or MSB-first storage and transmission of data.

25.4.12 Addressing Mode

Besides 7-bit addressing, the ESP32-S3 I2C controller also supports 10-bit addressing and double addressing. 10-bit addressing can be mixed with 7-bit addressing.

Define the slave address as SLV_ADDR. In 7-bit addressing mode, the slave address is SLV_ADDR[6:0]; in 10-bit addressing mode, the slave address is SLV_ADDR[9:0].

In 7-bit addressing mode, the master only needs to send one byte of address, which comprises SLV_ADDR[6:0] and a $R/\overline{W}$ bit. In 7-bit addressing mode, there is a special case called general call addressing (broadcast). It is enabled by setting I2C_ADDR_BROADCASTING_EN in a slave. When the slave receives the general call address (0x00) from the master and the $R/\overline{W}$ bit followed is 0, it responds to the master regardless of its own address.

In 10-bit addressing mode, the master needs to send two bytes of address. The first byte is slave_addr_first_7bits followed by a $R/\overline{W}$ bit, and slave_addr_first_7bits should be configured as (0x78 | SLV_ADDR[9:8]). The second byte is slave_addr_second_byte, which should be configured as SLV_ADDR[7:0]. The slave can enable 10-bit addressing by configuring I2C_ADDR_10BIT_EN. I2C_SLAVE_ADDR is used to configure I2C slave address. Specifically, I2C_SLAVE_ADDR[14:7] should be configured as SLV_ADDR[7:0], and I2C_SLAVE_ADDR[6:0] should be configured as (0x78 | SLV_ADDR[9:8]). Since a 10-bit slave address has one more byte than a 7-bit address, byte_num of the WRITE command and the number of bytes in the RAM increase by one.

When working in slave mode, the I2C controller supports double addressing, where the first address is the address of an I2C slave, and the second one is the slave's memory address. When using double addressing, RAM must be accessed in non-FIFO mode. Double addressing is enabled by setting I2C_FIFO_ADDR_CFG_EN.

25.4.13 $R/\overline{W}$ Bit Check in 10-bit Addressing Mode

In 10-bit addressing mode, when I2C_ADDR_10BIT_RW_CHECK_EN is set to 1, the I2C controller performs a check on the first byte, which consists of slave_addr_first_7bits and a $R/\overline{W}$ bit. When the $R/\overline{W}$ bit does not

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indicate a WRITE operation, i.e. not in line with the I2C protocol, the data transfer ends. If the check feature is not enabled, when the $R/\overline{W}$ bit does not indicate a WRITE, the data transfer still continues, but transfer failure may occur.

25.4.14 To Start the I2C Controller

To start the I2C controller in master mode, after configuring the controller to master mode and command registers, write 1 to I2C_TRANS_START in order that the master starts to parse and execute command sequences. The master always executes a command sequence starting from command register 0 to a STOP or an END at the end. To execute another command sequence starting from command register 0, refresh commands by writing 1 again to I2C_TRANS_START.

To start the I2C controller in slave mode, there are two ways:

- Set I2C_SLV_TX_AUTO_START_EN, and the slave starts automatic transfer upon an address match;
- Clear I2C_SLV_TX_AUTO_START_EN, and always set I2C_TRANS_START before transfer.

25.5 Programming Example

This sections provides programming examples for typical communication scenarios. ESP32-S3 has one I2C controller. For the convenience of description, I2C masters and slaves in all subsequent figures are ESP32-S3 I2C controllers. I2C master is referred to as $I2C_{master}$, and I2C slave is referred to as $I2C_{slave}$.

25.5.1 $I2C_{master}$ Writes to $I2C_{slave}$ with a 7-bit Address in One Command Sequence

25.5.1.1 Introduction

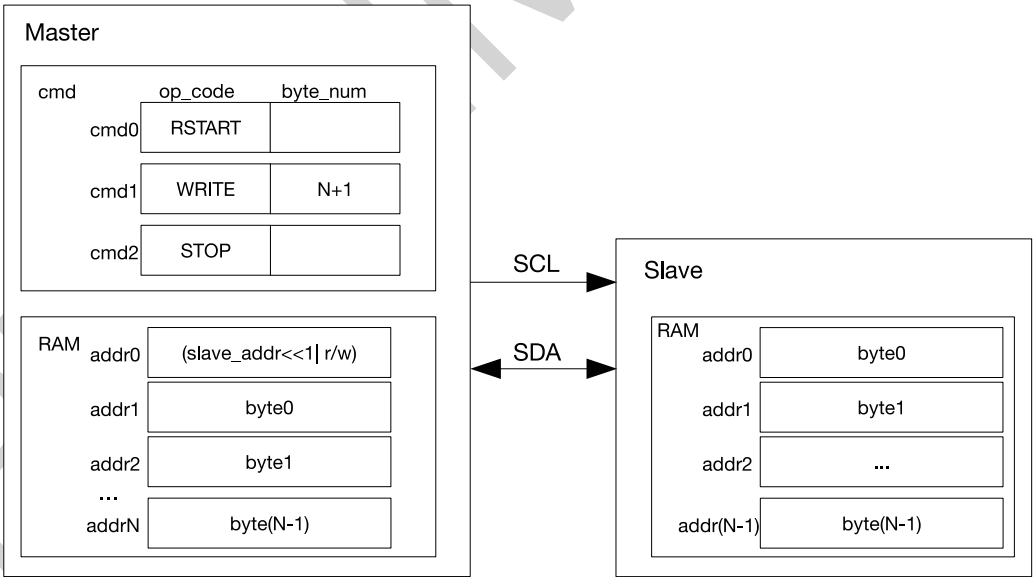


Figure 25-7. $I2C_{master}$ Writing to $I2C_{slave}$ with a 7-bit Address

Figure 25-7 shows how $I2C_{master}$ writes N bytes of data to $I2C_{slave}$ registers or RAM using 7-bit addressing. As shown in figure 25-7 , the first byte in the RAM of $I2C_{master}$ is a 7-bit $I2C_{slave}$ address followed by a $R/\overline{W}$ bit. When the $R/\overline{W}$ bit is 0, it indicates a WRITE operation. The remaining bytes are used to store data ready for transfer. The cmd box contains related command sequences.

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After the command sequence is configured and data in RAM is ready, $I2C_{master}$ enables the controller and initiates data transfer by setting the I2C_TRANS_START bit. The controller has four steps to take:

1. Wait for SCL to go high, to avoid SCL being used by other masters or slaves.
2. Execute a RSTART command and send a START bit.
3. Execute a WRITE command by taking N+1 bytes from the RAM in order and send them to $I2C_{slave}$ in the same order. The first byte is the address of $I2C_{slave}$.
4. Send a STOP. Once the $I2C_{master}$ transfers a STOP bit, an I2C_TRANS_COMPLETE_INT interrupt is generated.

25.5.1.2 Configuration Example

1. Configure the timing parameter registers of $I2C_{master}$ and $I2C_{slave}$ according to Section 25.4.7.
2. Set I2C_MS_MODE (master) to 1, and I2C_MS_MODE (slave) to 0.
3. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
4. Configure command registers of $I2C_{master}$.

Command register	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND0 (master)	RSTART	—	—	—	—
I2C_COMMAND1 (master)	WRITE	ack_value	ack_exp	1	N+1
I2C_COMMAND2 (master)	STOP	—	—	—	—

5. Write the address of $I2C_{slave}$ and data to be sent to TX RAM of $I2C_{master}$ in either FIFO mode or non-FIFO mode according to Section 25.4.10.
6. Write the address of $I2C_{slave}$ to I2C_SLAVE_ADDR (slave) in I2C_SLAVE_ADDR_REG (slave) register.
7. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
8. Write 1 to I2C_TRANS_START (master) and I2C_TRANS_START (slave) to start transfer.
9. $I2C_{slave}$ compares the slave address sent by $I2C_{master}$ with its own address in I2C_SLAVE_ADDR (slave). When ack_check_en (master) in $I2C_{master}$'s WRITE command is 1, $I2C_{master}$ checks ACK value each time it sends a byte. When ack_check_en (master) is 0, $I2C_{master}$ does not check ACK value and take $I2C_{slave}$ as a matching slave by default.
   - Match: If the received ACK value matches ack_exp (master) (the expected ACK value), $I2C_{master}$ continues data transfer.
   - Not match: If the received ACK value does not match ack_exp, $I2C_{master}$ generates an I2C_NACK_INT (master) interrupt and stops data transfer.
10. $I2C_{master}$ sends data, and checks ACK value or not according to ack_check_en (master).
11. If data to be sent (N) is larger than 32 bytes, TX RAM of $I2C_{master}$ may wrap around in FIFO mode. For details, please refer to Section 25.4.10.
12. If data to be received (N) is larger than 32 bytes, RX RAM of $I2C_{slave}$ may wrap around in FIFO mode. For details, please refer to Section 25.4.10.

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If data to be received (N) is larger than 32 bytes, the other way is to enable clock stretching by setting the I2C_SLAVE_SCL_STRETCH_EN (slave), and clearing I2C_RX_FULL_ACK_LEVEL. When RX RAM is full, an I2C_SLAVE_STRETCH_INT (slave) interrupt is generated. In this way, $I2C_{slave}$ can hold SCL low, in exchange for more time to read data. After software has finished reading, you can set I2C_SLAVE_STRETCH_INT_CLR (slave) to 1 to clear interrupt, and set I2C_SLAVE_SCL_STRETCH_CLR (slave) to release the SCL line.

13. After data transfer completes, $I2C_{master}$ executes the STOP command, and generates an I2C_TRANS_COMPLETE_INT (master) interrupt.

25.5.2 $I2C_{master}$ Writes to $I2C_{slave}$ with a 10-bit Address in One Command Sequence

25.5.2.1 Introduction

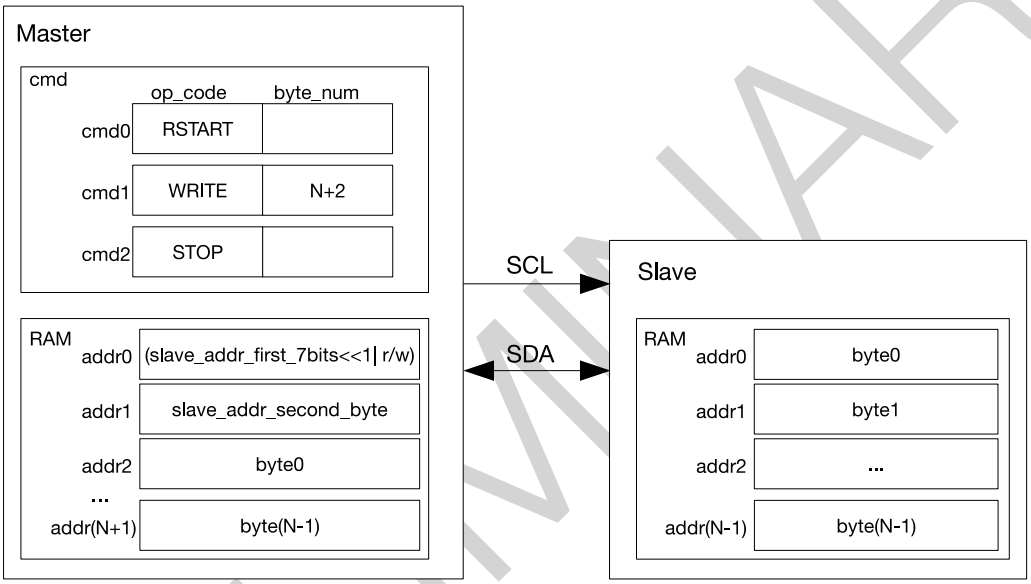


Figure 25-8. $I2C_{master}$ Writing to a Slave with a 10-bit Address

Figure 25-8 shows how $I2C_{master}$ writes N bytes of data using 10-bit addressing to an I2C slave. The configuration and transfer process is similar to what is described in 25.5.1, except that a 10-bit $I2C_{slave}$ address is formed from two bytes. Since a 10-bit $I2C_{slave}$ address has one more byte than a 7-bit $I2C_{slave}$ address, byte_num and length of data in TX RAM increase by 1 accordingly.

25.5.2.2 Configuration Example

1. Set I2C_MS_MODE (master) to 1, and I2C_MS_MODE (slave) to 0.
2. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
3. Configure command registers of $I2C_{master}$.

Command registers	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND0 (master)	RSTART	—	—	—	—
I2C_COMMAND1 (master)	WRITE	ack_value	ack_exp	1	N+2
I2C_COMMAND2 (master)	STOP	—	—	—	—

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4. Configure I2C_SLAVE_ADDR (slave) in I2C_SLAVE_ADDR_REG (slave) as $I2C_{slave}$'s 10-bit address, and set I2C_ADDR_10BIT_EN (slave) to 1 to enable 10-bit addressing.
5. Write the address of $I2C_{slave}$ and data to be sent to TX RAM of $I2C_{master}$. The first byte of the address of $I2C_{slave}$ comprises ((0x78 | I2C_SLAVE_ADDR[9:8])«1) and a $R/\overline{W}$ bit. The second byte of the address of $I2C_{slave}$ is I2C_SLAVE_ADDR[7:0]. These two bytes are followed by data to be sent in FIFO or non-FIFO mode.
6. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
7. Write 1 to I2C_TRANS_START (master) and I2C_TRANS_START (slave) to start transfer.
8. $I2C_{slave}$ compares the slave address sent by $I2C_{master}$ with its own address in I2C_SLAVE_ADDR (slave). When ack_check_en (master) in $I2C_{master}$'s WRITE command is 1, $I2C_{master}$ checks ACK value each time it sends a byte. When ack_check_en (master) is 0, $I2C_{master}$ does not check ACK value and take $I2C_{slave}$ as matching slave by default.
   - Match: If the received ACK value matches ack_exp (master) (the expected ACK value), $I2C_{master}$ continues data transfer.
   - Not match: If the received ACK value does not match ack_exp, $I2C_{master}$ generates an I2C_NACK_INT (master) interrupt and stops data transfer.
9. $I2C_{master}$ sends data, and checks ACK value or not according to ack_check_en (master).
10. If data to be sent is larger than 32 bytes, TX RAM of $I2C_{master}$ may wrap around in FIFO mode. For details, please refer to Section 25.4.10.
11. If data to be received is larger than 32 bytes, RX RAM of $I2C_{slave}$ may wrap around in FIFO mode. For details, please refer to Section 25.4.10.

    If data to be received is larger than 32 bytes, the other way is to enable clock stretching by setting I2C_SLAVE_SCL_STRETCH_EN (slave), and clearing I2C_RX_FULL_ACK_LEVEL to 0. When RX RAM is full, an I2C_SLAVE_STRETCH_INT (slave) interrupt is generated. In this way, $I2C_{slave}$ can hold SCL low, in exchange for more time to read data. After software has finished reading, you can set I2C_SLAVE_STRETCH_INT_CLR (slave) to 1 to clear interrupt, and set I2C_SLAVE_SCL_STRETCH_CLR (slave) to release the SCL line.
12. After data transfer completes, $I2C_{master}$ executes the STOP command, and generates an I2C_TRANS_COMPLETE_INT (master) interrupt.

25.5.3 $I2C_{master}$ Writes to $I2C_{slave}$ with Two 7-bit Addresses in One Command Sequence

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25.5.3.1 Introduction

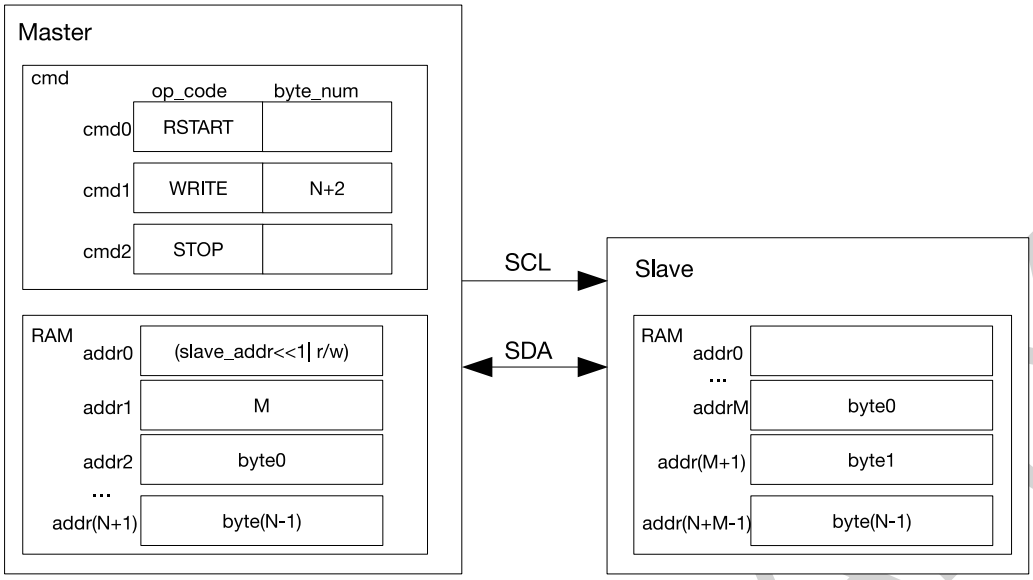


Figure 25-9. $I2C_{master}$ Writing to $I2C_{slave}$ with Two 7-bit Addresses

Figure 25-9 shows how $I2C_{master}$ writes N bytes of data to $I2C_{slave}$ registers or RAM using 7-bit double addressing. The configuration and transfer process is similar to what is described in Section 25.5.1, except that in 7-bit double addressing mode $I2C_{master}$ sends two 7-bit addresses. The first address is the address of an I2C slave, and the second one is $I2C_{slave}$'s memory address (i.e. addrM in Figure 25-9). When using double addressing, RAM must be accessed in non-FIFO mode. The I2C slave put received byte0 ~ byte(N-1) into its RAM in an order staring from addrM. The RAM is overwritten every 32 bytes.

25.5.3.2 Configuration Example

1. Set I2C_MS_MODE (master) to 1, and I2C_MS_MODE (slave) to 0.
2. Set I2C_FIFO_ADDR_CFG_EN (slave) to 1 to enable double addressing mode.
3. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
4. Configure command registers of $I2C_{master}$.

Command registers	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND0 (master)	RSTART	—	—	—	—
I2C_COMMAND1 (master)	WRITE	ack_value	ack_exp	1	N+2
I2C_COMMAND2 (master)	STOP	—	—	—	—

5. Write the address of $I2C_{slave}$ and data to be sent to TX RAM of $I2C_{master}$ in FIFO or non-FIFO mode.
6. Write the address of $I2C_{slave}$ to I2C_SLAVE_ADDR (slave) in I2C_SLAVE_ADDR_REG (slave) register.
7. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
8. Write 1 to I2C_TRANS_START (master) and I2C_TRANS_START (slave) to start transfer.
9. $I2C_{slave}$ compares the slave address sent by $I2C_{master}$ with its own address in I2C_SLAVE_ADDR (slave).

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When ack_check_en (master) in $I2C_{master}$'s WRITE command is 1, $I2C_{master}$ checks ACK value each time it sends a byte. When ack_check_en (master) is 0, $I2C_{master}$ does not check ACK value and take $I2C_{slave}$ as matching slave by default.

- Match: If the received ACK value matches ack_exp (master) (the expected ACK value), $I2C_{master}$ continues data transfer.
- Not match: If the received ACK value does not match ack_exp, $I2C_{master}$ generates an I2C_NACK_INT (master) interrupt and stops data transfer.

10. $I2C_{slave}$ receives the RX RAM address sent by $I2C_{master}$ and adds the offset.
11. $I2C_{master}$ sends data, and checks ACK value or not according to ack_check_en (master).
12. If data to be sent is larger than 32 bytes, TX RAM of $I2C_{master}$ may wrap around in FIFO mode. For details, please refer to Section 25.4.10.
13. If data to be received is larger than 32 bytes, you may enable clock stretching by setting I2C_SLAVE_SCL_STRETCH_EN (slave), and clearing I2C_RX_FULL_ACK_LEVEL to 0. When RX RAM is full, an I2C_SLAVE_STRETCH_INT (slave) interrupt is generated. In this way, $I2C_{slave}$ can hold SCL low, in exchange for more time to read data. After software has finished reading, you can set I2C_SLAVE_STRETCH_INT_CLR (slave) to 1 to clear interrupt, and set I2C_SLAVE_SCL_STRETCH_CLR (slave) to release the SCL line.
14. After data transfer completes, $I2C_{master}$ executes the STOP command, and generates an I2C_TRANS_COMPLETE_INT (master) interrupt.

25.5.4 $I2C_{master}$ Writes to $I2C_{slave}$ with a 7-bit Address in Multiple Command Sequences

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25.5.4.1 Introduction

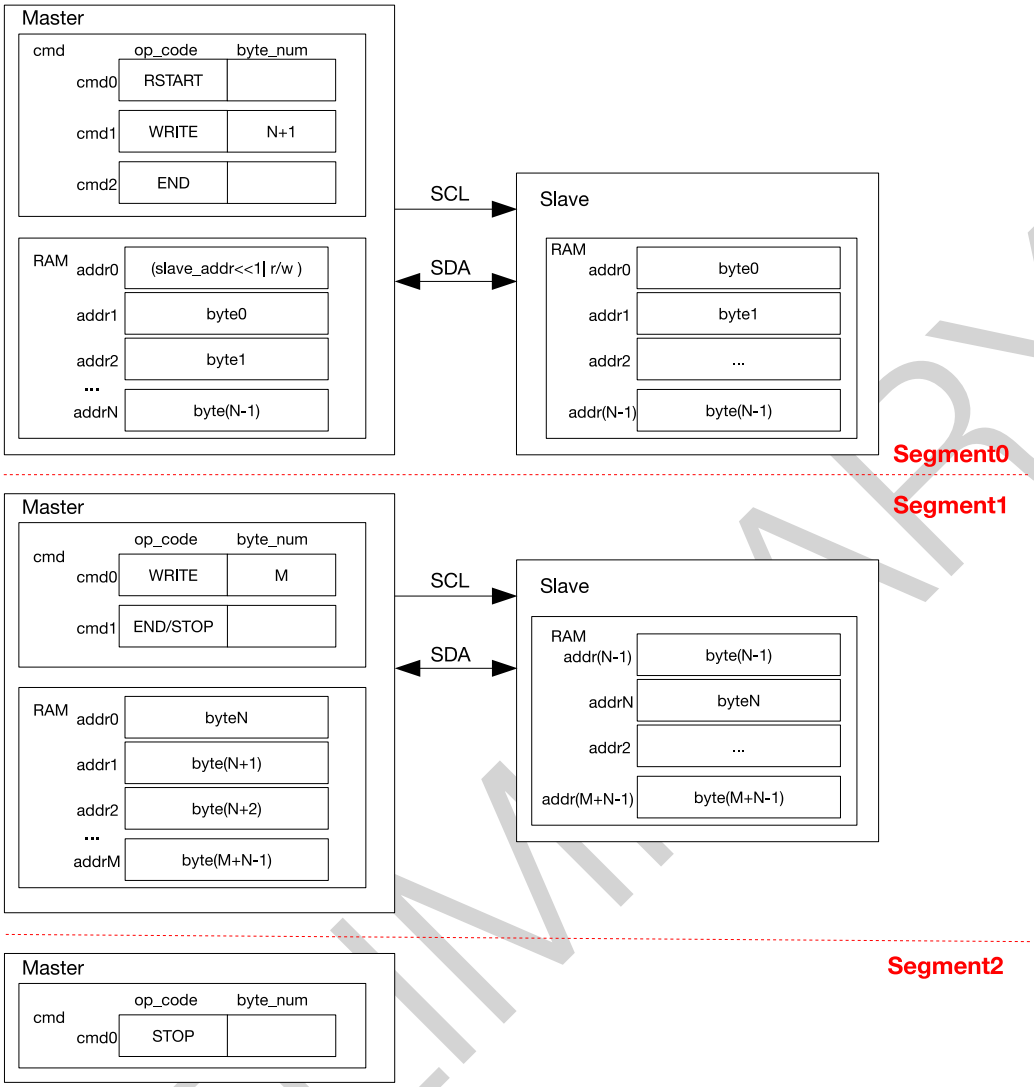


Figure 25-10. $I2C_{master}$ Writing to $I2C_{slave}$ with a 7-bit Address in Multiple Sequences

Given that the I2C Controller RAM holds only 32 bytes, when data are too large to be processed even by the wrapped RAM, it is advised to transmit them in multiple command sequences. At the end of every command sequence is an END command. When the controller executes this END command to pull SCL low, software refreshes command sequence registers and the RAM for next the transfer.

Figure 25-10 shows how $I2C_{master}$ writes to an I2C slave in two or three segments as an example. For the first segment, the CMD_Controller registers are configured as shown in Segment0. Once data in $I2C_{master}$'s RAM is ready and I2C_TRANS_START is set, $I2C_{master}$ initiates data transfer. After executing the END command, $I2C_{master}$ turns off the SCL clock and pulls SCL low to reserve the bus. Meanwhile, the controller generates an I2C_END_DETECT_INT interrupt.

For the second segment, after detecting the I2C_END_DETECT_INT interrupt, software refreshes the CMD_Controller registers, reloads the RAM and clears this interrupt, as shown in Segment1. If cmd1 in the second segment is a STOP, then data is transmitted to $I2C_{slave}$ in two segments. $I2C_{master}$ resumes data transfer after I2C_TRANS_START is set, and terminates the transfer by sending a STOP bit.

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For the third segment, after the second data transfer finishes and an I2C_END_DETECT_INT is detected, the CMD_Controller registers of $I2C_{master}$ are configured as shown in Segment2. Once I2C_TRANS_START is set, $I2C_{master}$ generates a STOP bit and terminates the transfer.

Note that other $I2C_{master}$s will not transact on the bus between two segments. The bus is only released after a STOP signal is sent. The I2C controller can be reset by setting I2C_FSM_RST field at any time. This field will later be cleared automatically by hardware.

25.5.4.2 Configuration Example

1. Set I2C_MS_MODE (master) to 1, and I2C_MS_MODE (slave) to 0.
2. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
3. Configure command registers of $I2C_{master}$.

Command registers	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND0 (master)	RSTART	—	—	—	—
I2C_COMMAND1 (master)	WRITE	ack_value	ack_exp	1	N+1
I2C_COMMAND2 (master)	END	—	—	—	—

4. Write the address of $I2C_{slave}$ and data to be sent to TX RAM of $I2C_{master}$ in either FIFO mode or non-FIFO mode according to Section 25.4.10.
5. Write the address of $I2C_{slave}$ to I2C_SLAVE_ADDR (slave) in I2C_SLAVE_ADDR_REG (slave) register
6. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
7. Write 1 to I2C_TRANS_START (master) and I2C_TRANS_START (slave) to start transfer.
8. $I2C_{slave}$ compares the slave address sent by $I2C_{master}$ with its own address in I2C_SLAVE_ADDR (slave). When ack_check_en (master) in $I2C_{master}$'s WRITE command is 1, $I2C_{master}$ checks ACK value each time it sends a byte. When ack_check_en (master) is 0, $I2C_{master}$ does not check ACK value and take $I2C_{slave}$ as matching slave by default.
   - Match: If the received ACK value matches ack_exp (master) (the expected ACK value), $I2C_{master}$ continues data transfer.
   - Not match: If the received ACK value does not match ack_exp, $I2C_{master}$ generates an I2C_NACK_INT (master) interrupt and stops data transfer.
9. $I2C_{master}$ sends data, and checks ACK value or not according to ack_check_en (master).
10. After the I2C_END_DETECT_INT (master) interrupt is generated, set I2C_END_DETECT_INT_CLR (master) to 1 to clear this interrupt.
11. Update $I2C_{master}$'s command registers.

Command registers	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND0 (master)	WRITE	ack_value	ack_exp	1	M
I2C_COMMAND1 (master)	END/STOP	—	—	—	—

12. Write M bytes of data to be sent to TX RAM of $I2C_{master}$ in FIFO or non-FIFO mode.

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13. Write 1 to I2C_TRANS_START (master) bit to start transfer and repeat step 9.
14. If the command is a STOP, I2C stops transfer and generates an I2C_TRANS_COMPLETE_INT (master) interrupt.
15. If the command is an END, repeat step 10.
16. Update $I2C_{master}$'s command registers.

Command registers of $I2C_{master}$	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND1 (master)	STOP	—	—	—	—

17. Write 1 to I2C_TRANS_START (master) bit to start transfer.
18. $I2C_{master}$ executes the STOP command and generates an I2C_TRANS_COMPLETE_INT (master) interrupt.

25.5.5 $I2C_{master}$ Reads $I2C_{slave}$ with a 7-bit Address in One Command Sequence

25.5.5.1 Introduction

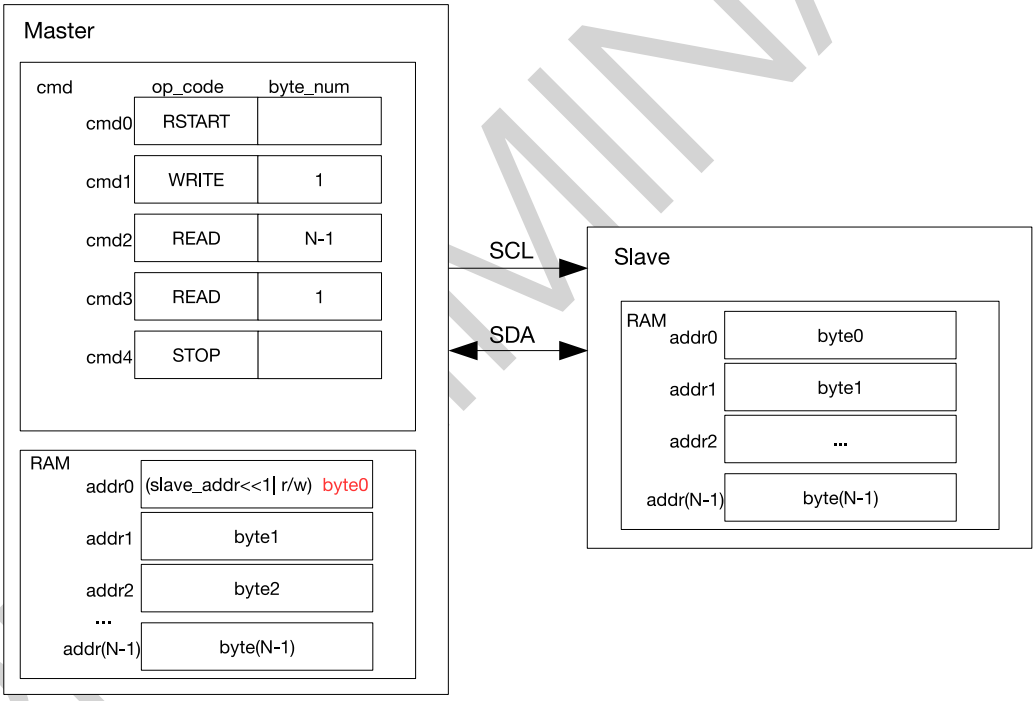


Figure 25-11. $I2C_{master}$ Reading $I2C_{slave}$ with a 7-bit Address

Figure 25-11 shows how $I2C_{master}$ reads N bytes of data from an I2C slave using 7-bit addressing. cmd1 is a WRITE command, and when this command is executed $I2C_{master}$ sends the address of $I2C_{slave}$. The byte sent comprises a 7-bit $I2C_{slave}$ address and a $R/\overline{W}$ bit. When the $R/\overline{W}$ bit is 1, it indicates a READ operation. If the address of an I2C slave matches the sent address, this matching slave starts sending data to $I2C_{master}$. $I2C_{master}$ generates acknowledgements according to ack_value defined in the READ command upon receiving a byte.

As illustrated in Figure 25-11, $I2C_{master}$ executes two READ commands: it generates ACKs for (N-1) bytes of data in cmd2, and a NACK for the last byte of data in cmd 3. This configuration may be changed as required.

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I2C$_{master}$ writes received data into the controller RAM from addr0, whose original content (a the address of I2C$_{slave}$ and a $R/\overline{W}$ bit) is overwritten by byte0 marked red in Figure 25-11.

25.5.5.2 Configuration Example

1. Set I2C_MS_MODE (master) to 1, and I2C_MS_MODE (slave) to 0.
2. We recommend setting I2C_SLAVE_SCL_STRETCH_EN (slave) to 1, so that SCL can be held low for more processing time when I2C$_{slave}$ needs to send data. If this bit is not set, software should write data to be sent to I2C$_{slave}$'s TX RAM before I2C$_{master}$ initiates transfer. Configuration below is applicable to scenario where I2C_SLAVE_SCL_STRETCH_EN (slave) is 1.
3. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
4. Configure command registers of I2C$_{master}$.

Command registers of I2C$_{master}$	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND0 (master)	RSTART	—	—	—	—
I2C_COMMAND1 (master)	WRITE	0	0	1	1
I2C_COMMAND2 (master)	READ	0	0	1	N-1
I2C_COMMAND3 (master)	READ	1	0	1	1
I2C_COMMAND4 (master)	STOP	—	—	—	—

5. Write the address of I2C$_{slave}$ to TX RAM of I2C$_{master}$ in either FIFO mode or non-FIFO mode according to Section 25.4.10.
6. Write the address of I2C$_{slave}$ to I2C_SLAVE_ADDR (slave) in I2C_SLAVE_ADDR_REG (slave) register.
7. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
8. Write 1 to I2C_TRANS_START (master) bit to start I2C$_{master}$'s transfer.
9. Start I2C$_{slave}$'s transfer according to Section 25.4.14.
10. I2C$_{slave}$ compares the slave address sent by I2C$_{master}$ with its own address in I2C_SLAVE_ADDR (slave). When ack_check_en (master) in I2C$_{master}$'s WRITE command is 1, I2C$_{master}$ checks ACK value each time it sends a byte. When ack_check_en (master) is 0, I2C$_{master}$ does not check ACK value and take I2C$_{slave}$ as matching slave by default.
    - Match: If the received ACK value matches ack_exp (master) (the expected ACK value), I2C$_{master}$ continues data transfer.
    - Not match: If the received ACK value does not match ack_exp, I2C$_{master}$ generates an I2C_NACK_INT (master) interrupt and stops data transfer.
11. After I2C_SLAVE_STRETCH_INT (slave) is generated, the I2C_STRETCH_CAUSE bit is 0. The address of I2C$_{slave}$ matches the address sent over SDA, and I2C$_{slave}$ needs to send data.
12. Write data to be sent to TX RAM of I2C$_{slave}$ in either FIFO mode or non-FIFO mode according to Section 25.4.10.
13. Set I2C_SLAVE_SCL_STRETCH_CLR (slave) to 1 to release SCL.

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14. $I2C_{slave}$ sends data, and $I2C_{master}$ checks ACK value or not according to ack_check_en (master) in the READ command.
15. If data to be read by $I2C_{master}$ is larger than 32 bytes, an I2C_SLAVE_STRETCH_INT (slave) interrupt will be generated when TX RAM of $I2C_{slave}$ becomes empty. In this way, $I2C_{slave}$ can hold SCL low, so that software has more time to pad data in TX RAM of $I2C_{slave}$ and read data in RX RAM of $I2C_{master}$. After software has finished reading, you can set I2C_SLAVE_STRETCH_INT_CLR (slave) to 1 to clear interrupt, and set I2C_SLAVE_SCL_STRETCH_CLR (slave) to release the SCL line.
16. After $I2C_{master}$ has received the last byte of data, set ack_value (master) to 1. $I2C_{slave}$ will stop transfer once receiving the I2C_NACK_INT interrupt.
17. After data transfer completes, $I2C_{master}$ executes the STOP command, and generates an I2C_TRANS_COMPLETE_INT (master) interrupt.

25.5.6 $I2C_{master}$ Reads $I2C_{slave}$ with a 10-bit Address in One Command Sequence

25.5.6.1 Introduction

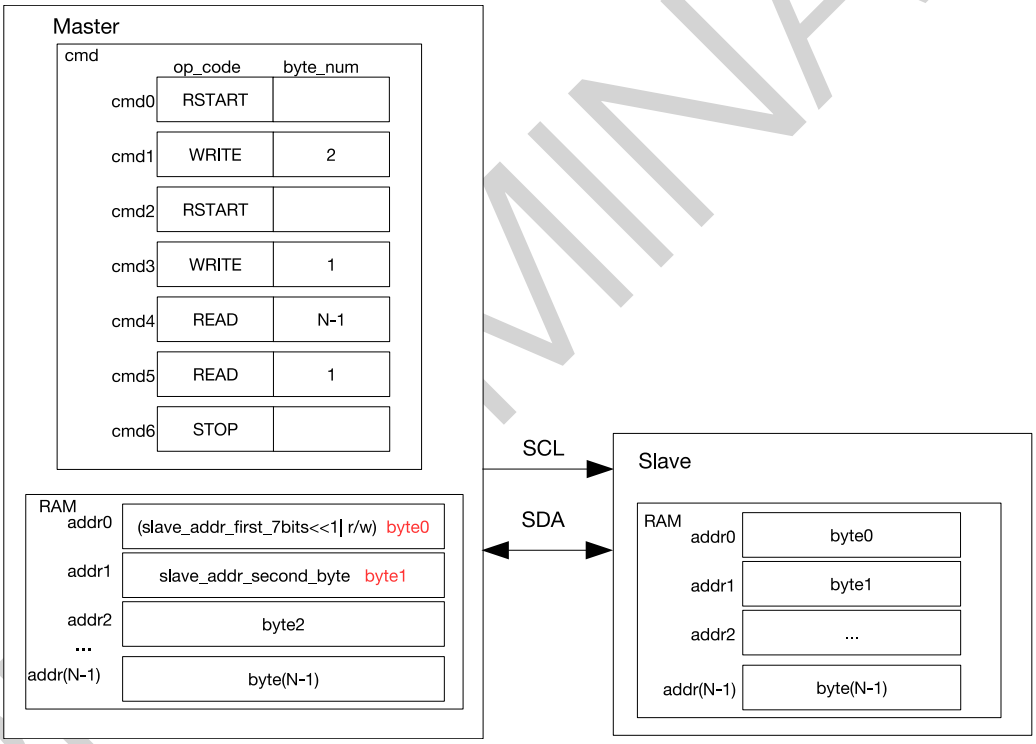


Figure 25-12. $I2C_{master}$ Reading $I2C_{slave}$ with a 10-bit Address

Figure 25-12 shows how $I2C_{master}$ reads data from an I2C slave using 10-bit addressing. Unlike 7-bit addressing, in 10-bit addressing the WRITE command of the $I2C_{master}$ is formed from two bytes, and correspondingly TX RAM of this master stores a 10-bit address of two bytes. The $R/\overline{W}$ bit in the first byte is 0, which indicates a WRITE operation. After a RSTART condition, $I2C_{master}$ sends the first byte of address again to read data from $I2C_{slave}$, but the $R/\overline{W}$ bit is 1, which indicates a READ operation. The two address bytes can be configured as described in Section 25.5.2.

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25.5.6.2 Configuration Example

1. Set I2C_MS_MODE (master) to 1, and I2C_MS_MODE (slave) to 0.
2. We recommend setting I2C_SLAVE_SCL_STRETCH_EN (slave) to 1, so that SCL can be held low for more processing time when $I2C_{slave}$ needs to send data. If this bit is not set, software should write data to be sent to $I2C_{slave}$'s TX RAM before $I2C_{master}$ initiates transfer. Configuration below is applicable to scenario where I2C_SLAVE_SCL_STRETCH_EN (slave) is 1.
3. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
4. Configure command registers of $I2C_{master}$.

Command registers of $I2C_{master}$	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND0 (master)	RSTART	—	—	—	—
I2C_COMMAND1 (master)	WRITE	0	0	1	2
I2C_COMMAND2 (master)	RSTART	—	—	—	—
I2C_COMMAND3 (master)	WRITE	0	0	1	1
I2C_COMMAND4 (master)	READ	0	0	1	N-1
I2C_COMMAND5 (master)	READ	1	0	1	1
I2C_COMMAND6 (master)	STOP	—	—	—	—

5. Configure I2C_SLAVE_ADDR (slave) in I2C_SLAVE_ADDR_REG (slave) as $I2C_{slave}$'s 10-bit address, and set I2C_ADDR_10BIT_EN (slave) to 1 to enable 10-bit addressing.
6. Write the address of $I2C_{slave}$ and data to be sent to TX RAM of $I2C_{master}$ in either FIFO or non-FIFO mode. The first byte of address comprises ((0x78 | I2C_SLAVE_ADDR[9:8])«1) and a $R/\overline{W}$ bit, which is 1 and indicates a WRITE operation. The second byte of address is I2C_SLAVE_ADDR[7:0]. The third byte is ((0x78 | I2C_SLAVE_ADDR[9:8])«1) and a $R/\overline{W}$ bit, which is 1 and indicates a READ operation.
7. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
8. Write 1 to I2C_TRANS_START (master) to start $I2C_{master}$'s transfer.
9. Start $I2C_{slave}$'s transfer according to Section 25.4.14.
10. $I2C_{slave}$ compares the slave address sent by $I2C_{master}$ with its own address in I2C_SLAVE_ADDR (slave). When ack_check_en (master) in $I2C_{master}$'s WRITE command is 1, $I2C_{master}$ checks ACK value each time it sends a byte. When ack_check_en (master) is 0, $I2C_{master}$ does not check ACK value and take $I2C_{slave}$ as matching slave by default.
    - Match: If the received ACK value matches ack_exp (master) (the expected ACK value), $I2C_{master}$ continues data transfer.
    - Not match: If the received ACK value does not match ack_exp, $I2C_{master}$ generates an I2C_NACK_INT (master) interrupt and stops data transfer.
11. $I2C_{master}$ sends a RSTART and the third byte in TX RAM, which is ((0x78 | I2C_SLAVE_ADDR[9:8])«1) and a $R/\overline{W}$ bit that indicates READ.
12. $I2C_{slave}$ repeats step 10. If its address matches the address sent by $I2C_{master}$, $I2C_{slave}$ proceed on to the next steps.

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13. After I2C_SLAVE_STRETCH_INT (slave) is generated, the I2C_STRETCH_CAUSE bit is 0. The address of $I2C_{slave}$ matches the address sent over SDA, and $I2C_{slave}$ needs to send data.
14. Write data to be sent to TX RAM of $I2C_{slave}$ in either FIFO mode or non-FIFO mode according to Section 25.4.10.
15. Set I2C_SLAVE_SCL_STRETCH_CLR (slave) to 1 to release SCL.
16. $I2C_{slave}$ sends data, and $I2C_{master}$ checks ACK value or not according to ack_check_en (master) in the READ command.
17. If data to be read by $I2C_{master}$ is larger than 32 bytes, an I2C_SLAVE_STRETCH_INT (slave) interrupt will be generated when TX RAM of $I2C_{slave}$ becomes empty. In this way, $I2C_{slave}$ can hold SCL low, so that software has more time to pad data in TX RAM of $I2C_{slave}$ and read data in RX RAM of $I2C_{master}$. After software has finished reading, you can set I2C_SLAVE_STRETCH_INT_CLR (slave) to 1 to clear interrupt, and set I2C_SLAVE_SCL_STRETCH_CLR (slave) to release the SCL line.
18. After $I2C_{master}$ has received the last byte of data, set ack_value (master) to 1. $I2C_{slave}$ will stop transfer once receiving the I2C_NACK_INT interrupt.
19. After data transfer completes, $I2C_{master}$ executes the STOP command, and generates an I2C_TRANS_COMPLETE_INT (master) interrupt.

25.5.7 $I2C_{master}$ Reads $I2C_{slave}$ with Two 7-bit Addresses in One Command Sequence

25.5.7.1 Introduction

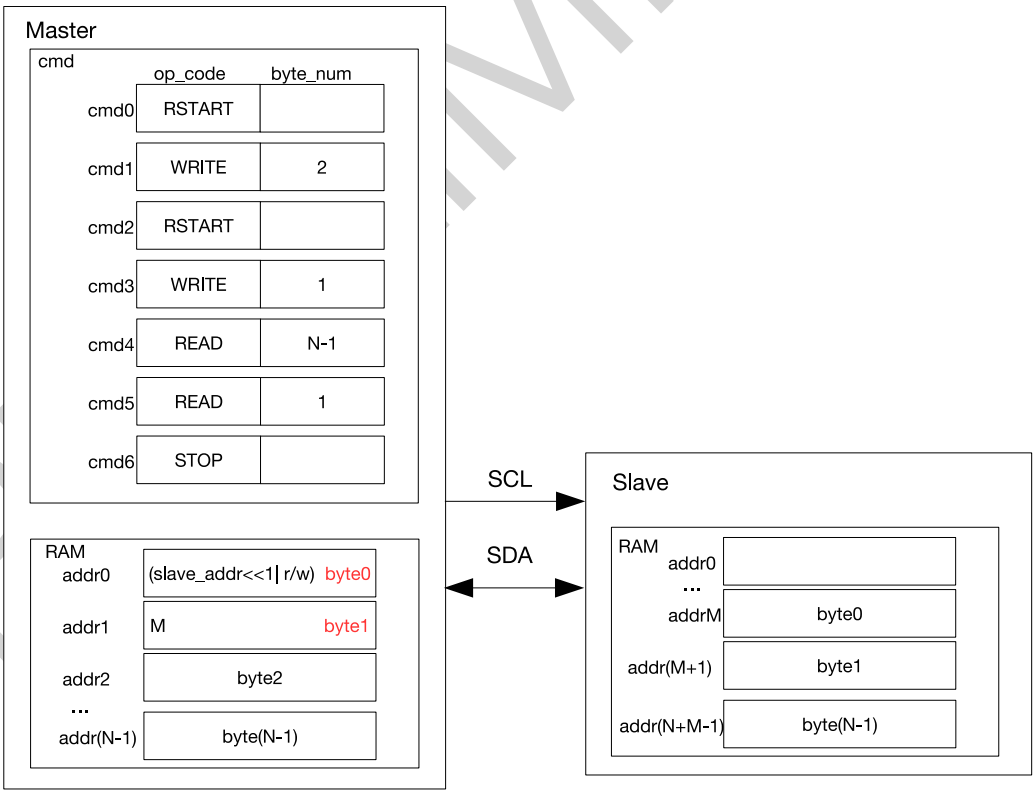


Figure 25-13. $I2C_{master}$ Reading N Bytes of Data from addrM of $I2C_{slave}$ with a 7-bit Address

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Figure 25-13 shows how I2C$_{master}$ reads data from specified addresses in an I2C slave. I2C$_{master}$ sends two bytes of addresses: the first byte is a 7-bit I2C$_{slave}$ address followed by a $R/\overline{W}$ bit, which is 0 and indicates a WRITE; the second byte is I2C$_{slave}$'s memory address. After a RSTART condition, I2C$_{master}$ sends the first byte of address again, but the $R/\overline{W}$ bit is 1 which indicates a READ. Then, I2C$_{master}$ reads data starting from addrM.

25.5.7.2 Configuration Example

1. Set I2C_MS_MODE (master) to 1, and I2C_MS_MODE (slave) to 0.
2. We recommend setting I2C_SLAVE_SCL_STRETCH_EN (slave) to 1, so that SCL can be held low for more processing time when I2C$_{slave}$ needs to send data. If this bit is not set, software should write data to be sent to I2C$_{slave}$'s TX RAM before I2C$_{master}$ initiates transfer. Configuration below is applicable to scenario where I2C_SLAVE_SCL_STRETCH_EN (slave) is 1.
3. Set I2C_FIFO_ADDR_CFG_EN (slave) to 1 to enable double addressing mode.
4. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
5. Configure command registers of I2C$_{master}$.

Command registers of I2C$_{master}$	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND0 (master)	RSTART	—	—	—	—
I2C_COMMAND1 (master)	WRITE	0	0	1	2
I2C_COMMAND2 (master)	RSTART	—	—	—	—
I2C_COMMAND3 (master)	WRITE	0	0	1	1
I2C_COMMAND4 (master)	READ	0	0	1	N-1
I2C_COMMAND5 (master)	READ	1	0	1	1
I2C_COMMAND6 (master)	STOP	—	—	—	—

6. Configure I2C_SLAVE_ADDR (slave) in I2C_SLAVE_ADDR_REG (slave) register as I2C$_{slave}$'s 7-bit address, and set I2C_ADDR_10BIT_EN (slave) to 0 to enable 7-bit addressing.
7. Write the address of I2C$_{slave}$ and data to be sent to TX RAM of I2C$_{master}$ in either FIFO or non-FIFO mode according to Section 25.4.10. The first byte of address comprises (I2C_SLAVE_ADDR[6:0])«1) and a $R/\overline{W}$ bit, which is 0 and indicates a WRITE. The second byte of address is memory address M of I2C$_{slave}$. The third byte is (I2C_SLAVE_ADDR[6:0])«1) and a $R/\overline{W}$ bit, which is 1 and indicates a READ.
8. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
9. Write 1 to I2C_TRANS_START (master) to start I2C$_{master}$'s transfer.
10. Start I2C$_{slave}$'s transfer according to Section 25.4.14.
11. I2C$_{slave}$ compares the slave address sent by I2C$_{master}$ with its own address in I2C_SLAVE_ADDR (slave). When ack_check_en (master) in I2C$_{master}$'s WRITE command is 1, I2C$_{master}$ checks ACK value each time it sends a byte. When ack_check_en (master) is 0, I2C$_{master}$ does not check ACK value and take I2C$_{slave}$ as matching slave by default.
    - Match: If the received ACK value matches ack_exp (master) (the expected ACK value), I2C$_{master}$ continues data transfer.

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- Not match: If the received ACK value does not match ack_exp, $I2C_{master}$ generates an I2C_NACK_INT (master) interrupt and stops data transfer.

12. $I2C_{slave}$ receives memory address sent by $I2C_{master}$ and adds the offset.
13. $I2C_{master}$ sends a RSTART and the third byte in TX RAM, which is ((0x78 | I2C_SLAVE_ADDR[9:8])«1) and a R bit.
14. $I2C_{slave}$ repeats step 11. If its address matches the address sent by $I2C_{master}$, $I2C_{slave}$ proceed on to the next steps.
15. After I2C_SLAVE_STRETCH_INT (slave) is generated, the I2C_STRETCH_CAUSE bit is 0. The address of $I2C_{slave}$ matches the address sent over SDA, and $I2C_{slave}$ needs to send data.
16. Write data to be sent to TX RAM of $I2C_{slave}$ in either FIFO mode or non-FIFO mode according to Section 25.4.10.
17. Set I2C_SLAVE_SCL_STRETCH_CLR (slave) to 1 to release SCL.
18. $I2C_{slave}$ sends data, and $I2C_{master}$ checks ACK value or not according to ack_check_en (master) in the READ command.
19. If data to be read by $I2C_{master}$ is larger than 32 bytes, an I2C_SLAVE_STRETCH_INT (slave) interrupt will be generated when TX RAM of $I2C_{slave}$ becomes empty. In this way, $I2C_{slave}$ can hold SCL low, so that software has more time to pad data in TX RAM of $I2C_{slave}$ and read data in RX RAM of $I2C_{master}$. After software has finished reading, you can set I2C_SLAVE_STRETCH_INT_CLR (slave) to 1 to clear interrupt, and set I2C_SLAVE_SCL_STRETCH_CLR (slave) to release the SCL line.
20. After $I2C_{master}$ has received the last byte of data, set ack_value (master) to 1. $I2C_{slave}$ will stop transfer once receiving the I2C_NACK_INT interrupt.
21. After data transfer completes, $I2C_{master}$ executes the STOP command, and generates an I2C_TRANS_COMPLETE_INT (master) interrupt.

25.5.8 $I2C_{master}$ Reads $I2C_{slave}$ with a 7-bit Address in Multiple Command Sequences

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25.5.8.1 Introduction

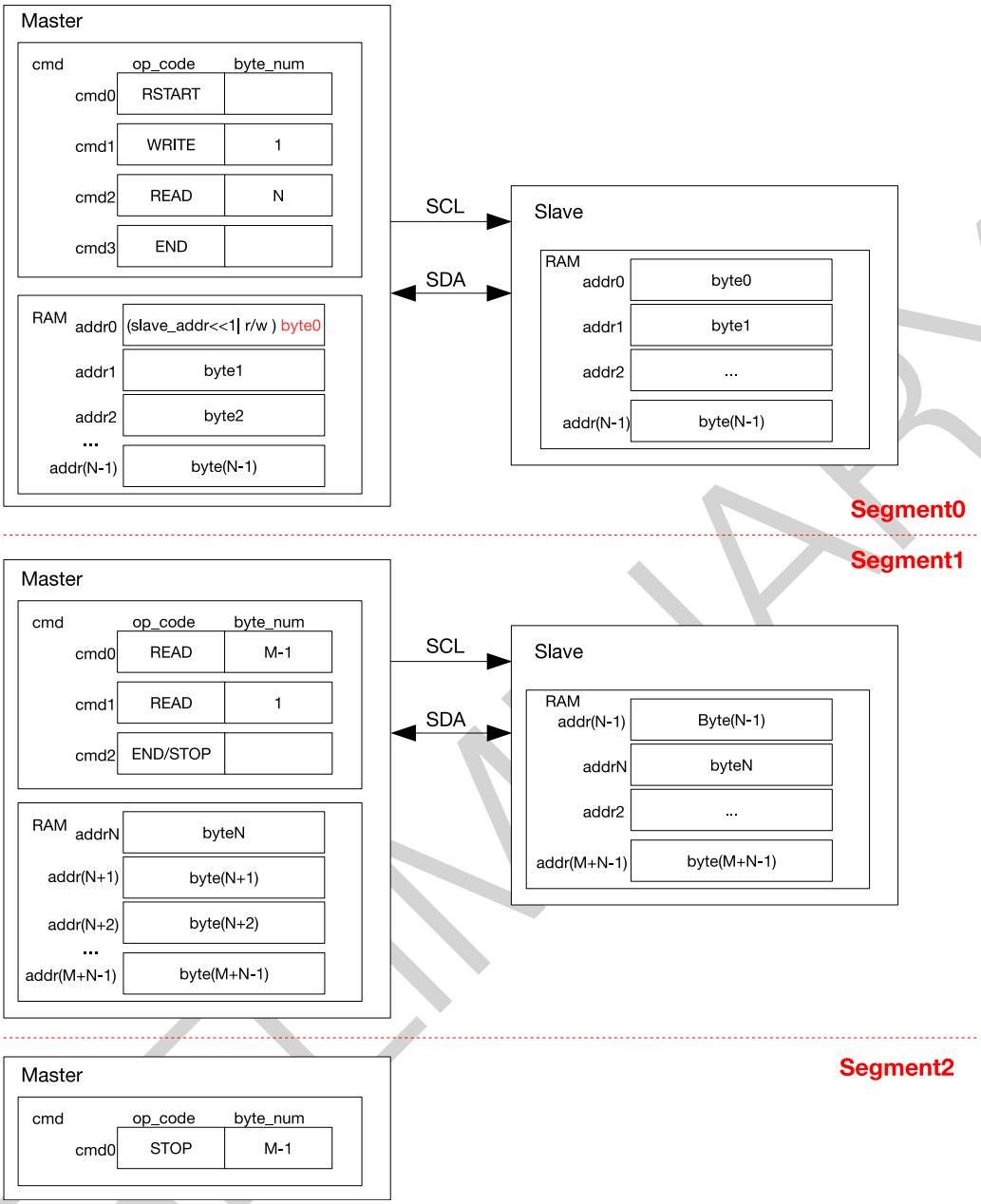


Figure 25-14. $I2C_{master}$ Reading $I2C_{slave}$ with a 7-bit Address in Segments

Figure 25-14 shows how $I2C_{master}$ reads (N+M) bytes of data from an I2C slave in two/three segments separated by END commands. Configuration procedures are described as follows:

1. The procedures for Segment0 is similar to 25-11, except that the last command is an END.
2. Prepare data in the TX RAM of $I2C_{slave}$, and set I2C_TRANS_START to start data transfer. After executing the END command, $I2C_{master}$ refreshes command registers and the RAM as shown in Segment1, and clears the corresponding I2C_END_DETECT_INT interrupt. If cmd2 in Segment1 is a STOP, then data is read from $I2C_{slave}$ in two segments. $I2C_{master}$ resumes data transfer by setting I2C_TRANS_START and terminates the transfer by sending a STOP bit.
3. If cmd2 in Segment1 is an END, then data is read from $I2C_{slave}$ in three segments. After the second data

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transfer finishes and an I2C_END_DETECT_INT interrupt is detected, the cmd box is configured as shown in Segment2. Once I2C_TRANS_START is set, $I2C_{master}$ terminates the transfer by sending a STOP bit.

25.5.8.2 Configuration Example

1. Set I2C_MS_MODE (master) to 1, and I2C_MS_MODE (slave) to 0.
2. We recommend setting I2C_SLAVE_SCL_STRETCH_EN (slave) to 1, so that SCL can be held low for more processing time when $I2C_{slave}$ needs to send data. If this bit is not set, software should write data to be sent to $I2C_{slave}$'s TX RAM before $I2C_{master}$ initiates transfer. Configuration below is applicable to scenario where I2C_SLAVE_SCL_STRETCH_EN (slave) is 1.
3. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
4. Configure command registers of $I2C_{master}$.

Command registers of $I2C_{master}$	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND0 (master)	RSTART	—	—	—	—
I2C_COMMAND1 (master)	WRITE	0	0	1	1
I2C_COMMAND2 (master)	READ	0	0	1	N
I2C_COMMAND3 (master)	END	—	—	—	—

5. Write the address of $I2C_{slave}$ to TX RAM of $I2C_{master}$ in FIFO or non-FIFO mode.
6. Write the address of $I2C_{slave}$ to I2C_SLAVE_ADDR (slave) in I2C_SLAVE_ADDR_REG (slave) register.
7. Write 1 to I2C_CONF_UPGATE (master) and I2C_CONF_UPGATE (slave) to synchronize registers.
8. Write 1 to I2C_TRANS_START (master) to start $I2C_{master}$'s transfer.
9. Start $I2C_{slave}$'s transfer according to Section 25.4.14.
10. $I2C_{slave}$ compares the slave address sent by $I2C_{master}$ with its own address in I2C_SLAVE_ADDR (slave). When ack_check_en (master) in $I2C_{master}$'s WRITE command is 1, $I2C_{master}$ checks ACK value each time it sends a byte. When ack_check_en (master) is 0, $I2C_{master}$ does not check ACK value and take $I2C_{slave}$ as matching slave by default.
    - Match: If the received ACK value matches ack_exp (master) (the expected ACK value), $I2C_{master}$ continues data transfer.
    - Not match: If the received ACK value does not match ack_exp, $I2C_{master}$ generates an I2C_NACK_INT (master) interrupt and stops data transfer.
11. After I2C_SLAVE_STRETCH_INT (slave) is generated, the I2C_STRETCH_CAUSE bit is 0. The address of $I2C_{slave}$ matches the address sent over SDA, and $I2C_{slave}$ needs to send data.
12. Write data to be sent to TX RAM of $I2C_{slave}$ in either FIFO mode or non-FIFO mode according to Section 25.4.10.
13. Set I2C_SLAVE_SCL_STRETCH_CLR (slave) to 1 to release SCL.
14. $I2C_{slave}$ sends data, and $I2C_{master}$ checks ACK value or not according to ack_check_en (master) in the READ command.

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15. If data to be read by $I2C_{master}$ in one READ command (N or M) is larger than 32 bytes, an I2C_SLAVE_STRETCH_INT (slave) interrupt will be generated when TX RAM of $I2C_{slave}$ becomes empty. In this way, $I2C_{slave}$ can hold SCL low, so that software has more time to pad data in TX RAM of $I2C_{slave}$ and read data in RX RAM of $I2C_{master}$. After software has finished reading, you can set I2C_SLAVE_STRETCH_INT_CLR (slave) to 1 to clear interrupt, and set I2C_SLAVE_SCL_STRETCH_CLR (slave) to release the SCL line.
16. Once finishing reading data in the first READ command, $I2C_{master}$ executes the END command and triggers an I2C_END_DETECT_INT (master) interrupt, which is cleared by setting I2C_END_DETECT_INT_CLR (master) to 1.
17. Update $I2C_{master}$'s command registers using one of the following two methods:

Command registers of $I2C_{master}$	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND0 (master)	READ	ack_value	ack_exp	1	M
I2C_COMMAND1 (master)	END	—	—	—	—

Or

Command registers of $I2C_{master}$	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND0 (master)	READ	0	0	1	M-1
I2C_COMMAND0 (master)	READ	1	0	1	1
I2C_COMMAND1 (master)	STOP	—	—	—	—

18. Write M bytes of data to be sent to TX RAM of $I2C_{slave}$. If M is larger than 32, then repeat step 14 in FIFO or non-FIFO mode.
19. Write 1 to I2C_TRANS_START (master) bit to start transfer and repeat step 14.
20. If the last command is a STOP, then set ack_value (master) to 1 after $I2C_{master}$ has received the last byte of data. $I2C_{slave}$ stops transfer upon the I2C_NACK_INT interrupt. $I2C_{master}$ executes the STOP command to stop transfer and generates an I2C_TRANS_COMPLETE_INT (master) interrupt.
21. If the last command is an END, then repeat step 16 and proceed on to the next steps.
22. Update $I2C_{master}$'s command registers.

Command registers of $I2C_{master}$	op_code	ack_value	ack_exp	ack_check_en	byte_num
I2C_COMMAND1 (master)	STOP	—	—	—	—

23. Write 1 to I2C_TRANS_START (master) bit to start transfer.
24. $I2C_{master}$ executes the STOP command to stop transfer, and generates an I2C_TRANS_COMPLETE_INT (master) interrupt.

25.6 Interrupts

- I2C_SLAVE_STRETCH_INT: Generated when one of the four stretching events occurs in slave mode.

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- I2C_DET_START_INT: Triggered when the master or the slave detects a START bit.
- I2C_SCL_MAIN_ST_TO_INT: Triggered when the main state machine SCL_MAIN_FSM remains unchanged for over I2C_SCL_MAIN_ST_TO_I2C[23:0] clock cycles.
- I2C_SCL_ST_TO_INT: Triggered when the state machine SCL_FSM remains unchanged for over I2C_SCL_ST_TO_I2C[23:0] clock cycles.
- I2C_RXFIFO_UDF_INT: Triggered when the I2C controller reads RX FIFO via the APB bus, but RX FIFO is empty.
- I2C_TXFIFO_OVF_INT: Triggered when the I2C controller writes TX FIFO via the APB bus, but TX FIFO is full.
- I2C_NACK_INT: Triggered when the ACK value received by the master is not as expected, or when the ACK value received by the slave is 1.
- I2C_TRANS_START_INT: Triggered when the I2C controller sends a START bit.
- I2C_TIME_OUT_INT: Triggered when SCL stays high or low for more than I2C_TIME_OUT_VALUE clock cycles during data transfer.
- I2C_TRANS_COMPLETE_INT: Triggered when the I2C controller detects a STOP bit.
- I2C_MST_TXFIFO_UDF_INT: Triggered when TX FIFO of the master underflows.
- I2C_ARBITRATION_LOST_INT: Triggered when the SDA's output value does not match its input value while the master's SCL is high.
- I2C_BYTE_TRANS_DONE_INT: Triggered when the I2C controller sends or receives a byte.
- I2C_END_DETECT_INT: Triggered when op_code of the master indicates an END command and an END condition is detected.
- I2C_RXFIFO_OVF_INT: Triggered when RX FIFO of the I2C controller overflows.
- I2C_TXFIFO_WM_INT: I2C TX FIFO watermark interrupt. Triggered when I2C_FIFO_PRT_EN is 1 and the pointers of TX FIFO are less than I2C_TXFIFO_WM_THRHD[4:0].
- I2C_RXFIFO_WM_INT: I2C RX FIFO watermark interrupt. Triggered when I2C_FIFO_PRT_EN is 1 and the pointers of RX FIFO are greater than I2C_RXFIFO_WM_THRHD[4:0].

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25.7 Register Summary

The addresses in this section are relative to I2C Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
Timing registers			
I2C_SCL_LOW_PERIOD_REG	Configures the low level width of SCL	0x0000	R/W
I2C_SDA_HOLD_REG	Configures the hold time after a negative SCL edge	0x0030	R/W
I2C_SDA_SAMPLE_REG	Configures the sample time after a positive SCL edge	0x0034	R/W
I2C_SCL_HIGH_PERIOD_REG	Configures the high level width of SCL	0x0038	R/W
I2C_SCL_START_HOLD_REG	Configures the delay between the SDA and SCL negative edge for a START condition	0x0040	R/W
I2C_SCL_RSTART_SETUP_REG	Configures the delay between the positive edge of SCL and the negative edge of SDA	0x0044	R/W
I2C_SCL_STOP_HOLD_REG	Configures the delay after the SCL clock edge for a STOP condition	0x0048	R/W
I2C_SCL_STOP_SETUP_REG	Configures the delay between the SDA and SCL positive edge for a STOP condition	0x004C	R/W
I2C_SCL_ST_TIME_OUT_REG	SCL status timeout register	0x0078	R/W
I2C_SCL_MAIN_ST_TIME_OUT_REG	SCL main status timeout register	0x007C	R/W
Configuration registers			
I2C_CTR_REG	Transmission configuration register	0x0004	varies
I2C_TO_REG	Timeout control register	0x000C	R/W
I2C_SLAVE_ADDR_REG	Slave address configuration register	0x0010	R/W
I2C_FIFO_CONF_REG	FIFO configuration register	0x0018	R/W
I2C_FILTER_CFG_REG	SCL and SDA filter configuration register	0x0050	R/W
I2C_CLK_CONF_REG	I2C clock configuration register	0x0054	R/W
I2C_SCL_SP_CONF_REG	Power configuration register	0x0080	varies
I2C_SCL_STRETCH_CONF_REG	Configures SCL clock stretching	0x0084	varies
Status registers			
I2C_SR_REG	Describes I2C work status	0x0008	RO
I2C_FIFO_ST_REG	FIFO status register	0x0014	RO
I2C_DATA_REG	Read/write FIFO register	0x001C	R/W
Interrupt registers			
I2C_INT_RAW_REG	Raw interrupt status	0x0020	R/SS/WTC
I2C_INT_CLR_REG	Interrupt clear bits	0x0024	WT
I2C_INT_ENA_REG	Interrupt enable bits	0x0028	R/W
I2C_INT_STATUS_REG	Status of captured I2C communication events	0x002C	RO
Command registers			
I2C_COMD0_REG	I2C command register 0	0x0058	varies
I2C_COMD1_REG	I2C command register 1	0x005C	varies
I2C_COMD2_REG	I2C command register 2	0x0060	varies

PRELIMINARY

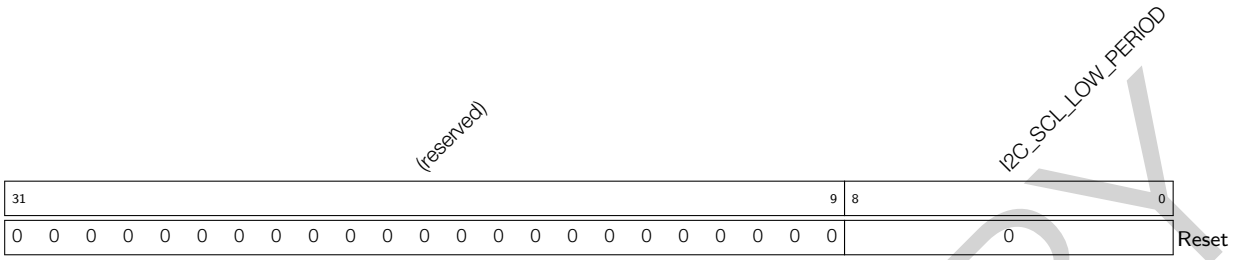
Name	Description	Address	Access
I2C_COMD3_REG	I2C command register 3	0x0064	varies
I2C_COMD4_REG	I2C command register 4	0x0068	varies
I2C_COMD5_REG	I2C command register 5	0x006C	varies
I2C_COMD6_REG	I2C command register 6	0x0070	varies
I2C_COMD7_REG	I2C command register 7	0x0074	varies
Version register			
I2C_DATE_REG	Version control register	0x00F8	R/W

PRELIMINARY

25.8 Registers

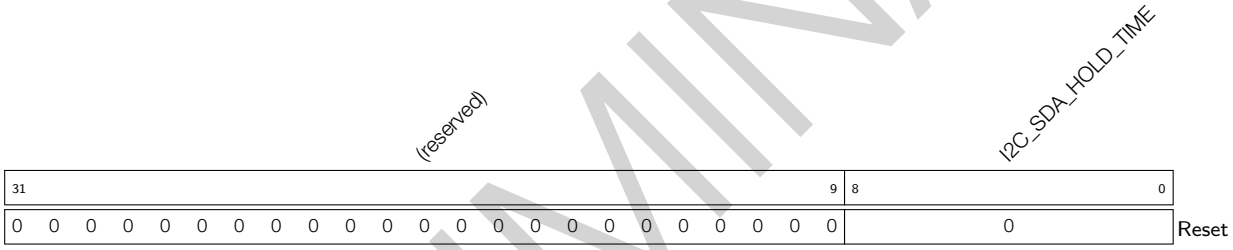
The addresses in this section are relative to I2C Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 25.1. I2C_SCL_LOW_PERIOD_REG (0x0000)



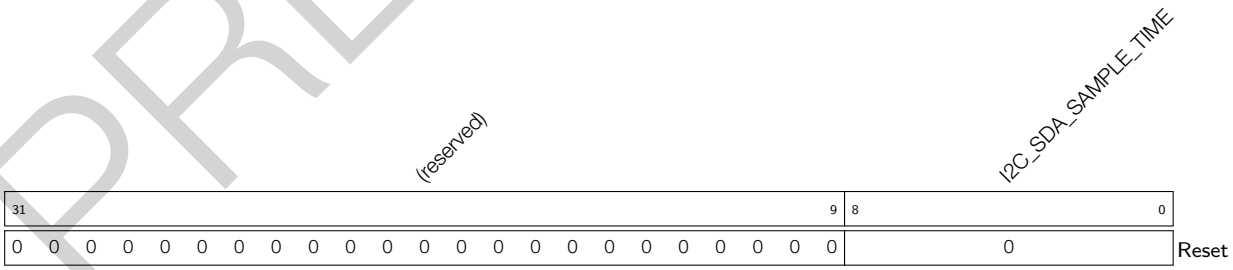
I2C_SCL_LOW_PERIOD This field is used to configure how long SCL remains low in master mode, in I2C module clock cycles. (R/W)

Register 25.2. I2C_SDA_HOLD_REG (0x0030)



I2C_SDA_HOLD_TIME This field is used to configure the time to hold the data after the falling edge of SCL, in I2C module clock cycles. (R/W)

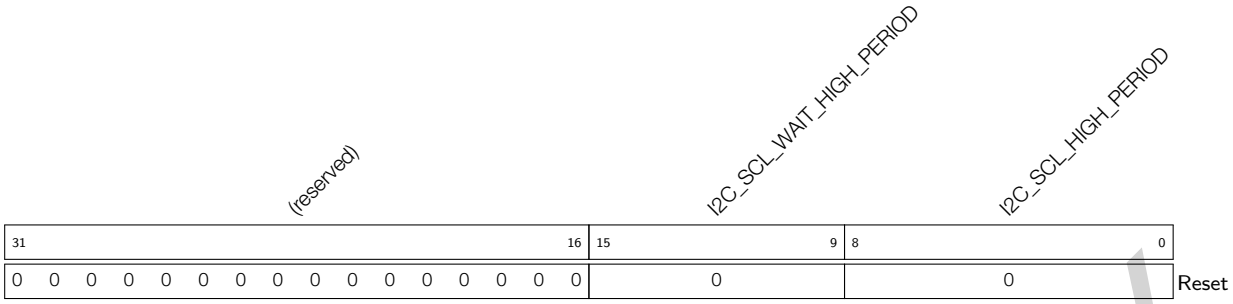
Register 25.3. I2C_SDA_SAMPLE_REG (0x0034)



I2C_SDA_SAMPLE_TIME This field is used to configure how long SDA is sampled, in I2C module clock cycles. (R/W)

PRELIMINARY

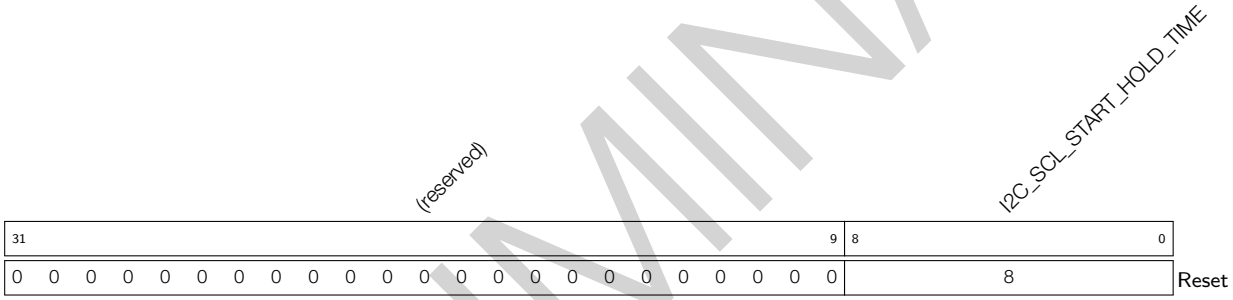
Register 25.4. I2C_SCL_HIGH_PERIOD_REG (0x0038)



I2C_SCL_HIGH_PERIOD This field is used to configure how long SCL remains high in master mode, in I2C module clock cycles. (R/W)

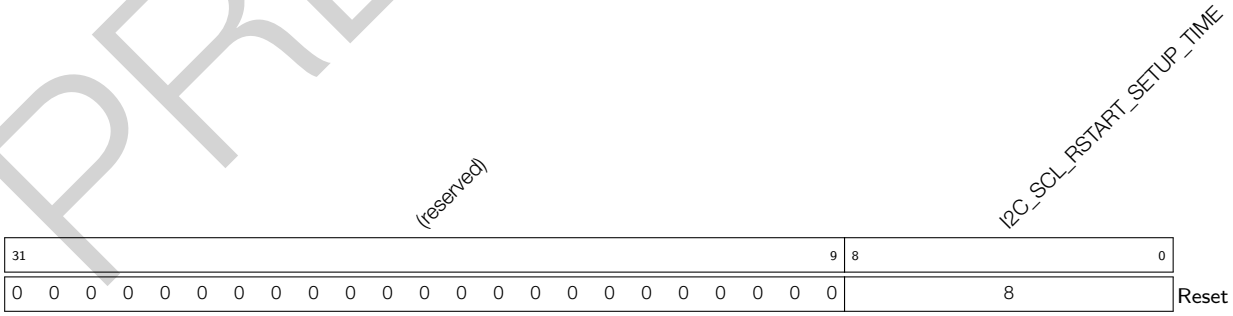
I2C_SCL_WAIT_HIGH_PERIOD This field is used to configure the SCL_FSM's waiting period for SCL high level in master mode, in I2C module clock cycles. (R/W)

Register 25.5. I2C_SCL_START_HOLD_REG (0x0040)



I2C_SCL_START_HOLD_TIME This field is used to configure the time between the falling edge of SDA and the falling edge of SCL for a START condition, in I2C module clock cycles. (R/W)

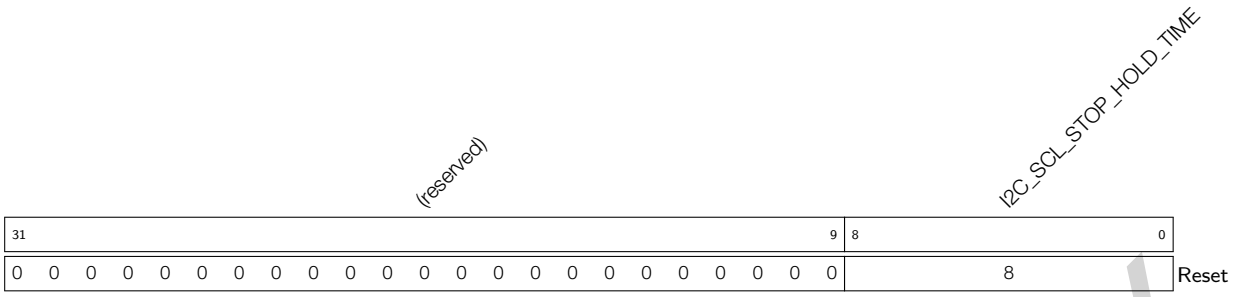
Register 25.6. I2C_SCL_RSTART_SETUP_REG (0x0044)



I2C_SCL_RSTART_SETUP_TIME This field is used to configure the time between the rising edge of SCL and the falling edge of SDA for a RSTART condition, in I2C module clock cycles. (R/W)

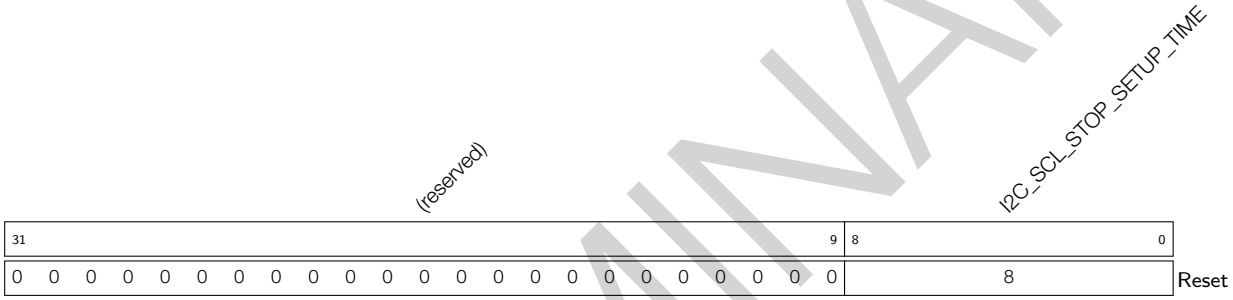
PRELIMINARY

Register 25.7. I2C_SCL_STOP_HOLD_REG (0x0048)



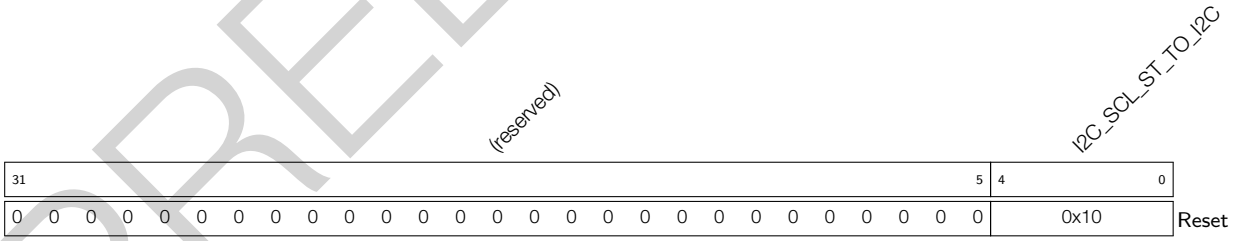
I2C_SCL_STOP_HOLD_TIME This field is used to configure the delay after the STOP condition, in I2C module clock cycles. (R/W)

Register 25.8. I2C_SCL_STOP_SETUP_REG (0x004C)



I2C_SCL_STOP_SETUP_TIME This field is used to configure the time between the rising edge of SCL and the rising edge of SDA, in I2C module clock cycles. (R/W)

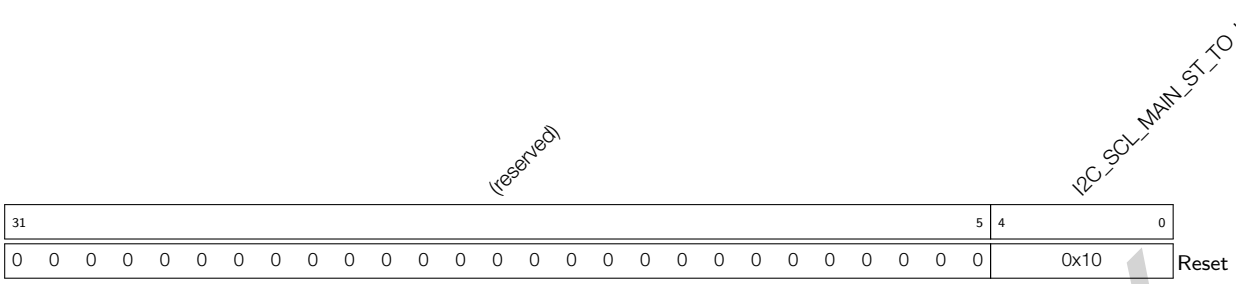
Register 25.9. I2C_SCL_ST_TIME_OUT_REG (0x0078)



I2C_SCL_ST_TO_I2C The maximum time that SCL_FSM remains unchanged. It should be no more than 23. (R/W)

PRELIMINARY

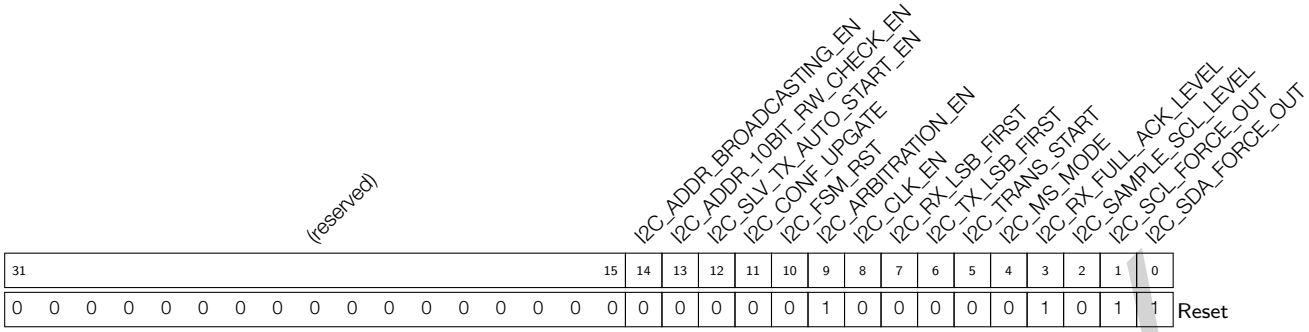
Register 25.10. I2C_SCL_MAIN_ST_TIME_OUT_REG (0x007C)



I2C_SCL_MAIN_ST_TO_I2C The maximum time that SCL_MAIN_FSM remains unchanged. It should be no more than 23. (R/W)

PRELIMINARY

Register 25.11. I2C_CTR_REG (0x0004)



I2C_SDA_FORCE_OUT 0: direct output; 1: open-drain output. (R/W)

I2C_SCL_FORCE_OUT 0: direct output; 1: open-drain output. (R/W)

I2C_SAMPLE_SCL_LEVEL This bit is used to select the sampling mode. 0: samples SDA data on the SCL high level; 1: samples SDA data on the SCL low level. (R/W)

I2C_RX_FULL_ACK_LEVEL This bit is used to configure the ACK value that need to be sent by master when I2C_RXFIFO_CNT has reached the threshold. (R/W)

I2C_MS_MODE Set this bit to configure the I2C controller as an I2C Master. Clear this bit to configure the I2C controller as a slave. (R/W)

I2C_TRANS_START Set this bit to start sending the data in TX FIFO. (WT)

I2C_TX_LSB_FIRST This bit is used to control the order to send data. 0: sends data from the most significant bit; 1: sends data from the least significant bit. (R/W)

I2C_RX_LSB_FIRST This bit is used to control the order to receive data. 0: receives data from the most significant bit; 1: receives data from the least significant bit. (R/W)

I2C_CLK_EN This field controls APB_CLK clock gating. 0: APB_CLK is gated to save power; 1: APB_CLK is always on. (R/W)

I2C_ARBITRATION_EN This is the enable bit for I2C bus arbitration function. (R/W)

I2C_FSM_RST This bit is used to reset the SCL_FSM. (WT)

I2C_CONF_UPGATE Synchronization bit. (WT)

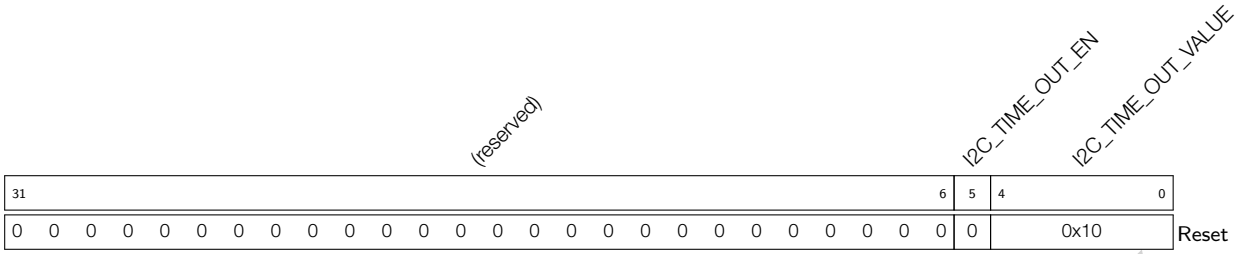
I2C_SLV_TX_AUTO_START_EN This is the enable bit for slave to send data automatically. (R/W)

I2C_ADDR_10BIT_RW_CHECK_EN This is the enable bit to check if the R/W bit of 10-bit addressing is consistent with the I2C protocol. (R/W)

I2C_ADDR_BROADCASTING_EN This is the enable bit for 7-bit general call addressing. (R/W)

PRELIMINARY

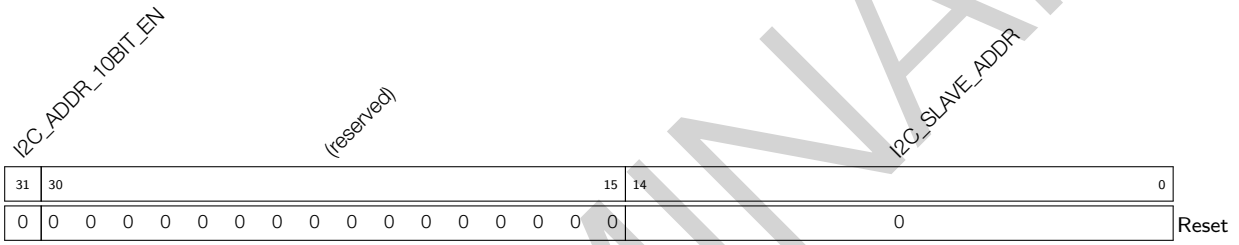
Register 25.12. I2C_TO_REG (0x000C)



I2C_TIME_OUT_VALUE This field is used to configure the timeout for receiving a data bit in APB clock cycles. (R/W)

I2C_TIME_OUT_EN This is the enable bit for timeout control. (R/W)

Register 25.13. I2C_SLAVE_ADDR_REG (0x0010)

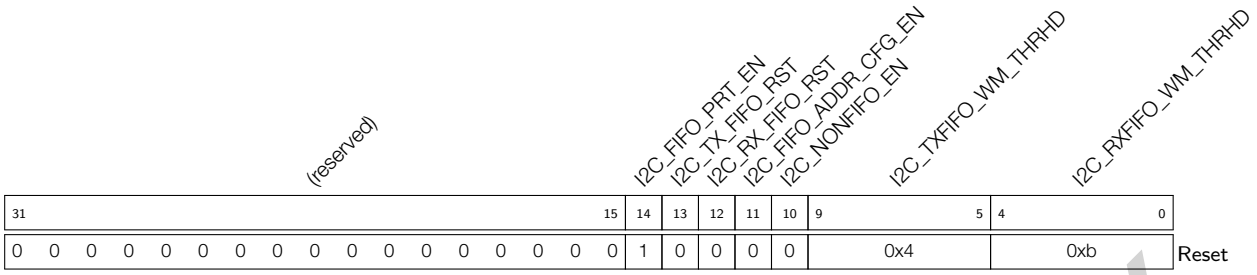


I2C_SLAVE_ADDR When the I2C controller is in slave mode, this field is used to configure the slave address. (R/W)

I2C_ADDR_10BIT_EN This field is used to enable the 10-bit addressing mode in master mode. (R/W)

PRELIMINARY

Register 25.14. I2C_FIFO_CONF_REG (0x0018)



I2C_RXFIFO_WM_THRHD The watermark threshold of RX FIFO in non-FIFO mode. When I2C_FIFO_PRT_EN is 1 and RX FIFO counter is bigger than I2C_RXFIFO_WM_THRHD[4:0], I2C_RXFIFO_WM_INT_RAW bit is valid. (R/W)

I2C_TXFIFO_WM_THRHD The watermark threshold of TX FIFO in non-FIFO mode. When I2C_FIFO_PRT_EN is 1 and TX FIFO counter is smaller than I2C_TXFIFO_WM_THRHD[4:0], I2C_TXFIFO_WM_INT_RAW bit is valid. (R/W)

I2C_NONFIFO_EN Set this bit to enable APB non-FIFO mode. (R/W)

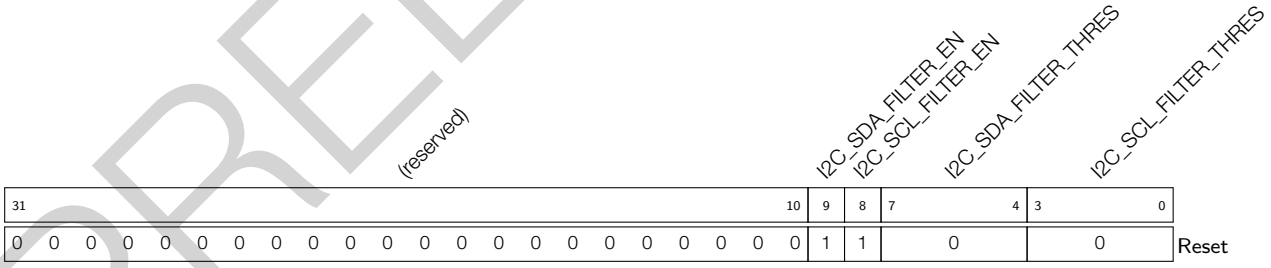
I2C_FIFO_ADDR_CFG_EN When this bit is set to 1, the byte received after the I2C address byte represents the offset address in the I2C Slave RAM. (R/W)

I2C_RX_FIFO_RST Set this bit to reset RX FIFO. (R/W)

I2C_TX_FIFO_RST Set this bit to reset TX FIFO. (R/W)

I2C_FIFO_PRT_EN The control enable bit of FIFO pointer in non-FIFO mode. This bit controls the valid bits and TX/RX FIFO overflow, underflow, full and empty interrupts. (R/W)

Register 25.15. I2C_FILTER_CFG_REG (0x0050)



I2C_SCL_FILTER_THRES When a pulse on the SCL input has smaller width than the value of this field in I2C module clock cycles, the I2C controller ignores that pulse. (R/W)

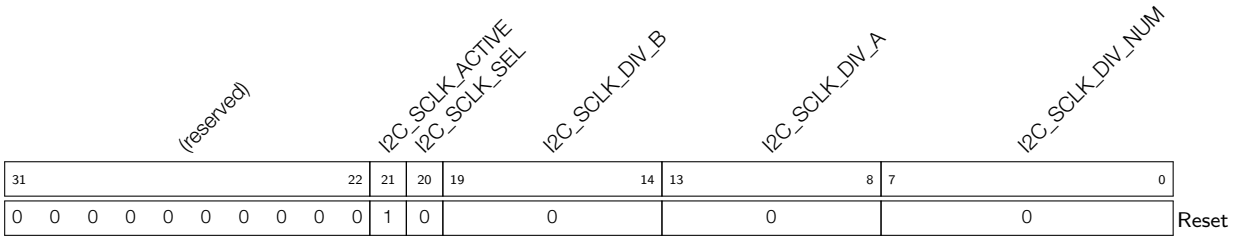
I2C_SDA_FILTER_THRES When a pulse on the SDA input has smaller width than the value of this field in I2C module clock cycles, the I2C controller ignores that pulse. (R/W)

I2C_SCL_FILTER_EN This is the filter enable bit for SCL. (R/W)

I2C_SDA_FILTER_EN This is the filter enable bit for SDA. (R/W)

PRELIMINARY

Register 25.16. I2C_CLK_CONF_REG (0x0054)



I2C_SCLK_DIV_NUM The integral part of the divisor. (R/W)

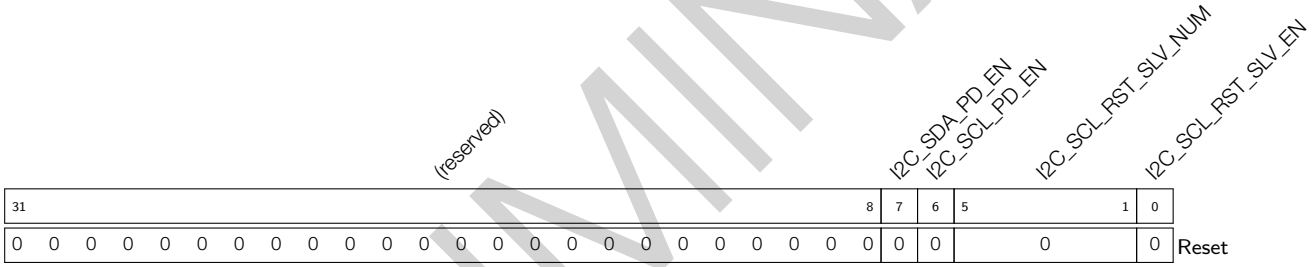
I2C_SCLK_DIV_A The numerator of the divisor's fractional part. (R/W)

I2C_SCLK_DIV_B The denominator of the divisor's fractional part. (R/W)

I2C_SCLK_SEL The clock selection bit for the I2C controller. 0: XTAL_CLK; 1: FOSC_CLK. (R/W)

I2C_SCLK_ACTIVE The clock switch bit for the I2C controller. (R/W)

Register 25.17. I2C_SCL_SP_CONF_REG (0x0080)



I2C_SCL_RST_SLV_EN When the master is idle, set this bit to send out SCL pulses. The number of pulses equals to I2C_SCL_RST_SLV_NUM[4:0]. (R/W/SC)

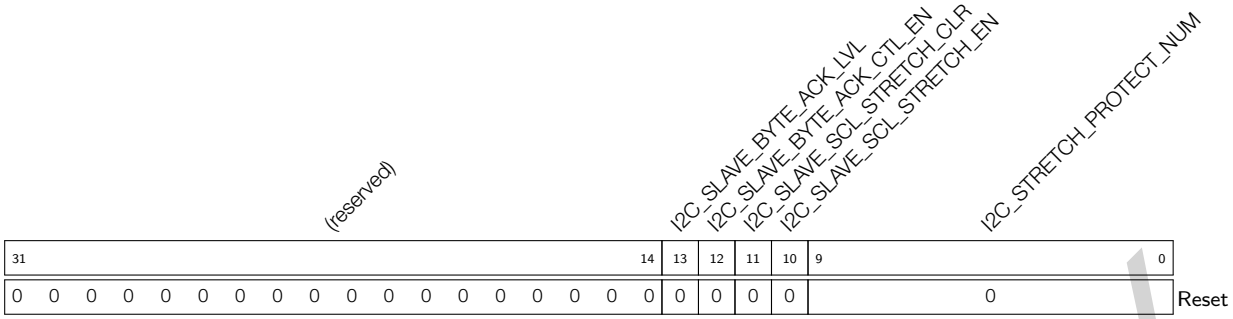
I2C_SCL_RST_SLV_NUM Configures the pulses of SCL generated in master mode. Valid when I2C_SCL_RST_SLV_EN is 1. (R/W)

I2C_SCL_PD_EN The power down enable bit for the I2C output SCL line. 0: Not power down; 1: Power down. Set I2C_SCL_FORCE_OUT and I2C_SCL_PD_EN to 1 to stretch SCL low. (R/W)

I2C_SDA_PD_EN The power down enable bit for the I2C output SDA line. 0: Not power down; 1: Power down. Set I2C_SDA_FORCE_OUT and I2C_SDA_PD_EN to 1 to stretch SDA low. (R/W)

PRELIMINARY

Register 25.18. I2C_SCL_STRETCH_CONF_REG (0x0084)



I2C_STRETCH_PROTECT_NUM Configures the time period to release the SCL line from stretching to avoid timing violation. Usually it should be larger than the SDA steup time. (R/W)

I2C_SLAVE_SCL_STRETCH_EN The enable bit for SCL clock stretching. 0: Disable; 1: Enable. The SCL output line will be stretched low when I2C_SLAVE_SCL_STRETCH_EN is 1 and one of the four stretching events occurs. The cause of stretching can be seen in I2C_STRETCH_CAUSE. (R/W)

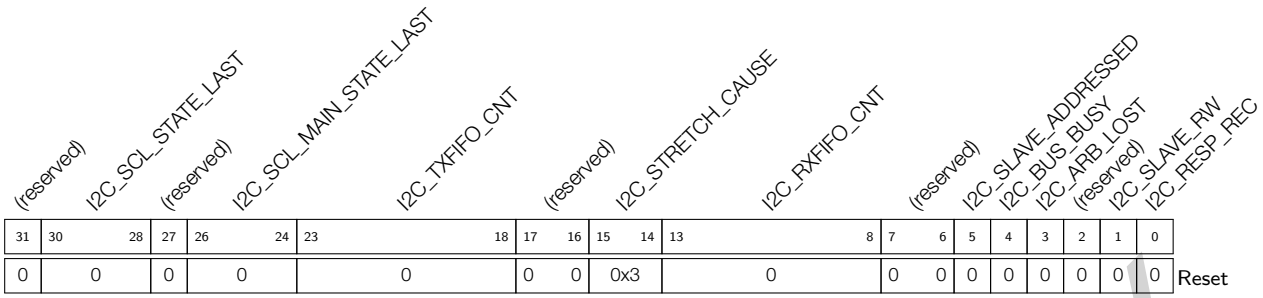
I2C_SLAVE_SCL_STRETCH_CLR Set this bit to clear SCL clock stretching. (WT)

I2C_SLAVE_BYTE_ACK_CTL_EN The enable bit for slave to control the level of the ACK bit. (R/W)

I2C_SLAVE_BYTE_ACK_LVL Set the level of the ACK bit when I2C_SLAVE_BYTE_ACK_CTL_EN is set. (R/W)

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Register 25.19. I2C_SR_REG (0x0008)



I2C_RESP_REC The received ACK value in master mode or slave mode. 0: ACK; 1: NACK. (RO)

I2C_SLAVE_RW When in slave mode, 0: master writes to slave; 1: master reads from slave. (RO)

I2C_ARB_LOST When the I2C controller loses control of the SCL line, this bit changes to 1. (RO)

I2C_BUS_BUSY 0: the I2C bus is in idle state; 1: the I2C bus is busy transferring data. (RO)

I2C_SLAVE_ADDRESSED When the I2C controller is in slave mode, and the address sent by the master matches the address of the slave, this bit is at high level. (RO)

I2C_RXFIFO_CNT This field represents the number of data bytes to be sent. (RO)

I2C_STRETCH_CAUSE The cause of SCL clock stretching in slave mode. 0: stretching SCL low when the master starts to read data; 1: stretching SCL low when TX FIFO is empty in slave mode; 2: stretching SCL low when RX FIFO is full in slave mode. (RO)

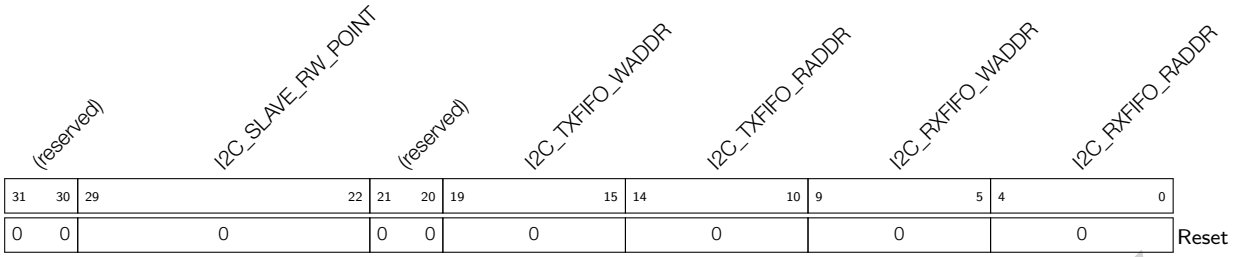
I2C_TXFIFO_CNT This field stores the number of data bytes received in RAM. (RO)

I2C_SCL_MAIN_STATE_LAST This field indicates the status of the state machine. 0: idle; 1: address shift; 2: ACK address; 3: receive data; 4: transmit data; 5: send ACK; 6: wait for ACK. (RO)

I2C_SCL_STATE_LAST This field indicates the status of the state machine used to produce SCL. 0: idle; 1: start; 2: falling edge; 3: low; 4: rising edge; 5: high; 6: stop. (RO)

PRELIMINARY

Register 25.20. I2C_FIFO_ST_REG (0x0014)



I2C_RXFIFO_RADDR This is the offset address of the APB reading from RX FIFO. (RO)

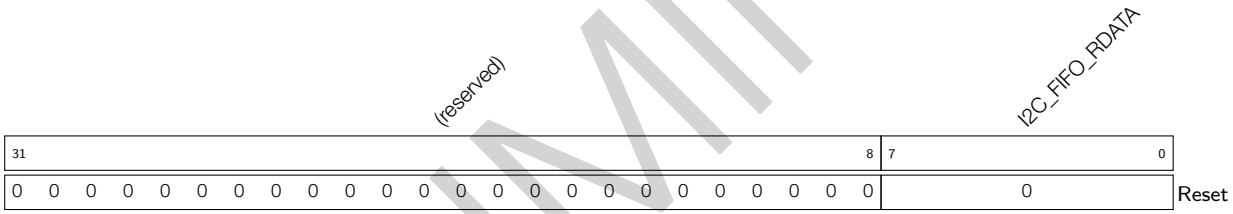
I2C_RXFIFO_WADDR This is the offset address of the I2C controller receiving data and writing to RX FIFO. (RO)

I2C_TXFIFO_RADDR This is the offset address of the I2C controller reading from TX FIFO. (RO)

I2C_TXFIFO_WADDR This is the offset address of APB bus writing to TX FIFO. (RO)

I2C_SLAVE_RW_POINT The received data in I2C slave mode. (RO)

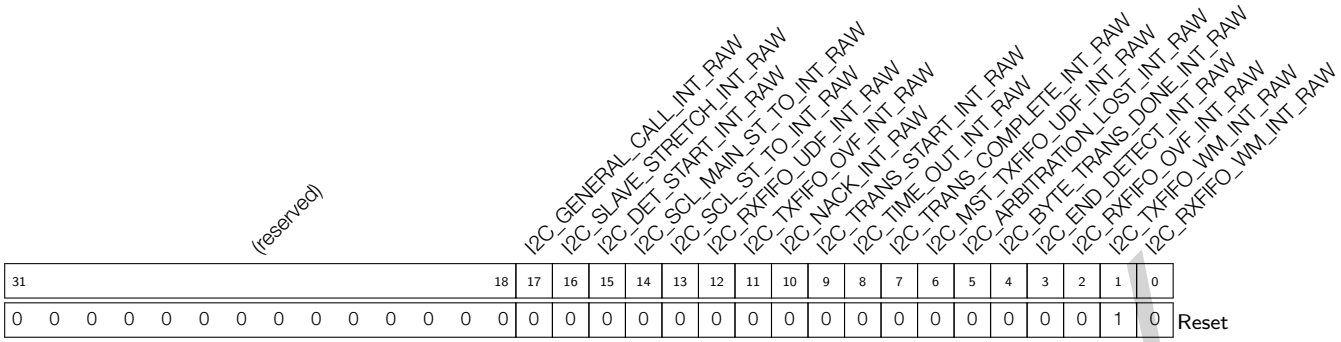
Register 25.21. I2C_DATA_REG (0x001C)



I2C_FIFO_RDATA This field is used to read data from RX FIFO, or write data to TX FIFO. (R/W)

PRELIMINARY

Register 25.22. I2C_INT_RAW_REG (0x0020)



I2C_RXFIFO_WM_INT_RAW The raw interrupt bit for the I2C_RXFIFO_WM_INT interrupt. (R/SS/WTC)

I2C_TXFIFO_WM_INT_RAW The raw interrupt bit for the I2C_TXFIFO_WM_INT interrupt. (R/SS/WTC)

I2C_RXFIFO_OVF_INT_RAW The raw interrupt bit for the I2C_RXFIFO_OVF_INT interrupt. (R/SS/WTC)

I2C_END_DETECT_INT_RAW The raw interrupt bit for the I2C_END_DETECT_INT interrupt. (R/SS/WTC)

I2C_BYTE_TRANS_DONE_INT_RAW The raw interrupt bit for the I2C_END_DETECT_INT interrupt. (R/SS/WTC)

I2C_ARBITRATION_LOST_INT_RAW The raw interrupt bit for the I2C_ARBITRATION_LOST_INT interrupt. (R/SS/WTC)

I2C_MST_TXFIFO_UDF_INT_RAW The raw interrupt bit for the I2C_TRANS_COMPLETE_INT interrupt. (R/SS/WTC)

I2C_TRANS_COMPLETE_INT_RAW The raw interrupt bit for the I2C_TRANS_COMPLETE_INT interrupt. (R/SS/WTC)

I2C_TIME_OUT_INT_RAW The raw interrupt bit for the I2C_TIME_OUT_INT interrupt. (R/SS/WTC)

I2C_TRANS_START_INT_RAW The raw interrupt bit for the I2C_TRANS_START_INT interrupt. (R/SS/WTC)

I2C_NACK_INT_RAW The raw interrupt bit for the I2C_SLAVE_STRETCH_INT interrupt. (R/SS/WTC)

I2C_TXFIFO_OVF_INT_RAW The raw interrupt bit for the I2C_TXFIFO_OVF_INT interrupt. (R/SS/WTC)

I2C_RXFIFO_UDF_INT_RAW The raw interrupt bit for the I2C_RXFIFO_UDF_INT interrupt. (R/SS/WTC)

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PRELIMINARY

Register 25.22. I2C_INT_RAW_REG (0x0020)

Continued from the previous page...

I2C_SCL_ST_TO_INT_RAW The raw interrupt bit for the I2C_SCL_ST_TO_INT interrupt. (R/SS/WTC)

I2C_SCL_MAIN_ST_TO_INT_RAW The raw interrupt bit for the I2C_SCL_MAIN_ST_TO_INT interrupt. (R/SS/WTC)

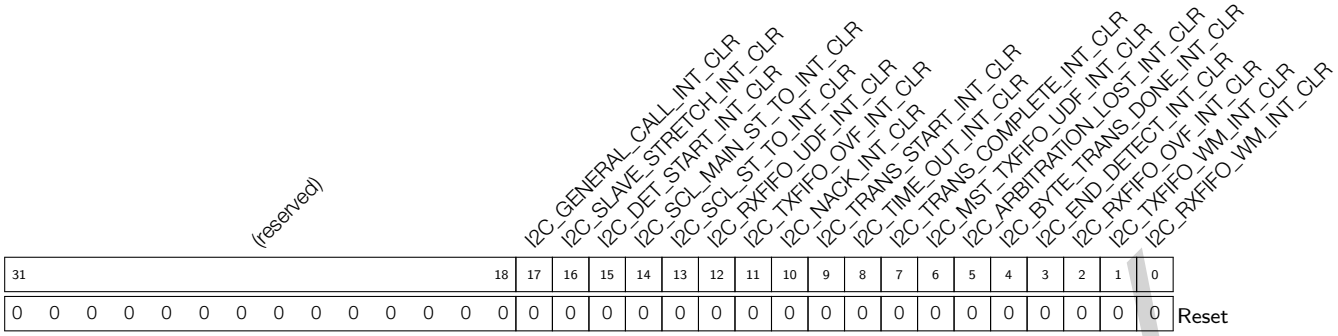
I2C_DET_START_INT_RAW The raw interrupt bit for the I2C_DET_START_INT interrupt. (R/SS/WTC)

I2C_SLAVE_STRETCH_INT_RAW The raw interrupt bit for the I2C_SLAVE_STRETCH_INT interrupt. (R/SS/WTC)

I2C_GENERAL_CALL_INT_RAW The raw interrupt bit for the I2C_GENARAL_CALL_INT interrupt. (R/SS/WTC)

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Register 25.23. I2C_INT_CLR_REG (0x0024)



I2C_RXFIFO_WM_INT_CLR Set this bit to clear the I2C_RXFIFO_WM_INT interrupt. (WT)

I2C_TXFIFO_WM_INT_CLR Set this bit to clear the I2C_TXFIFO_WM_INT interrupt. (WT)

I2C_RXFIFO_OVF_INT_CLR Set this bit to clear the I2C_RXFIFO_OVF_INT interrupt. (WT)

I2C_END_DETECT_INT_CLR Set this bit to clear the I2C_END_DETECT_INT interrupt. (WT)

I2C_BYTE_TRANS_DONE_INT_CLR Set this bit to clear the I2C_END_DETECT_INT interrupt. (WT)

I2C_ARBITRATION_LOST_INT_CLR Set this bit to clear the I2C_ARBITRATION_LOST_INT interrupt. (WT)

I2C_MST_TXFIFO_UDF_INT_CLR Set this bit to clear the I2C_TRANS_COMPLETE_INT interrupt. (WT)

I2C_TRANS_COMPLETE_INT_CLR Set this bit to clear the I2C_TRANS_COMPLETE_INT interrupt. (WT)

I2C_TIME_OUT_INT_CLR Set this bit to clear the I2C_TIME_OUT_INT interrupt. (WT)

I2C_TRANS_START_INT_CLR Set this bit to clear the I2C_TRANS_START_INT interrupt. (WT)

I2C_NACK_INT_CLR Set this bit to clear the I2C_SLAVE_STRETCH_INT interrupt. (WT)

I2C_TXFIFO_OVF_INT_CLR Set this bit to clear the I2C_TXFIFO_OVF_INT interrupt. (WT)

I2C_RXFIFO_UDF_INT_CLR Set this bit to clear the I2C_RXFIFO_UDF_INT interrupt. (WT)

I2C_SCL_ST_TO_INT_CLR Set this bit to clear the I2C_SCL_ST_TO_INT interrupt. (WT)

I2C_SCL_MAIN_ST_TO_INT_CLR Set this bit to clear the I2C_SCL_MAIN_ST_TO_INT interrupt. (WT)

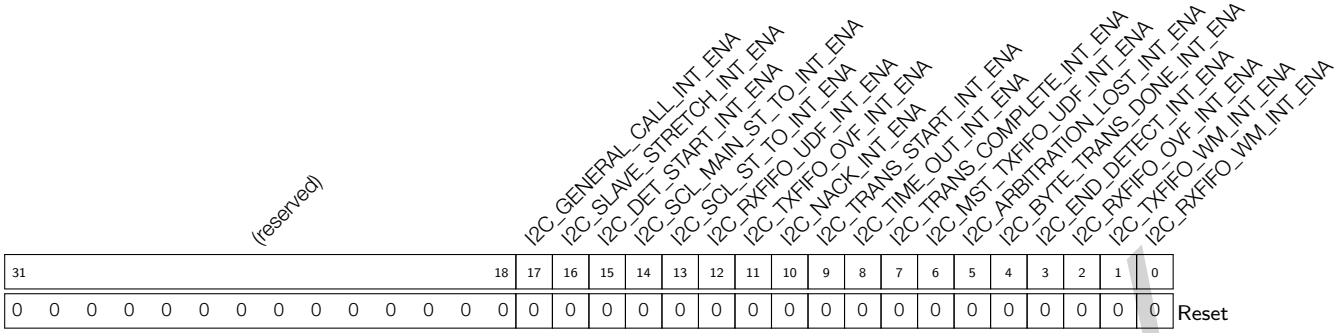
I2C_DET_START_INT_CLR Set this bit to clear the I2C_DET_START_INT interrupt. (WT)

I2C_SLAVE_STRETCH_INT_CLR Set this bit to clear the I2C_SLAVE_STRETCH_INT interrupt. (WT)

I2C_GENERAL_CALL_INT_CLR Set this bit for the I2C_GENARAL_CALL_INT interrupt. (WT)

PRELIMINARY

Register 25.24. I2C_INT_ENA_REG (0x0028)



I2C_RXFIFO_WM_INT_ENA The interrupt enable bit for the I2C_RXFIFO_WM_INT interrupt. (R/W)

I2C_TXFIFO_WM_INT_ENA The interrupt enable bit for the I2C_TXFIFO_WM_INT interrupt. (R/W)

I2C_RXFIFO_OVF_INT_ENA The interrupt enable bit for the I2C_RXFIFO_OVF_INT interrupt. (R/W)

I2C_END_DETECT_INT_ENA The interrupt enable bit for the I2C_END_DETECT_INT interrupt. (R/W)

I2C_BYTE_TRANS_DONE_INT_ENA The interrupt enable bit for the I2C_BYTE_TRANS_DONE_INT interrupt. (R/W)

I2C_ARBITRATION_LOST_INT_ENA The interrupt enable bit for the I2C_ARBITRATION_LOST_INT interrupt. (R/W)

I2C_MST_TXFIFO_UDF_INT_ENA The interrupt enable bit for the I2C_TRANS_COMPLETE_INT interrupt. (R/W)

I2C_TRANS_COMPLETE_INT_ENA The interrupt enable bit for the I2C_TRANS_COMPLETE_INT interrupt. (R/W)

I2C_TIME_OUT_INT_ENA The interrupt enable bit for the I2C_TIME_OUT_INT interrupt. (R/W)

I2C_TRANS_START_INT_ENA The interrupt enable bit for the I2C_TRANS_START_INT interrupt. (R/W)

I2C_NACK_INT_ENA The interrupt enable bit for the I2C_SLAVE_STRETCH_INT interrupt. (R/W)

I2C_TXFIFO_OVF_INT_ENA The interrupt enable bit for the I2C_TXFIFO_OVF_INT interrupt. (R/W)

I2C_RXFIFO_UDF_INT_ENA The interrupt enable bit for the I2C_RXFIFO_UDF_INT interrupt. (R/W)

I2C_SCL_ST_TO_INT_ENA The interrupt enable bit for the I2C_SCL_ST_TO_INT interrupt. (R/W)

I2C_SCL_MAIN_ST_TO_INT_ENA The interrupt enable bit for the I2C_SCL_MAIN_ST_TO_INT interrupt. (R/W)

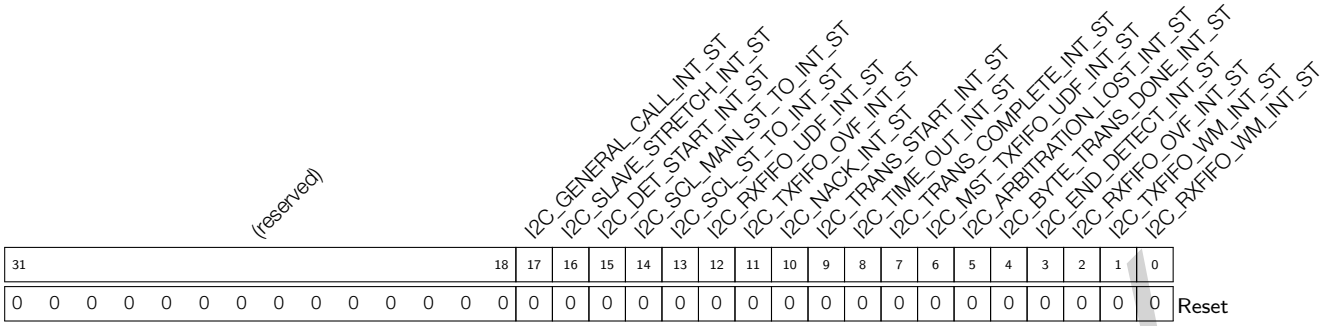
I2C_DET_START_INT_ENA The interrupt enable bit for the I2C_DET_START_INT interrupt. (R/W)

I2C_SLAVE_STRETCH_INT_ENA The interrupt enable bit for the I2C_SLAVE_STRETCH_INT interrupt. (R/W)

I2C_GENERAL_CALL_INT_ENA The interrupt enable bit for the I2C_GENARAL_CALL_INT interrupt. (R/W)

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Register 25.25. I2C_INT_STATUS_REG (0x002C)



I2C_RXFIFO_WM_INT_ST The masked interrupt status bit for the I2C_RXFIFO_WM_INT interrupt. (RO)

I2C_TXFIFO_WM_INT_ST The masked interrupt status bit for the I2C_TXFIFO_WM_INT interrupt. (RO)

I2C_RXFIFO_OVF_INT_ST The masked interrupt status bit for the I2C_RXFIFO_OVF_INT interrupt. (RO)

I2C_END_DETECT_INT_ST The masked interrupt status bit for the I2C_END_DETECT_INT interrupt. (RO)

I2C_BYTE_TRANS_DONE_INT_ST The masked interrupt status bit for the I2C_END_DETECT_INT interrupt. (RO)

I2C_ARBITRATION_LOST_INT_ST The masked interrupt status bit for the I2C_ARBITRATION_LOST_INT interrupt. (RO)

I2C_MST_TXFIFO_UDF_INT_ST The masked interrupt status bit for the I2C_TRANS_COMPLETE_INT interrupt. (RO)

I2C_TRANS_COMPLETE_INT_ST The masked interrupt status bit for the I2C_TRANS_COMPLETE_INT interrupt. (RO)

I2C_TIME_OUT_INT_ST The masked interrupt status bit for the I2C_TIME_OUT_INT interrupt. (RO)

I2C_TRANS_START_INT_ST The masked interrupt status bit for the I2C_TRANS_START_INT interrupt. (RO)

I2C_NACK_INT_ST The masked interrupt status bit for the I2C_SLAVE_STRETCH_INT interrupt. (RO)

I2C_TXFIFO_OVF_INT_ST The masked interrupt status bit for the I2C_TXFIFO_OVF_INT interrupt. (RO)

I2C_RXFIFO_UDF_INT_ST The masked interrupt status bit for the I2C_RXFIFO_UDF_INT interrupt. (RO)

Continued on the next page...

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Register 25.25. I2C_INT_STATUS_REG (0x002C)

Continued from the previous page...

I2C_SCL_ST_TO_INT_ST The masked interrupt status bit for the I2C_SCL_ST_TO_INT interrupt. (RO)

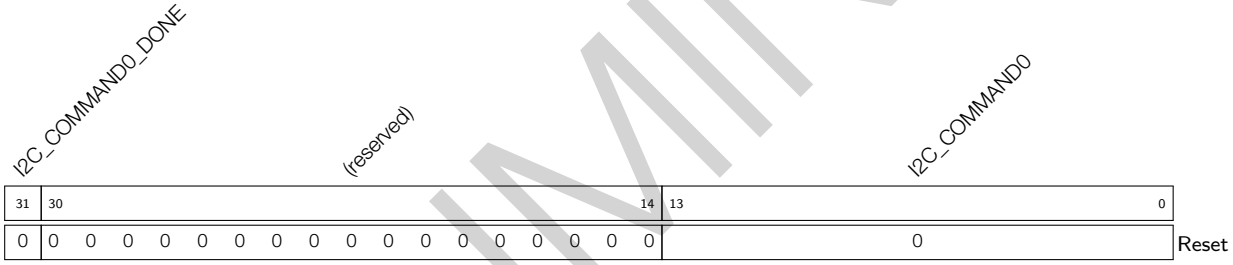
I2C_SCL_MAIN_ST_TO_INT_ST The masked interrupt status bit for the I2C_SCL_MAIN_ST_TO_INT interrupt. (RO)

I2C_DET_START_INT_ST The masked interrupt status bit for the I2C_DET_START_INT interrupt. (RO)

I2C_SLAVE_STRETCH_INT_ST The masked interrupt status bit for the I2C_SLAVE_STRETCH_INT interrupt. (RO)

I2C_GENERAL_CALL_INT_ST The masked interrupt status bit for the I2C_GENARAL_CALL_INT interrupt. (RO)

Register 25.26. I2C_COMD0_REG (0x0058)



I2C_COMMAND0 This is the content of command register 0. It consists of three parts:

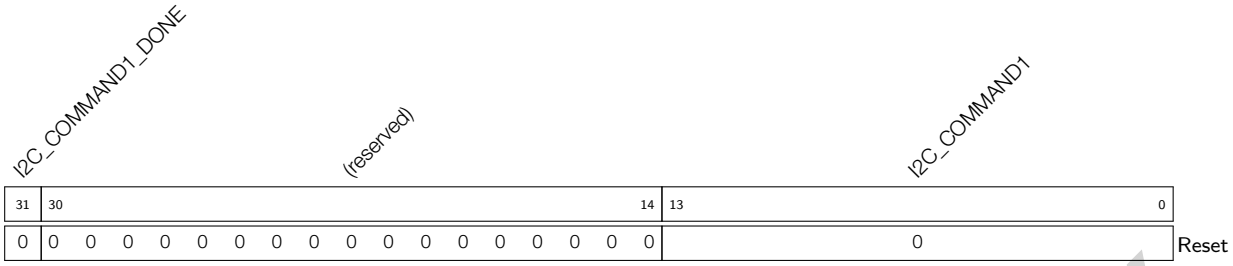
- op_code is the command. 0: RSTART; 1: WRITE; 2: READ; 3: STOP; 4: END.
- Byte_num represents the number of bytes that need to be sent or received.
- ack_check_en, ack_exp and ack are used to control the ACK bit. For more information, see Section 25.4.9.

(R/W)

I2C_COMMAND0_DONE When command 0 has been executed in master mode, this bit changes to high level. (R/W/SS)

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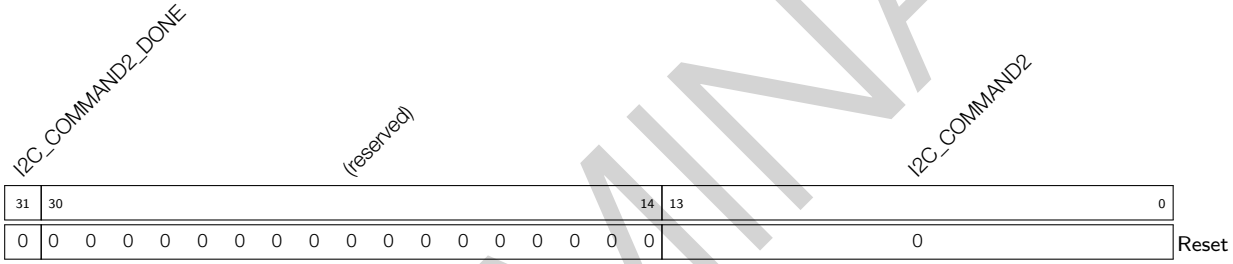
Register 25.27. I2C_COMD1_REG (0x005C)



I2C_COMMAND1 This is the content of command register 1. It is the same as that of I2C_COMMAND0. (R/W)

I2C_COMMAND1_DONE When command 1 has been executed in master mode, this bit changes to high level. (R/W/SS)

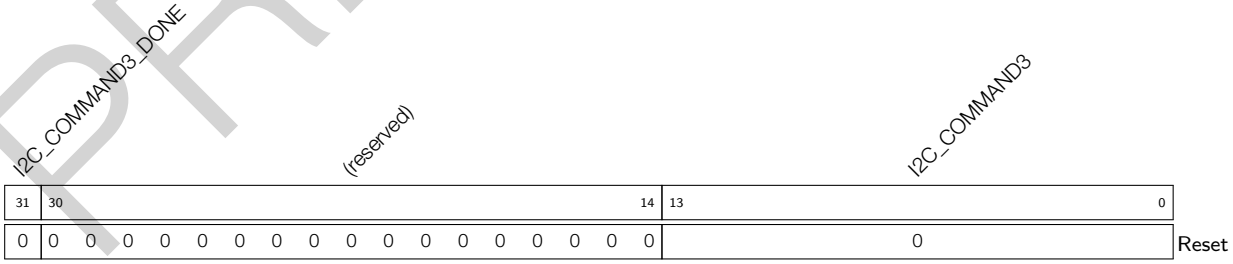
Register 25.28. I2C_COMD2_REG (0x0060)



I2C_COMMAND2 This is the content of command register 2. It is the same as that of I2C_COMMAND0. (R/W)

I2C_COMMAND2_DONE When command 2 has been executed in master mode, this bit changes to high Level. (R/W/SS)

Register 25.29. I2C_COMD3_REG (0x0064)

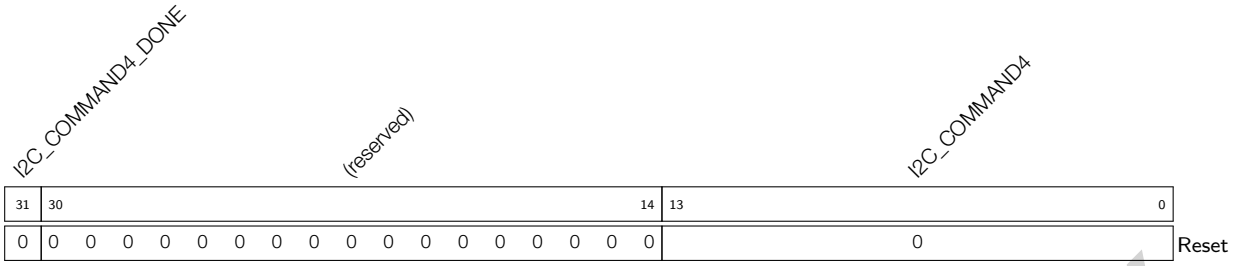


I2C_COMMAND3 This is the content of command register 3. It is the same as that of I2C_COMMAND0. (R/W)

I2C_COMMAND3_DONE When command 3 has been executed in master mode, this bit changes to high level. (R/W/SS)

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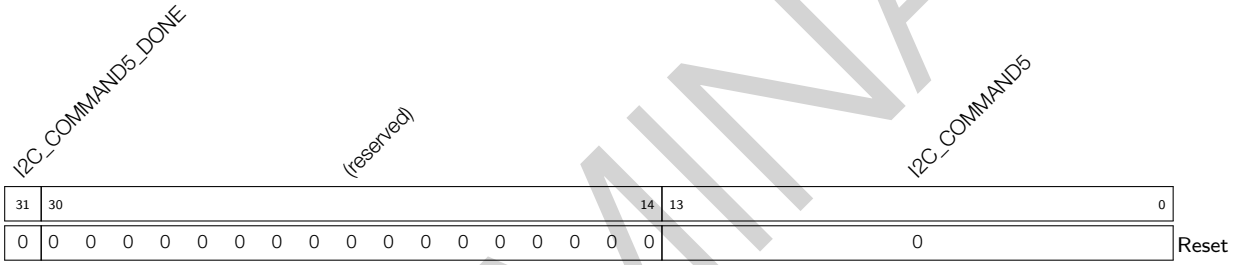
Register 25.30. I2C_COMD4_REG (0x0068)



I2C_COMMAND4 This is the content of command register 4. It is the same as that of I2C_COMMAND0. (R/W)

I2C_COMMAND4_DONE When command 4 has been executed in master mode, this bit changes to high level. (R/W/SS)

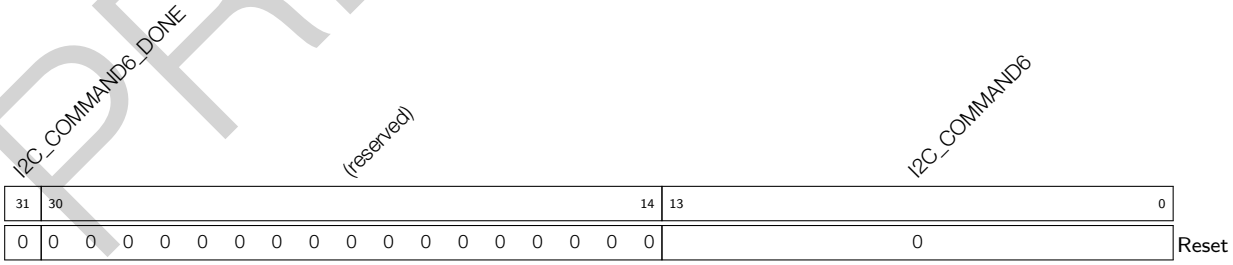
Register 25.31. I2C_COMD5_REG (0x006C)



I2C_COMMAND5 This is the content of command register 5. It is the same as that of I2C_COMMAND0. (R/W)

I2C_COMMAND5_DONE When command 5 has been executed in master mode, this bit changes to high level. (R/W/SS)

Register 25.32. I2C_COMD6_REG (0x0070)

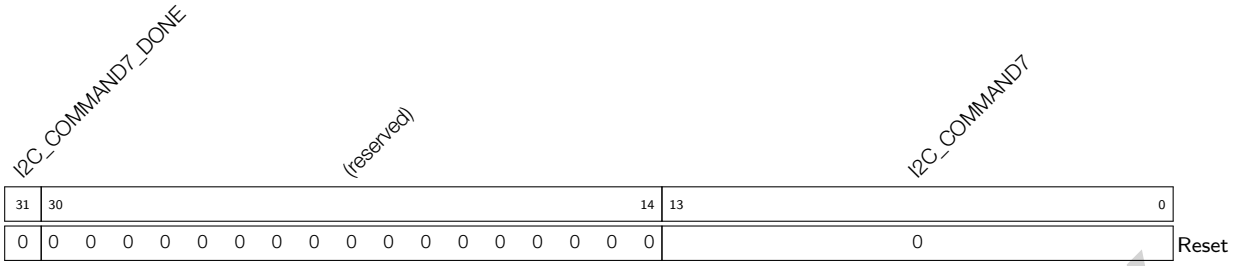


I2C_COMMAND6 This is the content of command register 6. It is the same as that of I2C_COMMAND0. (R/W)

I2C_COMMAND6_DONE When command 6 has been executed in master mode, this bit changes to high level. (R/W/SS)

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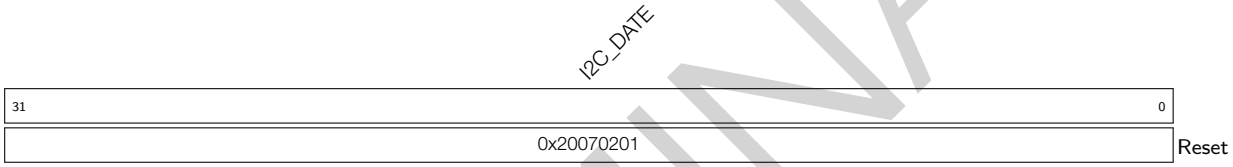
Register 25.33. I2C_COMD7_REG (0x0074)



I2C_COMMAND7 This is the content of command register 7. It is the same as that of I2C_COMMAND0. (R/W)

I2C_COMMAND7_DONE When command 7 has been executed in master mode, this bit changes to high level. (R/W/SS)

Register 25.34. I2C_DATE_REG (0x00F8)



I2C_DATE This is the version control register. (R/W)

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26 LCD and Camera Controller (LCD_CAM)

26.1 Overview

This LCD and Camera (LCD_CAM) controller consists of a LCD module and a camera module. The LCD module is designed to send parallel video data signals, and its bus supports RGB, MOTO6800, and I8080 interface timing. The camera module is designed to receive parallel video data signals, and its bus supports DVP 8-/16-bit modes.

26.2 Features

- Supports the following operation modes:
  - LCD master TX mode
  - Camera slave RX mode
  - Camera master RX mode
- Supports simultaneous connection to an external LCD and an external camera
- When connected with an external LCD, the following is supported:
  - 8-/16-bit parallel output mode
  - RGB, MOTO6800, and I8080 LCD formats
  - LCD data retrieved from internal memory via GDMA
- When connected with an external camera (i.e. DVP image sensor), the following is supported:
  - 8-/16-bit parallel input mode
  - Camera data stored into internal memory via GDMA
- Supports LCD_CAM interface interrupts

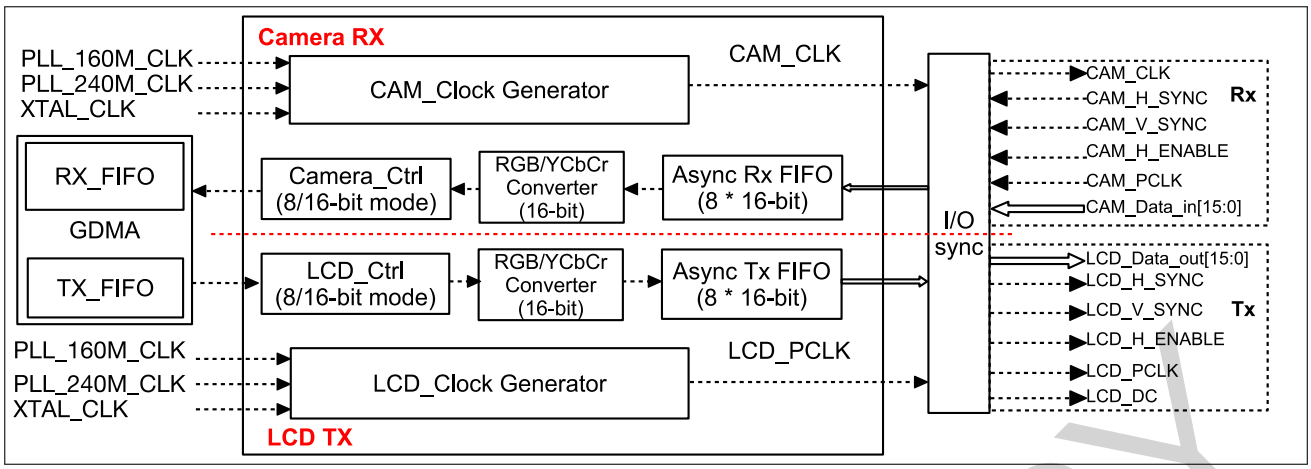
26.3 Functional Description

26.3.1 Block Diagram

Figure 26-1 shows the structure of this LCD_CAM module, including

- 1 x TX control unit (LCD_Ctrl)
- 1 x RX control unit (Camera_Ctrl)
- 1 x asynchronous TX FIFO (Async Tx FIFO) for communicating with external devices
- 1 x asynchronous RX FIFO (Async Rx FIFO) for communicating with external devices
- 2 x clock generators (LCD_Clock Generator and CAM_Clock Generator) for generating the module clocks
- 2 x format converters (RGB/YCbCr Converter) for converting video data into various formats

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- ->: control signal =>: data flow

Figure 26-1. LCD_CAM Block Diagram

26.3.2 Signal Description

Table 26-1. Signal Description

Operation Mode	Signal[1]	Direction	Function
Camera Slave RX Mode	CAM_PCLK	Input	Camera pixel clock signal
	CAM_V_SYNC	Input	Vertical synchronization signal (VSYNC)[3]
	CAM_H_SYNC	Input	Horizontal synchronization signal (HSYNC)[3]
	CAM_H_ENABLE	Input	Horizontal enable signal (DE)[3]
	CAM_Data_in[*N*:0][2]	Input	Camera parallel input data bus, 8-/16-bit supported
Camera Master RX Mode	CAM_PCLK	Input	Camera pixel clock input signal
	CAM_CLK	Output	Camera master clock output signal
	CAM_V_SYNC	Input	Vertical synchronization signal[3]
	CAM_H_SYNC	Input	Horizontal synchronization signal[3]
	CAM_H_ENABLE	Input	Horizontal enable signal[3]
	CAM_Data_in[*N*:0][2]	Input	Camera parallel input data bus, 8-/16-bit supported
LCD Master TX Mode	LCD_PCLK	Output	LCD pixel clock signal
	LCD_H_SYNC	Output	Horizontal synchronization signal in RGB format
	LCD_V_SYNC	Output	Vertical synchronization signal in RGB mode
	LCD_H_ENABLE	Output	Horizontal enable signal in RGB format
	LCD_CD	Output	Command and data (CD) signal in I8080 format
	LCD_CS	Output	Chip select (CS) signal in I8080/MOTO6800 format
	LCD_Data_out[*N*:0][2]	Output	LCD parallel output data bus, 8-/16-bit supported

[1] All signals of LCD_CAM must be mapped to the chip's pin via GPIO matrix. For more information, see Chapter 5 *IO MUX and GPIO Matrix (GPIO, IO MUX)*.

[2] For the input/output signals with 8 or 16 bit width, *N* = 7 or 15 respectively.

[3] If LCD_CAM_CAM_VH_DE_MODE_EN is set, i.e., VSYNC + HSYNC mode is selected, in this mode, the signals of VSYNC, HSYNC and DE are used to control the data. For this case, users need to wire the three signal lines. If LCD_CAM_CAM_VH_DE_MODE_EN is cleared, i.e. DE mode is selected, the signals of VSYNC and DE are used to control the data. For this case, wiring HSYNC signal line is not a must. But in this case, the YUV-RGB conversion function of camera module is not available.

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26.3.3 LCD_CAM Module Clocks

26.3.3.1 LCD Clock

The clocks used in LCD module are generated by LCD_Clock Generator from clock sources, see Figure 26-2.

The clocks include:

- master clock: LCD_CLK, divided from clock sources
- pixel clock: LCD_PCLK, divided from LCD_CLK

The clock source can be one of the following, depending on the configuration of LCD_CAM_LCD_CLK_SEL in register LCD_CAM_LCD_CLOCK_REG:

- 0: disable LCD clock source
- 1: XTAL_CLK
- 2: PLL_240M_CLK
- 3: PLL_160M_CLK

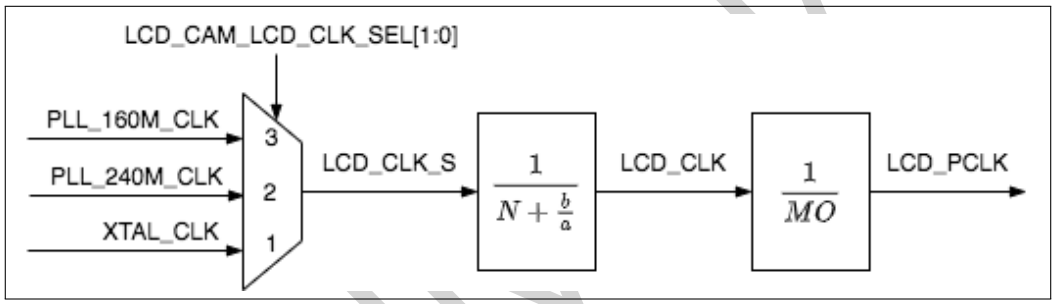


Figure 26-2. LCD Clock

The following formula shows the relation between the frequency of LCD_CLK (f_{LCD_CLK}) and the divider clock source frequency ($f_{LCD\_CLK\_S}$):

$$f_{LCD\_CLK} = \frac{f_{LCD\_CLK\_S}}{N + \frac{b}{a}}$$

N is an integer value between 2 and 256. The value of N corresponds to the value of LCD_CAM_LCD_CLKM_DIV_NUM in register LCD_CAM_LCD_CLOCK_REG as follows:

- When LCD_CAM_LCD_CLKM_DIV_NUM = 0, N = 256.
- When LCD_CAM_LCD_CLKM_DIV_NUM = 1, N = 2.
- When LCD_CAM_LCD_CLKM_DIV_NUM has any other value, N = LCD_CAM_LCD_CLKM_DIV_NUM.

"b" corresponds to the value of LCD_CAM_LCD_CLKM_DIV_B, and "a" to the value of LCD_CAM_LCD_CLKM_DIV_A. For integer divider, LCD_CAM_LCD_CLKM_DIV_A and LCD_CAM_LCD_CLKM_DIV_B are cleared. For fractional divider, the value of LCD_CAM_LCD_CLKM_DIV_B should be less than the value of LCD_CAM_LCD_CLKM_DIV_A.

The following formula shows the relation between the frequencies of LCD_PCLK (f_{LCD_PCLK}) and LCD_CLK (f_{LCD_CLK}):

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$$f_{\text{LCD\_PCLK}} = \frac{f_{\text{LCD\_CLK}}}{\text{MO}}$$

MO is determined by LCD_CAM_LCD_CLK_EQU_SYSCLK and LCD_CAM_LCD_CLKCNT_N.

- When LCD_CAM_LCD_CLK_EQU_SYSCLK = 1, MO = 1.
- When LCD_CAM_LCD_CLK_EQU_SYSCLK = 0, MO = LCD_CAM_LCD_CLKCNT_N + 1.

Notes:

- LCD_CAM_LCD_CLKCNT_N must not be configured as 0.
- Using fractional divider may bring clock jitter. In case that LCD_CLK and LCD_PCLK can not be generated from PLL_160M_CLK by integer divider, PLL_240M_CLK can be used as clock source. For more information, please refer to Chapter 6 *Reset and Clock*.

26.3.3.2 Camera Clock

The clocks used in camera module are generated by CAM_Clock Generator from clock sources, see Figure 26-3.

The clocks include:

- master clock: CAM_CLK, master clock output from camera module, divided from clock sources.
- pixel clock: CAM_CLK, clock input from camera slave.

LCD_CAM_CAM_CLK_SEL in register LCD_CAM_CAM_CTRL_REG is used to select one of the following clock sources for camera module:

- 0: disable camera clock source
- 1: XTAL_CLK
- 2: PLL_240M_CLK
- 3: PLL_160M_CLK

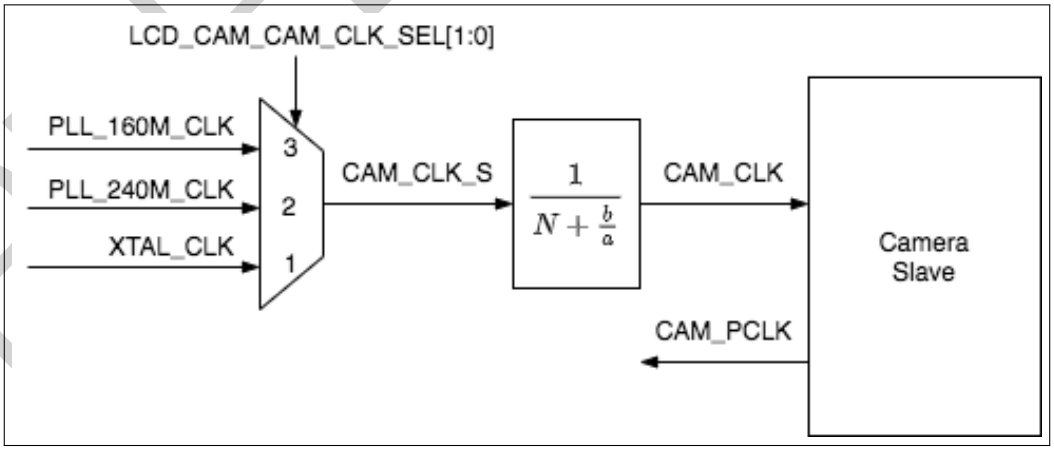


Figure 26-3. Camera Clock

The following formula shows the relation between the frequencies of CAM_CLK ($f_{\text{CAM\_CLK}}$) and the divider clock

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source ($f_{CAM\_CLK\_S}$):

$$f_{CAM\_CLK} = \frac{f_{CAM\_CLK\_S}}{N + \frac{b}{a}}$$

N is an integer value between 2 and 256. The value of N corresponds to the value of LCD_CAM_CAM_CLKM_DIV_NUM in register LCD_CAM_CAM_CTRL_REG as follows:

- When LCD_CAM_CAM_CLKM_DIV_NUM = 0, N = 256.
- When LCD_CAM_CAM_CLKM_DIV_NUM = 1, N = 2.
- When LCD_CAM_CAM_CLKM_DIV_NUM has any other value, N = LCD_CAM_CAM_CLKM_DIV_NUM.

"b" corresponds to the value of LCD_CAM_CAM_CLKM_DIV_B, and "a" to the value of LCD_CAM_CAM_CLKM_DIV_A. For integer divider, LCD_CAM_CAM_CLKM_DIV_A and LCD_CAM_CAM_CLKM_DIV_B are cleared. For fractional divider, the value of LCD_CAM_CAM_CLKM_DIV_B should be less than the value of LCD_CAM_CAM_CLKM_DIV_A.

26.3.4 LCD_CAM Reset

The units in LCD_CAM module can be reset by the following bits:

- LCD_CAM_LCD_RESET: set this bit to reset LCD control unit (LCD_Ctrl) and LCD video data format converter (RGB/YCbCr Converter).
- LCD_CAM_CAM_RESET: set this bit to reset camera control unit (Camera_Ctrl) and camera video data format converter (RGB/YCbCr Converter).
- LCD_CAM_LCD_AFIFO_RESET: set this bit to reset Async Tx FIFO.
- LCD_CAM_CAM_AFIFO_RESET: set this bit to reset Async Rx FIFO.

Notes:

- The above-mentioned reset bits are hardware self-clearing, i.e., the hardware automatically clears these bits once 1 is written.
- LCD/camera module clock must be configured first before the module and FIFO are reset.

26.3.5 LCD_CAM Data Format Control

26.3.5.1 LCD Data Format Control

When the LCD module is used to send data, the bit/byte order of the data from DMA can be adjusted by configuring

- LCD_CAM_LCD_2BYTE_EN
  - 1: LCD output data is in 16-bit mode.
  - 0: LCD output data is in 8-bit mode.
- LCD_CAM_LCD_BIT_ORDER
  - 1: Change data bit order.
    - Change LCD_DATA_out[7:0] to LCD_DATA_out[0:7] in 8-bit mode.
    - Change LCD_DATA_out[15:0] to LCD_DATA_out[0:15] in 16-bit mode.

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  - 0: Do not change the bit order.

- LCD_CAM_LCD_BYTE_ORDER
  - 1: Invert data byte order, only valid in 16-bit mode.
  - 0: Do not invert.
- LCD_CAM_LCD_8BITS_ORDER
  - 1: Swap every two data bytes, valid in 8-bit mode
  - 0: Do not swap.

For the detailed configuration, see Table 26-2.

Table 26-2. LCD Data Format Control

Data from DMA[1]	LCD_CAM_LCD_2BYTE_EN	LCD_CAM_LCD_BIT_ORDER	LCD_CAM_LCD_BYTE_ORDER[2]	LCD_CAM_LCD_8BITS_ORDER[2]	TX Data[3,4]
B0,B1,B2,B3	0	0	0	0	{B0}{B1}{B2}{B3}
			0	1	{B1}{B0}{B3}{B2}
		1	0	0	{B0'}{B1'}{B2'}{B3'}
			0	1	{B1'}{B0'}{B3'}{B2'}
	1	0	0	0	{B1,B0}{B3,B2}
			1	0	{B0,B1}{B2,B3}
		1	0	0	{B1',B0'}{B3',B2'}
			1	0	{B0',B1'}{B2',B3'}

[1] B0 ~ B3 represent the bytes of the data from DMA, from low address to high address.

[2] Only the configuration listed in the table is valid. Other configuration may cause unexpected data errors.

[3] In TX data, the bits in {} are in big-endian, and are in parallel with each other, while the data of {} is in serial with the data of other {}. Data is sent out from left to right. Take {B0}{B1}{B2}{B3} as an example. The bits in {B0} are in parallel with each other, but are in serial with the bits in {B1}{B2}{B3}. {B0} is sent out first.

[4] In TX data, Bn'[7:0] = Bn[0:7] (n = 0,1,2,3).

Note:
If only one byte of data is sent out each time, LCD_Data_out[7:0] is valid, while LCD_Data_out[15:8] is invalid.

26.3.5.2 Camera Data Format Control

When the camera module is used to receive data, the bit/byte order of the data to DMA can be adjusted by configuring

- LCD_CAM_CAM_2BYTE_EN
  - 1: Camera input data is in 16-bit mode.
  - 0: Camera input data is in 8-bit mode.
- LCD_CAM_CAM_BIT_ORDER
  - 1: Change data bit order.

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  * Change CAM_DATA_in[7:0] to CAM_DATA_in[0:7] in 8-bit mode.
  * Change CAM_DATA_in[15:0] to CAM_DATA_in[0:15] in 16-bit mode.
- 0: Do not change the bit order.

- LCD_CAM_CAM_BYTE_ORDER
  - 1: Invert data byte order, only valid in 16-bit mode.
  - 0: Do not invert.

For the detailed configuration, see Table 26-3.

Table 26-3. CAM Data Format Control

RX Data[1]	LCD_CAM_CAM_2BYTE_EN	LCD_CAM_CAM_BIT_ORDER[2]	LCD_CAM_CAM_BYTE_ORDER[2]	Data to DMA[3,4]
{B0}{B1}{B2}{B3}	0	0	0	B0,B1,B2,B3
		1	0	B0',B1',B2',B3'
{B1,B0}{B3,B2}	1	0	0	B0,B1,B2,B3
			1	B1,B0,B3,B2
		1	0	B0',B1',B2',B3'
			1	B1',B0',B3',B2'

[1] In RX data, the bits in {} are in big-endian, and are in parallel with each other, while the data of {} is in serial with the data of other {}. Data is received from left to right. Take {B0}{B1}{B2}{B3} as an example. The bits in {B0} are in parallel with each other, but are in serial with the bits in {B1}{B2}{B3}. {B1} is received first.

[2] Only the configuration listed in the table is valid. Other configuration may cause unexpected data errors.

[3] B0 ~ B3 represent the bytes of the data to DMA, from low address to high address.

[4] In the data to DMA, Bn'[7:0] = Bn[0:7] (n = 0,1,2,3).

Note:
If only one byte is received each time, CAM_Data_in[7:0] is valid data. For such case, users must connect CAM_Data_in[7:0] with the master.

26.3.6 YUV-RGB Data Format Conversion

The LCD_CAM module supports data format conversion among YUV and RGB. LCD module and camera module each has a data format converter. The converter supports format conversion over:

- BT601 and BT709 standards
- RGB565 (full/limited range) and YUV422/420/411 (full/limited range) formats
- YUV422/420/411 (full/limited range) formats

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26.3.6.1 YUV Timing

In LCD_CAM module, assume that there are 8 pixels to be transmitted, corresponding to YUV data [Y_i, U_i, V_i] (i = 1 ~ 8). Then:

- in YUV422 mode, the LCD sends (or the camera receives) the data as follows:

Y_1	U_1	Y_2	V_2	Y_3	U_3	Y_4	V_4	Y_5	U_5	Y_6	V_6	Y_7	U_7	Y_8	V_8

- in YUV420 mode, the LCD sends (or the camera receives) the data as follows:

Y_1	U_1	Y_2	Y_3	U_3	Y_4	Y_5	V_5	Y_6	Y_7	V_7	Y_8

- in YUV411 mode, the LCD sends (or the camera receives) the data as follows:

Y_1	U_1	Y_2	Y_3	V_3	Y_4	Y_5	U_5	Y_6	Y_7	V_7	Y_8

26.3.6.2 Data Conversion Configuration

The configuration for format converter in camera module is identical to that in LCD module. Therefore, the configuration process is illustrated below using the format conversion in LCD module as an example:

- Enable YUV-RGB format converter by setting LCD_CAM_LCD_CONV_BYPASS.
- Configure the data transfer mode by configuring LCD_CAM_LCD_CONV_MODE_8BITS_ON:
  - 0: use 16-bit data transfer mode
  - 1: use 8-bit data transfer mode
- Select the standard by configuring LCD_CAM_LCD_CONV_PROTOCOL_MODE:
  - 0: use BT601 standard
  - 1: use BT709 standard
- Configure the conversion mode:

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Table 26-4. Conversion Mode Control

Conversion Mode	TRANS_MODE[1]	YUV_MODE[2]	YUV2YUV_MODE[3]
RGB565 -> YUV422	1	0	3
RGB565 -> YUV420	1	1	3
RGB565 -> YUV411	1	2	3
YUV422 -> RGB565	0	0	3
YUV420 -> RGB565	0	1	3
YUV411 -> RGB565	0	2	3
YUV422 -> YUV420	1	0	1
YUV422 -> YUV411	1	0	2
YUV420 -> YUV422	1	1	0
YUV420 -> YUV411	1	1	2
YUV411 -> YUV422	1	2	0
YUV411 -> YUV420	1	2	1

[1] The value of LCD_CAM_LCD_CONV_TRANS_MODE

[2] The value of LCD_CAM_LCD_CONV_YUV_MODE

[3] The value of LCD_CAM_LCD_CONV_YUV2YUV_MODE

- Configure the color range for input data by configuring LCD_CAM_LCD_CONV_DATA_IN_MODE:
  - 1: full color range[1]
  - 0: limited color range[2]
- Configure the color range for output data by configuring LCD_CAM_LCD_CONV_DATA_OUT_MODE:
  - 0: limited color range
  - 1: full color range

Note:

1. If full color range is selected, the color range of RGB or YUV is 0 ~ 255.
2. If limited color range is selected,
   - the color range of RGB is: 16 ~ 240.
   - the color range of YUV is:
     - Y: 16 ~ 240.
     - U-V: 16 ~ 235.

26.4 Software Configuration Process

Note:

Updating the register configuration described in LCD module or camera module requires to set LCD_CAM_LCD_UPDATE and LCD_CAM_CAM_UPDATE, respectively, to synchronize registers from APB clock domain to LCD/camera clock domain. For more detailed configuration, see the configuration examples below.

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26.4.1 Configure LCD (RGB Format) as TX Mode

Follow the steps below to configure LCD (RGB format) as TX mode via software:

1. Configure clock according to Section 26.3.3.
2. Configure signal pins according to Table 26-1.
3. Enable corresponding interrupts, see Section 26.5.
4. Enable RGB format by setting LCD_CAM_LCD_RGB_MODE_EN.
5. Configure frame format by the following registers. See the figures below.
   - LCD_CAM_LCD_VT_HEIGHT
   - LCD_CAM_LCD_VA_HEIGHT
   - LCD_CAM_LCD_HB_FRONT
   - LCD_CAM_LCD_HT_WIDTH
   - LCD_CAM_LCD_HA_WIDTH
   - LCD_CAM_VB_FRONT
   - LCD_CAM_LCD_VSYNC_WIDTH

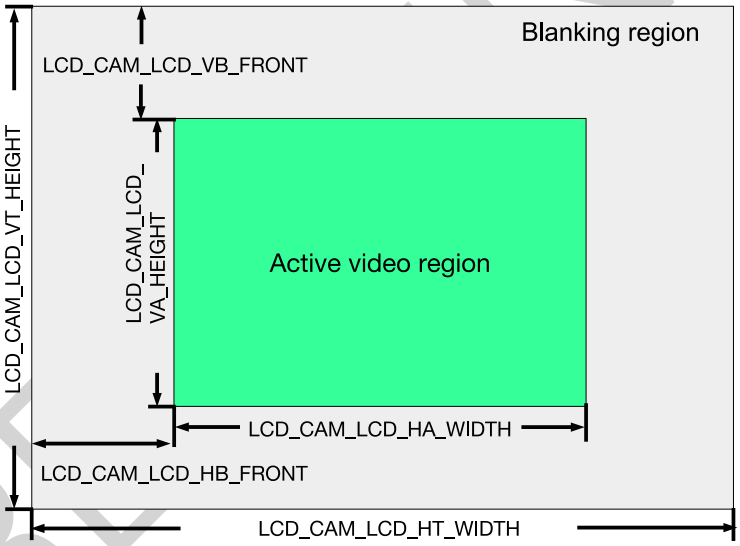


Figure 26-4. LCD Frame Structure

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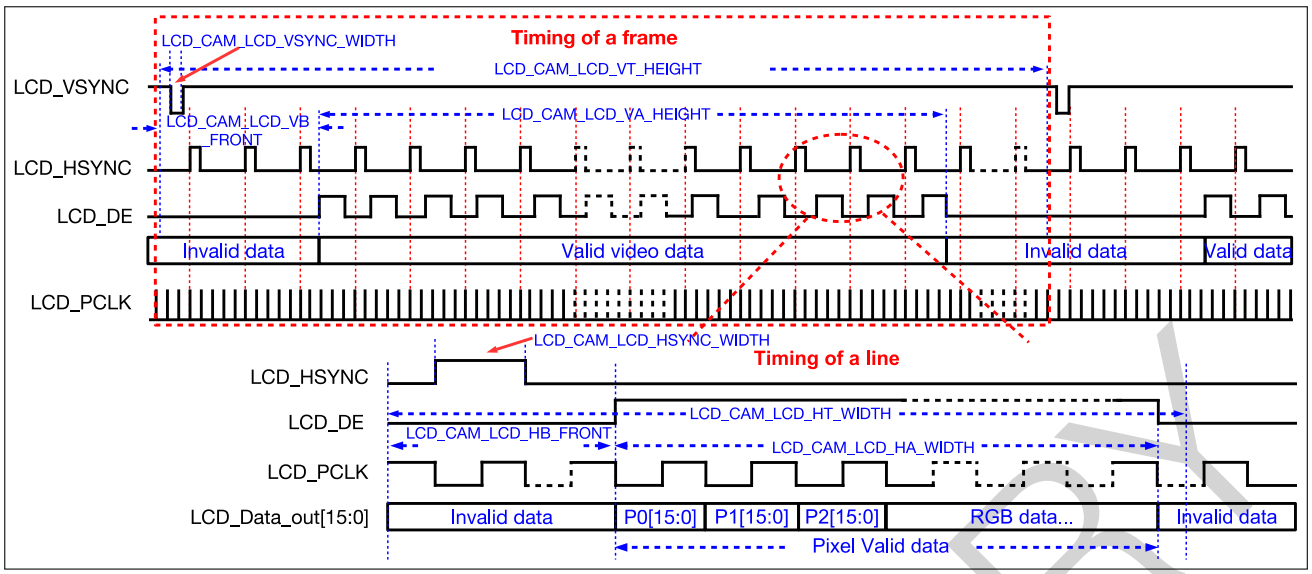


Figure 26-5. LCD Timing (RGB Format)

Note:

When configuring the parameters shown in the figures above, please note that the parameter is equal to the register value + 1. For example, if the expected VSYNC width is 1, then please configure LCD_CAM_LCD_VSYNC_WIDTH to 0. For more information, see the register description.

6. Set LCD_CAM_LCD_UPDATE.
7. Reset TX control unit (LCD_Ctrl) and Async Tx FIFO as described in Section 26.3.4.
8. Configure GDMA outlink.
9. Start transmitting data:
   - wait till LCD slave gets ready.
   - then set LCD_CAM_LCD_START to start transmitting data.
10. Wait for the interrupt signals set in Step 3.
11. In frame intervals during data transmitting, check if the bit LCD_CAM_LCD_NEXT_FRAME_EN is set:
    - If yes, set LCD_CAM_LCD_UPDATE (repeating the steps above) to continue transmitting next frame.
    - If not, LCD stops transmitting data.
12. Clear LCD_CAM_LCD_START if data transmission is done.

26.4.2 Configure LCD (I8080/MOTO6800 Format) as TX Mode

Figure 26-6 shows the LCD timing sequence in I8080 format.

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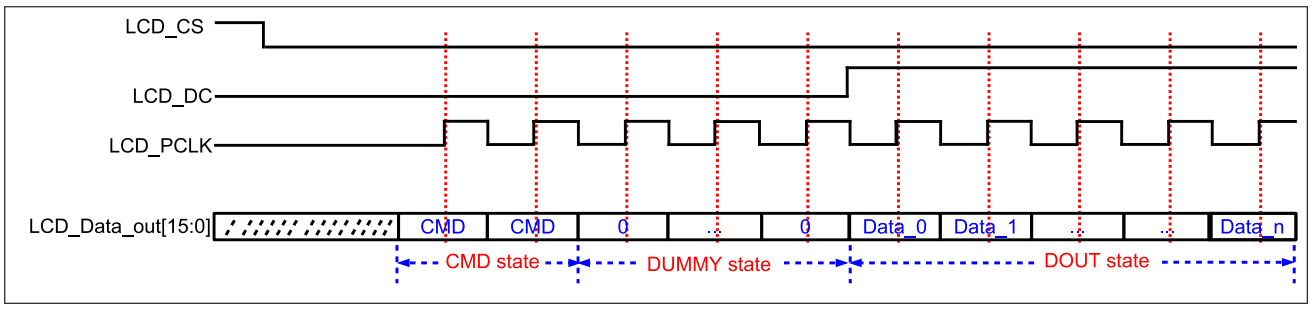


Figure 26-6. LCD Timing (I8080 Format)

Follow the steps below to configure LCD (I8080 format) as TX mode via software:

1. Configure clock according to Section 26.3.3.
2. Configure signal pins according to Table 26-1.
3. Enable corresponding interrupts, see Section 26.5.
4. Clear LCD_CAM_LCD_RGB_MODE_EN.
5. Configure CMD phase by LCD_CAM_LCD_CMD, LCD_CAM_LCD_CMD_2_CYCLE_EN, and LCD_CAM_LCD_CMD_VALUE.
6. Configure DUMMY phase by LCD_CAM_LCD_DUMMY and LCD_CAM_LCD_DUMMY_CYCLELEN.
7. Configure DOUT phase by LCD_CAM_LCD_DOUT, depending on the output mode:
   - In a fixed-length output[a], configure data length in LCD_CAM_LCD_DOUT_CYCLELEN.
   - In a continuous output[b], set LCD_CAM_LCD_ALWAYS_OUT_EN. Users do not need to configure LCD_CAM_LCD_DOUT_CYCLELEN.

   Note:

   (a) In a fixed-length output, the LCD module stops sending data once the data length reaches the value set in LCD_CAM_LCD_DOUT_CYCLELEN.

   (b) In a continuous output, LCD module keeps sending data till:

   i. LCD_CAM_LCD_START is cleared;

   ii. or LCD_CAM_LCD_RESET is set;

   iii. or all the data in GDMA is sent out.
8. Configure the CD signal mode, including the default value of the CD signal and the values at each phase, see the description of LCD_CAM_LCD_MISC_REG.
9. Set LCD_CAM_LCD_UPDATE.
10. Reset TX control unit (LCD_Ctrl) and Async Tx FIFO as described in Section 26.3.4.
11. Configure GDMA outlink.
12. Start transmitting data:
    - wait till LCD slave gets ready.

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- then set LCD_CAM_LCD_START to start transmitting data.

13. Wait for the interrupt signals set in Step 3.
14. Clear LCD_CAM_LCD_START if data transmission is done.

Notes:

No matter in which format, RGB or I8080/MOTO6800, the rules below must be followed when accessing internal memory via GDMA:

- If LCD data bus is configured to 8-bit parallel output mode, then
  - pixel clock frequency must be less than 80 MHz.
  - if YUV-RGB format conversion is used meanwhile, the pixel clock frequency must be less than 60 MHz.
- If LCD data bus is configured to 16-bit parallel output mode, then
  - pixel clock frequency must be less than 40 MHz.
  - if YUV-RGB format conversion is used meanwhile, the pixel clock frequency must be less than 30 MHz.

26.4.3 Configure Camera as RX Mode

Follow the steps below to configure camera as RX mode via software:

1. Configure clock according to Section 26.3.3. Note that in slave mode, the module clock frequency should be two times faster than the PCLK frequency of the image sensor.
2. Configure signal pins according to Table 26-1.
3. Set or clear LCD_CAM_CAM_VH_DE_MODE_EN according to the control signal HSYNC.
4. Set needed RX channel mode and RX data mode, then set the bit LCD_CAM_CAM_UPDATE.
5. Reset RX control unit (Camera_Ctrl) and Async Rx FIFO as described in Section 26.3.4.
6. Enable corresponding interrupts, see Section 26.5.
7. Configure GDMA inlink, and set the length of RX data in LCD_CAM_CAM_REC_DATA_BYTELEN.
8. Start receiving data:
   - In master mode, when the slave is ready, set LCD_CAM_CAM_START to start receiving data.
   - In slave mode, set LCD_CAM_CAM_START. Receiving data starts after the master provides clock signal and control signal.
9. Receive data and store the data to the specified address of ESP32-S3 memory. Then corresponding interrupts set in Step 6 will be generated.

Notes:

- No matter in which operation mode, camera master RX mode or camera slave RX mode, the rules below must be followed when accessing internal memory via GDMA:
  - If 8-bit parallel data input mode is selected, then
    - pixel clock frequency must be less than 80 MHz.

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    * if YUV-RGB format conversion is used meanwhile, the pixel clock frequency must be less than 60 MHz.
  - If 16-bit parallel data input mode is selected, then
    * pixel clock frequency must be less than 40 MHz.
    * if YUV-RGB format conversion is used meanwhile, the pixel clock frequency must be less than 30 MHz.
- If an external camera and an external LCD are connected simultaneously, ensure that the maximum data throughput on the interface is less than GDMA total data bandwidth of 80 MB/s. Note the default frequency of APB_CLK is 80 MHz here. For more information, see Chapter 6 *Reset and Clock*.

26.5 LCD_CAM Interrupts

- LCD_CAM_CAM_HS_INT: triggered when the total number of received lines by camera is greater than or equal to LCD_CAM_CAM_LINE_INT_NUM + 1.
- LCD_CAM_CAM_VSYNC_INT: triggered when the camera received a VSYNC signal.
- LCD_CAM_LCD_TRANS_DONE_INT: triggered when the LCD transmitted all the data.
- LCD_CAM_LCD_VSYNC_INT: triggered when the LCD transmitted a VSYNC signal.

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26.6 Register Summary

The addresses in this section are relative to LCD_CAM controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

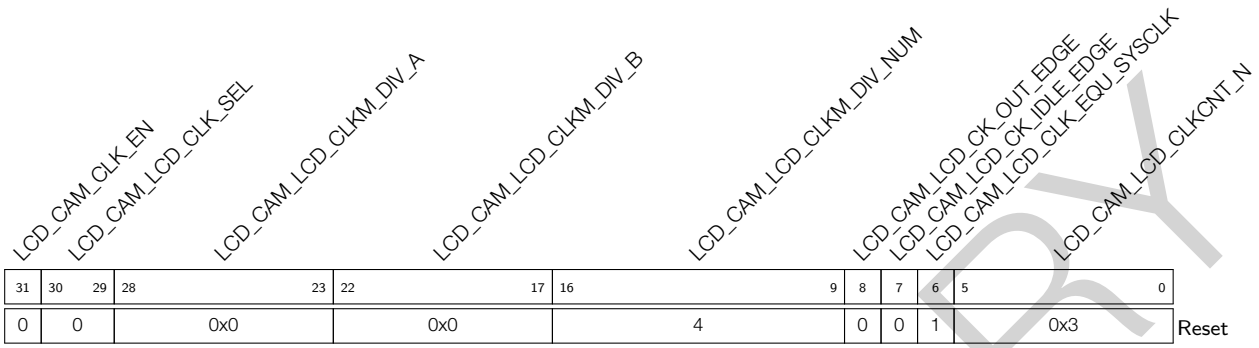
Name	Description	Address	Access
LCD configuration registers			
LCD_CAM_LCD_CLOCK_REG	LCD clock configuration register	0x0000	R/W
LCD_CAM_LCD_RGB_YUV_REG	LCD data format conversion register	0x0010	R/W
LCD_CAM_LCD_USER_REG	LCD user configuration register	0x0014	varies
LCD_CAM_LCD_MISC_REG	LCD MISC configuration register	0x0018	varies
LCD_CAM_LCD_CTRL_REG	LCD signal configuration register	0x001C	R/W
LCD_CAM_LCD_CTRL1_REG	LCD signal configuration register 1	0x0020	R/W
LCD_CAM_LCD_CTRL2_REG	LCD signal configuration register 2	0x0024	R/W
LCD_CAM_LCD_CMD_VAL_REG	LCD command value configuration register	0x0028	R/W
LCD_CAM_LCD_DLY_MODE_REG	LCD signal delay configuration register	0x0030	R/W
LCD_CAM_LCD_DATA_DOUT_MODE_REG	LCD data delay configuration register	0x0038	R/W
Camera configuration registers			
LCD_CAM_CAM_CTRL_REG	Camera clock configuration register	0x0004	R/W
LCD_CAM_CAM_CTRL1_REG	Camera control register	0x0008	varies
LCD_CAM_CAM_RGB_YUV_REG	Camera data format conversion register	0x000C	R/W
Interrupt registers			
LCD_CAM_LC_DMA_INT_ENA_REG	LCD_CAM GDMA interrupt enable register	0x0064	R/W
LCD_CAM_LC_DMA_INT_RAW_REG	LCD_CAM GDMA raw interrupt status register	0x0068	RO
LCD_CAM_LC_DMA_INT_ST_REG	LCD_CAM GDMA masked interrupt status register	0x006C	RO
LCD_CAM_LC_DMA_INT_CLR_REG	LCD_CAM GDMA interrupt clear register	0x0070	WO
Version register			
LCD_CAM_LC_REG_DATE_REG	Version control register	0x00FC	R/W

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26.7 Registers

The addresses in this section are relative to LCD_CAM controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 26.1. LCD_CAM_LCD_CLOCK_REG (0x0000)



LCD_CAM_LCD_CLKCNT_N $f_{LCD\_PCLK} = f_{LCD\_CLK}/$(LCD_CAM_LCD_CLKCNT_N + 1) when LCD_CAM_LCD_CLK_EQU_SYSCLK is 0. Note: this field must not be configured to 0. (R/W)

LCD_CAM_LCD_CLK_EQU_SYSCLK 1: $f_{LCD\_PCLK} = f_{LCD\_CLK}$. 0: $f_{LCD\_PCLK} = f_{LCD\_CLK}/$(LCD_CAM_LCD_CLKCNT_N + 1). (R/W)

LCD_CAM_LCD_CK_IDLE_EDGE 1: LCD_PCLK line is high in idle. 0: LCD_PCLK line is low in idle. (R/W)

LCD_CAM_LCD_CK_OUT_EDGE 1: LCD_PCLK is high in the first half clock cycle. 0: LCD_PCLK is low in the first half clock cycle. (R/W)

LCD_CAM_LCD_CLKM_DIV_NUM Integral LCD clock divider value. (R/W)

LCD_CAM_LCD_CLKM_DIV_B Fractional clock divider numerator value. (R/W)

LCD_CAM_LCD_CLKM_DIV_A Fractional clock divider denominator value. (R/W)

LCD_CAM_LCD_CLK_SEL Select LCD module source clock. 0: clock source is disabled. 1: XTAL_CLK. 2: PLL_240M_CLK. 3: PLL_160M_CLK. (R/W)

LCD_CAM_CLK_EN Set this bit to force enable the clock for all configuration registers. Clock gate is not used. (R/W)

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Register 26.2. LCD_CAM_LCD_RGB_YUV_REG (0x0010)

31	30	29	28	27	26	25 24	23 22	21	20	19 … 0	
LCD_CAM_LCD_CONV_BYPASS	LCD_CAM_LCD_CONV_TRANS_MODE	LCD_CAM_LCD_CONV_MODE_8BITS_ON	LCD_CAM_LCD_CONV_DATA_IN_MODE	LCD_CAM_LCD_CONV_DATA_OUT_MODE	LCD_CAM_LCD_CONV_PROTOCOL_MODE	LCD_CAM_LCD_CONV_YUV_MODE	LCD_CAM_LCD_CONV_YUV2YUV_MODE	(reserved)	LCD_CAM_LCD_CONV_8BITS_DATA_INV	(reserved)	
0	0	0	0	0	0	0	3	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Reset

LCD_CAM_LCD_CONV_8BITS_DATA_INV Swap every two 8-bit input data. 1: Enabled. 0: Disabled. (R/W)

LCD_CAM_LCD_CONV_YUV2YUV_MODE In YUV-to-YUV mode, 0: data is converted to YUV422 format. 1: data is converted to YUV420 format. 2: data is converted to YUV411 format. 3: disabled. To enable YUV-to-YUV mode, LCD_CAM_LCD_CONV_TRANS_MODE must be set to 1. (R/W)

LCD_CAM_LCD_CONV_YUV_MODE In YUV-to-YUV mode and YUV-to-RGB mode, LCD_CAM_LCD_CONV_YUV_MODE decides the YUV mode of input data. 0: input data is in YUV422 format. 1: input data is in YUV420 format. 2: input data is in YUV411 format. In RGB-to-YUV mode, 0: data is converted to YUV422 format. 1: data is converted to YUV420 format. 2: data is converted to YUV411 format. (R/W)

LCD_CAM_LCD_CONV_PROTOCOL_MODE 0: BT601. 1: BT709. (R/W)

LCD_CAM_LCD_CONV_DATA_OUT_MODE Configure color range for output data. 0: limited color range. 1: full color range. (R/W)

LCD_CAM_LCD_CONV_DATA_IN_MODE Configure color range for input data. 0: limited color range. 1: full color range. (R/W)

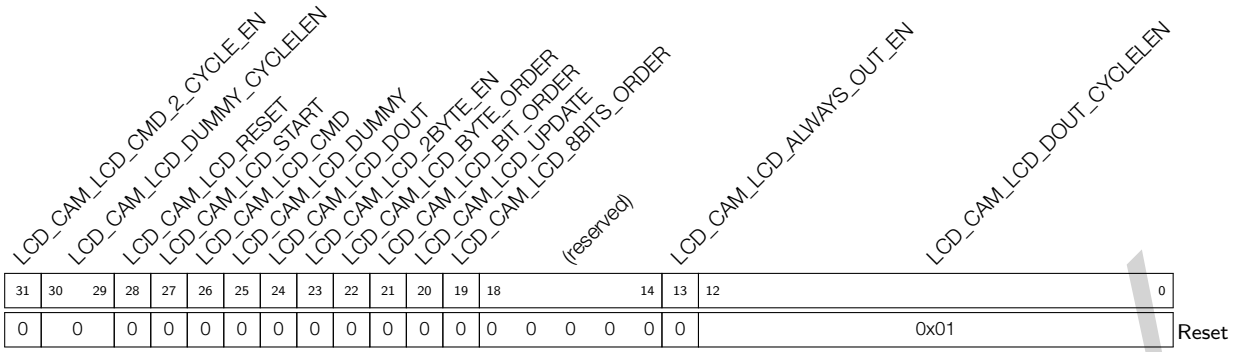
LCD_CAM_LCD_CONV_MODE_8BITS_ON 0: 16-bit mode. 1: 8-bit mode. (R/W)

LCD_CAM_LCD_CONV_TRANS_MODE 0: converted to RGB format. 1: converted to YUV format. (R/W)

LCD_CAM_LCD_CONV_BYPASS 0: Bypass converter. 1: Enable converter. (R/W)

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Register 26.3. LCD_CAM_LCD_USER_REG (0x0014)



LCD_CAM_LCD_DOUT_CYCLELEN Configure the cycles for DOUT phase of LCD module. The cycles = this value + 1. (R/W)

LCD_CAM_LCD_ALWAYS_OUT_EN LCD continues outputting data when LCD is in DOUT phase, till LCD_CAM_LCD_START is cleared or LCD_CAM_LCD_RESET is set. (R/W)

LCD_CAM_LCD_8BITS_ORDER 1: Swap every two data bytes, valid in 8-bit mode. 0: Do not swap. (R/W)

LCD_CAM_LCD_UPDATE 1: Update LCD registers. This bit is cleared by hardware. 0: Do not care. (R/W)

LCD_CAM_LCD_BIT_ORDER 1: Change data bit order. Change LCD_DATA_out[7:0] to LCD_DATA_out[0:7] in 8-bit mode, and bits[15:0] to bits[0:15] in 16-bit mode. 0: Do not change. (R/W)

LCD_CAM_LCD_BYTE_ORDER 1: Invert data byte order, only valid in 16-bit mode. 0: Do not invert. (R/W)

LCD_CAM_LCD_2BYTE_EN 1: The width of output LCD data is 16 bits. 0: The width of output LCD data is 8 bits. (R/W)

LCD_CAM_LCD_DOUT 1: Be able to send data out in LCD sequence when LCD starts. 0: Disable. (R/W)

LCD_CAM_LCD_DUMMY 1: Enable DUMMY phase in LCD sequence when LCD starts. 0: Disable. (R/W)

LCD_CAM_LCD_CMD 1: Be able to send command in LCD sequence when LCD starts. 0: Disable. (R/W)

LCD_CAM_LCD_START LCD starts sending data enable signal, valid in high level. (R/W)

LCD_CAM_LCD_RESET Reset LCD module. (WO)

LCD_CAM_LCD_DUMMY_CYCLELEN Configure DUMMY cycles. DUMMY cycles = this value + 1. (R/W)

LCD_CAM_LCD_CMD_2_CYCLE_EN The cycle length of command phase. 1: 2 cycles. 0: 1 cycle. (R/W)

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Register 26.4. LCD_CAM_LCD_MISC_REG (0x0018)



LCD_CAM_LCD_AFIFO_THRESHOLD_NUM Set the threshold for Async Tx FIFO full event. (R/W)

LCD_CAM_LCD_VFK_CYCLELEN Configure the setup cycles in LCD non-RGB mode. Setup cycles expected = this value + 1. (R/W)

LCD_CAM_LCD_VBK_CYCLELEN Configure the hold time cycles in LCD non-RGB mode. Hold cycles expected = this value + 1. (R/W)

LCD_CAM_LCD_NEXT_FRAME_EN 1: Send the next frame data when the current frame is sent out. 0: LCD stops when the current frame is sent out. (R/W)

LCD_CAM_LCD_BK_EN 1: Enable blank region when LCD sends data out. 0: No blank region. (R/W)

LCD_CAM_LCD_AFIFO_RESET Async Tx FIFO reset signal. (WO)

LCD_CAM_LCD_CD_DATA_SET 1: LCD_CD = !LCD_CAM_LCD_CD_IDLE_EDGE when LCD is in DOUT phase. 0: LCD_CD = LCD_CAM_LCD_CD_IDLE_EDGE. (R/W)

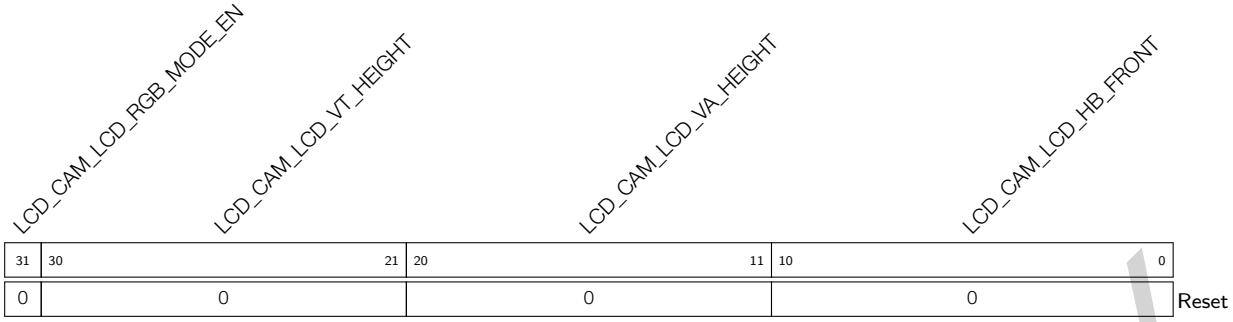
LCD_CAM_LCD_CD_DUMMY_SET 1: LCD_CD = !LCD_CAM_LCD_CD_IDLE_EDGE when LCD is in DUMMY phase. 0: LCD_CD = LCD_CAM_LCD_CD_IDLE_EDGE. (R/W)

LCD_CAM_LCD_CD_CMD_SET 1: LCD_CD = !LCD_CAM_LCD_CD_IDLE_EDGE when LCD is in CMD phase. 0: LCD_CD = LCD_CAM_LCD_CD_IDLE_EDGE. (R/W)

LCD_CAM_LCD_CD_IDLE_EDGE The default value of LCD_CD. (R/W)

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Register 26.5. LCD_CAM_LCD_CTRL_REG (0x001C)



LCD_CAM_LCD_HB_FRONT It is the horizontal blank front porch of a frame. (R/W)

LCD_CAM_LCD_VA_HEIGHT It is the vertical active height of a frame. (R/W)

LCD_CAM_LCD_VT_HEIGHT It is the vertical total height of a frame. (R/W)

LCD_CAM_LCD_RGB_MODE_EN 1: Enable RGB mode, and input VSYNC, HSYNC, and DE signals. 0: Disable. (R/W)

Register 26.6. LCD_CAM_LCD_CTRL1_REG (0x0020)



LCD_CAM_LCD_VB_FRONT It is the vertical blank front porch of a frame. (R/W)

LCD_CAM_LCD_HA_WIDTH It is the horizontal active width of a frame. (R/W)

LCD_CAM_LCD_HT_WIDTH It is the horizontal total width of a frame. (R/W)

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Register 26.7. LCD_CAM_LCD_CTRL2_REG (0x0024)



LCD_CAM_LCD_VSYNC_WIDTH It is the width of LCD_VSYNC active pulse in a line. (R/W)

LCD_CAM_LCD_VSYNC_IDLE_POL It is the idle value of LCD_VSYNC. (R/W)

LCD_CAM_LCD_DE_IDLE_POL It is the idle value of LCD_DE. (R/W)

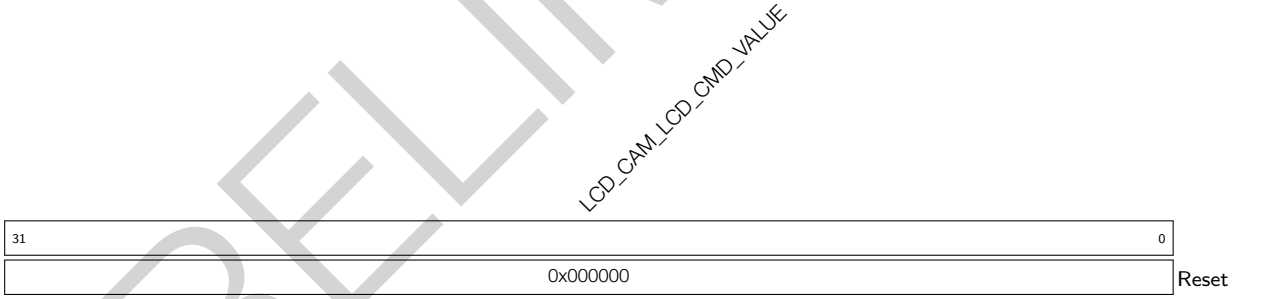
LCD_CAM_LCD_HS_BLANK_EN 1: The pulse of LCD_HSYNC is out in vertical blanking lines in RGB mode. 0: LCD_HSYNC pulse is valid only in active region lines in RGB mode. (R/W)

LCD_CAM_LCD_HSYNC_WIDTH It is the width of LCD_HSYNC active pulse in a line. (R/W)

LCD_CAM_LCD_HSYNC_IDLE_POL It is the idle value of LCD_HSYNC. (R/W)

LCD_CAM_LCD_HSYNC_POSITION It is the position of LCD_HSYNC active pulse in a line. (R/W)

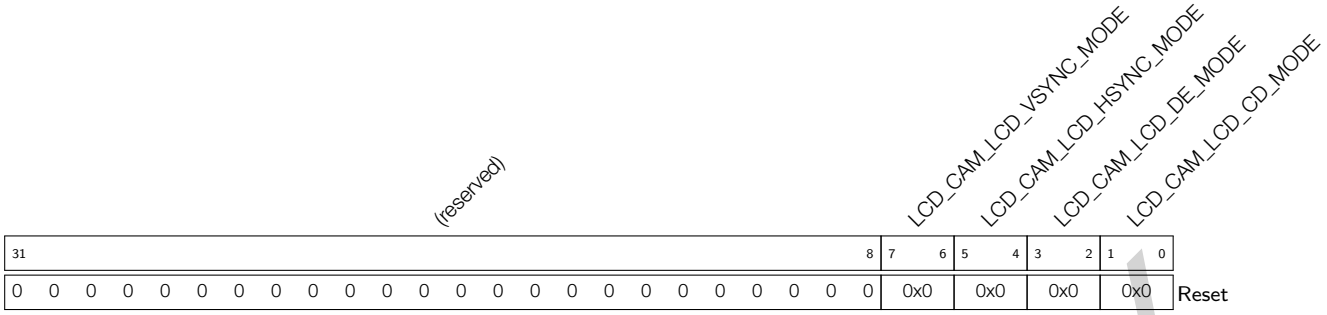
Register 26.8. LCD_CAM_LCD_CMD_VAL_REG (0x0028)



LCD_CAM_LCD_CMD_VALUE The LCD write command value. (R/W)

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Register 26.9. LCD_CAM_LCD_DLY_MODE_REG (0x0030)



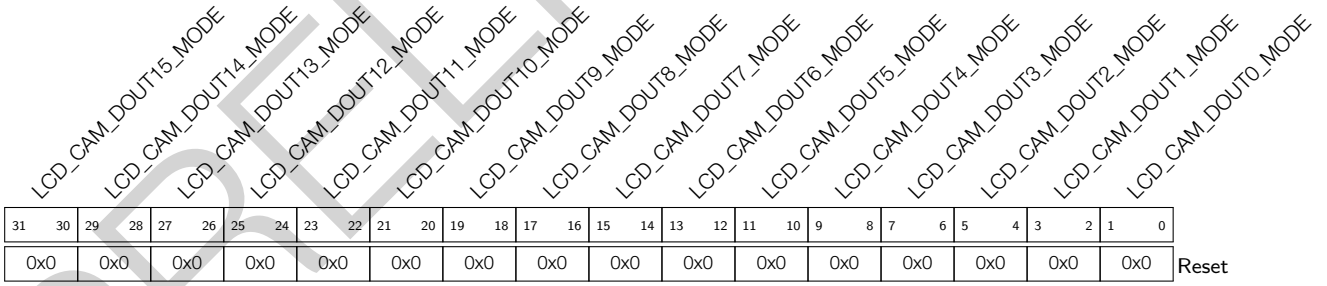
LCD_CAM_LCD_CD_MODE The output LCD_CD is delayed by module clock LCD_CLK. 0: output without delay. 1: delayed by the rising edge of LCD_CLK. 2: delayed by the falling edge of LCD_CLK. (R/W)

LCD_CAM_LCD_DE_MODE The output LCD_DE is delayed by module clock LCD_CLK. 0: output without delay. 1: delayed by the rising edge of LCD_CLK. 2: delayed by the falling edge of LCD_CLK. (R/W)

LCD_CAM_LCD_HSYNC_MODE The output LCD_HSYNC is delayed by module clock LCD_CLK. 0: output without delay. 1: delayed by the rising edge of LCD_CLK. 2: delayed by the falling edge of LCD_CLK. (R/W)

LCD_CAM_LCD_VSYNC_MODE The output LCD_VSYNC is delayed by module clock LCD_CLK. 0: output without delay. 1: delayed by the rising edge of LCD_CLK. 2: delay by the falling edge of LCD_CLK. (R/W)

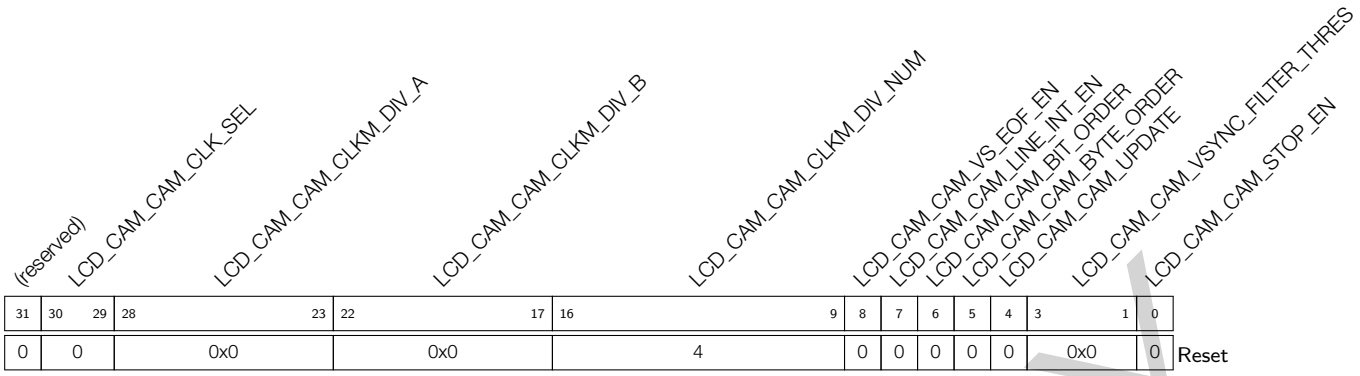
Register 26.10. LCD_CAM_LCD_DATA_DOUT_MODE_REG (0x0038)



LCD_CAM_DOUT*n*_MODE (*n* = 0 - 15) The output data bit *n* is delayed by module clock LCD_CLK. 0: output without delay. 1: delayed by the rising edge of LCD_CLK. 2: delayed by the falling edge of LCD_CLK. (R/W)

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Register 26.11. LCD_CAM_CAM_CTRL_REG (0x0004)



LCD_CAM_CAM_STOP_EN Camera stop enable signal, 1: camera stops when GDMA Rx FIFO is full. 0: Do not stop. (R/W)

LCD_CAM_CAM_VSYNC_FILTER_THRES Filter threshold value for CAM_VSYNC signal. (R/W)

LCD_CAM_CAM_UPDATE 1: Update camera registers. This bit is cleared by hardware. 0: Do not care. (R/W)

LCD_CAM_CAM_BYTE_ORDER 1: Invert data byte order, only valid in 16-bit mode. 0: Do not change. (R/W)

LCD_CAM_CAM_BIT_ORDER 1: Change data bit order, change CAM_DATA_in[7:0] to CAM_DATA_in[0:7] in 8-bit mode, and bits[15:0] to bits[0:15] in 16-bit mode. 0: Do not change. (R/W)

LCD_CAM_CAM_LINE_INT_EN 1: Enable to generate LCD_CAM_CAM_HS_INT. 0: Disable. (R/W)

LCD_CAM_CAM_VS_EOF_EN 1: Enable CAM_VSYNC to generate in_suc_eof. 0: in_suc_eof is controlled by LCD_CAM_CAM_REC_DATA_BYTELEN. (R/W)

LCD_CAM_CAM_CLKM_DIV_NUM Integral camera clock divider value. (R/W)

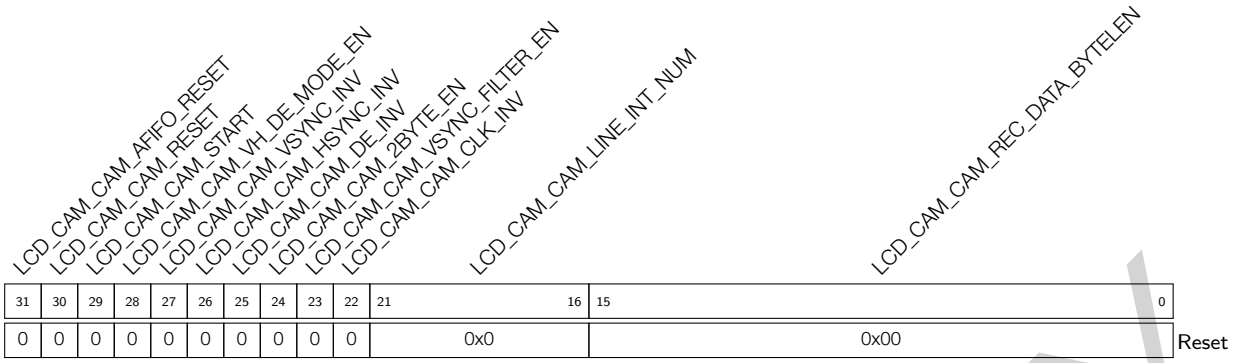
LCD_CAM_CAM_CLKM_DIV_B Fractional clock divider numerator value. (R/W)

LCD_CAM_CAM_CLKM_DIV_A Fractional clock divider denominator value. (R/W)

LCD_CAM_CAM_CLK_SEL Select camera module source clock. 0: Clock source is disabled. 1: XTAL_CLK. 2: PLL_240M_CLK. 3: PLL_240M_CLK. (R/W)

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Register 26.12. LCD_CAM_CAM_CTRL1_REG (0x0008)



LCD_CAM_CAM_REC_DATA_BYTELEN Configure camera received data byte length. When the length of received data reaches this value + 1, GDMA in_suc_eof_int is triggered. (R/W)

LCD_CAM_CAM_LINE_INT_NUM Configure line number. When the number of received lines reaches this value + 1, LCD_CAM_CAM_HS_INT is triggered. (R/W)

LCD_CAM_CAM_CLK_INV 1: Invert the input signal CAM_PCLK. 0: Do not invert. (R/W)

LCD_CAM_CAM_VSYNC_FILTER_EN 1: Enable CAM_VSYNC filter function. 0: Bypass. (R/W)

LCD_CAM_CAM_2BYTE_EN 1: The width of input data is 16 bits. 0: The width of input data is 8 bits. (R/W)

LCD_CAM_CAM_DE_INV CAM_DE invert enable signal, valid in high level. (R/W)

LCD_CAM_CAM_HSYNC_INV CAM_HSYNC invert enable signal, valid in high level. (R/W)

LCD_CAM_CAM_VSYNC_INV CAM_VSYNC invert enable signal, valid in high level. (R/W)

LCD_CAM_CAM_VH_DE_MODE_EN 1: Input control signals are CAM_DE and CAM_HSYNC. CAM_VSYNC is 1. 0: Input control signals are CAM_DE and CAM_VSYNC. CAM_HSYNC and CAM_DE are all 1 at the the same time. (R/W)

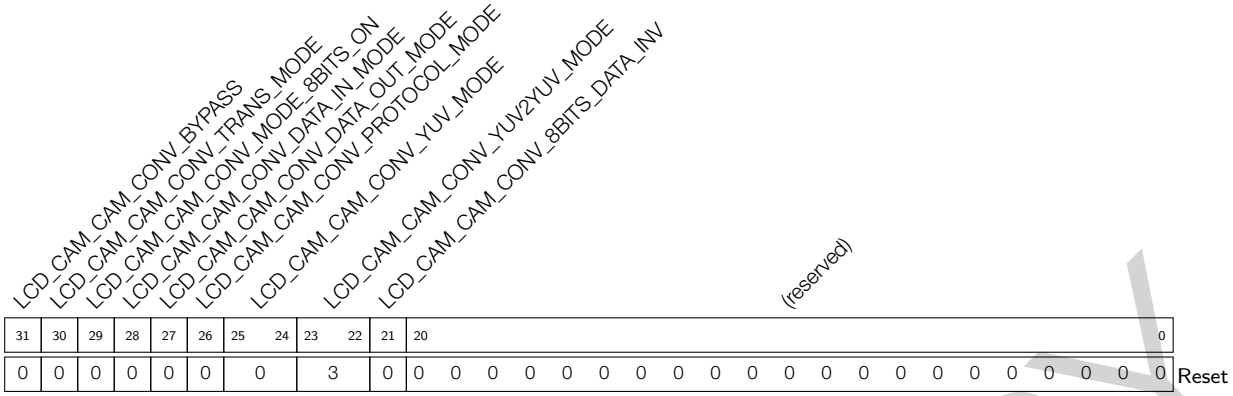
LCD_CAM_CAM_START Camera module start signal. (R/W)

LCD_CAM_CAM_RESET Camera module reset signal. (WO)

LCD_CAM_CAM_AFIFO_RESET Camera Async Rx FIFO reset signal. (WO)

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Register 26.13. LCD_CAM_CAM_RGB_YUV_REG (0x000C)



LCD_CAM_CAM_CONV_8BITS_DATA_INV Swap every two 8-bit input data. 1: Enabled. 0: Disabled. (R/W)

LCD_CAM_CAM_CONV_YUV2YUV_MODE In YUV-to-YUV mode, 0: data is converted to YUV422 format. 1: data is converted to YUV420 format. 2: data is converted to YUV411 format. 3: disabled. To enable YUV-to-YUV mode, LCD_CAM_CAM_CONV_TRANS_MODE must be set to 1. (R/W)

LCD_CAM_CAM_CONV_YUV_MODE In YUV-to-YUV mode and YUV-to-RGB mode, LCD_CAM_CAM_CONV_YUV_MODE decides the YUV mode of input data. 0: input data is in YUV422 format. 1: input data is in YUV420 format. 2: input data is in YUV411 format. In RGB-to-YUV mode, 0: data is converted to YUV422 format. 1: data is converted to YUV420 format. 2: data is converted to YUV411 format. (R/W)

LCD_CAM_CAM_CONV_PROTOCOL_MODE 0: BT601. 1: BT709. (R/W)

LCD_CAM_CAM_CONV_DATA_OUT_MODE Configure color range for output data. 0: limited color range. 1: full color range. (R/W)

LCD_CAM_CAM_CONV_DATA_IN_MODE Configure color range for input data. 0: limited color range. 1: full color range. (R/W)

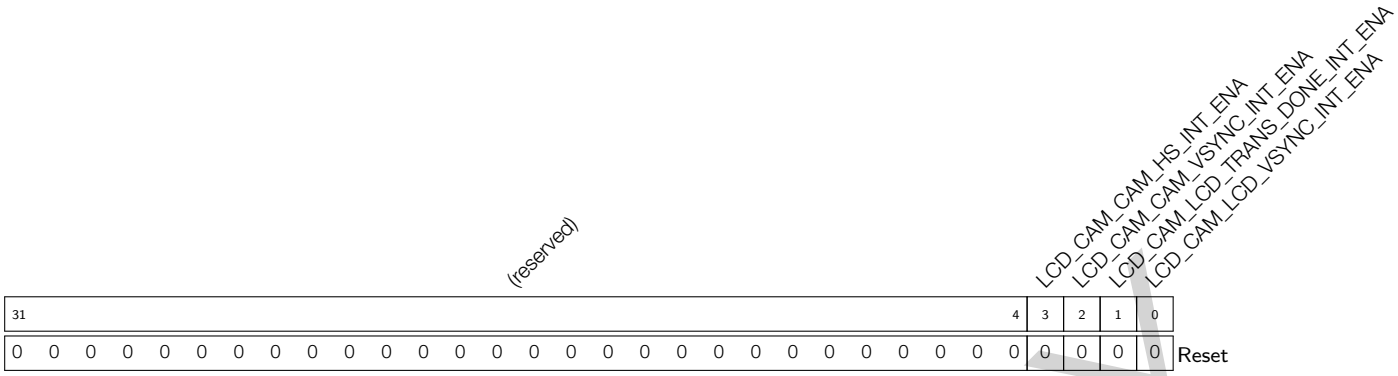
LCD_CAM_CAM_CONV_MODE_8BITS_ON 0: 16-bit mode. 1: 8-bit mode. (R/W)

LCD_CAM_CAM_CONV_TRANS_MODE 0: converted to RGB format. 1: converted to YUV format. (R/W)

LCD_CAM_CAM_CONV_BYPASS 0: Bypass converter. 1: Enable converter. (R/W)

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Register 26.14. LCD_CAM_LC_DMA_INT_ENA_REG (0x0064)



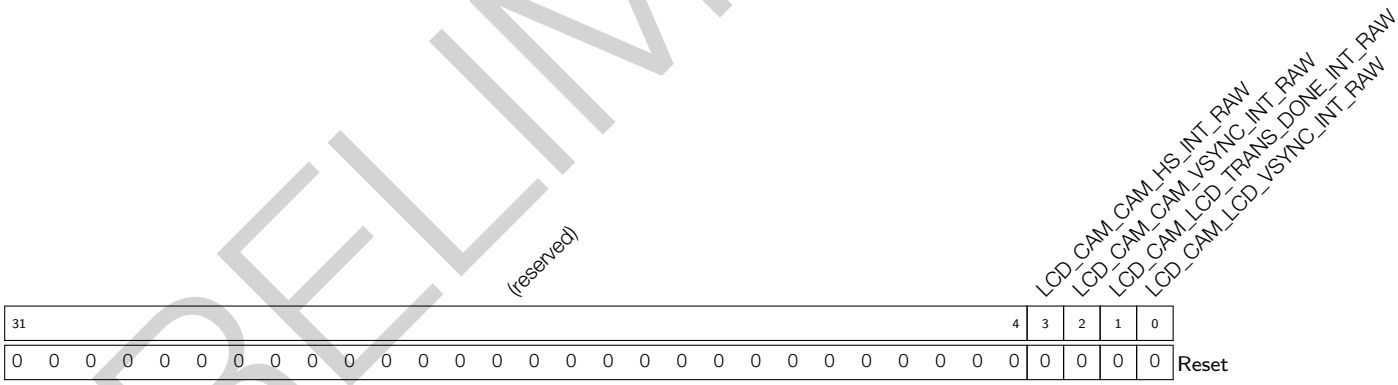
LCD_CAM_LCD_VSYNC_INT_ENA The enable bit for LCD_CAM_LCD_VSYNC_INT interrupt. (R/W)

LCD_CAM_LCD_TRANS_DONE_INT_ENA The enable bit for LCD_CAM_LCD_TRANS_DONE_INT interrupt. (R/W)

LCD_CAM_CAM_VSYNC_INT_ENA The enable bit for LCD_CAM_CAM_VSYNC_INT interrupt. (R/W)

LCD_CAM_CAM_HS_INT_ENA The enable bit for LCD_CAM_CAM_HS_INT interrupt. (R/W)

Register 26.15. LCD_CAM_LC_DMA_INT_RAW_REG (0x0068)



LCD_CAM_LCD_VSYNC_INT_RAW The raw bit for LCD_CAM_LCD_VSYNC_INT interrupt. (RO)

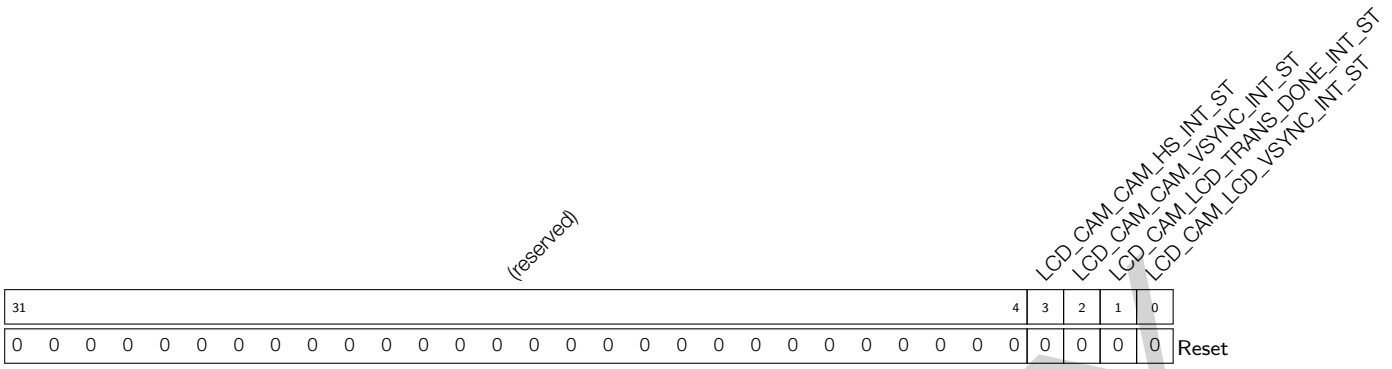
LCD_CAM_LCD_TRANS_DONE_INT_RAW The raw bit for LCD_CAM_LCD_TRANS_DONE_INT interrupt. (RO)

LCD_CAM_CAM_VSYNC_INT_RAW The raw bit for LCD_CAM_CAM_VSYNC_INT interrupt. (RO)

LCD_CAM_CAM_HS_INT_RAW The raw bit for LCD_CAM_CAM_HS_INT interrupt. (RO)

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Register 26.16. LCD_CAM_LC_DMA_INT_ST_REG (0x006C)



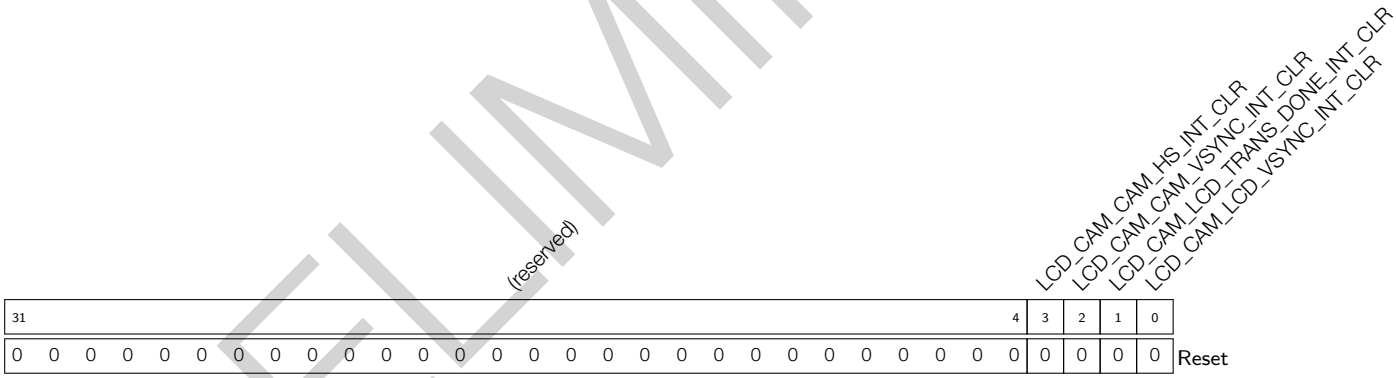
LCD_CAM_LCD_VSYNC_INT_ST The status bit for LCD_CAM_LCD_VSYNC_INT interrupt. (RO)

LCD_CAM_LCD_TRANS_DONE_INT_ST The status bit for LCD_CAM_LCD_TRANS_DONE_INT interrupt. (RO)

LCD_CAM_CAM_VSYNC_INT_ST The status bit for LCD_CAM_CAM_VSYNC_INT interrupt. (RO)

LCD_CAM_CAM_HS_INT_ST The status bit for LCD_CAM_CAM_HS_INT interrupt. (RO)

Register 26.17. LCD_CAM_LC_DMA_INT_CLR_REG (0x0070)



LCD_CAM_LCD_VSYNC_INT_CLR The clear bit for LCD_CAM_LCD_VSYNC_INT interrupt. (WO)

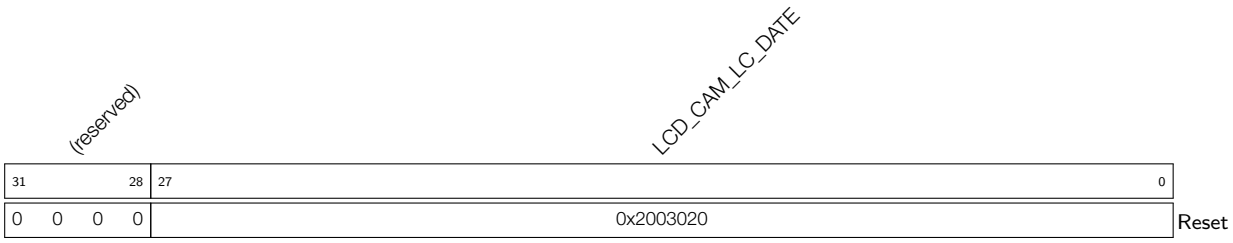
LCD_CAM_LCD_TRANS_DONE_INT_CLR The clear bit for LCD_CAM_LCD_TRANS_DONE_INT interrupt. (WO)

LCD_CAM_CAM_VSYNC_INT_CLR The clear bit for LCD_CAM_CAM_VSYNC_INT interrupt. (WO)

LCD_CAM_CAM_HS_INT_CLR The clear bit for LCD_CAM_CAM_HS_INT interrupt. (WO)

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Register 26.18. LCD_CAM_LC_REG_DATE_REG (0x00FC)



LCD_CAM_LC_DATE Version control register (R/W)

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27 Two-wire Automotive Interface (TWAI®)

27.1 Overview

The Two-wire Automotive Interface (TWAI)® is a multi-master, multi-cast communication protocol with error detection and signaling and inbuilt message priorities and arbitration. The TWAI protocol is suited for automotive and industrial applications (see Section 27.3 for more details).

ESP32-S3 contains a TWAI controller that can be connected to a TWAI bus via an external transceiver. The TWAI controller contains numerous advanced features, and can be utilized in a wide range of use cases such as automotive products, industrial automation controls, building automation etc.

27.2 Features

ESP32-S3 TWAI controller supports the following features:

- Compatible with ISO 11898-1 protocol (CAN Specification 2.0)
- Supports Standard Frame Format (11-bit ID) and Extended Frame Format (29-bit ID)
- Bit rates from 1 Kbit/s to 1 Mbit/s
- Multiple modes of operation
  - Normal
  - Listen-only (no influence on bus)
  - Self-test (no acknowledgment required during data transmission)
- 64-byte Receive FIFO
- Special transmissions
  - Single-shot transmissions (does not automatically re-transmit upon error)
  - Self Reception (the TWAI controller transmits and receives messages simultaneously)
- Acceptance Filter (supports single and dual filter modes)
- Error detection and handling
  - Error Counters
  - Configurable Error Warning Limit
  - Error Code Capture
  - Arbitration Lost Capture

27.3 Functional Protocol

27.3.1 TWAI Properties

The TWAI protocol connects two or more nodes in a bus network, and allows nodes to exchange messages in a latency bounded manner. A TWAI bus has the following properties.

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Single Channel and Non-Return-to-Zero: The bus consists of a single channel to carry bits, thus communication is half-duplex. Synchronization is also implemented in this channel, so extra channels (e.g., clock or enable) are not required. The bit stream of a TWAI message is encoded using the Non-Return-to-Zero (NRZ) method.

Bit Values: The single channel can either be in a dominant or recessive state, representing a logical 0 and a logical 1 respectively. A node transmitting data in a dominant state will always override another node transmitting data in a recessive state. The physical implementation on the bus is left to the application level to decide (e.g., differential pair or a single wire).

Bit Stuffing: Certain fields of TWAI messages are bit-stuffed. A transmitter that transmits five consecutive bits of the same value should automatically insert a complementary bit. Likewise, a receiver that receives five consecutive bits should treat the next bit as a stuffed bit. Bit stuffing is applied to the following fields: SOF, arbitration field, control field, data field, and CRC sequence (see Section 27.3.2 for more details).

Multi-cast: All nodes receive the same bits as they are connected to the same bus. Data is consistent across all nodes unless there is a bus error (see Section 27.3.3 for more details).

Multi-master: Any node can initiate a transmission. If a transmission is already ongoing, a node will wait until the current transmission is over before beginning its own transmission.

Message Priorities and Arbitration: If two or more nodes simultaneously initiate a transmission, the TWAI protocol ensures that one node will win arbitration of the bus. The arbitration field of the message transmitted by each node is used to determine which node will win arbitration.

Error Detection and Signaling: Each node will actively monitor the bus for errors, and signal the detection errors by transmitting an error frame.

Fault Confinement: Each node will maintain a set of error counts that are incremented/decremented according to a set of rules. When the error counts surpass a certain threshold, a node will automatically eliminate itself from the network by switching itself off.

Configurable Bit Rate: The bit rate for a single TWAI bus is configurable. However, all nodes within the same bus must operate at the same bit rate.

Transmitters and Receivers: At any point in time, a TWAI node can either be a transmitter or a receiver.

- A node originating a message is a transmitter. The node remains a transmitter until the bus is idle or until the node loses arbitration. Note that multiple nodes can be transmitters if they have yet to lose arbitration.
- All nodes that are not transmitters are receivers.

27.3.2 TWAI Messages

TWAI nodes use messages to transmit data, and signal errors to other nodes. Messages are split into various frame types, and some frame types will have different frame formats.

The TWAI protocol has of the following frame types:

- Data frames
- Remote frames
- Error frames
- Overload frames

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- Interframe space

The TWAI protocol has the following frame formats:

- Standard Frame Format (SFF) that consists of a 11-bit identifier
- Extended Frame Format (EFF) that consists of a 29-bit identifier

27.3.2.1 Data Frames and Remote Frames

Data frames are used by nodes to send data to other nodes, and can have a payload of 0 to 8 data bytes. Remote frames are used for nodes to request a data frame with the same identifier from another node, thus they do not contain any data bytes. However, data frames and remote frames share many common fields. Figure 27-1 illustrates the fields and sub-fields of different frames and formats.

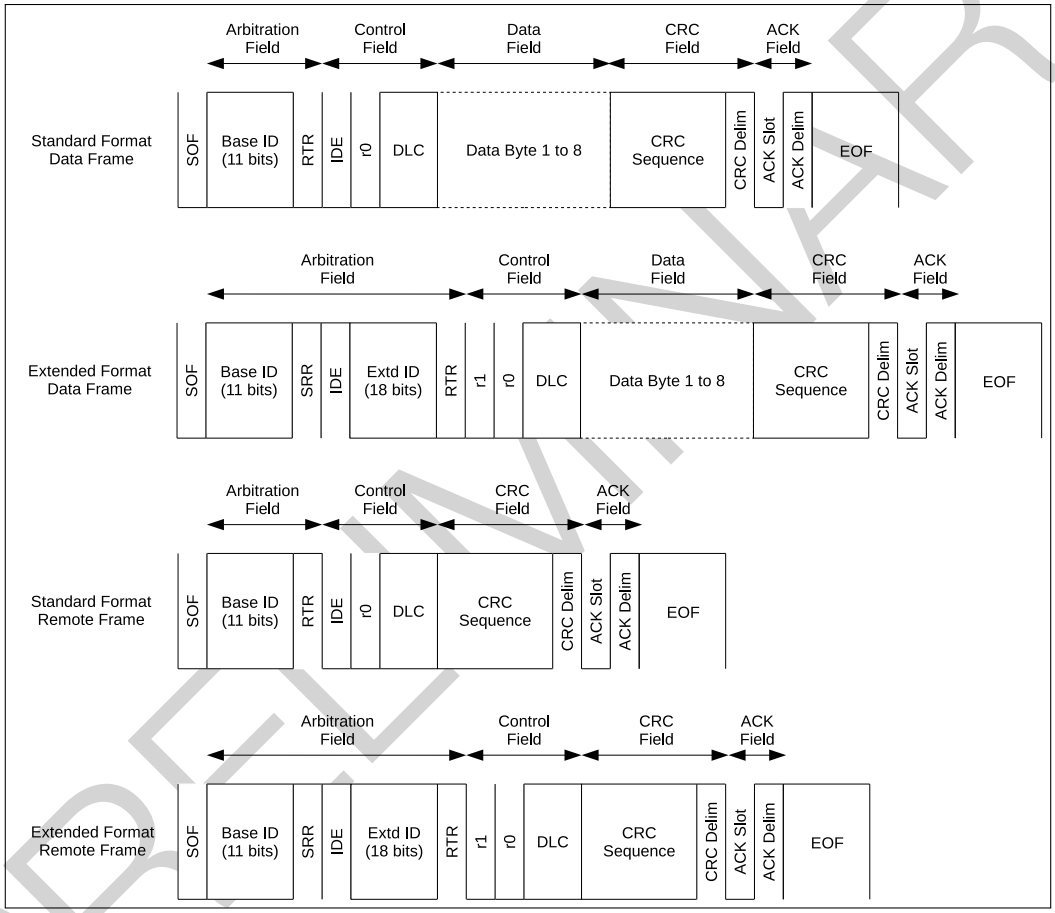


Figure 27-1. Bit Fields in Data Frames and Remote Frames

Arbitration Field

When two or more nodes transmits a data or remote frame simultaneously, the arbitration field is used to determine which node will win arbitration of the bus. During the arbitration field, if a node transmits a recessive bit while observes a dominant bit, this indicates that another node has overridden its recessive bit. Therefore, the node transmitting the recessive bit has lost arbitration of the bus and should immediately switch to be a receiver.

The arbitration field primarily consists of the frame identifier that is transmitted from the most significant bit first. Given that a dominant bit represents a logical 0, and a recessive bit represents a logical 1:

- A frame with the smallest ID value will always win arbitration.

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- Given the same ID and format, data frames will always prevail over remote frames.
- Given the same first 11 bits of ID, a Standard Format Data Frame will prevail over an Extended Format Data Frame due to the SRR being recessive.

Control Field

The control field primarily consists of the DLC (Data Length Code) which indicates the number of payload data bytes for a data frame, or the number of requested data bytes for a remote frame. The DLC is transmitted from the most significant bit first.

Data Field

The data field contains the actual payload data bytes of a data frame. Remote frames do not contain a data field.

CRC Field

The CRC field primarily consists of a CRC sequence. The CRC sequence is a 15-bit cyclic redundancy code calculated form the de-stuffed contents (everything from the SOF to the end of the data field) of a data or remote frame.

ACK Field

The ACK field primarily consists of an ACK Slot and an ACK Delim. The ACK field is mainly intended for the receiver to indicate to a transmitter that it has received an effective message.

Table 27-1. Data Frames and Remote Frames in SFF and EFF

Data/Remote Frames	Description
SOF	The SOF (Start of Frame) is a single dominant bit used to synchronize nodes on the bus.
Base ID	The Base ID (ID.28 to ID.18) is the 11-bit identifier for SFF, or the first 11-bits of the 29-bit identifier for EFF.
RTR	The RTR (Remote Transmission Request) bit indicates whether the message is a data frame (dominant) or a remote frame (recessive). This means that a remote frame will always lose arbitration to a data frame given they have the same ID.
SRR	The SRR (Substitute Remote Request) bit is transmitted in EFF to substitute for the RTR bit at the same position in SFF.
IDE	The IDE (Identifier Extension) bit indicates whether the message is SFF (dominant) or EFF (recessive). This means that a SFF frame will always win arbitration over an EFF frame given they have the same Base ID.
Extd ID	The Extended ID (ID.17 to ID.0) is the remaining 18-bits of the 29-bit identifier for EFF.
r1	The r1 bit (reserved bit 1) is always dominant.
r0	The r0 bit (reserved bit 0) is always dominant.
DLC	The DLC (Data Length Code) is 4-bit long and should contain any value from 0 to 8. Data frames use the DLC to indicate the number of data bytes in the data frame. Remote frames used the DLC to indicate the number of data bytes to request from another node.
Data Bytes	The data payload of data frames. The number of bytes should match the value of DLC. Data byte 0 is transmitted first, and each data byte is transmitted from the most significant bit first.

Cont'd on next page

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Table 27-1 – cont'd from previous page

Data/Remote Frames	Description
CRC Sequence	The CRC sequence is a 15-bit cyclic redundancy code.
CRC Delim	The CRC Delim (CRC Delimiter) is a single recessive bit that follows the CRC sequence.
ACK Slot	The ACK Slot (Acknowledgment Slot) is intended for receiver nodes to indicate that the data or remote frame was received without an issue. The transmitter node will send a recessive bit in the ACK Slot and receiver nodes should override the ACK Slot with a dominant bit if the frame was received without errors.
ACK Delim	The ACK Delim (Acknowledgment Delimiter) is a single recessive bit.
EOF	The EOF (End of Frame) marks the end of a data or remote frame, and consists of seven recessive bits.

27.3.2.2 Error and Overload Frames

Error Frames

Error frames are transmitted when a node detects a bus error. Error frames notably consist of an Error Flag which is made up of 6 consecutive bits of the same value, thus violating the bit-stuffing rule. Therefore, when a particular node detects a bus error and transmits an error frame, all other nodes will then detect a stuff error and transmit their own error frames in response. This has the effect of propagating the detection of a bus error across all nodes on the bus.

When a node detects a bus error, it will transmit an error frame starting from the next bit. However, if the type of bus error was a CRC error, then the error frame will start at the bit following the ACK Delim (see Section 27.3.3 for more details). The following Figure 27-2 shows different fields of an error frame:

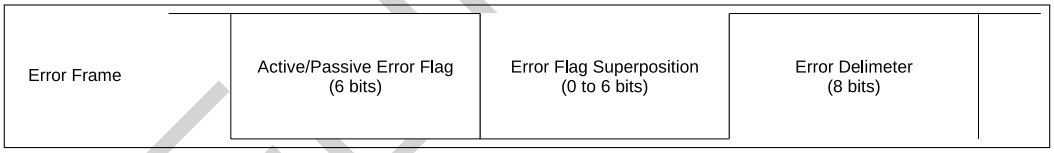


Figure 27-2. Fields of an Error Frame

Table 27-2. Error Frame

Error Frame	Description
Error Flag	The Error Flag has two forms, the Active Error Flag consisting of 6 dominant bits and the Passive Error Flag consisting of 6 recessive bits (unless overridden by dominant bits of other nodes). Active Error Flags are sent by error active nodes, whilst Passive Error Flags are sent by error passive nodes.
Error Flag Superposition	The Error Flag Superposition field meant to allow for other nodes on the bus to transmit their respective Active Error Flags. The superposition field can range from 0 to 6 bits, and ends when the first recessive bit is detected (i.e., the first it of the Delimiter).
Error Delimeter	The Delimiter field marks the end of the error/overload frame, and consists of 8 recessive bits.

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Overload Frames

An overload frame has the same bit fields as an error frame containing an Active Error Flag. The key difference is in the conditions that can trigger the transmission of an overload frame. Figure 27-3 below shows the bit fields of an overload frame.

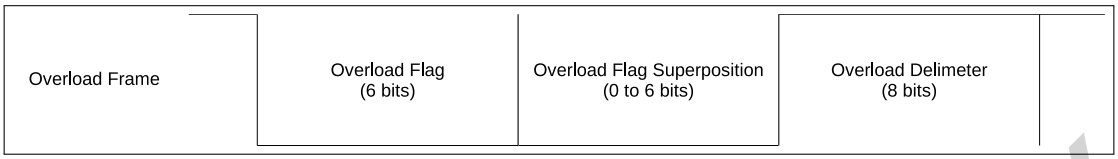


Figure 27-3. Fields of an Overload Frame

Table 27-3. Overload Frame

Overload Flag	Description
Overload Flag	Consists of 6 dominant bits. Same as an Active Error Flag.
Overload Flag Superposition	Allows for the superposition of Overload Flags from other nodes, similar to an Error Flag Superposition.
Overload Delimiter	Consists of 8 recessive bits. Same as an Error Delimiter.

Overload frames will be transmitted under the following conditions:

1. A receiver requires a delay of the next data or remote frame.
2. A dominant bit is detected at the first and second bit of intermission.
3. A dominant bit is detected at the eighth (last) bit of an Error Delimiter. Note that in this case, TEC and REC will not be incremented (see Section 27.3.3 for more details).

Transmitting an overload frame due to one of the conditions must also satisfy the following rules:

- Transmitting an overload frame due to condition 1 must only be started at the first bit of intermission.
- Transmitting an overload frame due to condition 2 and 3 must start one bit after the detecting the dominant bit of the condition.
- A maximum of two overload frames may be generated in order to delay the next data or remote frame.

27.3.2.3 Interframe Space

The Interframe Space acts as a separator between frames. Data frames and remote frames must be separated from preceding frames by an Interframe Space, regardless of the preceding frame's type (data frame, remote frame, error frame, overload frame). However, error frames and overload frames do not need to be separated from preceding frames.

Figure 27-4 shows the fields within an Interframe Space:

Table 27-4. Interframe Space

Interframe Space	Description
Intermission	The Intermission consists of 3 recessive bits.

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Table 27-4 – cont'd from previous page

Interframe Space	Description
Suspend Transmission	An Error Passive node that has just transmitted a message must include a Suspend Transmission field. This field consists of 8 recessive bits. Error Active nodes should not include this field.
Bus Idle	The Bus Idle field is of arbitrary length. Bus Idle ends when an SOF is transmitted. If a node has a pending transmission, the SOF should be transmitted at the first bit following Intermission.

27.3.3 TWAI Errors

27.3.3.1 Error Types

Bus Errors in TWAI are categorized into one of the following types:

Bit Error

A Bit Error occurs when a node transmits a bit value (i.e., dominant or recessive) but the opposite bit is detected (e.g., a dominant bit is transmitted but a recessive is detected). However, if the transmitted bit is recessive and is located in the Arbitration Field or ACK Slot or Passive Error Flag, then detecting a dominant bit will not be considered a Bit Error.

Stuff Error

A stuff error is detected when 6 consecutive bits of the same value are detected (thus violating the bit-stuffing encoding rules).

CRC Error

A receiver of a data or remote frame will calculate a CRC based on the bits it has received. A CRC error occurs when the CRC calculated by the receiver does not match the CRC sequence in the received data or remote Frame.

Format Error

A Format Error is detected when a fixed-form bit field of a message contains an illegal bit. For example, the r1 and r0 fields must be dominant.

ACK Error

An ACK Error occurs when a transmitter does not detect a dominant bit at the ACK Slot.

27.3.3.2 Error States

TWAI nodes implement fault confinement by each maintaining two error counters, where the counter values determine the error state. The two error counters are known as the Transmit Error Counter (TEC) and Receive Error Counter (REC). TWAI has the following error states.

Error Active

An Error Active node is able to participate in bus communication and transmit an Active Error Flag when it detects an error.

Error Passive

An Error Passive node is able to participate in bus communication, but can only transmit an Passive Error Flag when it detects an error. Error Passive nodes that have transmitted a data or remote frame must also include the Suspend Transmission field in the subsequent Interframe Space.

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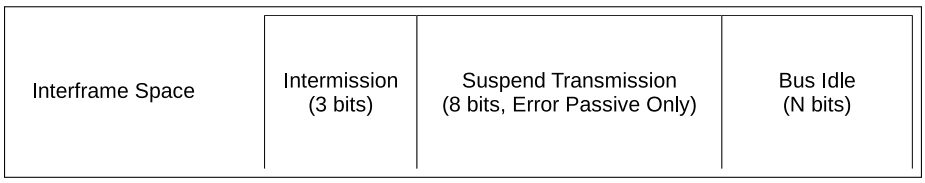


Figure 27-4. The Fields within an Interframe Space

Bus Off

A Bus Off node is not permitted to influence the bus in any way (i.e., is not allowed to transmit anything).

27.3.3.3 Error Counters

The TEC and REC are incremented/decremented according to the following rules. **Note that more than one rule can apply for a given message transfer.**

1. When a receiver detects an error, the REC is increased by 1, except when the detected error was a Bit Error during the transmission of an Active Error Flag or an Overload Flag.
2. When a receiver detects a dominant bit as the first bit after sending an Error Flag, the REC is increased by 8.
3. When a transmitter sends an Error Flag, the TEC is increased by 8. However, the following scenarios are exempt from this rule:
   - If a transmitter is Error Passive that detects an Acknowledgment Error due to not detecting a dominant bit in the ACK Slot, it should send a Passive Error Flag. If no dominant bit is detected in that Passive Error Flag, the TEC should not be increased.
   - A transmitter transmits an Error Flag due to a Stuff Error during Arbitration. If the offending bit should have been recessive but was monitored as dominant, then the TEC should not be increased.
4. If a transmitter detects a Bit Error whilst sending an Active Error Flag or Overload Flag, the TEC is increased by 8.
5. If a receiver detects a Bit Error while sending an Active Error Flag or Overload Flag, the REC is increased by 8.
6. A node can tolerate up to 7 consecutive dominant bits after sending an Active/Passive Error Flag, or Overload Flag. After detecting the 14th consecutive dominant bit (when sending an Active Error Flag or Overload Flag), or the 8th consecutive dominant bit following a Passive Error Flag, a transmitter will increase its TEC by 8 and a receiver will increase its REC by 8. Every additional eight consecutive dominant bits will also increase the TEC (for transmitters) or REC (for receivers) by 8 as well.
7. When a transmitter successfully transmits a message (getting ACK and no errors until the EOF is complete), the TEC is decremented by 1, unless the TEC is already at 0.
8. When a receiver successfully receives a message (no errors before ACK Slot, and successful sending of ACK), the REC is decremented.
   - If the REC was between 1 and 127, the REC is decremented by 1.
   - If the REC was greater than 127, the REC is set to 127.
   - If the REC was 0, the REC remains 0.

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9. A node becomes Error Passive when its TEC and/or REC is greater than or equal to 128. The error condition that causes a node to become Error Passive will cause the node to send an Active Error Flag. Note that once the REC has reached to 128, any further increases to its value are invalid until the REC returns to a value less than 128.
10. A node becomes Bus Off when its TEC is greater than or equal to 256.
11. An Error Passive node becomes Error Active when both the TEC and REC are less than or equal to 127.
12. A Bus Off node can become Error Active (with both its TEC and REC reset to 0) after it monitors 128 occurrences of 11 consecutive recessive bits on the bus.

27.3.4 TWAI Bit Timing

27.3.4.1 Nominal Bit

The TWAI protocol allows a TWAI bus to operate at a particular bit rate. However, all nodes within a TWAI bus must operate at the same bit rate.

- **The Nominal Bit Rate** is defined as the number of bits transmitted per second from an ideal transmitter and without any synchronization.
- **The Nominal Bit Time** is defined as **1/Nominal Bit Rate**.

A single Nominal Bit Time is divided into multiple segments, and each segment is made up of multiple Time Quanta. A **Time Quantum** is a fixed unit of time, and is implemented as some form of prescaled clock signal in each node. Figure 27-5 illustrates the segments within a single Nominal Bit Time.

TWAI controllers will operate in time steps of one Time Quanta where the state of the TWAI bus is analyzed. If two consecutive Time Quantas have different bus states (i.e., recessive to dominant or vice versa), this will be considered an edge. When the bus is analyzed at the intersection of PBS1 and PBS2, this is considered the Sample Point and the sampled bus value is considered the value of that bit.

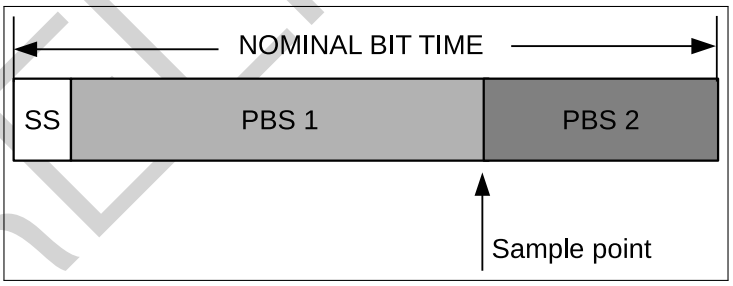


Figure 27-5. Layout of a Bit

Table 27-5. Segments of a Nominal Bit Time

Segment	Description
SS	The SS (Synchronization Segment) is 1 Time Quantum long. If all nodes are perfectly synchronized, the edge of a bit will lie in the SS.
PBS1	PBS1 (Phase Buffer Segment 1) can be 1 to 16 Time Quanta long. PBS1 is meant to compensate for the physical delay times within the network. PBS1 can also be lengthened for synchronization purposes.

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Table 27-5 – cont'd from previous page

Segment	Description
PBS2	PBS2 (Phase Buffer Segment 2) can be 1 to 8 Time Quanta long. PBS2 is meant to compensate for the information processing time of nodes. PBS2 can also be shortened for synchronization purposes.

27.3.4.2 Hard Synchronization and Resynchronization

Due to clock skew and jitter, the bit timing of nodes on the same bus may become out of phase. Therefore, a bit edge may come before or after the SS. To ensure that the internal bit timing clocks of each node are kept in phase, TWAI has various methods of synchronization. The **Phase Error "e"** is measured in the number of Time Quanta and relative to the SS.

- A positive Phase Error (e > 0) is when the edge lies after the SS and before the Sample Point (i.e., the edge is late).
- A negative Phase Error (e < 0) is when the edge lies after the Sample Point of the previous bit and before SS (i.e., the edge is early).

To correct for Phase Errors, there are two forms of synchronization, known as **Hard Synchronization** and **Resynchronization**. **Hard Synchronization** and **Resynchronization** obey the following rules:

- Only one synchronization may occur in a single bit time.
- Synchronizations only occurs on recessive to dominant edges.

Hard Synchronization

Hard Synchronization occurs on the recessive to dominant edges when the bus is idle (i.e., the first SOF bit after Bus Idle). All nodes will restart their internal bit timings so that the recessive to dominant edge lies within the SS of the restarted bit timing.

Resynchronization

Resynchronization occurs on recessive to dominant edges not during Bus Idle. If the edge has a positive Phase Error (e > 0), PBS1 is lengthened by a certain number of Time Quanta. If the edge has a negative Phase Error (e < 0), PBS2 will be shortened by a certain number of Time Quanta.

The number of Time Quanta to lengthen or shorten depends on the magnitude of the Phase Error, and is also limited by the Synchronization Jump Width (SJW) value which is programmable.

- When the magnitude of the Phase Error (**e**) is less than or equal to the SJW, PBS1/PBS2 are lengthened/shortened by the **e** number of Time Quanta. This has a same effect as Hard Synchronization.
- When the magnitude of the Phase Error is greater to the SJW, PBS1/PBS2 are lengthened/shortened by the SJW number of Time Quanta. This means it may take multiple bits of synchronization before the Phase Error is entirely corrected.

27.4 Architectural Overview

The major functional blocks of the TWAI controller are shown in Figure 27-6.

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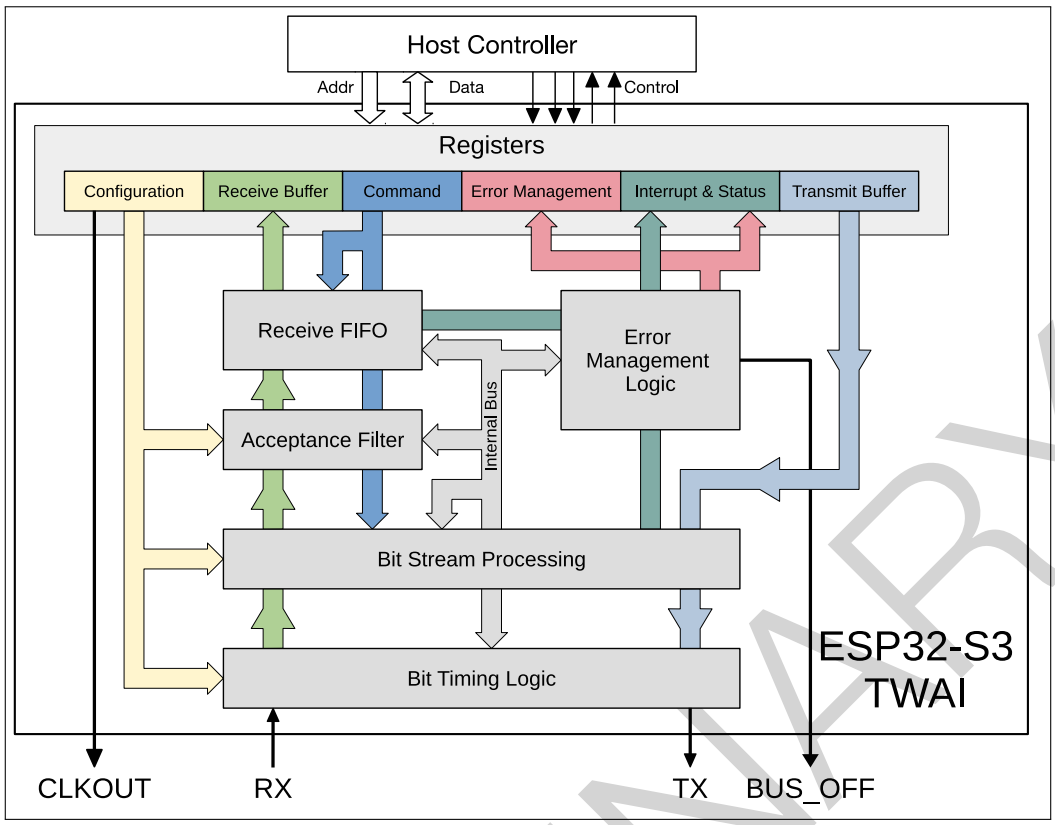


Figure 27-6. TWAI Overview Diagram

27.4.1 Registers Block

The ESP32-S3 CPU accesses peripherals using 32-bit aligned words. However, the majority of registers in the TWAI controller only contain useful data at the least significant byte (bits [7:0]). Therefore, in these registers, bits [31:8] are ignored on writes, and return 0 on reads.

Configuration Registers

The configuration registers store various configuration items for the TWAI controller such as bit rates, operation mode, Acceptance Filter etc. Configuration registers can only be modified whilst the TWAI controller is in Reset Mode (See Section 27.5.1).

Command Registers

The command register is used by the CPU to drive the TWAI controller to initiate certain actions such as transmitting a message or clearing the Receive Buffer. The command register can only be modified when the TWAI controller is in Operation Mode (see section 27.5.1).

Interrupt & Status Registers

The interrupt register indicates what events have occurred in the TWAI controller (each event is represented by a separate bit). The status register indicates the current status of the TWAI controller.

Error Management Registers

The error management registers include error counters and capture registers. The error counter registers represent TEC and REC values. The capture registers will record information about instances where TWAI controller detects a bus error, or when it loses arbitration.

Transmit Buffer Registers

The transmit buffer is a 13-byte buffer used to store a TWAI message to be transmitted.

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Receive Buffer Registers

The Receive Buffer is a 13-byte buffer which stores a single message. The Receive Buffer acts as a window of Receive FIFO, whose first message will be mapped into the Receive Buffer.

Note that the Transmit Buffer registers, Receive Buffer registers, and the Acceptance Filter registers share the same address range (offset 0x0040 to 0x0070). Their access is governed by the following rules:

- When the TWAI controller is in Reset Mode, all reads and writes to the address range maps to the Acceptance Filter registers.
- When the TWAI controller is in Operation Mode:
  - All reads to the address range maps to the Receive Buffer registers.
  - All writes to the address range maps to the Transmit Buffer registers.

27.4.2 Bit Stream Processor

The Bit Stream Processing (BSP) module frames data from the Transmit Buffer (e.g. bit stuffing and additional CRC fields) and generating a bit stream for the Bit Timing Logic (BTL) module. At the same time, the BSP module is also responsible for processing the received bit stream (e.g., de-stuffing and verifying CRC) from the BTL module and placing the message into the Receive FIFO. The BSP will also detect errors on the TWAI bus and report them to the Error Management Logic (EML).

27.4.3 Error Management Logic

The Error Management Logic (EML) module updates the TEC and REC, recording error information like error types and positions, and updating the error state of the TWAI controller such that the BSP module generates the correct Error Flags. Furthermore, this module also records the bit position when the TWAI controller loses arbitration.

27.4.4 Bit Timing Logic

The Bit Timing Logic (BTL) module transmits and receives messages at the configured bit rate. The BTL module also handles synchronization of out of phase bits so that communication remains stable. A single bit time consists of multiple programmable segments that allows users to set the length of each segment to account for factors such as propagation delay and controller processing time etc.

27.4.5 Acceptance Filter

The Acceptance Filter is a programmable message filtering unit that allows the TWAI controller to accept or reject a received message based on the message's ID field. Only accepted messages will be stored in the Receive FIFO. The Acceptance Filter's registers can be programmed to specify a single filter, or two separate filters (dual filter mode).

27.4.6 Receive FIFO

The Receive FIFO is a 64-byte buffer (inside the TWAI controller) that stores received messages accepted by the Acceptance Filter. Messages in the Receive FIFO can vary in size (between 3 to 13-bytes). When the Receive FIFO is full (or does not have enough space to store the next received message in its entirety), the Overrun Interrupt will be triggered, and any subsequent received messages will be lost until adequate space is cleared in the Receive FIFO. The first message in the Receive FIFO will be mapped to the 13-byte Receive Buffer until that

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message is cleared (using the Release Receive Buffer command bit). After clearing, the Receive Buffer will map to the next message in the Receive FIFO, and the space occupied by the previous message in the Receive FIFO can be used to receive new messages.

27.5 Functional Description

27.5.1 Modes

The ESP32-S3 TWAI controller has two working modes: Reset Mode and Operation Mode. Reset Mode and Operation Mode are entered by setting or clearing the TWAI_RESET_MODE bit.

27.5.1.1 Reset Mode

Entering Reset Mode is required in order to modify the various configuration registers of the TWAI controller. When entering Reset Mode, the TWAI controller is essentially disconnected from the TWAI bus. When in Reset Mode, the TWAI controller will not be able to transmit any messages (including error signals). Any transmission in progress is immediately terminated. Likewise, the TWAI controller will not be able to receive any messages either.

27.5.1.2 Operation Mode

In operation mode, the TWAI controller connects to the bus and write-protect all configuration registers to ensure consistency during operation. When in Operation Mode, the TWAI controller can transmit and receive messages (including error signaling) depending on which operation sub-mode the TWAI controller was configured with. The TWAI controller supports the following operation sub-modes:

- **Normal Mode:** The TWAI controller can transmit and receive messages including error signaling (such as error and overload Frames).
- **Self-test Mode:** Self-test mode is similar to normal Mode, but the TWAI controller will consider the transmission of a data or RTR frame successful and do not generate ACK error even if it was not acknowledged. This is commonly used when self-testing the TWAI controller.
- **Listen-only Mode:** The TWAI controller will be able to receive messages, but will remain completely passive on the TWAI bus. Thus, the TWAI controller will not be able to transmit any messages, acknowledgments, or error signals. The error counters will remain frozen. This mode is useful for TWAI bus monitoring.

Note that when exiting Reset Mode (i.e., entering Operation Mode), the TWAI controller must wait for 11 consecutive recessive bits to occur before being able to fully connect the TWAI bus (i.e., be able to transmit or receive).

27.5.2 Bit Timing

The operating bit rate of the TWAI controller must be configured whilst the TWAI controller is in Reset Mode. The bit rate is configured using TWAI_BUS_TIMING_0_REG and TWAI_BUS_TIMING_1_REG, and the two registers contain the following fields:

The following Table 27-6 illustrates the bit fields of TWAI_BUS_TIMING_0_REG.

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Table 27-6. Bit Information of TWAI_BUS_TIMING_0_REG (0x18)

Bit 31-16	Bit 15	Bit 14	Bit 13	Bit 12	.....	Bit 1	Bit 0
Reserved	SJW.1	SJW.0	Reserved	BRP.12	.....	BRP.1	BRP.0

Notes:

- BRP: The TWAI Time Quanta clock is derived from the APB clock that is usually 80 MHz. The Baud Rate Prescaler (BRP) field is used to define the prescaler according to the equation below, where t_{Tq} is the Time Quanta clock cycle and t_{CLK} is APB clock cycle:
  $t_{Tq} = 2 \times t_{CLK} \times (2^{12} \times BRP.12 + 2^{11} \times BRP.11 + ... + 2^{1} \times BRP.1 + 2^{0} \times BRP.0 + 1)$
- SJW: Synchronization Jump Width (SJW) is configured in SJW.0 and SJW.1 where SJW = (2 x SJW.1 + SJW.0 + 1)

The following Table 27-7 illustrates the bit fields of TWAI_BUS_TIMING_1_REG.

Table 27-7. Bit Information of TWAI_BUS_TIMING_1_REG (0x1c)

Bit 31-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SAM	PBS2.2	PBS2.1	PBS2.0	PBS1.3	PBS1.2	PBS1.1	PBS1.0

Notes:

- PBS1: The number of Time Quanta in Phase Buffer Segment 1 is defined according to the following equation: (8 x PBS1.3 + 4 x PBS1.2 + 2 x PBS1.1 + PBS1.0 + 1)
- PBS2: The number of Time Quanta in Phase Buffer Segment 2 is defined according to the following equation: (4 x PBS2.2 + 2 x PBS2.1 + PBS2.0 + 1)
- SAM: Enables triple sampling if set to 1. This is useful for low/medium speed buses to filter spikes on the bus line.

27.5.3 Interrupt Management

The ESP32-S3 TWAI controller provides eight interrupts, each represented by a single bit in the TWAI_INT_RAW_REG. For a particular interrupt to be triggered, the corresponding enable bit in TWAI_INT ENA_REG must be set.

The TWAI controller provides the following interrupts:

- Receive Interrupt
- Transmit Interrupt
- Error Warning Interrupt
- Data Overrun Interrupt
- Error Passive Interrupt
- Arbitration Lost Interrupt
- Bus Error Interrupt
- Bus Status Interrupt

The TWAI controller's interrupt signal to the interrupt matrix will be asserted whenever one or more interrupt bits are set in the TWAI_INT_RAW_REG, and deasserted when all bits in TWAI_INT_RAW_REG are cleared. The

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majority of interrupt bits in TWAI_INT_RAW_REG are automatically cleared when the register is read, except for the Receive Interrupt which can only be cleared when all the messages are released by setting the TWAI_RELEASE_BUF bit.

27.5.3.1 Receive Interrupt (RXI)

The Receive Interrupt (RXI) is asserted whenever the TWAI controller has received messages that are pending to be read from the Receive Buffer (i.e., when TWAI_RX_MESSAGE_CNT_REG > 0). Pending received messages includes valid messages in the Receive FIFO and also overrun messages. The RXI will not be deasserted until all pending received messages are cleared using the TWAI_RELEASE_BUF command bit.

27.5.3.2 Transmit Interrupt (TXI)

The Transmit Interrupt (TXI) is triggered whenever Transmit Buffer becomes free, indicating another message can be loaded into the Transmit Buffer to be transmitted. The Transmit Buffer becomes free under the following scenarios:

- A message transmission has completed successfully, i.e., acknowledged without any errors. (Any failed messages will automatically be resent.)
- A single shot transmission has completed (successfully or unsuccessfully, indicated by the TWAI_TX_COMPLETE bit).
- A message transmission was aborted using the TWAI_ABORT_TX command bit.

27.5.3.3 Error Warning Interrupt (EWI)

The Error Warning Interrupt (EWI) is triggered whenever there is a change to the TWAI_ERR_ST and TWAI_BUS_OFF_ST bits of the TWAI_STATUS_REG (i.e., transition from 0 to 1 or vice versa). Thus, an EWI could indicate one of the following events, depending on the values TWAI_ERR_ST and TWAI_BUS_OFF_ST at the moment when the EWI is triggered.

- If TWAI_ERR_ST = 0 and TWAI_BUS_OFF_ST = 0:
  - If the TWAI controller was in the Error Active state, it indicates both the TEC and REC have returned below the threshold value set by TWAI_ERR_WARNING_LIMIT_REG.
  - If the TWAI controller was previously in the Bus Off Recovery state, it indicates that Bus Recovery has completed successfully.
- If TWAI_ERR_ST = 1 and TWAI_BUS_OFF_ST = 0: The TEC or REC error counters have exceeded the threshold value set by TWAI_ERR_WARNING_LIMIT_REG.
- If TWAI_ERR_ST = 1 and TWAI_BUS_OFF_ST = 1: The TWAI controller has entered the BUS_OFF state (due to the TEC >= 256).
- If TWAI_ERR_ST = 0 and TWAI_BUS_OFF_ST = 1: The TWAI controller's TEC has dropped below the threshold value set by TWAI_ERR_WARNING_LIMIT_REG during BUS_OFF recovery.

27.5.3.4 Data Overrun Interrupt (DOI)

The Data Overrun Interrupt (DOI) is triggered whenever the Receive FIFO has overrun. The DOI indicates that the Receive FIFO is full and should be cleared immediately to prevent any further overrun messages.

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The DOI is only triggered by the first message that causes the Receive FIFO to overrun (i.e., the transition from the Receive FIFO not being full to the Receive FIFO overrunning). Any subsequent overrun messages will not trigger the DOI again. The DOI could be triggered again when all received messages (valid or overrun) have been cleared.

27.5.3.5 Error Passive Interrupt (TXI)

The Error Passive Interrupt (EPI) is triggered whenever the TWAI controller switches from Error Active to Error Passive, or vice versa.

27.5.3.6 Arbitration Lost Interrupt (ALI)

The Arbitration Lost Interrupt (ALI) is triggered whenever the TWAI controller is attempting to transmit a message and loses arbitration. The bit position where the TWAI controller lost arbitration is automatically recorded in Arbitration Lost Capture register (TWAI_ARB LOST CAP_REG). When the ALI occurs again, the Arbitration Lost Capture register will no longer record new bit location until it is cleared (via reading this register through the CPU).

27.5.3.7 Bus Error Interrupt (BEI)

The Bus Error Interrupt (BEI) is triggered whenever TWAI controller detects an error on the TWAI bus. When a bus error occurs, the Bus Error type and its bit position are automatically recorded in the Error Code Capture register (TWAI_ERR_CODE_CAP_REG). When the BEI occurs again, the Error Code Capture register will no longer record new error information until it is cleared (via a read from the CPU).

27.5.3.8 Bus Status Interrupt (BSI)

The Bus Status Interrupt (BSI) is triggered whenever TWAI controller is switching between receive/transmit status and idle status. When a BSI occurs, the current status of TWAI controller can be measured by reading TWAI_RX_ST and TWAI_TX_ST in TWAI_STATUS_REG register.

27.5.4 Transmit and Receive Buffers

27.5.4.1 Overview of Buffers

Table 27-8. Buffer Layout for Standard Frame Format and Extended Frame Format

Standard Frame Format (SFF)		Extended Frame Format (EFF)	
TWAI Address	**Content**	**TWAI Address**	**Content**
0x40	TX/RX frame information	0x40	TX/RX frame information
0x44	TX/RX identifier 1	0x44	TX/RX identifier 1
0x48	TX/RX identifier 2	0x48	TX/RX identifier 2
0x4c	TX/RX data byte 1	0x4c	TX/RX identifier 3
0x50	TX/RX data byte 2	0x50	TX/RX identifier 4
0x54	TX/RX data byte 3	0x54	TX/RX data byte 1
0x58	TX/RX data byte 4	0x58	TX/RX data byte 2
0x5c	TX/RX data byte 5	0x5c	TX/RX data byte 3

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Table 27-8 – cont'd from previous page

Standard Frame Format (SFF)		Extended Frame Format (EFF)	
TWAI Address	Content	TWAI Address	Content
0x60	TX/RX data byte 6	0x60	TX/RX data byte 4
0x64	TX/RX data byte 7	0x64	TX/RX data byte 5
0x68	TX/RX data byte 8	0x68	TX/RX data byte 6
0x6c	reserved	0x6c	TX/RX data byte 7
0x70	reserved	0x70	TX/RX data byte 8

Table 27-8 illustrates the layout of the Transmit Buffer and Receive Buffer registers. Both the Transmit and Receive Buffer registers share the same address space and are only accessible when the TWAI controller is in Operation Mode. CPU write operations access the Transmit Buffer registers, and CPU read operations access the Receive Buffer registers. However, both buffers share the exact same register layout and fields to represent a message (received or to be transmitted). The Transmit Buffer registers are used to configure a TWAI message to be transmitted. The CPU would write to the Transmit Buffer registers specifying the message's frame type, frame format, frame ID, and frame data (payload). Once the Transmit Buffer is configured, the CPU would then initiate the transmission by setting the TWAI_TX_REQ bit in TWAI_CMD_REG.

- For a self-reception request, set the TWAI_SELF_RX_REQ bit instead.
- For a single-shot transmission, set both the TWAI_TX_REQ and the TWAI_ABORT_TX simultaneously.

The Receive Buffer registers map the first message in the Receive FIFO. The CPU would read the Receive Buffer registers to obtain the first message's frame type, frame format, frame ID, and frame data (payload). Once the message has been read from the Receive Buffer registers, the CPU can set the TWAI_RELEASE_BUF bit in TWAI_CMD_REG to clear the Receive Buffer registers. If there are still messages in the Receive FIFO, the Receive Buffer registers will map the first message again.

27.5.4.2 Frame Information

The frame information is one byte long and specifies a message's frame type, frame format, and length of data. The frame information fields are shown in Table 27-9.

Table 27-9. TX/RX Frame Information (SFF/EFF) TWAI Address 0x40

Bit 31-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	FF[1]	RTR[2]	X[3]	X[3]	DLC.3[4]	DLC.2[4]	DLC.1[4]	DLC.0[4]

Notes:

1. FF: The Frame Format (FF) bit specifies whether the message is Extended Frame Format (EFF) or Standard Frame Format (SFF). The message is EFF when FF bit is 1, and SFF when FF bit is 0.
2. RTR: The Remote Transmission Request (RTR) bit specifies whether the message is a data frame or a remote frame. The message is a remote frame when the RTR bit is 1, and a data frame when the RTR bit is 0.
3. X: Don't care, can be any value.
4. DLC: The Data Length Code (DLC) field specifies the number of data bytes for a data frame, or the number of data bytes to request in a remote frame. TWAI data frames are limited to a maximum payload of 8 data

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bytes, and thus the DLC should range anywhere from 0 to 8.

27.5.4.3 Frame Identifier

The Frame Identifier fields is two-byte (11-bit) long if the message is SFF, and four-byte (29-bit) long if the message is EFF.

The Frame Identifier fields for an SFF (11-bit) message is shown in Table 27-10-27-11.

Table 27-10. TX/RX Identifier 1 (SFF); TWAI Address 0x44

Bit 31-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3

Table 27-11. TX/RX Identifier 2 (SFF); TWAI Address 0x48

Bit 31-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	ID.2	ID.1	ID.0	X[1]	X[2]	X[2]	X[2]	X[2]

Notes:

1. Don't care. Recommended to be compatible with receive buffer (i.e., set to RTR) in case of using the self reception functionality (or together with self-test functionality).
2. Don't care. Recommended to be compatible with receive buffer (i.e., set to 0) in case of using the self reception functionality (or together with self-test functionality).

The Frame Identifier fields for an EFF (29-bits) message is shown in Table 27-12-27-15.

Table 27-12. TX/RX Identifier 1 (EFF); TWAI Address 0x44

Bit 31-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	ID.28	ID.27	ID.26	ID.25	ID.24	ID.23	ID.22	ID.21

Table 27-13. TX/RX Identifier 2 (EFF); TWAI Address 0x48

Bit 31-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	ID.20	ID.19	ID.18	ID.17	ID.16	ID.15	ID.14	ID.13

Table 27-14. TX/RX Identifier 3 (EFF); TWAI Address 0x4c

Bit 31-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	ID.12	ID.11	ID.10	ID.9	ID.8	ID.7	ID.6	ID.5

Table 27-15. TX/RX Identifier 4 (EFF); TWAI Address 0x50

Bit 31-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	ID.4	ID.3	ID.2	ID.1	ID.0	X[1]	X[2]	X[2]

Notes:

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1. Don't care. Recommended to be compatible with receive buffer (i.e., set to RTR) in case of using the self reception functionality (or together with self-test functionality).
2. Don't care. Recommended to be compatible with receive buffer (i.e., set to 0) in case of using the self reception functionality (or together with self-test functionality).

27.5.4.4 Frame Data

The Frame Data field contains the payloads of transmitted or received data frame, and can range from 0 to eight bytes. The number of valid bytes should be equal to the DLC. However, if the DLC is larger than eight, the number of valid bytes would still be limited to eight. Remote frames do not have data payloads, thus their Frame Data fields will be unused.

For example, when transmitting a data frame with five bytes, the CPU should write five to the DLC field, and then write data to the corresponding register of the first to the fifth data field. Likewise, when receiving a data frame with a DLC of five data bytes, only the first to the fifth data byte will contain valid payload data for the CPU to read.

27.5.5 Receive FIFO and Data Overruns

The Receive FIFO is a 64-byte internal buffer used to store received messages in First In First Out order. A single received message can occupy between three to 13 bytes of space in the Receive FIFO, and their endianness is identical to the register layout of the Receive Buffer registers. The Receive Buffer registers are mapped to the bytes of the first message in the Receive FIFO.

When the TWAI controller receives a message, it will increment the value of TWAI_RX_MESSAGE_COUNTER up to a maximum of 64. If there is adequate space in the Receive FIFO, the message contents will be written into the Receive FIFO. Once a message has been read from the Receive Buffer, the TWAI_RELEASE_BUF bit should be set. This will decrement TWAI_RX_MESSAGE_COUNTER and free the space occupied by the first message in the Receive FIFO. The Receive Buffer will then map to the next message in the Receive FIFO.

A data overrun occurs when the TWAI controller receives a message, but the Receive FIFO lacks the adequate free space to store the received message in its entirety (either due to the message contents being larger than the free space in the Receive FIFO, or the Receive FIFO being completely full).

When a data overrun occurs:

- The free space left in the Receive FIFO is filled with the partial contents of the overrun message. If the Receive FIFO is already full, then none of the overrun message's contents will be stored.
- When data in the Receive FIFO overruns for the first time, a Data Overrun Interrupt will be triggered.
- Each overrun message will still increment the TWAI_RX_MESSAGE_COUNTER up to a maximum of 64.
- The RX FIFO will internally mark overrun messages as invalid. The TWAI_MISS_ST bit can be used to determine whether the message currently mapped to by the Receive Buffer is valid or overrun.

To clear an overrun Receive FIFO, the TWAI_RELEASE_BUF must be called repeatedly until TWAI_RX_MESSAGE_COUNTER is 0. This has the effect of freeing all valid messages in the Receive FIFO and clearing all overrun messages.

The Acceptance Filter allows the TWAI controller to filter out received messages based on their ID (and optionally their first data byte and frame type). Only accepted messages are passed on to the Receive FIFO. The use of

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Acceptance Filters allows a more lightweight operation of the TWAI controller (e.g., less use of Receive FIFO, fewer Receive Interrupts) since the TWAI Controller only need to handle a subset of messages.

The Acceptance Filter configuration registers can only be accessed whilst the TWAI controller is in Reset Mode, since they share the same address spaces as the Transmit Buffer and Receive Buffer registers.

The configuration registers consist of a 32-bit Acceptance Code Value and a 32-bit Acceptance Mask Value. The Acceptance Code value specifies a bit pattern which each filtered bit of the message must match in order for the message to be accepted. The Acceptance Mask Value is able to mask out certain bits of the Code value (i.e., set as “Don’t Care” bits). Each filtered bit of the message must either match the acceptance code or be masked in order for the message to be accepted, as demonstrated in Figure 27-7.

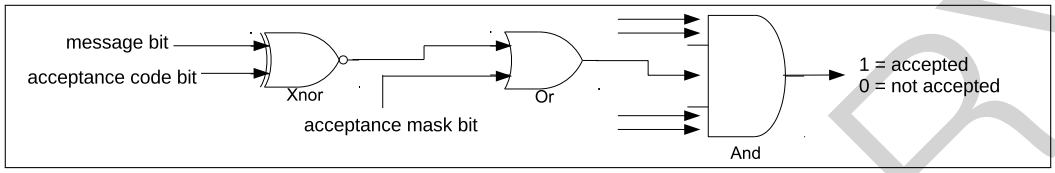


Figure 27-7. Acceptance Filter

The TWAI controller Acceptance Filter allows the 32-bit Acceptance Code and Mask Values to either define a single filter (i.e., Single Filter Mode), or two filters (i.e., Dual Filter Mode). How the Acceptance Filter interprets the 32-bit code and mask values is dependent on whether Single Filter Mode is enabled, and the received message format (i.e., SFF or EFF).

27.5.5.1 Single Filter Mode

Single Filter Mode is enabled by setting the TWAI_RX_FILTER_MODE bit to 1. This will cause the 32-bit code and mask values to define a single filter. The single filter can filter the following bits of a data or remote frame:

- SFF
  - The entire 11-bit ID
  - RTR bit
  - Data byte 1 and Data byte 2
- EFF
  - The entire 29-bit ID
  - RTR bit

The following Figure 27-8 illustrates how the 32-bit code and mask values will be interpreted under Single Filter Mode.

27.5.5.2 Dual FIlter Mode

Dual Filter Mode is enabled by clearing the TWAI_RX_FILTER_MODE bit to 0. This will cause the 32-bit code and mask values to define a two separate filters referred to as filter 1 or filter 2. Under Dual Filter Mode, a message will be accepted if it is accepted by one of the two filters.

The two filters can filter the following bits of a data or remote frame:

- SFF

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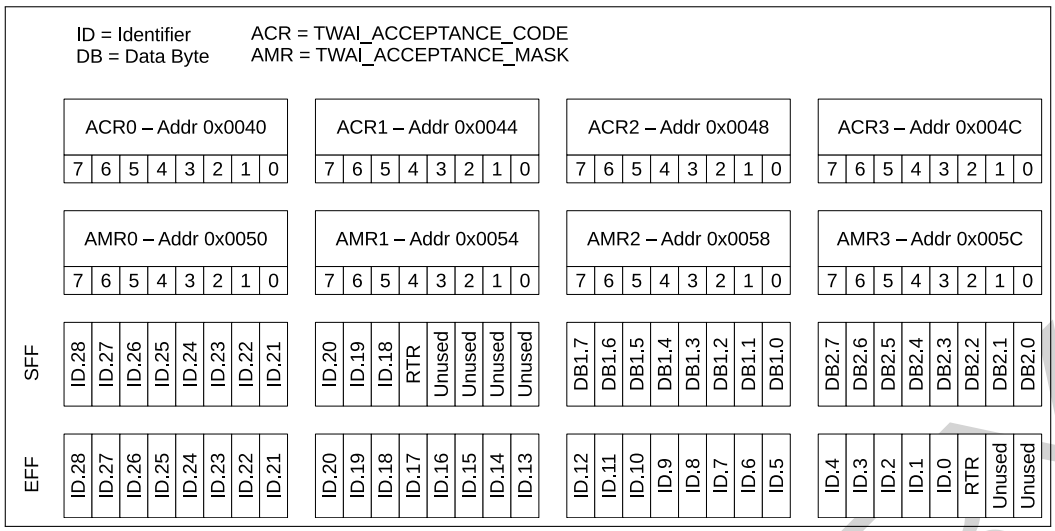


Figure 27-8. Single Filter Mode

  - The entire 11-bit ID
  - RTR bit
  - Data byte 1 (for filter 1 only)

- EFF
  - The first 16 bits of the 29-bit ID

The following Figure 27-9 illustrates how the 32-bit code and mask values will be interpreted in Dual Filter Mode.

27.5.6 Error Management

The TWAI protocol requires that each TWAI node maintains the Transmit Error Count (TEC) and Receive Error Count (REC). The value of both error counts determines the current error state of the TWAI controller (i.e., Error Active, Error Passive, Bus-Off). The TWAI controller stores the TEC and REC values in the TWAI_TX_ERR_CNT_REG and TWAI_RX_ERR_CNT_REG respectively, and they can be read by the CPU anytime. In addition to the error states, the TWAI controller also offers an Error Warning Limit (EWL) feature that can warn the user of the occurrence of severe bus errors before the TWAI controller enters the Error Passive state.

The current error state of the TWAI controller is indicated via a combination of the following values and status bits: TEC, REC, TWAI_ERR_ST, and TWAI_BUS_OFF_ST. Certain changes to these values and bits will also trigger interrupts, thus allowing the users to be notified of error state transitions (see section 27.5.3). The following figure 27-10 shows the relation between the error states, values and bits, and error state related interrupts.

27.5.6.1 Error Warning Limit

The Error Warning Limit (EWL) feature is a configurable threshold value for the TEC and REC, which will trigger an interrupt when exceeded. The EWL is intended to serve as a warning about severe TWAI bus errors, and is triggered before the TWAI controller enters the Error Passive state. The EWL is configured in the TWAI_ERR_WARNING_LIMIT_REG and can only be configured whilst the TWAI controller is in Reset Mode. The TWAI_ERR_WARNING_LIMIT_REG has a default value of 96. When the values of TEC and/or REC are larger than

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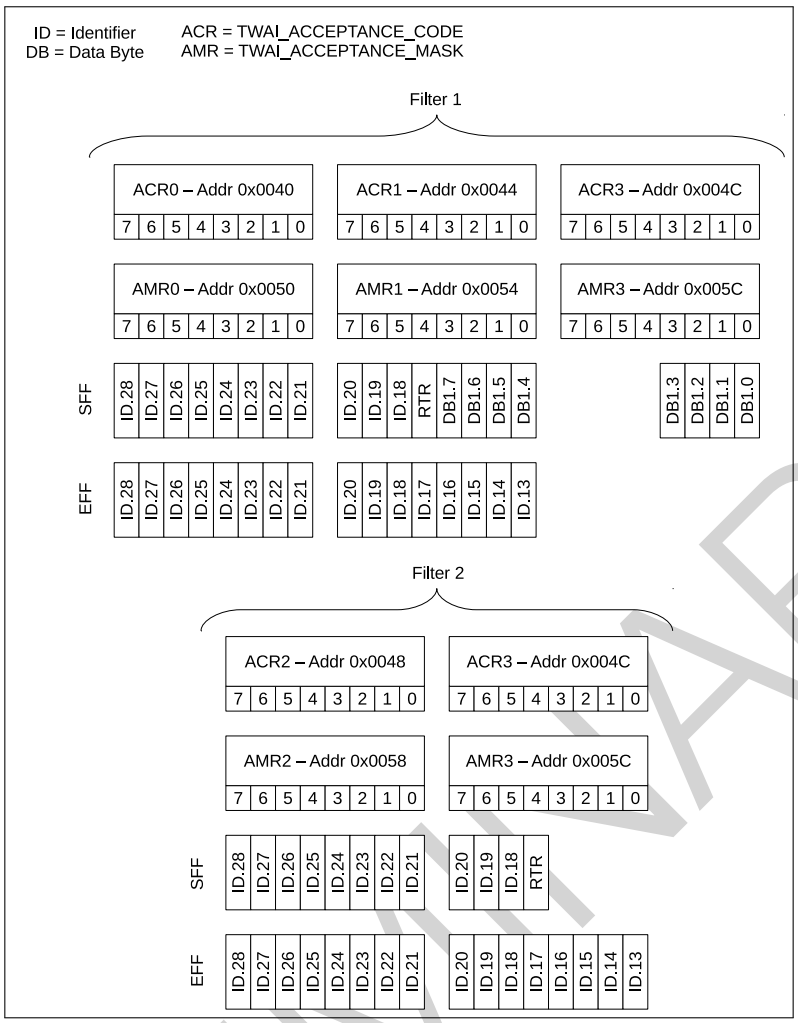


Figure 27-9. Dual Filter Mode

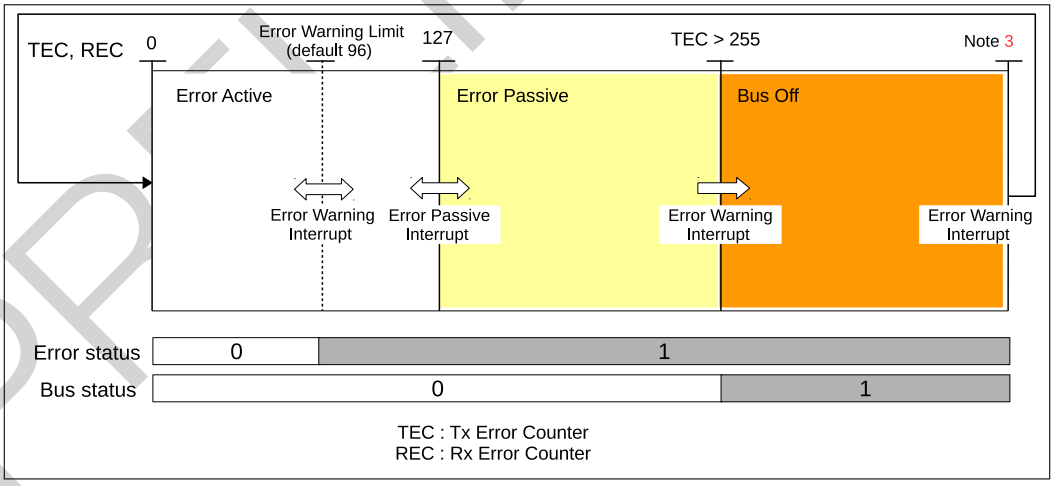


Figure 27-10. Error State Transition

or equal to the EWL value, the TWAI_ERR_ST bit is immediately set to 1. Likewise, when the values of both the TEC and REC are smaller than the EWL value, the TWAI_ERR_ST bit is immediately reset to 0. The Error Warning Interrupt is triggered whenever the value of the TWAI_ERR_ST bit (or the TWAI_BUS_OFF_ST) changes.

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27.5.6.2 Error Passive

The TWAI controller is in the Error Passive state when the TEC or REC value exceeds 127. Likewise, when both the TEC and REC are less than or equal to 127, the TWAI controller enters the Error Active state. The Error Passive Interrupt is triggered whenever the TWAI controller transitions from the Error Active state to the Error Passive state or vice versa.

27.5.6.3 Bus-Off and Bus-Off Recovery

The TWAI controller enters the Bus-Off state when the TEC value exceeds 255. On entering the Bus-Off state, the TWAI controller will automatically do the following:

- Set REC to 0
- Set TEC to 127
- Set the TWAI_BUS_OFF_ST bit to 1
- Enter Reset Mode

The Error Warning Interrupt is triggered whenever the value of the TWAI_BUS_OFF_ST bit (or the TWAI_ERR_ST bit) changes.

To return to the Error Active state, the TWAI controller must undergo Bus-Off Recovery. Bus-Off Recovery requires the TWAI controller to observe 128 occurrences of 11 consecutive recessive bits on the bus. To initiate Bus-Off Recovery (after entering the Bus-Off state), the TWAI controller should enter Operation Mode by setting the TWAI_RESET_MODE bit to 0. The TEC tracks the progress of Bus-Off Recovery by decrementing the TEC each time when the TWAI controller observes 11 consecutive recessive bits. When Bus-Off Recovery has completed (i.e., TEC has decremented from 127 to 0), the TWAI_BUS_OFF_ST bit will automatically be reset to 0, thus triggering the Error Warning Interrupt.

27.5.7 Error Code Capture

The Error Code Capture (ECC) feature allows the TWAI controller to record the error type and bit position of a TWAI bus error in the form of an error code. Upon detecting a TWAI bus error, the Bus Error Interrupt is triggered and the error code is recorded in the TWAI_ERR_CODE_CAP_REG. Subsequent bus errors will trigger the Bus Error Interrupt, but their error codes will not be recorded until the current error code is read from the TWAI_ERR_CODE_CAP_REG.

The following Table 27-16 shows the fields of the TWAI_ERR_CODE_CAP_REG:

Table 27-16. Bit Information of TWAI_ERR_CODE_CAP_REG (0x30)

Bit 31-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	ERRC.1[1]	ERRC.0[1]	DIR[2]	SEG.4[3]	SEG.3[3]	SEG.2[3]	SEG.1[3]	SEG.0[3]

Notes:

- ERRC: The Error Code (ERRC) indicates the type of bus error: 00 for bit error, 01 for format error, 10 for stuff error, 11 for other types of error.
- DIR: The Direction (DIR) indicates whether the TWAI controller was transmitting or receiving when the bus error occurred: 0 for transmitter, 1 for receiver.
- SEG: The Error Segment (SEG) indicates which segment of the TWAI message (i.e., bit position) the bus

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error occurred at.

The following Table 27-17 shows how to interpret the SEG.0 to SEG.4 bits.

Table 27-17. Bit Information of Bits SEG.4 - SEG.0

Bit SEG.4	Bit SEG.3	Bit SEG.2	Bit SEG.1	Bit SEG.0	Description
0	0	0	1	1	start of frame
0	0	0	1	0	ID.28 ~ ID.21
0	0	1	1	0	ID.20 ~ ID.18
0	0	1	0	0	bit SRTR
0	0	1	0	1	bit IDE
0	0	1	1	1	ID.17 ~ ID.13
0	1	1	1	1	ID.12 ~ ID.5
0	1	1	1	0	ID.4 ~ ID.0
0	1	1	0	0	bit RTR
0	1	1	0	1	reserved bit 1
0	1	0	0	1	reserved bit 0
0	1	0	1	1	data length code
0	1	0	1	0	data field
0	1	0	0	0	CRC sequence
1	1	0	0	0	CRC delimiter
1	1	0	0	1	ACK slot
1	1	0	1	1	ACK delimiter
1	1	0	1	0	end of frame
1	0	0	1	0	intermission
1	0	0	0	1	active error flag
1	0	1	1	0	passive error flag
1	0	0	1	1	tolerate dominant bits
1	0	1	1	1	error delimiter
1	1	1	0	0	overload flag

Notes:

- Bit SRTR: under Standard Frame Format.
- Bit IDE: Identifier Extension Bit, 0 for Standard Frame Format.

27.5.8 Arbitration Lost Capture

The Arbitration Lost Capture (ALC) feature allows the TWAI controller to record the bit position where it loses arbitration. When the TWAI controller loses arbitration, the bit position is recorded in the TWAI_ARB LOST CAP_REG and the Arbitration Lost Interrupt is triggered.

Subsequent loses in arbitration will trigger the Arbitration Lost Interrupt, but will not be recorded in the TWAI_ARB LOST CAP_REG until the current Arbitration Lost Capture is read from the TWAI_ERR_CODE_CAP_REG.

Table 27-18 illustrates bits and fields of the TWAI_ERR_CODE_CAP_REG whilst Figure 27-11 illustrates the bit positions of a TWAI message.

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Table 27-18. Bit Information of TWAI_ARB LOST CAP_REG (0x2c)

Bit 31-5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BITNO.4[1]	BITNO.3[1]	BITNO.2[1]	BITNO.1[1]	BITNO.0[1]

Notes:

- BITNO: Bit Number (BITNO) indicates the nth bit of a TWAI message where arbitration was lost.

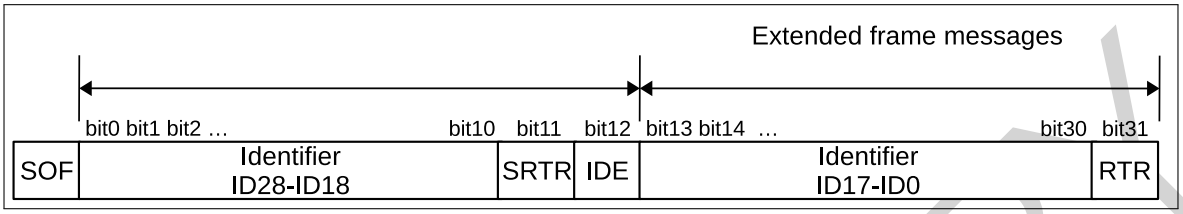


Figure 27-11. Positions of Arbitration Lost Bits

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27.6 Register Summary

'I' here means separate line. The left describes the access in Operation Mode. The right belongs to Reset Mode. The addresses in this section are relative to the [Two-wire Automotive Interface] base address provided in Table 3-3 in Chapter 3 *System and Memory*.

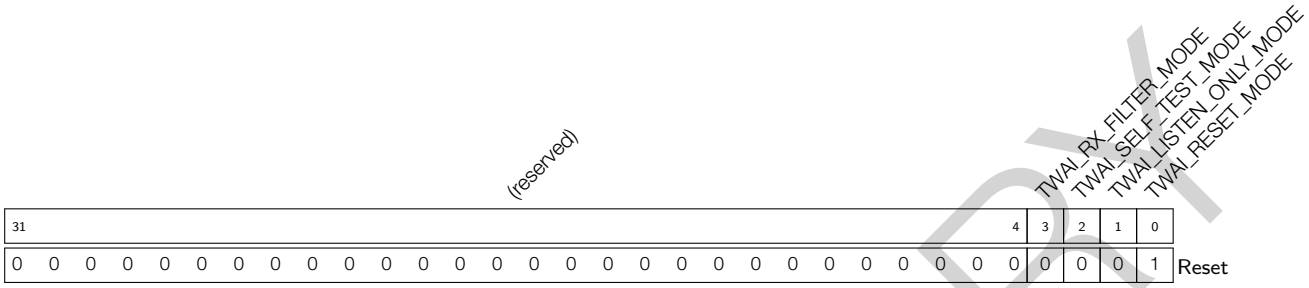
Name	Description	Address	Access
Configuration Registers			
TWAI_MODE_REG	Mode Register	0x0000	R/W
TWAI_BUS_TIMING_0_REG	Bus Timing Register 0	0x0018	RO I R/W
TWAI_BUS_TIMING_1_REG	Bus Timing Register 1	0x001C	RO I R/W
TWAI_ERR_WARNING_LIMIT_REG	Error Warning Limit Register	0x0034	RO I R/W
TWAI_DATA_0_REG	Data Register 0	0x0040	WO I R/W
TWAI_DATA_1_REG	Data Register 1	0x0044	WO I R/W
TWAI_DATA_2_REG	Data Register 2	0x0048	WO I R/W
TWAI_DATA_3_REG	Data Register 3	0x004C	WO I R/W
TWAI_DATA_4_REG	Data Register 4	0x0050	WO I R/W
TWAI_DATA_5_REG	Data Register 5	0x0054	WO I R/W
TWAI_DATA_6_REG	Data Register 6	0x0058	WO I R/W
TWAI_DATA_7_REG	Data Register 7	0x005C	WO I R/W
TWAI_DATA_8_REG	Data Register 8	0x0060	WO I RO
TWAI_DATA_9_REG	Data Register 9	0x0064	WO I RO
TWAI_DATA_10_REG	Data Register 10	0x0068	WO I RO
TWAI_DATA_11_REG	Data Register 11	0x006C	WO I RO
TWAI_DATA_12_REG	Data Register 12	0x0070	WO I RO
TWAI_CLOCK_DIVIDER_REG	Clock Divider Register	0x007C	varies
Contro Registers			
TWAI_CMD_REG	Command Register	0x0004	WO
Status Register			
TWAI_STATUS_REG	Status Register	0x0008	RO
TWAI_ARB LOST CAP_REG	Arbitration Lost Capture Register	0x002C	RO
TWAI_ERR_CODE_CAP_REG	Error Code Capture Register	0x0030	RO
TWAI_RX_ERR_CNT_REG	Receive Error Counter Register	0x0038	RO I R/W
TWAI_TX_ERR_CNT_REG	Transmit Error Counter Register	0x003C	RO I R/W
TWAI_RX_MESSAGE_CNT_REG	Receive Message Counter Register	0x0074	RO
Interrupt Registers			
TWAI_INT_RAW_REG	Interrupt Register	0x000C	RO
TWAI_INT ENA_REG	Interrupt Enable Register	0x0010	R/W

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27.7 Registers

'I' here means separate line. The left describes the access in Operation Mode. The right belongs to Reset Mode with red color. The addresses in this section are relative to the Two-wire Automotive Interface base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 27.1. TWAI_MODE_REG (0x0000)



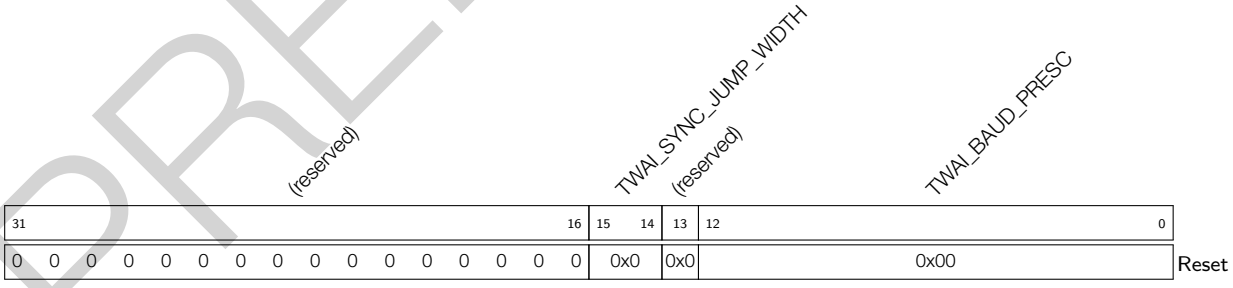
TWAI_RESET_MODE This bit is used to configure the operation mode of the TWAI Controller. 1: Reset mode; 0: Operation mode (R/W)

TWAI_LISTEN_ONLY_MODE 1: Listen only mode. In this mode the nodes will only receive messages from the bus, without generating the acknowledge signal nor updating the RX error counter. (R/W)

TWAI_SELF_TEST_MODE 1: Self test mode. In this mode the TX nodes can perform a successful transmission without receiving the acknowledge signal. This mode is often used to test a single node with the self reception request command. (R/W)

TWAI_RX_FILTER_MODE This bit is used to configure the filter mode. 0: Dual filter mode; 1: Single filter mode (R/W)

Register 27.2. TWAI_BUS_TIMING_0_REG (0x0018)

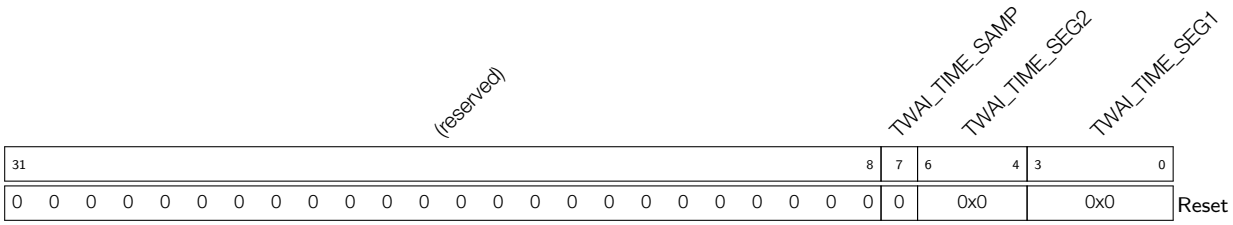


TWAI_BAUD_PRESC Baud Rate Prescaler value, determines the frequency dividing ratio. (RO | R/W)

TWAI_SYNC_JUMP_WIDTH Synchronization Jump Width (SJW), 1 ~ 14 Tq wide. (RO | R/W)

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Register 27.3. TWAI_BUS_TIMING_1_REG (0x001C)

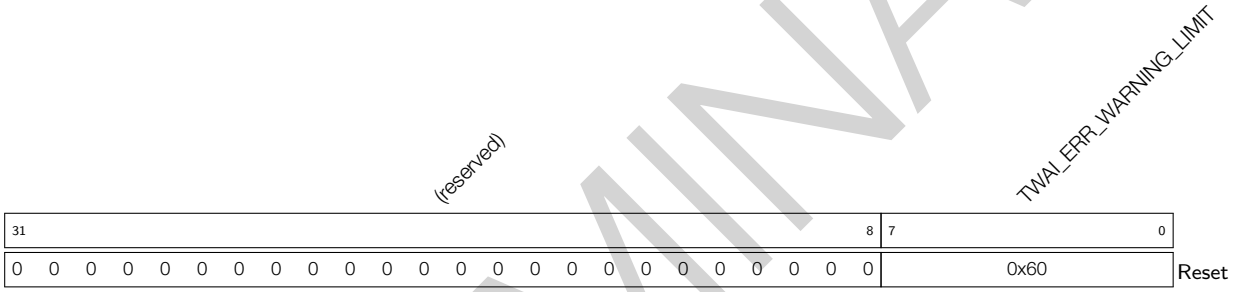


TWAI_TIME_SEG1 The width of PBS1. (RO | R/W)

TWAI_TIME_SEG2 The width of PBS2. (RO | R/W)

TWAI_TIME_SAMP The number of sample points. 0: the bus is sampled once; 1: the bus is sampled three times (RO | R/W)

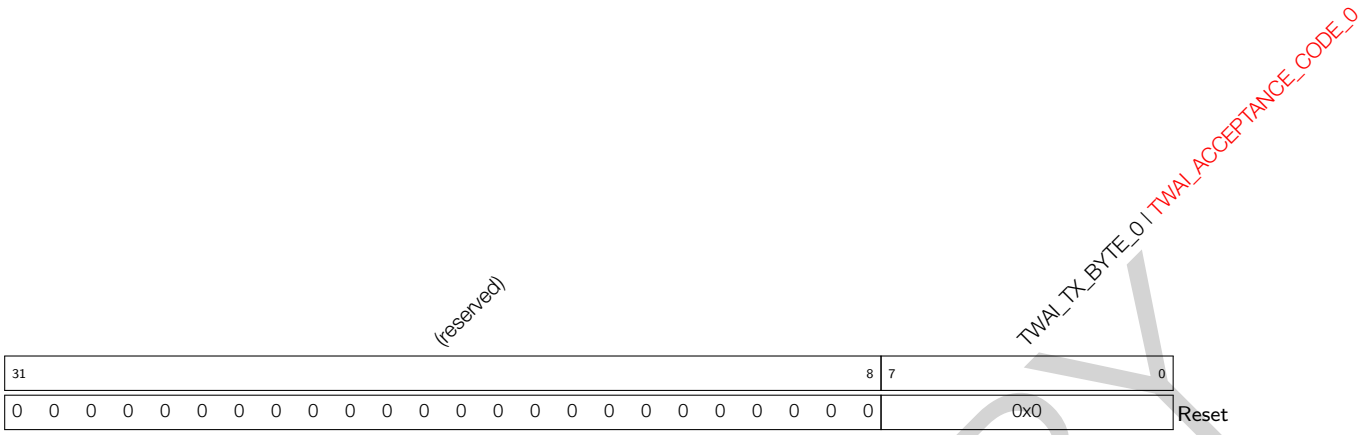
Register 27.4. TWAI_ERR_WARNING_LIMIT_REG (0x0034)



TWAI_ERR_WARNING_LIMIT Error warning threshold. In the case when any of an error counter value exceeds the threshold, or all the error counter values are below the threshold, an error warning interrupt will be triggered (given the enable signal is valid). (RO | R/W)

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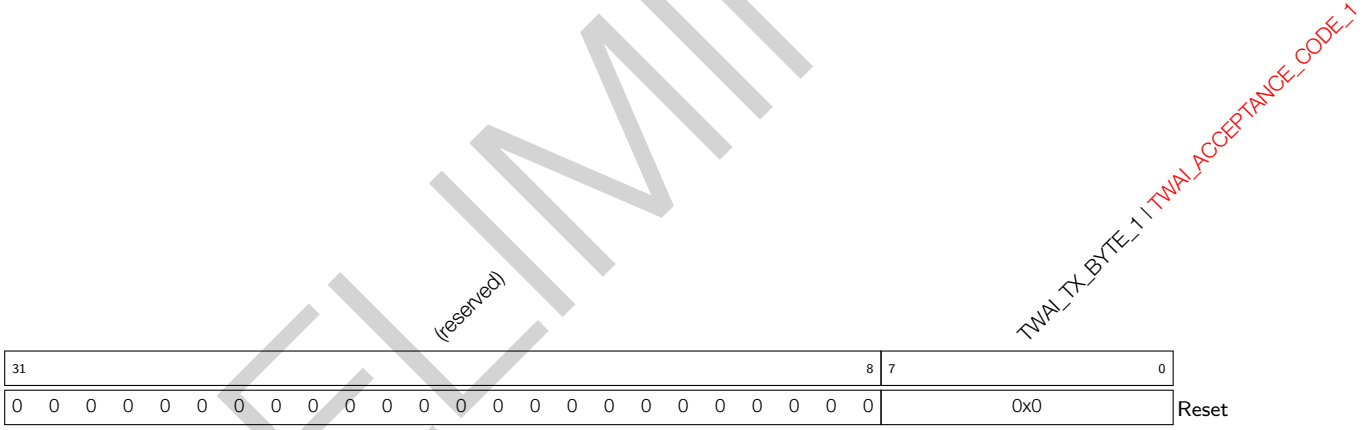
Register 27.5. TWAI_DATA_0_REG (0x0040)



TWAI_TX_BYTE_0 Stored the 0th byte information of the data to be transmitted in operation mode. (WO)

TWAI_ACCEPTANCE_CODE_0 Stored the 0th byte of the filter code in reset mode. (R/W)

Register 27.6. TWAI_DATA_1_REG (0x0044)

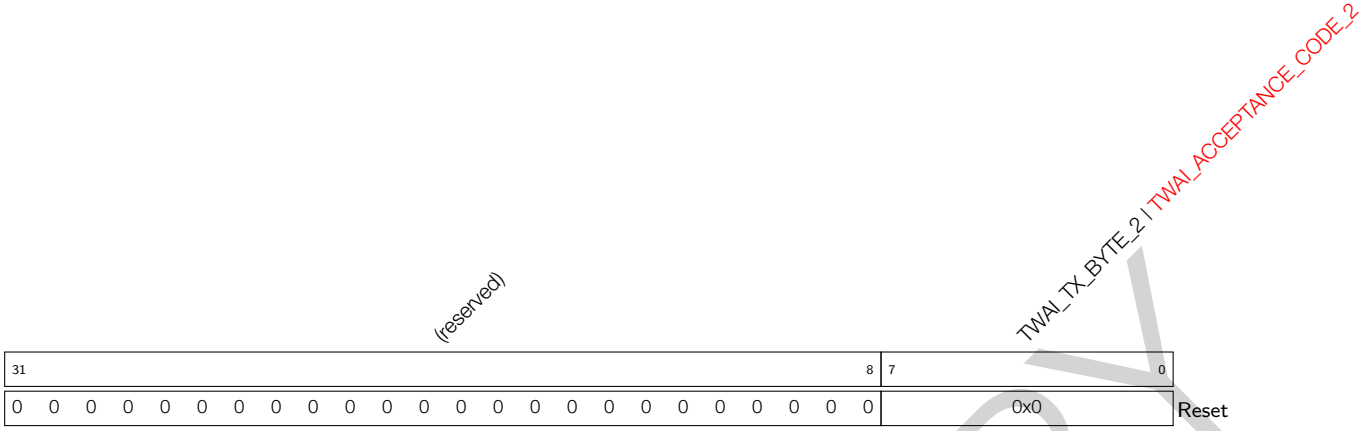


TWAI_TX_BYTE_1 Stored the 1st byte information of the data to be transmitted in operation mode. (WO)

TWAI_ACCEPTANCE_CODE_1 Stored the 1st byte of the filter code in reset mode. (R/W)

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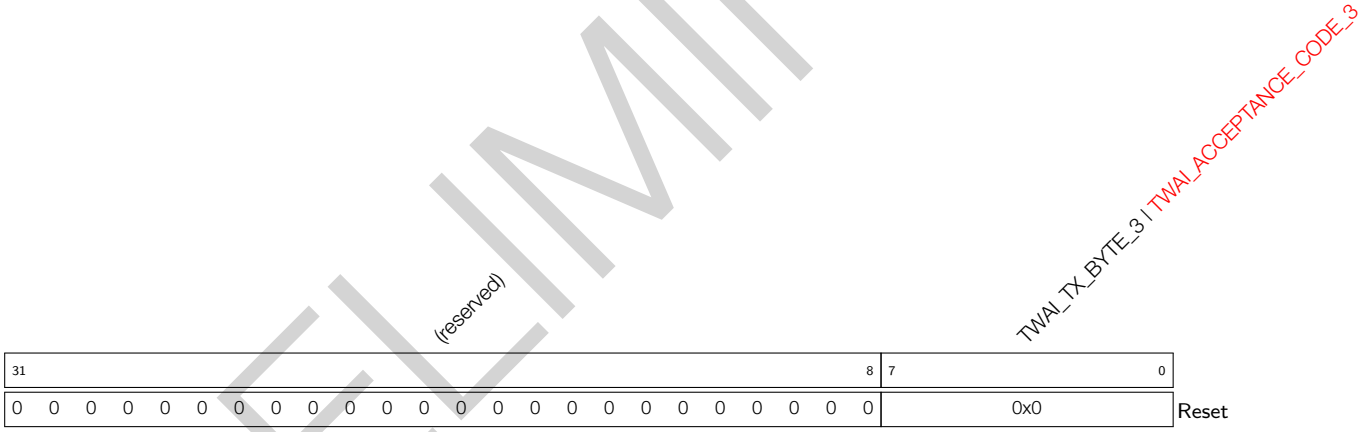
Register 27.7. TWAI_DATA_2_REG (0x0048)



TWAI_TX_BYTE_2 Stored the 2nd byte information of the data to be transmitted in operation mode. (WO)

TWAI_ACCEPTANCE_CODE_2 Stored the 2nd byte of the filter code in reset mode. (R/W)

Register 27.8. TWAI_DATA_3_REG (0x004C)

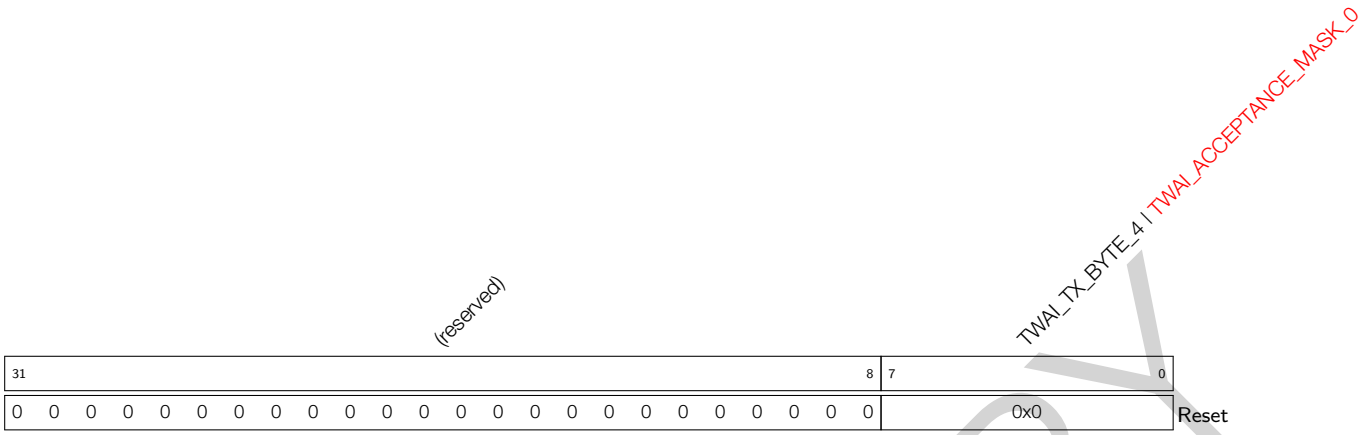


TWAI_TX_BYTE_3 Stored the 3rd byte information of the data to be transmitted in operation mode. (WO)

TWAI_ACCEPTANCE_CODE_3 Stored the 3rd byte of the filter code in reset mode. (R/W)

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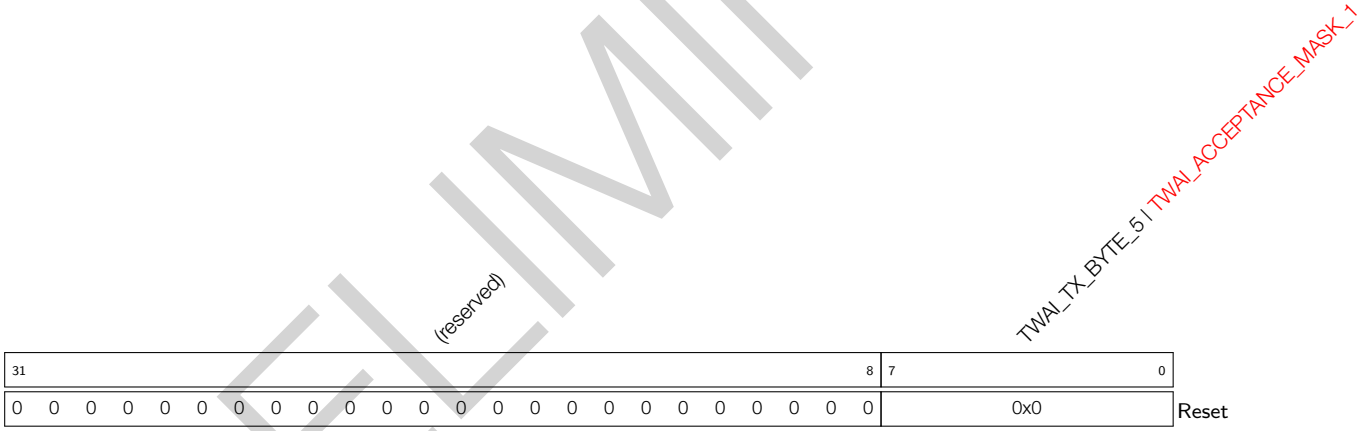
Register 27.9. TWAI_DATA_4_REG (0x0050)



TWAI_TX_BYTE_4 Stored the 4th byte information of the data to be transmitted in operation mode. (WO)

TWAI_ACCEPTANCE_MASK_0 Stored the 0th byte of the filter code in reset mode. (R/W)

Register 27.10. TWAI_DATA_5_REG (0x0054)

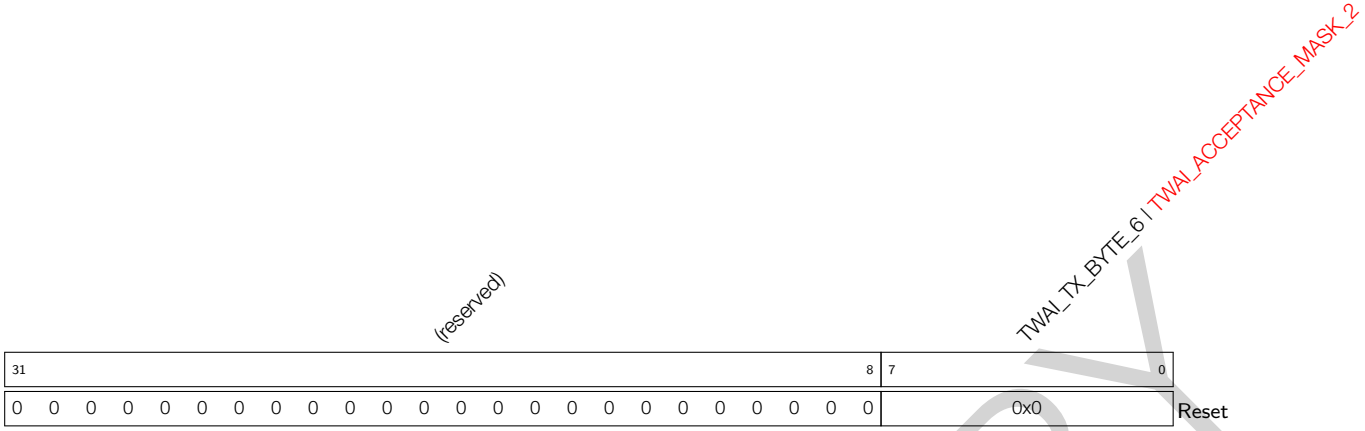


TWAI_TX_BYTE_5 Stored the 5th byte information of the data to be transmitted in operation mode. (WO)

TWAI_ACCEPTANCE_MASK_1 Stored the 1st byte of the filter code in reset mode. (R/W)

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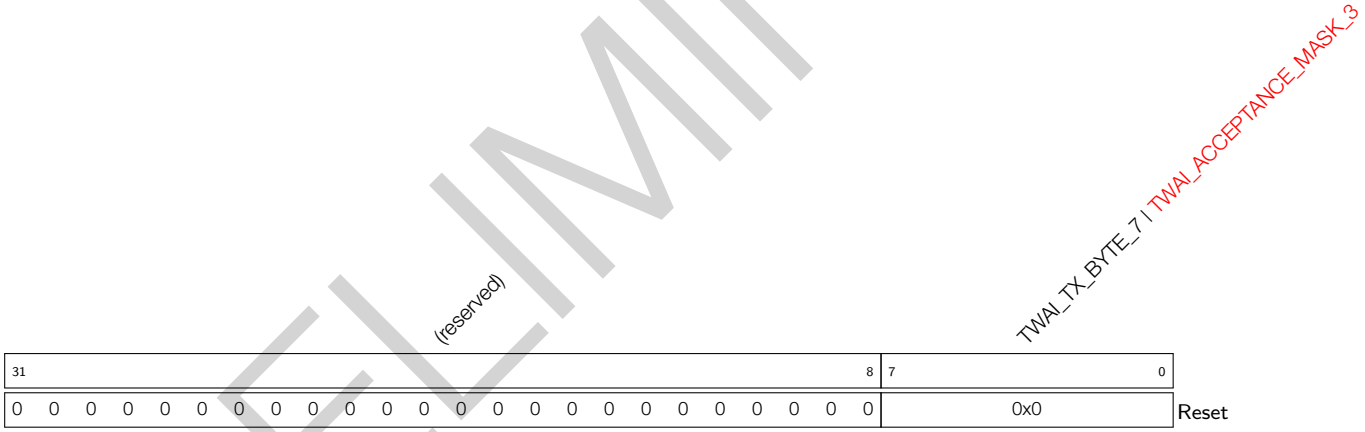
Register 27.11. TWAI_DATA_6_REG (0x0058)



TWAI_TX_BYTE_6 Stored the 6th byte information of the data to be transmitted in operation mode. (WO)

TWAI_ACCEPTANCE_MASK_2 Stored the 2nd byte of the filter code in reset mode. (R/W)

Register 27.12. TWAI_DATA_7_REG (0x005C)

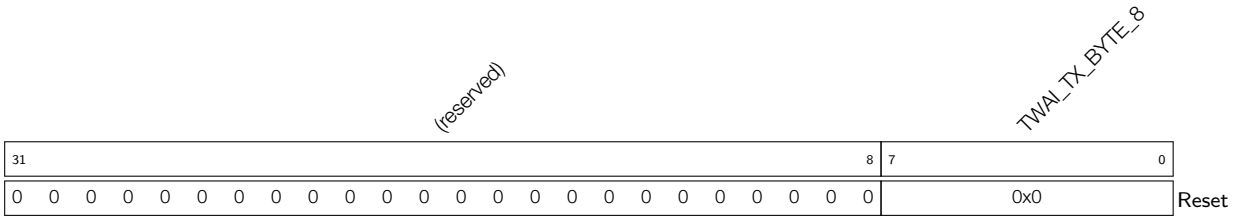


TWAI_TX_BYTE_7 Stored the 7th byte information of the data to be transmitted in operation mode. (WO)

TWAI_ACCEPTANCE_MASK_3 Stored the 3rd byte of the filter code in reset mode. (R/W)

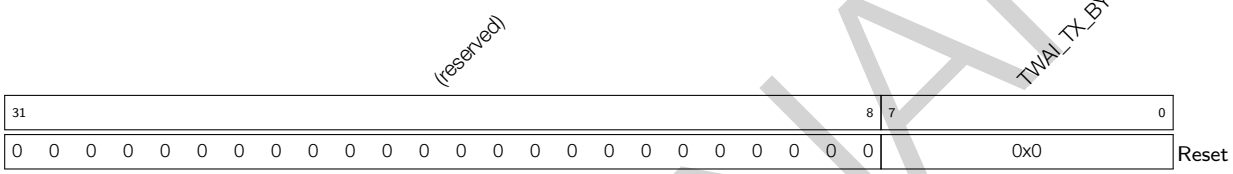
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Register 27.13. TWAI_DATA_8_REG (0x0060)



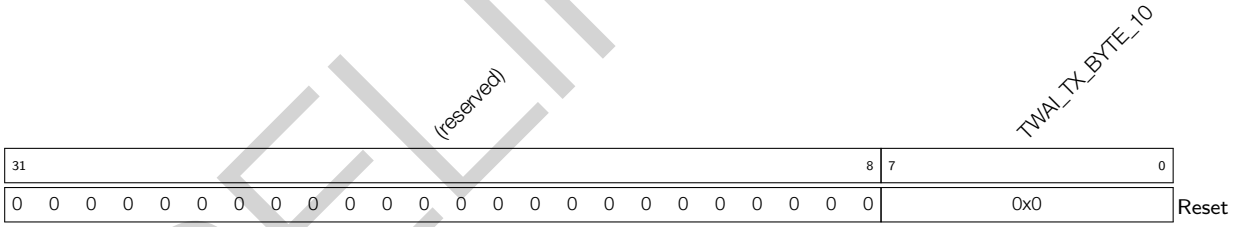
TWAI_TX_BYTE_8 Stored the 8th byte information of the data to be transmitted in operation mode. (WO)

Register 27.14. TWAI_DATA_9_REG (0x0064)



TWAI_TX_BYTE_9 Stored the 9th byte information of the data to be transmitted in operation mode. (WO)

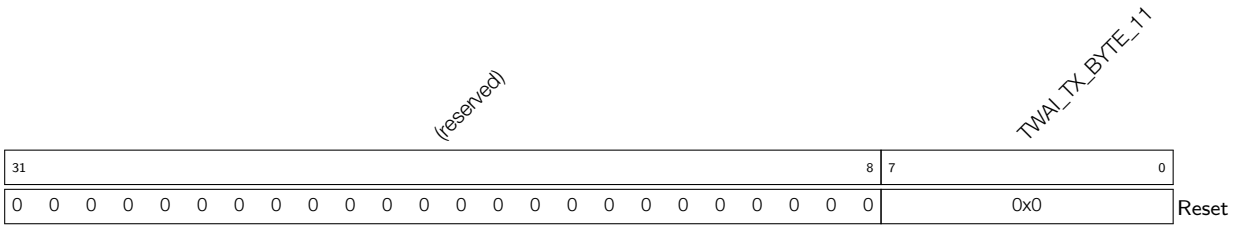
Register 27.15. TWAI_DATA_10_REG (0x0068)



TWAI_TX_BYTE_10 Stored the 10th byte information of the data to be transmitted in operation mode. (WO)

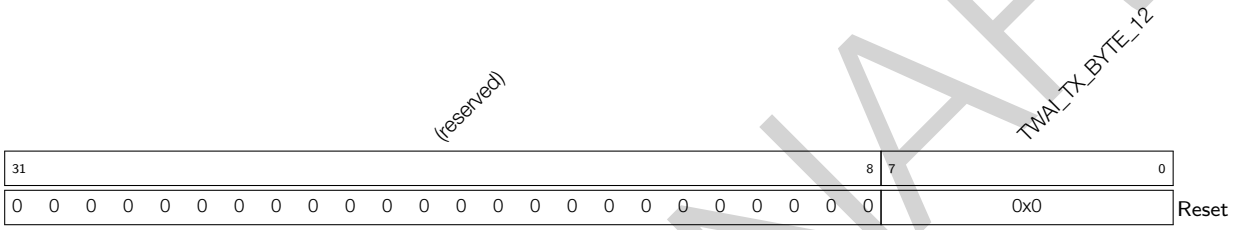
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Register 27.16. TWAI_DATA_11_REG (0x006C)



TWAI_TX_BYTE_11 Stored the 11th byte information of the data to be transmitted in operation mode. (WO)

Register 27.17. TWAI_DATA_12_REG (0x0070)



TWAI_TX_BYTE_12 Stored the 12th byte information of the data to be transmitted in operation mode. (WO)

Register 27.18. TWAI_CLOCK_DIVIDER_REG (0x007C)

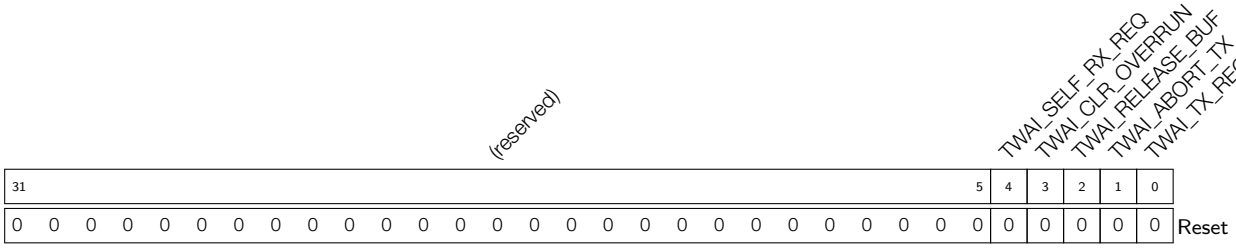


TWAI_CD These bits are used to configure the divisor of the external CLKOUT pin. (R/W)

TWAI_CLOCK_OFF This bit can be configured in reset mode. 1: Disable the external CLKOUT pin; 0: Enable the external CLKOUT pin (RO | R/W)

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Register 27.19. TWAI_CMD_REG (0x0004)



TWAI_TX_REQ Set the bit to 1 to drive nodes to start transmission. (WO)

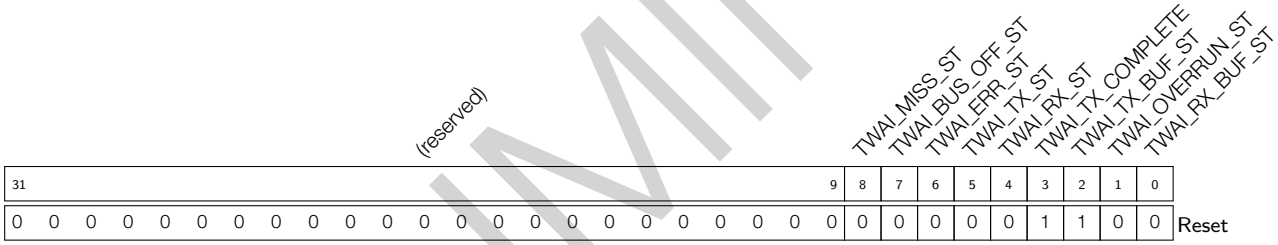
TWAI_ABORT_TX Set the bit to 1 to cancel a pending transmission request. (WO)

TWAI_RELEASE_BUF Set the bit to 1 to release the RX buffer. (WO)

TWAI_CLR_OVERRUN Set the bit to 1 to clear the data overrun status bit. (WO)

TWAI_SELF_RX_REQ Self reception request command. Set the bit to 1 to allow a message be transmitted and received simultaneously. (WO)

Register 27.20. TWAI_STATUS_REG (0x0008)



TWAI_RX_BUF_ST 1: The data in the RX buffer is not empty, with at least one received data packet. (RO)

TWAI_OVERRUN_ST 1: The RX FIFO is full and data overrun has occurred. (RO)

TWAI_TX_BUF_ST 1: The TX buffer is empty, the CPU may write a message into it. (RO)

TWAI_TX_COMPLETE 1: The TWAI controller has successfully received a packet from the bus. (RO)

TWAI_RX_ST 1: The TWAI Controller is receiving a message from the bus. (RO)

TWAI_TX_ST 1: The TWAI Controller is transmitting a message to the bus. (RO)

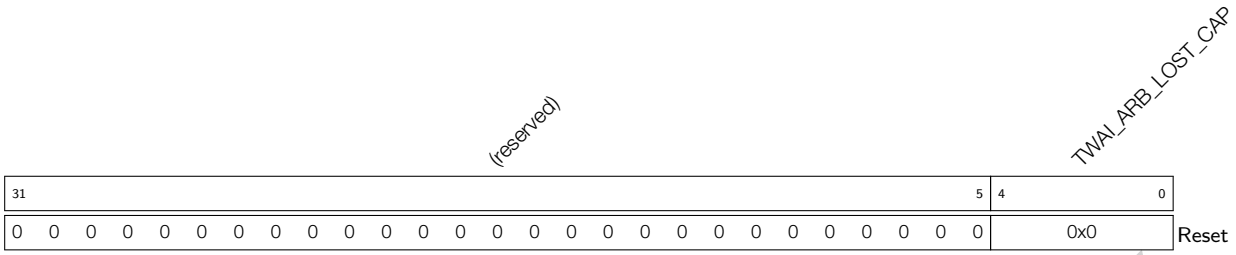
TWAI_ERR_ST 1: At least one of the RX/TX error counter has reached or exceeded the value set in register TWAI_ERR_WARNING_LIMIT_REG. (RO)

TWAI_BUS_OFF_ST 1: In bus-off status, the TWAI Controller is no longer involved in bus activities. (RO)

TWAI_MISS_ST This bit reflects whether the data packet in the RX FIFO is complete. 1: The current packet is missing; 0: The current packet is complete (RO)

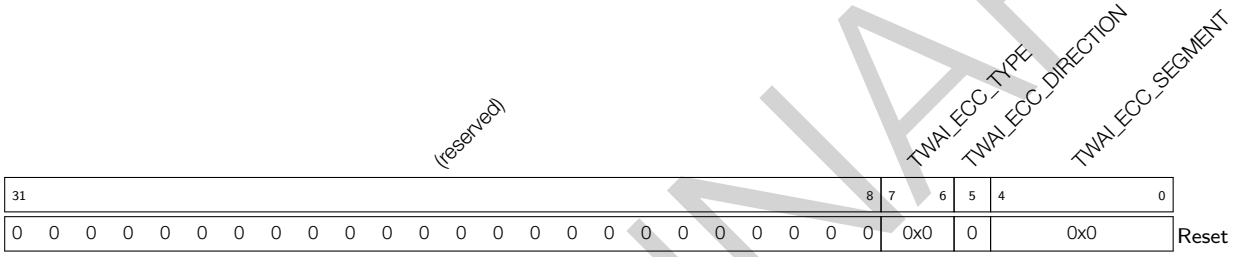
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Register 27.21. TWAI_ARB LOST CAP_REG (0x002C)



TWAI_ARB_LOST_CAP This register contains information about the bit position of lost arbitration. (RO)

Register 27.22. TWAI_ERR_CODE_CAP_REG (0x0030)

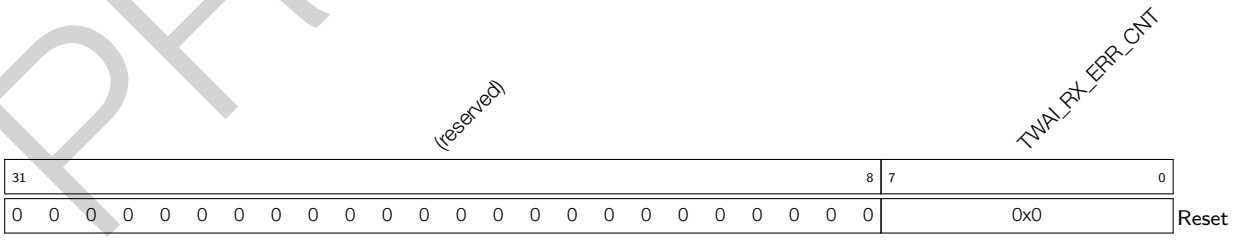


TWAI_ECC_SEGMENT This register contains information about the location of errors, see Table 27-16 for details. (RO)

TWAI_ECC_DIRECTION This register contains information about transmission direction of the node when error occurs. 1: Error occurs when receiving a message; 0: Error occurs when transmitting a message (RO)

TWAI_ECC_TYPE This register contains information about error types: 00: bit error; 01: form error; 10: stuff error; 11: other type of error (RO)

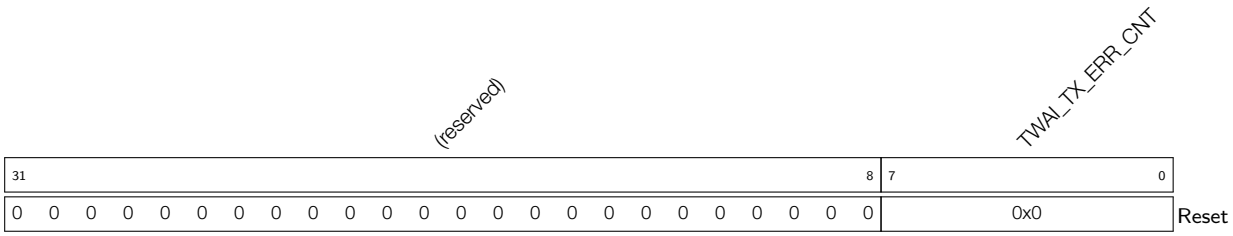
Register 27.23. TWAI_RX_ERR_CNT_REG (0x0038)



TWAI_RX_ERR_CNT The RX error counter register, reflects value changes in reception status. (RO | R/W)

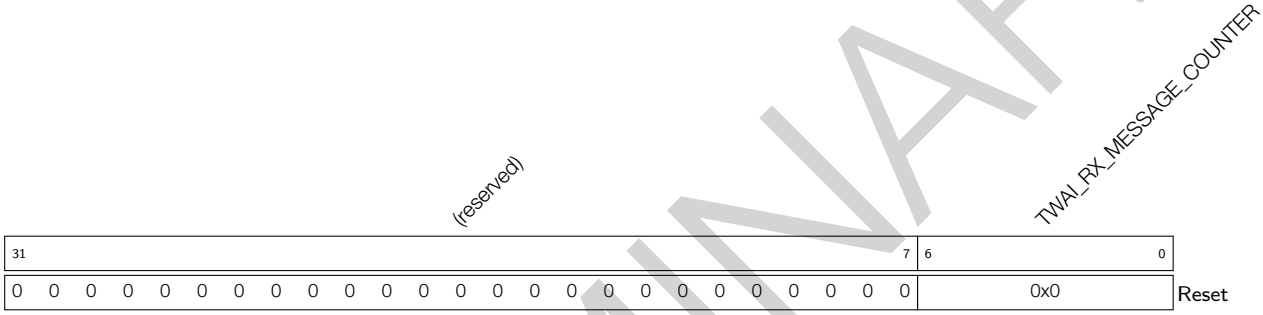
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Register 27.24. TWAI_TX_ERR_CNT_REG (0x003C)



TWAI_TX_ERR_CNT The TX error counter register, reflects value changes in transmission status. (RO | R/W)

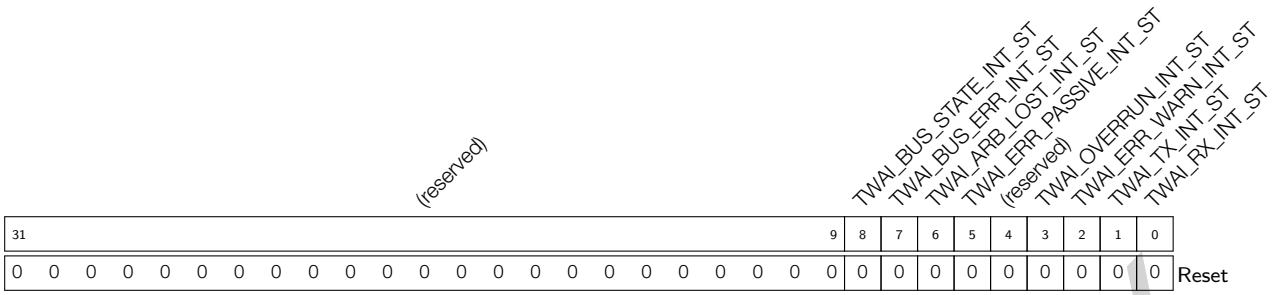
Register 27.25. TWAI_RX_MESSAGE_CNT_REG (0x0074)



TWAI_RX_MESSAGE_COUNTER This register reflects the number of messages available within the RX FIFO. (RO)

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Register 27.26. TWAI_INT_RAW_REG (0x000C)



TWAI_RX_INT_ST Receive interrupt. If this bit is set to 1, it indicates there are messages to be handled in the RX FIFO. (RO)

TWAI_TX_INT_ST Transmit interrupt. If this bit is set to 1, it indicates the message transmission is finished and a new transmission is able to start. (RO)

TWAI_ERR_WARN_INT_ST Error warning interrupt. If this bit is set to 1, it indicates the error status signal and the bus-off status signal of Status register have changed (e.g., switched from 0 to 1 or from 1 to 0). (RO)

TWAI_OVERRUN_INT_ST Data overrun interrupt. If this bit is set to 1, it indicates a data overrun interrupt is generated in the RX FIFO. (RO)

TWAI_ERR_PASSIVE_INT_ST Error passive interrupt. If this bit is set to 1, it indicates the TWAI Controller is switched between error active status and error passive status due to the change of error counters. (RO)

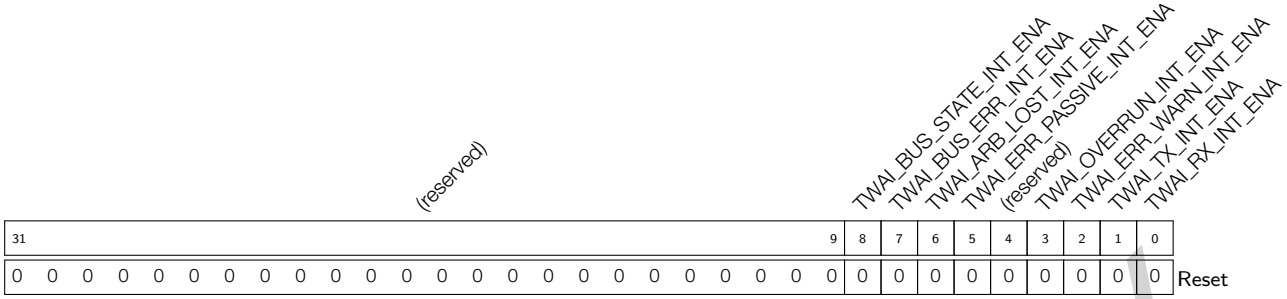
TWAI_ARB_LOST_INT_ST Arbitration lost interrupt. If this bit is set to 1, it indicates an arbitration lost interrupt is generated. (RO)

TWAI_BUS_ERR_INT_ST Error interrupt. If this bit is set to 1, it indicates an error is detected on the bus. (RO)

TWAI_BUS_STATE_INT_ST Bus state interrupt. If this bit is set to 1, it indicates the status of TWAI controller has changed. (RO)

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Register 27.27. TWAI_INT ENA_REG (0x0010)



TWAI_RX_INT_ENA Set this bit to 1 to enable receive interrupt. (R/W)

TWAI_TX_INT_ENA Set this bit to 1 to enable transmit interrupt. (R/W)

TWAI_ERR_WARN_INT_ENA Set this bit to 1 to enable error warning interrupt. (R/W)

TWAI_OVERRUN_INT_ENA Set this bit to 1 to enable data overrun interrupt. (R/W)

TWAI_ERR_PASSIVE_INT_ENA Set this bit to 1 to enable error passive interrupt. (R/W)

TWAI_ARB_LOST_INT_ENA Set this bit to 1 to enable arbitration lost interrupt. (R/W)

TWAI_BUS_ERR_INT_ENA Set this bit to 1 to enable bus error interrupt. (R/W)

TWAI_BUS_STATE_INT_ENA Set this bit to 1 to enable bus state interrupt. (R/W)

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28 USB On-The-Go (USB)

28.1 Overview

The ESP32-S3 features a USB On-The-Go peripheral (henceforth referred to as OTG_FS) along with an integrated transceiver. The OTG_FS can operate as either a USB Host or Device and supports 12 Mbit/s full-speed (FS) and 1.5 Mbit/s low-speed (LS) data rates of the USB 2.0 specification. The Host Negotiation Protocol (HNP) and the Session Request Protocol (SRP) are also supported.

28.2 Features

28.2.1 General Features

- FS and LS data rates
- HNP and SRP as A-device or B-device
- Dynamic FIFO (DFIFO) sizing
- Multiple modes of memory access
  - Scatter/Gather DMA mode
  - Buffer DMA mode
  - Slave mode
- Can choose integrated transceiver or external transceiver
- Utilizing integrated transceiver with USB Serial/JTAG by time-division multiplexing when only integrated transceiver is used
- Support USB OTG using one of the transceivers while USB Serial/JTAG using the other one when both integrated transceiver or external transceiver are used

28.2.2 Device Mode Features

- Endpoint number 0 always present (bi-directional, consisting of EP0 IN and EP0 OUT)
- Six additional endpoints (endpoint numbers 1 to 6), configurable as IN or OUT
- Maximum of five IN endpoints concurrently active at any time (including EP0 IN)
- All OUT endpoints share a single RX FIFO
- Each IN endpoint has a dedicated TX FIFO

28.2.3 Host Mode Features

- Eight channels (pipes)
  - A control pipe consists of two channels (IN and OUT), as IN and OUT transactions must be handled separately. Only Control transfer type is supported.
  - Each of the other seven channels is dynamically configurable to be IN or OUT, and supports Bulk, Isochronous, and Interrupt transfer types.

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- All channels share an RX FIFO, non-periodic TX FIFO, and periodic TX FIFO. The size of each FIFO is configurable.

28.3 Functional Description

28.3.1 Controller Core and Interfaces

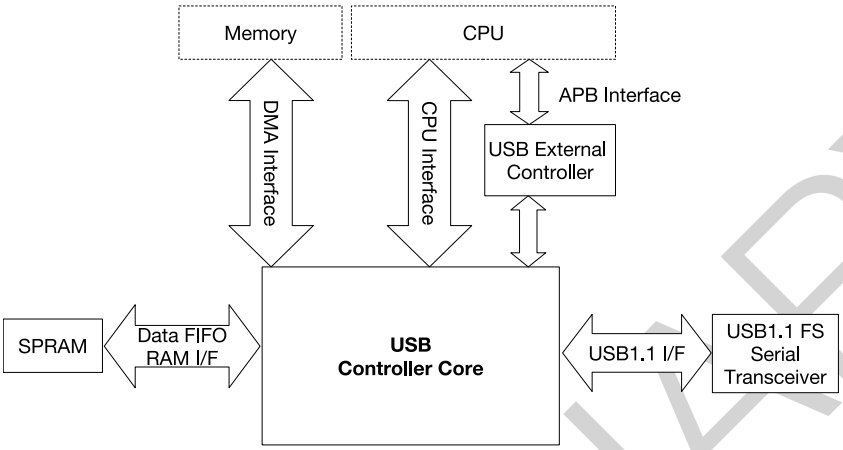


Figure 28-1. OTG_FS System Architecture

The core part of the OTG_FS peripheral is the USB Controller Core. The controller core has the following interfaces (see Figure 28-1):

- **CPU Interface**
  Provides the CPU with read/write access to the controller core's various registers and FIFOs. This interface is internally implemented as an AHB Slave Interface. The way to access the FIFOs through the CPU interface is called Slave mode.
- **APB Interface**
  Allows the CPU to control the USB controller core via the USB external controller.
- **DMA Interface**
  Provides the controller core's internal DMA with read/write access to system memory (e.g., fetching and writing data payloads when operating in DMA mode). This interface is internally implemented as an AHB Master interface.
- **USB 2.0 Interface**
  This interface is used to connect the controller core to a USB 2.0 FS serial transceiver. Aside from USB OTG, ESP32-S3 also includes a USB Serial/JTAG controller (see Chapter 29 *USB Serial/JTAG Controller (USB_SERIAL_JTAG)*). These two USB controllers can utilize the integrated internal transceiver by time-division multiplexing or one USB controller connects to internal transceiver and the other one connects to an external transceiver.

  When only internal transceiver is used, it is shared by USB OTG and USB Serial/JTAG. In default, internal transceiver is connected to USB Serial/JTAG. When RTC_CNTL_SW _HW_USB_PHY_SEL_CFG is 0, the connection of internal transceiver is controlled by efuse bit EFUSE_USB_PHY_SEL. When EFUSE_USB_PHY_SEL is 0, internal transceiver is connected with USB Serial/JTAG. Otherwise, it is connected to USB OTG. When RTC_CNTL_SW _HW_USB_PHY_SEL_CFG is 1, the connection switching is controlled by RTC_CNTL_SW _USB_PHY_SEL_CFG(it has the same meaning with

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EFUSE_USB_PHY_SEL).

When both internal transceiver and external transceiver are used, one USB controller select one of transceivers, the other would select the other transceiver. The specific connection mapping please refer to Chapter 29 *USB Serial/JTAG Controller (USB_SERIAL_JTAG)*.

- **USB External Controller**
  The USB External Controller is primarily used to control the routing of the USB 2.0 FS serial interface to either the internal or external transceiver. The External Controller can also enable a power saving mode by gating the controller core's clock (AHB clock) or powering down the connected SPRAM. Note that this power saving mode is different for the power savings via SRP.
- **Data FIFO RAM Interface**
  The multiple FIFOs used by the controller core are not actually located within the controller core itself, but on the SPRAM (Single-Port RAM). FIFOs are dynamically sized, thus are allocated at run-time in the SPRAM. When the CPU, DMA, or the controller core attempts to read/write to FIFOs, those accesses are routed through the data FIFO RAM interface.

28.3.2 Memory Layout

The following diagram illustrates the memory layout of the OTG_FS registers which are used to configure and control the USB Controller Core. Note that USB External Controller uses a separate set of registers (called wrap registers).

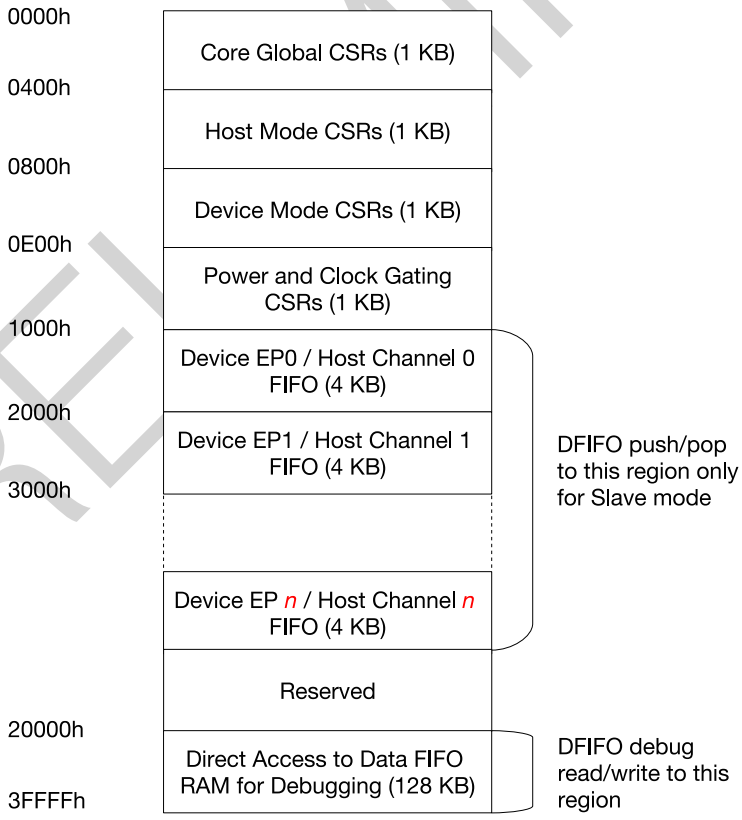


Figure 28-2. OTG_FS Register Layout

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28.3.2.1 Control & Status Registers

- **Global CSRs**
  These registers are responsible for the configuration/control/status of the global features of OTG_FS (i.e., features which are common to both Host and Device modes). These features include OTG control (HNP, SRP, and A/B-device detection), USB configuration (selecting Host or Device mode and PHY selection), and system-level interrupts. Software can access these registers whilst in Host or Device modes.
- **Host Mode CSRs**
  These registers are responsible for the configuration/control/status when operating in Host mode, thus should only be accessed when operating in Host mode. Each channel will have its own set of registers within the Host mode CSRs.
- **Device Mode CSRs**
  These registers are responsible for the configuration/control/status when operating in Device mode, thus should only be accessed when operating in Device mode. Each Endpoint will have its own set of registers within the Device mode CSRs.
- **Power and Clock Gating**
  A single register used to control power-down and gate various clocks.

28.3.2.2 FIFO Access

The OTG_FS makes use of multiple FIFOs to buffer transmitted or received data payloads. The number and type of FIFOs are dependent on Host or Device mode, and the number of channels or endpoints used (see Section 28.3.3). There are two ways to access the FIFOs: DMA mode and Slave mode. When using Slave mode, the CPU will need to access to these FIFOs by reading and writing to either the DFIFO push/pop regions or the DFIFO read/write debug region. FIFO access is governed by the following rules:

- Read access to any address in any one of the 4 KB push/pop regions will result in a pop from the shared RX FIFO.
- Write access to a particular 4 KB push/pop region will result in a push to the corresponding endpoint or channel's TX FIFO given that the endpoint is an IN endpoint, or the channel is an OUT channel.
  - In Device mode, data is pushed to the corresponding IN endpoint's dedicated TX FIFO.
  - In Host mode, data is pushed to the non-periodic TX FIFO or the periodic TX FIFO depending on whether the channel is a non-periodic channel, or a periodic channel.
- Access to the 128 KB read/write region will result in direct read/write instead of a push/pop. This is generally used for debugging purposes only.

Note that pushing and popping data to and from the FIFOs by the CPU is only required when operating in Slave mode. When operating in DMA mode, the internal DMA will handle all pushing/popping of data to and from the TX and RX FIFOs.

28.3.3 FIFO and Queue Organization

The FIFOs in OTG_FS are primarily used to hold data packet payloads (the data field of USB Data packets). TX FIFOs are used to store data payloads that will be transmitted by OUT transactions in Host mode or IN transactions in Device mode. RX FIFOs are used to store received data payloads of IN transactions in Host mode

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or OUT transactions in Device mode. In addition to storing data payloads, RX FIFOs also store a **status entry** for each data payload. Each status entry contains information about a data payload such as channel number, byte count, and validity status. When operating in slave mode, status entries are also used to indicate various channel events.

The portion of SPRAM that can be used for FIFO allocation has a depth of 256 and a width of 35 bits (32 data bits plus 3 control bits). The multiple FIFOs used by each channel (in Host mode) or endpoint (in Device mode) are allocated into the SPRAM and can be dynamically sized.

28.3.3.1 Host Mode FIFOs and Queues

The following FIFOs are used when operating in Host mode (see Figure 28-3):

- **Non-periodic TX FIFO**: Stores data payloads of bulk and control OUT transactions for all channels.
- **Periodic TX FIFO**: Stores data payloads of interrupt or isochronous OUT transactions for all channels.
- **RX FIFO**: Stores data payloads of all IN transactions, and status entries that are used to indicate size of data payloads and transaction/channel events such as transfer complete or channel halted.

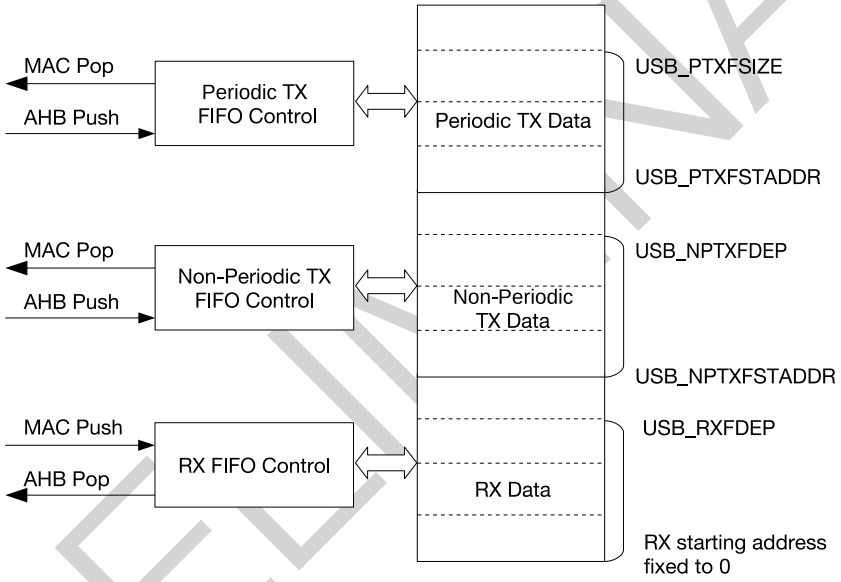


Figure 28-3. Host Mode FIFOs

In addition to FIFOs, Host mode also contains two request queues used to queue up the various transaction request from the multiple channels. Each entry in a request queue holds the IN/OUT channel number along with other information to perform the transaction (such as transaction type). Request queues are also used to queue other types of requests such as a channel halt request.

Unlike FIFOs, request queues are fixed in size and cannot be accessed directly by software. Rather, once a channel is enabled, requests will be automatically written to the request queue by the Host core. The order in which the requests are written into the queue determines the sequence of transactions on the USB.

Host mode contains the following request queues:

- **Non-periodic request queue**: Request queue for all non-periodic channels (bulk and control). The queue has a depth of four entries.

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- **Periodic request queue**: Request queue for all periodic channels (interrupt and isochronous). The queue has a depth of eight entries.

When scheduling transactions, hardware will execute all requests on the periodic request queue first before executing requests on the non-periodic request queue.

28.3.3.2 Device Mode FIFOs

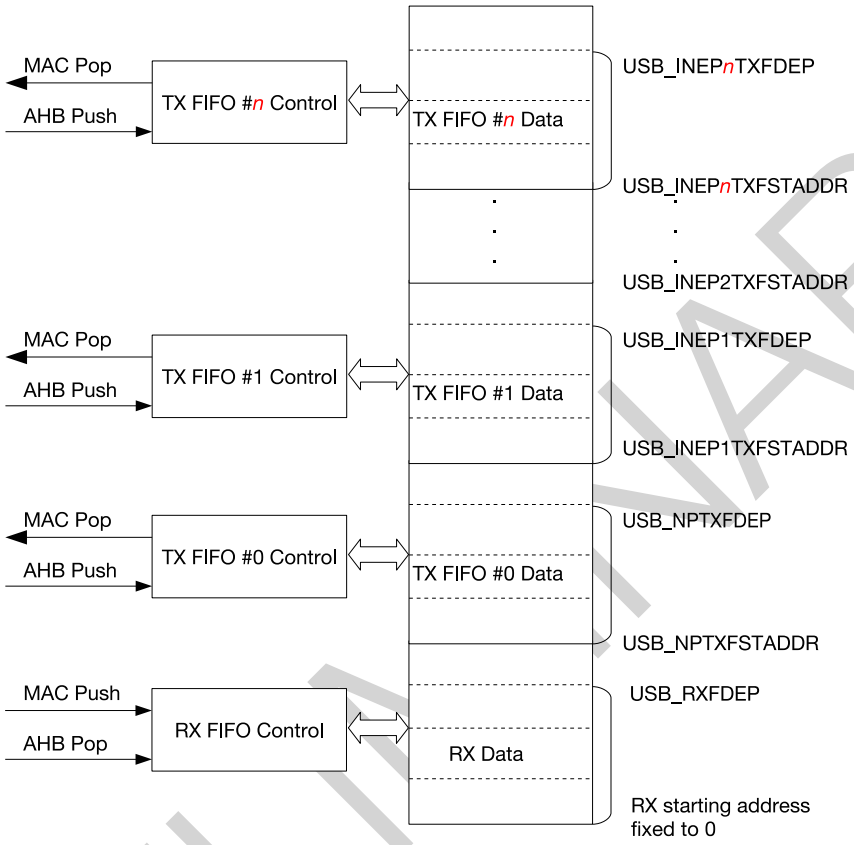


Figure 28-4. Device Mode FIFOs

The following FIFOs are used when operating in Device mode (See Figure 28-4):

- **RX FIFO**: Stores data payloads received in Data packet, and status entries (used to indicate size of those data payloads).
- **Dedicated TX FIFO**: Each active IN endpoint will have a dedicated TX FIFO used to store all IN data payloads of that endpoint, regardless of the transaction type (both periodic and non-periodic IN transactions).

Due to the dedicated FIFOs, Device mode does not use any request queues. Instead, the order of IN transactions are determined by the Host.

28.3.4 Interrupt Hierarchy

OTG_FS provides a single interrupt line which can be routed via the interrupt matrix to one of the CPUs. The interrupt signal can be unmasked by setting USB_GLBLINTRMSK. The OTG_FS interrupt is an OR of all bits in the USB_GINTSTS_REG register, and the bits in USB_GINTSTS_REG can be unmasked by setting the corresponding bits in the USB_GINTMSK_REG register. USB_GINTSTS_REG contains system level interrupts,

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and also specific bits for Host or Device mode interrupts, and OTG specific interrupts. OTG_FS interrupt sources are organized as Figure 28-5 shows.

The following bits of the USB_GINTSTS_REG register indicate an interrupt source lower in the hierarchy:

- **USB_PRTINT** indicates that the Host port has a pending interrupt. The USB_HPRT_REG register indicates the interrupt source.
- **USB_HCHINT** indicates that one or more Host channels have a pending interrupt. Read the USB_HAINT_REG register to determine which channel(s) have a pending interrupt, then read the pending channel's USB_HCINT*n*_REG register to determine the interrupt source.
- **USB_OEPINT** indicates that one or more OUT endpoints have a pending interrupt. Read the USB_DAINT_REG register to determine which OUT endpoint(s) have a pending interrupt, then read the USB_DOEPINT*n*_REG register to determine the interrupt source.
- **USB_IEPINT** indicates that one or more IN endpoints have a pending interrupt. Read the USB_DAINT_REG register to determine which IN endpoint(s) are pending, then read the pending IN endpoint's USB_DIEPINT*n*_REG register to determine the interrupt source.
- **USB_OTGINT** indicates an On-The-Go event has triggered an interrupt. Read the USB_GOTGINT_REG register to determine which OTG event(s) triggered the interrupt.

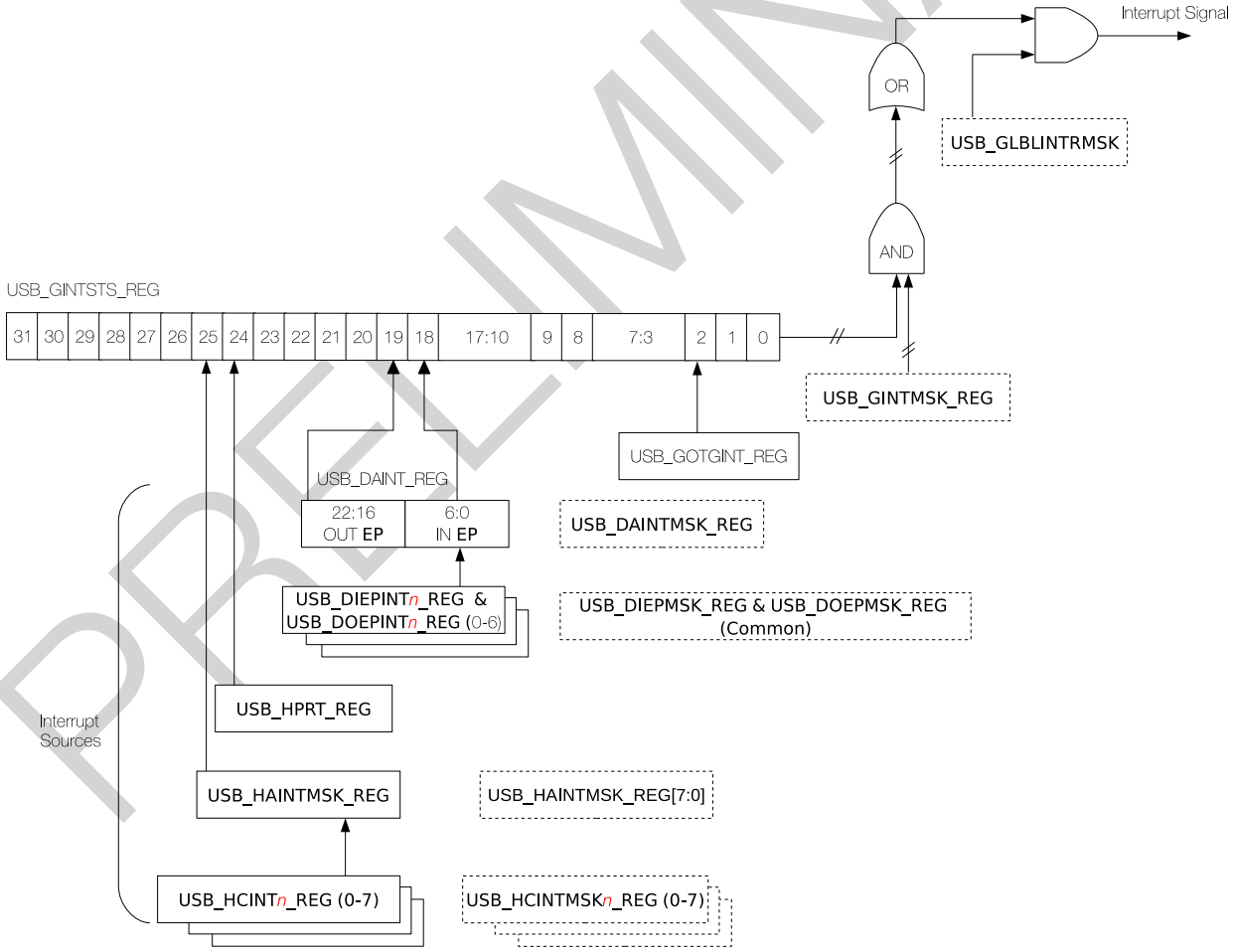


Figure 28-5. OTG_FS Interrupt Hierarchy

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28.3.5 DMA Modes and Slave Mode

USB On-The-Go supports three ways to access memory: Scatter/Gather DMA mode, Buffer DMA mode, and Slave mode.

28.3.5.1 Slave Mode

When operating in Slave mode, all data payloads must be pushed/popped to and from the FIFOs by the CPU.

- When transmitting a packet using IN endpoints or OUT channels, the data payload must be pushed into the corresponding endpoint or channel's TX FIFO.
- When receiving a packet, the packet's status entry must first be popped off the RX FIFO by reading USB_GRXSTSP_REG. The status entry should be used to determine the length of the packet's payload (in bytes). The corresponding number of bytes must then be manually popped off the RX FIFO by reading from the RX FIFO's memory region.

28.3.5.2 Buffer DMA Mode

Buffer mode is similar to Slave mode but utilizes the internal DMA to push and pop data payloads to the FIFOs.

- When transmitting a packet using IN endpoints or OUT channels, the data payload's address in memory should be written to the USB_HCDMA*n*_REG (in Host mode) or USB_DOEPDMA*n*_REG (in Device mode) registers. When the endpoint or channel is enabled, the internal DMA will push the data payload from memory into the TX FIFO of the channel or endpoint.
- When receiving a packet using OUT endpoints or IN channels, the address of an empty buffer in memory should be written to the USB_HCDMA*n*_REG (in Host mode) or USB_DOEPDMA*n*_REG (in Device mode) registers. When the endpoint or channel is enabled, the internal DMA will pop the data payload from RX FIFO into the buffer.

28.3.5.3 Scatter/Gather DMA Mode

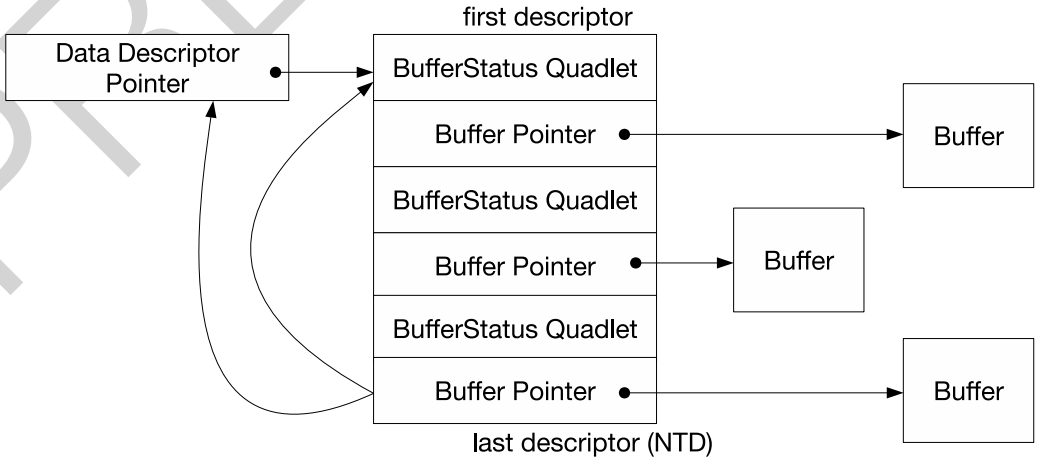


Figure 28-6. Scatter/Gather DMA Descriptor List

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When operating in Scatter/Gather DMA mode, buffers containing data payloads can be scattered throughout memory. Each endpoint or channel will have a contiguous DMA descriptor list, where each descriptor contains a 32-bit pointer to the data payload or buffer and a 32-bit buffer descriptor (BufferStatus Quadlet). The data payloads and buffers can correspond to a single transaction (i.e., < 1 MPS bytes) or an entire transfer (> 1 MPS bytes). (MPS: maximum packet size) The list is implemented as a ring buffer meaning that the DMA will return to the first entry when it encounters the last entry on the list.

- When transmitting a transfer/transaction using IN endpoints or OUT channels, the DMA will gather the data payloads from the multiple buffers and push them into a TX FIFO.
- When receiving a transfer/transaction using OUT endpoints or IN channels, the DMA will pop the received data payloads from the RX FIFO and scatter them to the multiple buffers pointed to by the DMA list entries.

28.3.6 Transaction and Transfer Level Operation

When operating in either Host or Device mode, communication can operate either at the transaction level or the transfer level.

28.3.6.1 Transaction and Transfer Level in DMA Mode

When operating at the transfer level in DMA Host mode, software is interrupted only when a channel has been halted. Channels are halted when their programmed transfer size has completed successfully, has received a STALL, or if there are excessive transaction errors (i.e., 3 consecutive transaction errors). When operating in DMA Device mode, all errors are handled by the controller core itself.

When operating at the transaction level in DMA mode, the transfer size is set to the size of one data packet (either a maximum packet size or a short packet size).

28.3.6.2 Transaction and Transfer Level in Slave Mode

When operating at the transaction level in Slave Mode, transfers are handled one transaction at a time. Each data payload should correspond to a single data packet, and software must determine whether a retry of the transaction is necessary based on the handshake response received on the USB (e.g., ACK or NAK).

The following table describes transaction level operation in Slave mode for both IN and OUT transactions.

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Table 28-1. IN and OUT Transactions in Slave Mode

Host Mode	Device Mode
OUT Transactions	
1. Software specifies the size of the data packet and the number of data packets (1 data packet) in the USB_HCTSIZ*n*_REG register, enables the channel, then copies the packet's data payload into the TX FIFO. 2. When the last DWORD of the data payload has been pushed, the controller core will automatically write a request into the appropriate request queue. 3. If the transaction was successful, the USB_XFERCOMPL interrupt will be generated. If the transaction was unsuccessful, an error interrupt (e.g. USB_H_NACK*n*) will occur.	1. Software specifies the expected size of the data packet (1 MPS) and the number of data packets (1 data packet) in the USB_DIEPTSIZ*n*_REG register. Once the endpoint is enabled, it will wait for the host to transmit a packet to it. 2. The received packet will be pushed into the RX FIFO along with a packet status entry. 3. If the transaction was unsuccessful (e.g., due to a full RX FIFO), the endpoint will automatically NAK the incoming packet.
IN Transactions	
1. Software specifies the expected size of the data packet and the number of packets (1 data packet) in the USB_HCTSIZ*n*_REG register, then enables the channel. 2. The controller core will automatically write a request into the appropriate request queue. 3. If the transaction was successful, the received data along with a status entry should be written to the RX FIFO. If the transaction was unsuccessful, an error interrupt (e.g., USB_H_NACK*n*) will occur.	1. Software specifies the size of the data packet and the number of data packets (1 data packet) in the USB_DIEPTSIZ*n*_REG register. Once the endpoint is enabled, it will wait for the host to read the packet. 2. When the packet has been transmitted, the USB_XFERCOMPL interrupt will be generated.

When operating at the transfer level in Slave mode, one or more transaction-level operations can be pipelined thus being analogous to transfer level operation in DMA mode. Within pipelined transactions, multiple packets of the same transfer can be read/written from the FIFOs in single instance, thus preventing the need for interrupting the software on a per-packet basis.

Operating on a transfer level in Slave mode is similar to operating on the transaction-level, except the transfer size and packet count for each transfer in the USB_HCTSIZ*n*_REG or USB_DIEPTSIZ*n*_REG register will need to be set to reflect the entire transfer. After the channel or endpoint is enabled, multiple data packets worth of payloads should be written to or read from the TX or RX FIFOs respectively (given that there is enough space or enough data).

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28.4 OTG

USB OTG allows OTG devices to act in the USB Host role or the USB Device role. Thus, OTG devices will typically have a Mini-AB or Micro-AB receptacle so that it can receive an A-plug or B-plug. OTG devices will become either an A-device or a B-device depending on whether an A-plug or a B-plug is connected.

- A-device defaults to the Host role (A-Host) whilst B-device defaults to the Device role (B-Peripheral).
- A-device and B-device may exchange roles by using the Host Negotiation Protocol (HNP), thus becoming A-peripheral and B-Host.
- A-device can turn off Vbus to save power. B-device can then wake up the A-device by requesting it to turn on Vbus and start a new session. This mechanism is called session request protocol (SRP).
- A-device always powers Vbus even if it is an A-peripheral.

OTG devices are able to determine whether they are connected to an A plug or a B plug using the ID pin of the plugs. The ID pin in A-plugs are pulled to ground whilst B-plugs have the ID pin left floating.

28.4.1 OTG Interface

The OTG_FS supports both the Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) of the OTG Revision 1.3 specification. The OTG_FS controller core interfaces with the transceiver (internal or external) using the UTMI+ OTG interface. The UTMI+ OTG interface allows the controller core to manipulate the transceiver for OTG purposes (e.g., enabling/disabling pull-ups and pull-downs in HNP), and also allows the transceiver to indicate OTG related events. If an external transceiver is used instead, the UTMI+ OTG interface signals will be routed to the ESP32-S3's GPIOs instead through GPIO Matrix, please refer to Chapter 5 *IO MUX and GPIO Matrix (GPIO, IO MUX)*. The UTMI+ OTG interface signals are described in Table 28-2.

Table 28-2. UTMI OTG Interface

Signal Name	I/O	Description
usb_otg_iddig_in	I	Mini A/B Plug Indicator. Indicates whether the connected plug is mini-A or mini-B. Valid only when usb_otg_idpullup is sampled asserted. 1'b0: Mini-A connected 1'b1: Mini-B connected
usb_otg_avalid_in	I	A-Peripheral Session Valid. Indicates if the voltage Vbus is at a valid level for an A-peripheral session. The comparator thresholds are: 1'b0: Vbus <0.8 V 1'b1: Vbus = 0.2 V to 2.0 V
usb_otg_bvalid_in	I	B-Peripheral Session Valid. Indicates if the voltage Vbus is at a valid level for a B-peripheral session. The comparator thresholds are: 1'b0: Vbus <0.8 V 1'b1: Vbus = 0.8 V to 4 V
usb_otg_vbusvalid_in	I	Vbus Valid. Indicates if the voltage Vbus is valid for A/B-device/peripheral operation. The comparator thresholds are: 1'b0: Vbus <4.4 V 1'b1: Vbus >4.75 V

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Signal Name	I/O	Description
usb_srp_sessend_in	I	B-device Session End. Indicates if the voltage Vbus is below the B-device Session End threshold. The comparator thresholds are: 1'b0: Vbus >0.8 V 1'b1: Vbus <0.2 V
usb_otg_idpullup	O	Analog ID input Sample Enable. Enables sampling the analog ID line. 1'b0: ID pin sampling disabled 1'b1: ID pin sampling enabled
usb_otg_dppulldown	O	D+ Pull-down Resistor Enable. Enables the 15 kΩ pull-down resistor on the D+ line.
usb_otg_dmpulldown	O	D- Pull-down Resistor Enable. Enables the 15 kΩ pull-down resistor on the D- line.
usb_otg_drvvbus	O	Drive Vbus. Enables driving Vbus to 5 V. 1'b0: Do not drive Vbus 1'b1: Drive Vbus
usb_srp_chrgvbus	O	Vbus Input Charge Enable. Directs the PHY to charge Vbus. 1'b0: Do not charge Vbus through a resistor 1'b1: Charge Vbus through a resistor (must be active for at least 30 ms)
usb_srp_dischrgvbus	O	Vbus Input Discharge Enable. Directs the PHY to discharge Vbus. 1'b0: Do not discharge Vbus through a resistor. 1'b1: Discharge Vbus through a resistor (must be active for at least 50 ms).

28.4.2 ID Pin Detection

Bit USB_CONIDSTS in register USB_GOTGCTL_REG indicates whether the OTG controller is an A-device (1'b0) or a B-device (1'b1). The USB_CONIDSTSCHNG interrupt will trigger whenever there is a change to USB_CONIDSTS (i.e., when a plug is connected or disconnected).

28.4.3 Session Request Protocol (SRP)

28.4.3.1 A-Device SRP

Figure 28-7 illustrates the flow of SRP when the OTG_FS is acting as an A-device (i.e., default host and the device that powers Vbus).

1. To save power, the application suspends and turns off port power when the bus is idle by writing to the Port Suspend (USB_PRTSUSP to 1'b0) and Port Power (USB_PRTPWR to 1'b0) bits in the Host Port Control and Status register.
2. PHY indicates port power off by deasserting the usb_otg_vbusvalid_in signal.
3. The A-device must detect SE0 for at least 2 ms to start SRP when Vbus power is off.
4. To initiate SRP, the B-device turns on its data line pull-up resistor for 5 to 10 ms. The OTG_FS core detects data-line pulsing.
5. The device drives Vbus above the A-device session valid (2.0 V minimum) for Vbus pulsing. The OTF_FS core interrupts the application on detecting SRP. The Session Request Detected bit (USB_SESSREQINT) is set in Global Interrupt Status register.

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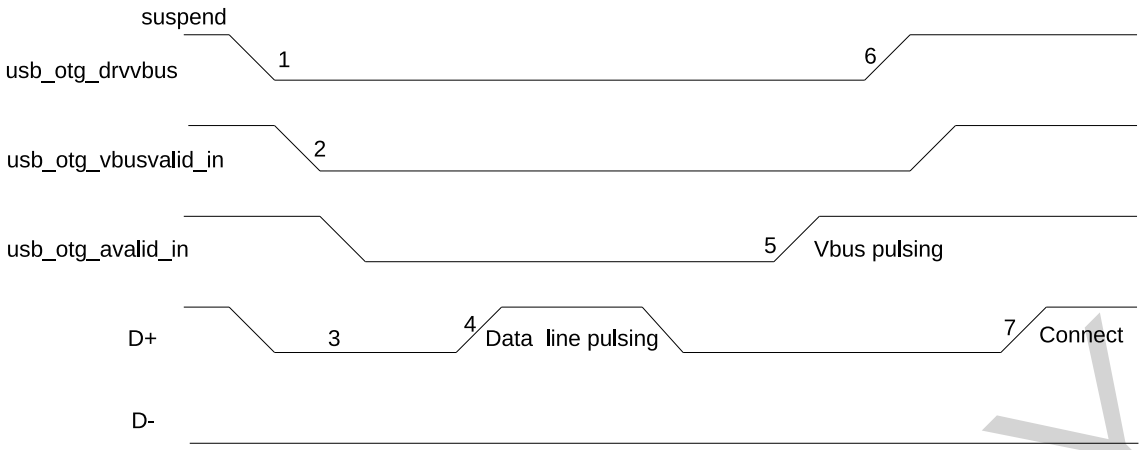


Figure 28-7. A-Device SRP

6. The application must service the Session Request Detected interrupt and turn on the Port Power bit by writing the Port Power bit in the Host Port Control and Status register. The PHY indicates port power-on by asserting usb_otg_vbusvalid_in signal.
7. When the USB is powered, the B-device connects, completing the SRP process.

28.4.3.2 B-Device SRP

Figure 28-8 illustrates the flow of SRP when the OTG_FS is acting as a B-device (i.e., does not power Vbus).

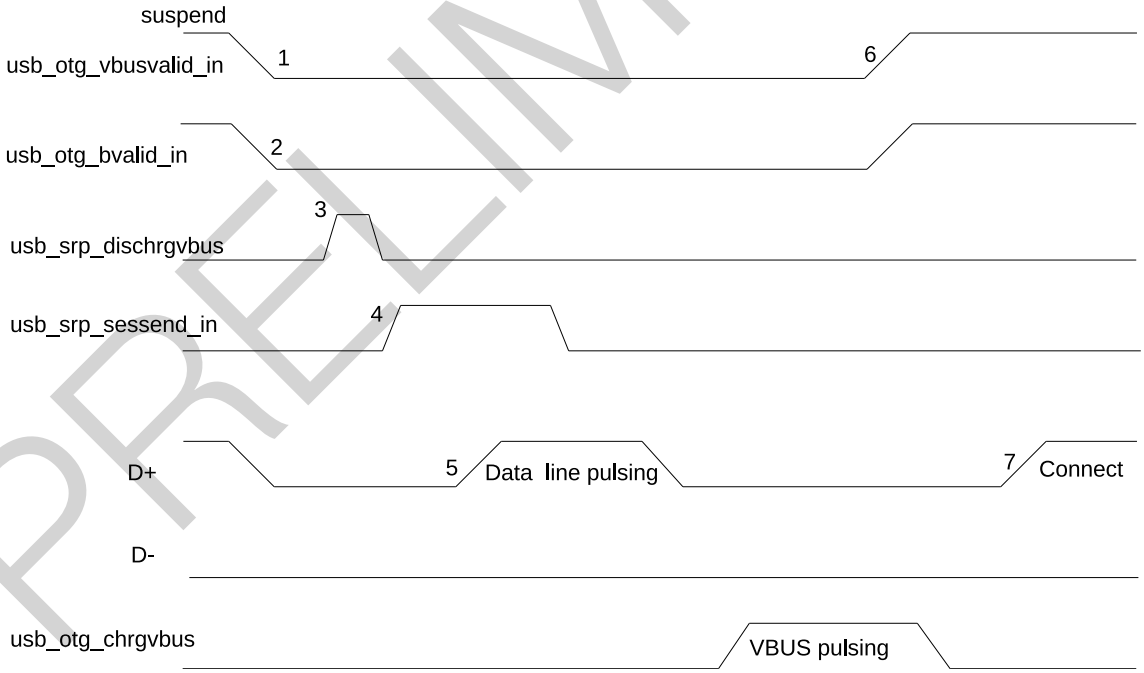


Figure 28-8. B-Device SRP

1. To save power, the host (A-device) suspends and turns off port power when the bus is idle. PHY indicates port power off by deasserting the usb_otg_vbusvalid_in signal. The OTG_FS core sets the Early Suspend bit in the Core Interrupt register (USB_ERLYSUSP interrupt) after detecting 3 ms of bus idleness. Following this, the OTF_FS core sets the USB Suspend bit (USB_USBSUSP) in the Core Interrupt register. The PHY

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indicates the end of the B-device session by deasserting the usb_otg_bvalid_in signal.

2. The OTG_FS core asserts the usb_otg_dischrgvbus signal to indicate to the PHY to speed up Vbus discharge.
3. The PHY indicates the session's end by asserting the usb_otg_sessend_in signal. This is the initial condition for SRP. The OTG_FS core requires 2 ms of SE0 before initiating SRP. For a USB 2.0 full-speed serial transceiver, the application must wait until Vbus discharges to 0.2 V after USB_BSESVLD is deasserted.
4. The application waits for 1.5 seconds (TB_SE0_SRP time) before initiating SRP by writing the Session Request bit (USB_SESREQ) in the OTG Control and Status register. The OTG_FS core performs data-line pulsing followed by Vbus pulsing.
5. The host (A-device) detects SRP from either the data-line or Vbus pulsing, and turns on Vbus. The PHY indicates Vbus power-on by asserting usb_otg_vbusvalid_in.
6. The OTG_FS core performs Vbus pulsing by asserting usb_srp_chrgvbus. The host (A-device) starts a new session by turning on Vbus, indicating SRP success. The OTG_FS core interrupts the application by setting the Session Request Success Status Change bit (USB_SESREQSC) in the OTG Interrupt Status register. The application reads the Session Request Success bit in the OTG Control and Status register.
7. When the USB is powered, the OTG_FS core connects, completing the SRP process.

28.4.4 Host Negotiation Protocol (HNP)

28.4.4.1 A-Device HNP

Figure 28-9 illustrates the flow of HNP when the OTG_FS is acting as an A-device.

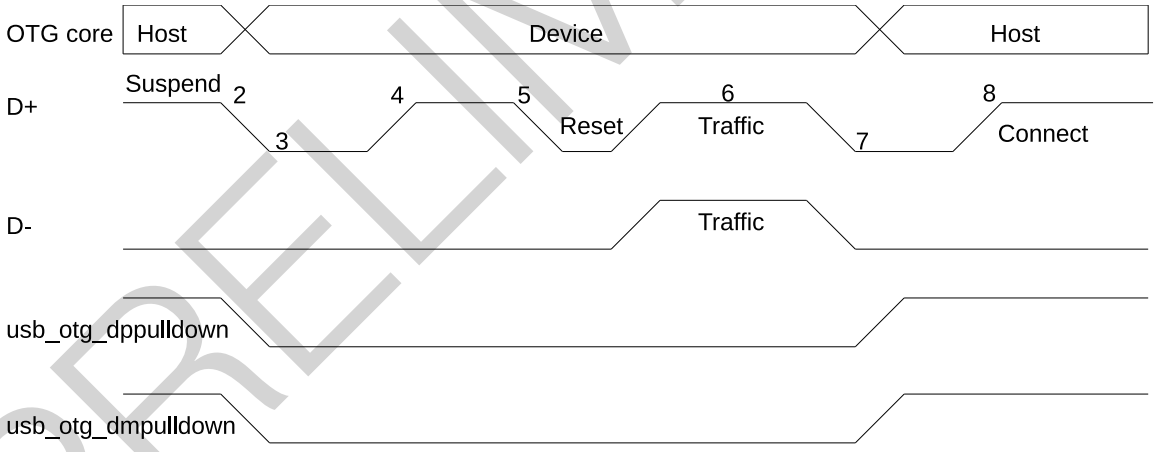


Figure 28-9. A-Device HNP

1. The OTG_FS core sends the B-device a SetFeature b_hnp_enable descriptor to enable HNP support. The B-device's ACK response indicates that the B-device supports HNP. The application must set Host Set HNP Enable bit (USB_HSTSETHNPEN) in the OTG Control and Status register to indicate to the OTG_FS core that the B-device supports HNP.
2. When it has finished using the bus, the application suspends by writing the Port Suspend bit (USB_PRTSUSP) in the Host Port Control and Status register.
3. When the B-device observes a USB suspend, it disconnects, indicating the initial condition for HNP. The B-device initiates HNP only when it must switch to the host role; otherwise, the bus continues to be

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suspended. The OTG_FS core sets the Host Negotiation Detected interrupt (USB_HSTNEGDET) in the OTG Interrupt Status register, indicating the start of HNP. The OTG_FS core deasserts the usb_otg_dppulldown and usb_otg_dmpulldown signals to indicate a device role. The PHY enables the D+ pull-up resistor, thus indicates a connection for the B-device. The application must read the Current Mode bit (USB_CURMOD_INT) in the OTG Control and Status register to determine Device mode operation.

4. The B-device detects the connection, issues a USB reset, and enumerates the OTG_FS core for data traffic.
5. The B-device continues the host role, initiating traffic, and suspends the bus when done. The OTG_FS core sets the Early Suspend bit (USB_ERLYSUSP) in the Core Interrupt register after detecting 3 ms of bus idleness. Following this, the OTG_FS core sets the USB Suspend bit (USB_USBSUSP) in the Core Interrupt register.
6. In Negotiated mode, the OTG_FS core detects the suspend, disconnects, and switches back to the host role. The OTG_FS core asserts the usb_otg_dppulldown and usb_otg_dmpulldown signals to indicate its assumption of the host role.
7. The OTG_FS core sets the Connector ID Status Change interrupt (USB_CONIDSTS) in the OTG Interrupt Status register. The application must read the connector ID status in the OTG Control and Status register to determine the OTG_FS core's operation as an A-device. This indicates the completion of HNP to the application. The application must read the Current Mode bit in the OTG Control and Status register to determine Host mode operation.
8. The B-device connects, completing the HNP process.

28.4.4.2 B-Device HNP

Figure 28-10 illustrates the flow of HNP when the OTG_FS is acting as an B-device.

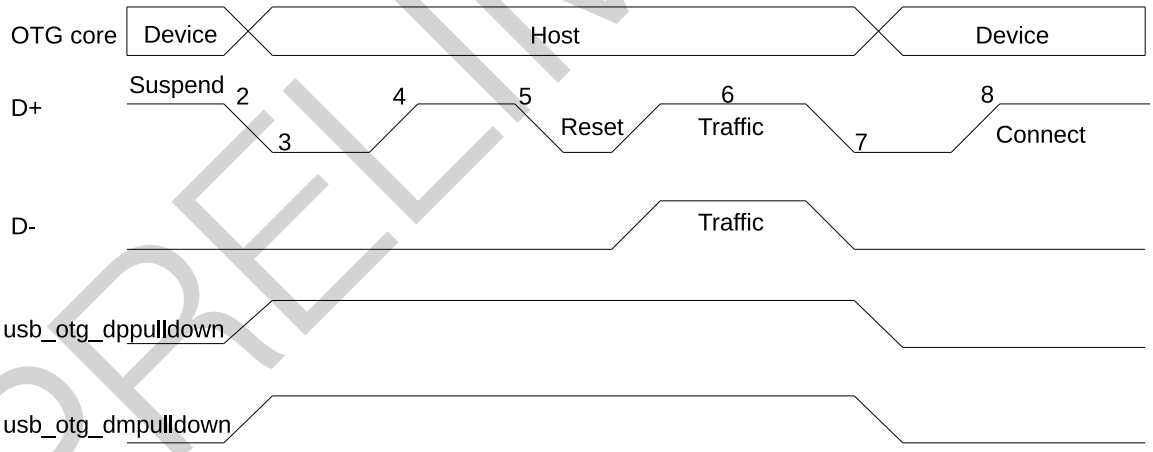


Figure 28-10. B-Device HNP

1. The A-device sends the SetFeature b_hnp_enable descriptor to enable HNP support. The OTG_FS core's ACK response indicates that it supports HNP. The application must set the Device HNP Enable bit (USB_DEVHNPEN) in the OTG Control and Status register to indicate HNP support. The application sets the HNP Request bit (USB_DEVHNPEN) in the OTG Control and Status register to indicate to the OTG_FS core to initiate HNP.
2. When A-device has finished using the bus, it suspends the bus.

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(a) The OTG_FS core sets the Early Suspend bit (USB_ERLYSUSP) in the Core Interrupt register after 3 ms of bus idleness. Following this, the OTG_FS core sets the USB Suspend bit (USB_USBSUSP) in the Core Interrupt register. The OTG_FS core disconnects and the A-device detects SE0 on the bus, indicating HNP.

(b) The OTG_FS core asserts the usb_otg_dppulldown and usb_otg_dmpulldown signals to indicate its assumption of the host role.

(c) The A-device responds by activating its D+ pull-up resistor within 3 ms of detecting SE0. The OTG_FS core detects this as a connect.

(d) The OTG_FS core sets the Host Negotiation Success Status Change interrupt in the OTG Interrupt Status register (USB_CONIDSTS), indicating the HNP status. The application must read the Host Negotiation Success bit (USB_HSTNEGSCS) in the OTG Control and Status register to determine host negotiation success. The application must read the Current Mode bit (USB_CURMOD_INT) in the Core Interrupt register to determine Host mode operation.

3. Program the USB_PRTPWR bit to 1'b1. This drives Vbus on the USB.
4. Wait for the USB_PRTCONNDET interrupt. This indicates that a device is connected to the port.
5. The application sets the reset bit (USB_PRTRST) and the OTG_FS core issues a USB reset and enumerates the A-device for data traffic.
6. Wait for the USB_PRTENCHNG interrupt.
7. The OTG_FS core continues the host role of initiating traffic, and when done, suspends the bus by writing the Port Suspend bit (USB_PRTSUSP) in the Host Port Control and Status register.
8. In Negotiated mode, when the A-device detects a suspend, it disconnects and switches back to the host role. The OTG_FS core deasserts the usb_otg_dppulldown and usb_otg_dmpulldown signals to indicate the assumption of the device role.
9. The application must read the Current Mode bit (USB_CURMOD_INT) in the Core Interrupt register to determine the Host mode operation.
10. The OTG_FS core connects, completing the HNP process.

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29 USB Serial/JTAG Controller (USB_SERIAL_JTAG)

The ESP32-S3 contains an USB Serial/JTAG Controller. This unit can be used to program the SoC's flash, read program output, as well as attach a debugger to the running program. All of these are possible for any computer with a USB host ('host' in the rest of this text) without any active external components.

29.1 Overview

The workflow of developing on previous versions of Espressif chips generally use two methods of communication with the SoC: one is a serial port and the other is the JTAG debugging port. The serial port is a two-wire interface traditionally used to push new firmware-under-development to the chip ('programming'). As most modern computers do not have a compatible serial port anymore, interfacing to this serial port requires an USB-to-serial converter IC or board. After programming is finished, the port is used to monitor any debugging output from the program, in order to keep an eye on the general state of program execution. When program execution is not what the developer expects (i.e. the program crashes), the JTAG debugging port is then used to inspect the state of the program and its variables and set break- and watchpoints. This requires interfacing with the JTAG debug port, which generally requires an external JTAG adapter.

All these external interfaces take up six pins in total, which cannot be used for other purposes while debugging. Especially on devices with small packages, like the ESP32-S3, not being able to use these pins can be limiting to a design.

In order to alleviate this issue, as well as to negate the need for external devices, the ESP32-S3 contains an USB Serial/JTAG Controller, which integrates the functionality of both an USB-to-serial converter as well as those of an USB-to-JTAG adapter. As this device directly interfaces to an external USB host using only the two data lines required by USB Specification 1.1, debugging the ESP32-S3 only requires two pins to be dedicated to this functionality.

29.2 Features

- USB Full-speed device.
- Can be configured to either use internal USB PHY of ESP32-S3 or external PHY via GPIO matrix.
- Fixed function device, hardwired for CDC-ACM (Communication Device Class - Abstract Control Model) and JTAG adapter functionality.
- 2 OUT Endpoints, 3 IN Endpoints in addition to Control Endpoint 0; Up to 64-byte data payload size.
- Internal PHY, so no or very few external components needed to connect to a host computer.
- CDC-ACM adherent serial port emulation is plug-and-play on most modern OSes.
- JTAG interface allows fast communication with CPU debug core using a compact representation of JTAG instructions.
- CDC-ACM supports host controllable chip reset and entry into download mode.

As shown in Figure 29-1, the USB Serial/JTAG Controller consists of an USB PHY, a USB device interface, a JTAG command processor and a response capture unit, as well as the CDC-ACM registers. The PHY and part of the device interface are clocked from a 48 MHz clock derived from the main PLL, the rest of the logic is clocked from APB_CLK. The JTAG command processor is connected to the JTAG debug unit of the main processor; the

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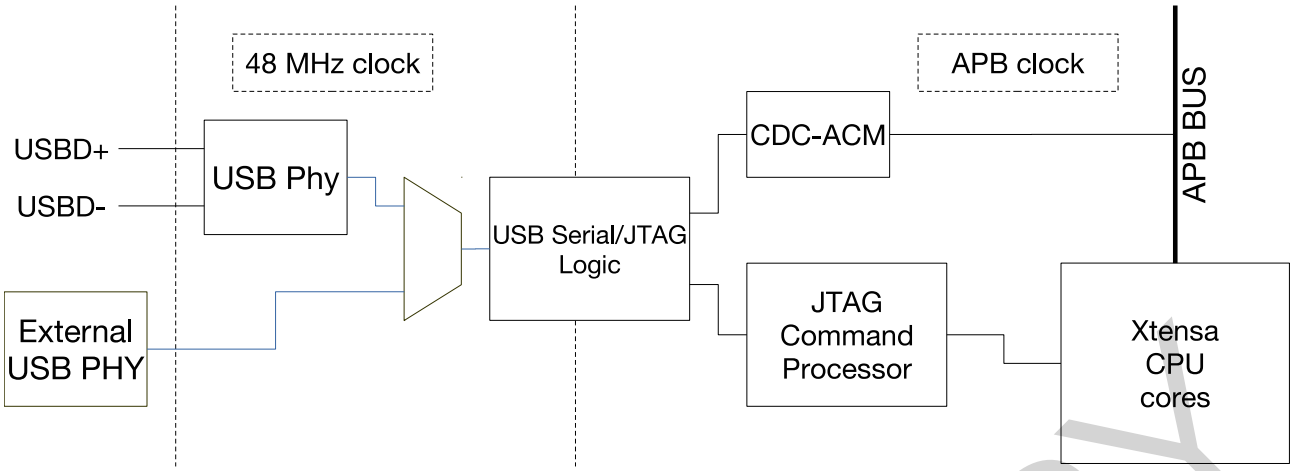


Figure 29-1. USB Serial/JTAG High Level Diagram

CDC-ACM registers are connected to the APB bus and as such can be read from and written to by software running on the main CPU.

Note that while the USB Serial/JTAG device is a USB 2.0 device, it only supports Full-speed (12 Mbps) and not the High-speed (480 Mbps) mode the USB2.0 standard introduced.

Figure 29-2 shows the internal details of the USB Serial/JTAG controller on the USB side. The USB Serial/JTAG Controller consists of an USB 2.0 Full Speed device. It contains a control endpoint, a dummy interrupt endpoint, two bulk input endpoints as well as two bulk output endpoints. Together, these form an USB Composite device, which consists of an CDC-ACM USB class device as well as a vendor-specific device implementing the JTAG interface. On the SoC side, the JTAG interface is directly connected to the debugging interface of the two Xtensa CPUs, allowing debugging of programs running on that core. Meanwhile, the CDC-ACM device is exposed as a set of registers, allowing a program on the CPU to read and write from this. Additionally, the ROM startup code of the SoC contains code allowing the user to reprogram attached flash memory using this interface.

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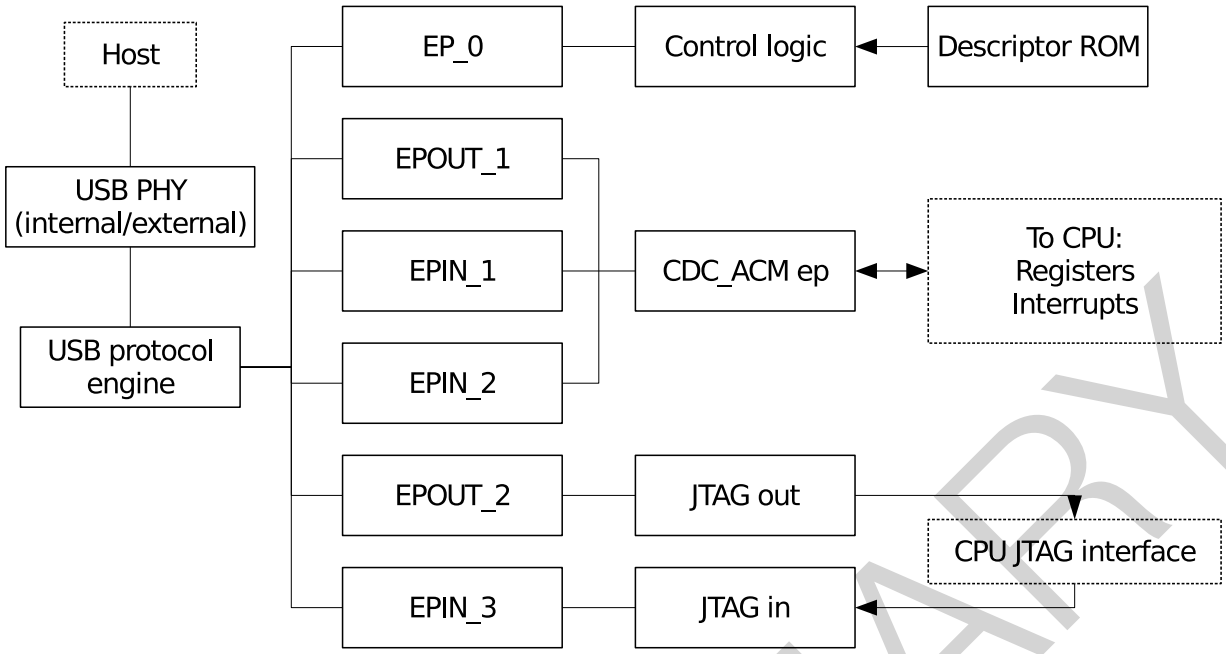


Figure 29-2. USB Serial/JTAG Block Diagram

29.3 Functional Description

The USB Serial/JTAG Controller interfaces with an USB host processor on one side, and the CPU debug hardware as well as the software running on the USB port on the other side.

29.3.1 USB Serial/JTAG host connection

As shown in Figure 29-3, interfacing with an USB host connection on the physical level is done with a PHY. The ESP32-S3 has an internal PHY, which is shared between the USB-OTG and the USB Serial/JTAG hardware. Either one of these can use the internal PHY. Optionally, the signals from the unit not using the internal PHY can be routed out via the GPIO matrix to IO pads. Adding an external USB PHY to these pads results in a second usable USB port.

The actual routing from USB Serial/JTAG Controller and USB-OTG to internal and external PHYs initially is decided using eFuses as described in Table 29-6. This configuration can later be modified using register writes.

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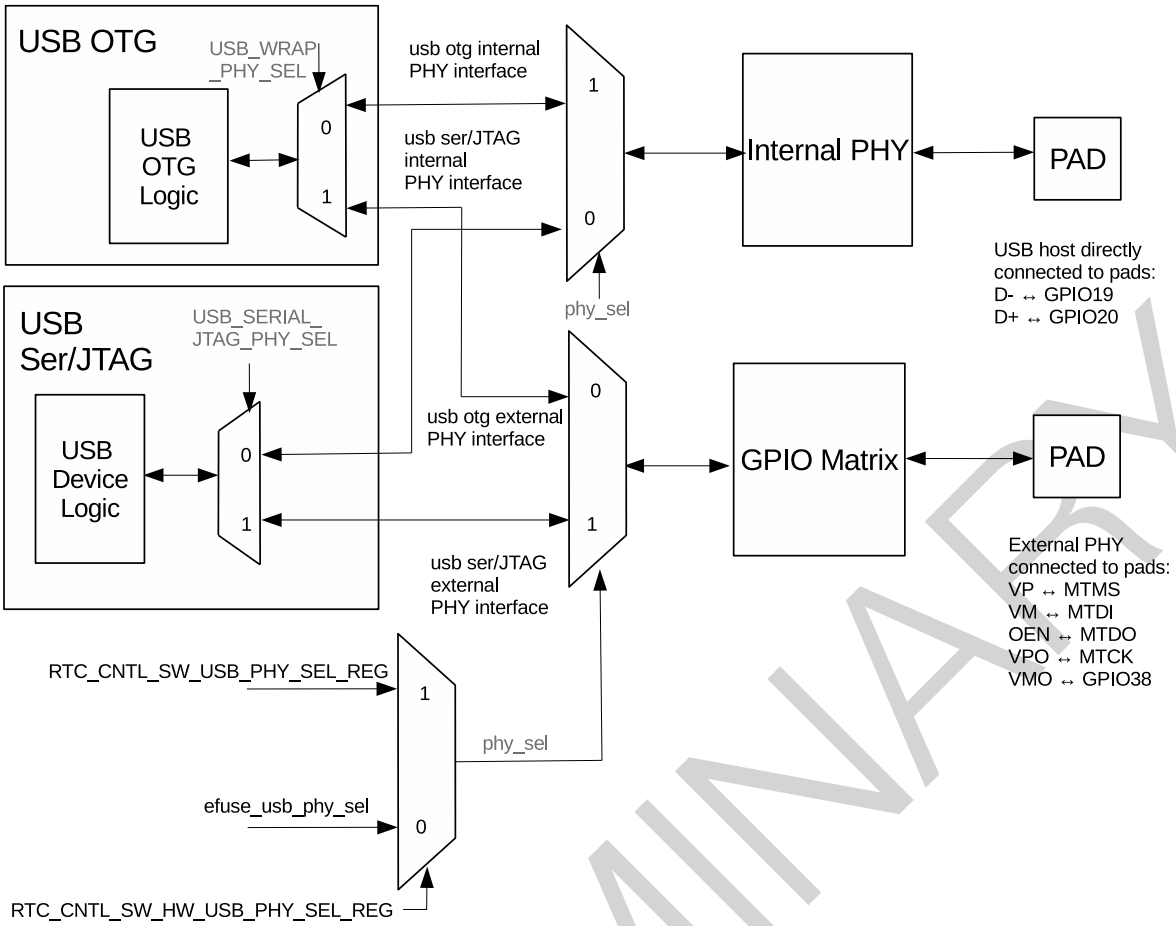


Figure 29-3. USB Serial/JTAG and USB-OTG Internal/External PHY Routing Diagram

The CPU JTAG signals can be routed to the USB Serial/JTAG Controller or external GPIO pads using eFuses and when the user program has started, software control as well. At that time, the JTAG signals from the USB Serial/JTAG can also be routed to the GPIO matrix. This allows debugging a secondary SoC via JTAG using the ESP32-S3 USB Serial/JTAG Controller.

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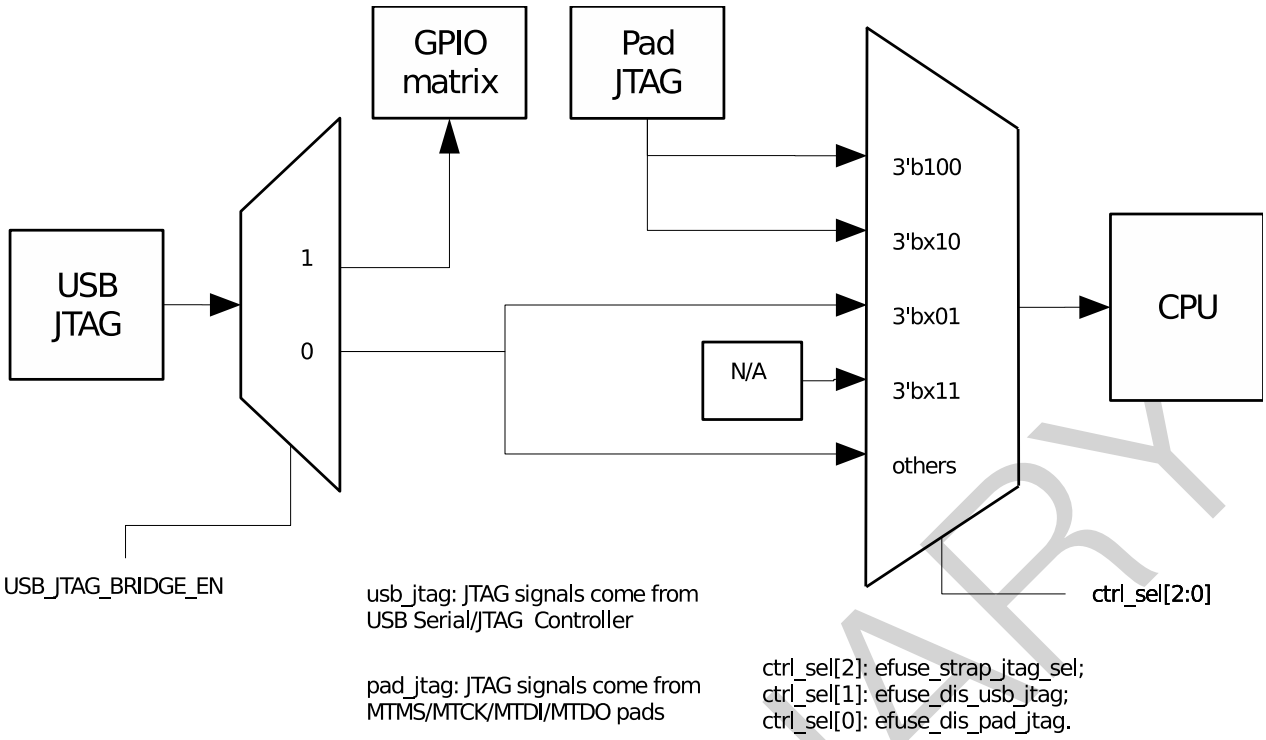


Figure 29-4. JTAG Routing Diagram

29.3.2 CDC-ACM USB Interface Functional Description

The CDC-ACM interface adheres to the standard USB CDC-ACM class for serial port emulation. It contains a dummy interrupt endpoint (which will never send any events, as they are not implemented nor needed) and a Bulk IN as well as a Bulk OUT endpoint for the host's received and sent serial data respectively. These endpoints can handle 64-byte packets at a time, allowing for high throughput. As CDC-ACM is a standard USB device class, a host generally does not need any special installation procedures for it to function: when the USB debugging device is properly connected to a host, the operating system should show a new serial port moments later.

The CDC-ACM interface accepts the following standard CDC-ACM control requests:

Table 29-1. Standard CDC-ACM Control Requests

Command	Action
SEND_BREAK	Accepted but ignored (dummy)
SET_LINE_CODING	Accepted but ignored (dummy)
GET_LINE_CODING	Always returns 9600 baud, no parity, 8 databits, 1 stopbit
SET_CONTROL_LINE_STATE	Set the state of the RTS/DTR lines, see Table 29-2

Aside from general-purpose communication, the CDC-ACM interface also can be used to reset the ESP32-S3 and optionally make it go into download mode in order to flash new firmware. This is done by setting the RTS and DTR lines on the virtual serial port.

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Table 29-2. CDC-ACM Settings with RTS and DTR

RTS	DTR	Action
0	0	Clear download mode flag
0	1	Set download mode flag
1	0	Reset ESP32-S3
1	1	No action

Note that if the download mode flag is set when the ESP32-S3 is reset, the ESP32-S3 will reboot into download mode. When this flag is cleared and the chip is reset, the ESP32-S3 will boot from flash. For specific sequences, please refer to Section 29.4. All these functions can also be disabled by programming various eFuses, please refer to Chapter 4 *eFuse Controller* for more details.

29.3.3 CDC-ACM Firmware Interface Functional Description

As the USB Serial/JTAG Controller is connected to the internal APB bus of the ESP32-S3, the CPU can interact with it. This is mainly used to read and write data from and to the virtual serial port on the attached host.

USB CDC-ACM serial data is sent to and received from the host in packets of 0 to 64 bytes in size. When enough CDC-ACM data has accumulated in the host, the host will send a packet to the CDC-ACM receive endpoint, and when the USB Serial/JTAG Controller has a free buffer, it will accept this packet. Conversely, the host will check periodically if the USB Serial/JTAG Controller has a packet ready to be sent to the host, and if so, receive this packet.

Firmware can get notified of new data from the host in one of two ways. First of all, the USB_SERIAL_JTAG_SERIAL_OUT_EP_DATA_AVAIL bit will remain set to 1 as long as there still is unread host data in the buffer. Secondly, the availability of data will trigger the USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT interrupt as well.

When data is available, it can be read by firmware by repeatedly reading bytes from USB_SERIAL_JTAG_EP1_REG. The amount of bytes to read can be determined by checking the USB_REG_SERIAL_OUT_EP_DATA_AVAIL bit after reading each byte to see if there is more data to read. After all data is read, the USB debug device is automatically readied to receive a new data packet from the host.

When the firmware has data to send, it can do so by putting it in the send buffer and triggering a flush, allowing the host to receive the data in a USB packet. In order to do so, there needs to be space available in the send buffer. Firmware can check this by reading USB_REG_SERIAL_IN_EP_DATA_FREE; a 1 in this register field indicates there is still free room in the buffer. While this is the case, firmware can fill the buffer by writing bytes to the USB_SERIAL_JTAG_EP1_REG register.

Writing the buffer doesn't immediately trigger sending data to the host. This does not happen until the buffer is flushed; a flush causes the entire buffer to be readied for reception by the USB host at once. A flush can be triggered in two ways: after the 64th byte is written to the buffer, the USB hardware will automatically flush the buffer to the host. Alternatively, firmware can trigger a flush by writing a 1 to USB_REG_SERIAL_WR_DONE.

Regardless of how a flush is triggered, the send buffer will be unavailable for firmware to write into until it has been fully read by the host. As soon as this happens, the USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT interrupt will be triggered, indicating the send buffer can receive another 64 bytes.

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29.3.4 USB-to-JTAG Interface

The USB-to-JTAG interface uses a vendor-specific class for its implementation. It consists of two endpoints, one to receive commands and one to send responses. Additionally, some less time-sensitive commands can be given as control requests.

29.3.5 JTAG Command Processor

Commands from the host to the JTAG interface are interpreted by the JTAG command processor. Internally, the JTAG command processor implements a full four-wire JTAG bus, consisting of the TCK, TMS and TDI output lines to the Xtensa CPUs, as well as the TDO line signalling back from the CPU to the JTAG response capture unit. These signals adhere to the IEEE 1149.1 JTAG standards. Additionally, there is a SRST line to reset the SoC.

The JTAG command processor parses each received nibble (4-bit value) as a command. As USB data is received in 8-bit bytes, this means each byte contains two commands. The USB command processor will execute high-nibble first and low-nibble second. The commands are used to control the TCK, TMS, TDI, and SRST lines of the internal JTAG bus, as well as signal the JTAG response capture unit that the state of the TDO line (which is driven by the CPU debug logic) needs to be captured.

Of this internal JTAG bus, TCK, TMS, TDI and TDO are connected directly to the JTAG debugging logic of the Xtensa CPUs. SRST is connected to the reset logic of the digital circuitry in the SoC and a high level on this line will cause a digital system reset. Note that the USB Serial/JTAG Controller itself is not affected by SRST.

A nibble can contain the following commands:

Table 29-3. Commands of a Nibble

bit	3	2	1	0
CMD_CLK	0	cap	tms	tdi
CMD_RST	1	0	0	srst
CMD_FLUSH	1	0	1	0
CMD_RSV	1	0	1	1
CMD_REP	1	1	R1	R0

- CMD_CLK will set the TDI and TMS to the indicated values and emit one clock pulse on TCK. If the CAP bit is 1, it will also instruct the JTAG response capture unit to capture the state of the TDO line. This instruction forms the basis of JTAG communication.
- CMD_RST will set the state of the SRST line to the indicated value. This can be used to reset the ESP32-S3.
- CMD_FLUSH will instruct the JTAG response capture unit to flush the buffer of all bits it collected so the host is able to read them. Note that in some cases, a JTAG transaction will end in an odd number of commands and as such an odd number of nibbles. In this case, it is allowable to repeat the CMD_FLUSH to get an even number of nibbles fitting an integer number of bytes.
- CMD_RSV is reserved in the current implementation. The ESP32-S3 will ignore this command when it receives it.
- CMD_REP repeats the last (non-CMD_REP) command a certain number of times. It's intended goal is to compress command streams which repeat the same CMD_CLK instruction multiple times. A command like

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CMD_CLK can be followed by multiple CMD_REP commands. The number of repetitions done by one CMD_REP can be expressed as $no\_repetitions = (R1 \times 2 + R0) \times (4^{cmd\_rep\_count})$, where cmd_rep_count is how many CMD_REP instructions went directly before it. Note that the CMD_REP is only intended to repeat a CMD_CLK command. Specifically, using it on a CMD_FLUSH command may lead to an unresponsive USB device, needing an USB reset to recover.

29.3.6 USB-to-JTAG Interface: CMD_REP usage example

Here is a list of commands as an illustration of the use of CMD_REP. Note each command is a nibble; in this example the bytewise command stream would be 0x0D 0x5E 0xCF.

1. 0x0 (CMD_CLK: cap=0, tdi=0, tms=0)
2. 0xD (CMD_REP: R1=0, R0=1)
3. 0x5 (CMD_CLK: cap=1, tdi=0, tms=1)
4. 0xE (CMD_REP: R1=1, R0=0)
5. 0xC (CMD_REP: R1=0, R0=0)
6. 0xF (CMD_REP: R1=1, R0=1)

This is what happens at every step:

1. TCK is clocked with the TDI and TMS lines set to 0. No data is captured.
2. TCK is clocked another $(0 \times 2 + 1) \times (4^2) = 1$ time with the same settings as step 1.
3. TCK is clocked with the TDI and TMS lines set to 0. Data on the TDO line is captured.
4. TCK is clocked another $(1 \times 2 + 0) \times (4^0) = 2$ times with the same settings as step 3.
5. Nothing happens: $(0 \times 2 + 0) \times (4^1) = 0$. Note that this does increase cmd_rep_count for the next step.
6. TCK is clocked another $(1 \times 2 + 1) \times (4^2) = 48$ times with the same settings as step 3.

In other words: This example stream has the same net effect as command 1 twice, then repeating command 3 for 51 times.

29.3.7 USB-to-JTAG Interface: Response Capture Unit

The response capture unit reads the TDO line of the internal JTAG bus and captures its value when the command parser executes a CMD_CLK with cap=1. It puts this bit into an internal shift register, and writes a byte into the USB buffer when 8 bits have been collected. Of these 8 bits, the least significant one is the one that is read from TDO the earliest.

As soon as either 64 bytes (512 bits) have been collected or a CMD_FLUSH command is executed, the response capture unit will make the buffer available for the host to receive. Note that the interface to the USB logic is double-buffered. This way, as long as USB throughput is sufficient, the response capture unit can always receive more data: while one of the buffers is waiting to be sent to the host, the other one can receive more data. When the host has received data from its buffer and the response capture unit flushes its buffer, the two buffers change position.

This also means that a command stream can cause at most 128 bytes of capture data to be generated (less if there are flush commands in the stream) without the host acting to receive the generated data. If more data is

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generated anyway, the command stream is paused and the device will not accept more commands before the generated capture data is read out.

Note that in general, the logic of the response capture unit tries not to send zero-byte responses: for instance, sending a series of CMD_FLUSH commands will not cause a series of zero-byte USB responses to be sent. However, in the current implementation, some zero-byte responses may be generated in extraordinary circumstances. It's recommended to ignore these responses.

29.3.8 USB-to-JTAG Interface: Control Transfer Requests

Aside from the command processor and the response capture unit, the USB-to-JTAG interface also understands some control requests, as documented in the table below:

Table 29-4. USB-to-JTAG Control Requests

bmRequestType	bRequest	wValue	wIndex	wLength	Data
01000000b	0 (VEND_JTAG_SETDIV)	[divider]	interface	0	None
01000000b	1 (VEND_JTAG_SETIO)	[iobits]	interface	0	None
11000000b	2 (VEND_JTAG_GETTDO)	0	interface	1	[iostate]
10000000b	6 (GET_DESCRIPTOR)	0x2000	0	256	[jtag cap desc]

- VEND_JTAG_SETDIV sets the divider used. This directly affects the duration of a TCK clock pulse. The TCK clock pulses are derived from APB_CLK, which is divided down using an internal divider. This control request allows the host to set this divider. Note that on startup, the divider is set to 2, meaning the TCK clock rate will generally be 40 MHz.
- VEND_JTAG_SETIO can bypass the JTAG command processor to set the internal TDI, TDO, TMS and SRST lines to given values. These values are encoded in the wValue field in the format of 11'b0, srst, trst, tck, tms, tdi.
- VEND_JTAG_GETTDO can bypass the JTAG response capture unit to read the internal TDO signal directly. This request returns one byte of data, of which the least significant bit represents the status of the TDO line.
- GET_DESCRIPTOR is a standard USB request, however it can also be used with a vendor-specific wValue of 0x2000 to get the JTAG capabilities descriptor. This returns a certain amount of bytes representing the following fixed structure, which describes the capabilities of the USB-to-JTAG adapter. This structure allows host software to automatically support future revisions of the hardware without needing an update.

The JTAG capabilities descriptor of the ESP32-S3 is as follows. Note that all 16-bit values are little-endian.

Table 29-5. JTAG Capabilities Descriptor

Byte	Value	Description
0	1	JTAG protocol capabilities structure version
1	10	Total length of JTAG protocol capabilities
2	1	Type of this struct: 1 for speed capabilities struct
3	8	Length of this speed capabilities struct
4 ~ 5	8000	APB_CLK speed in 10 kHz increments. Note that the maximal TCK speed is half of this
6 ~ 7	1	Minimum divisor
8 ~ 9	255	Maximum divisor

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29.4 Recommended Operation

29.4.1 Internal/external PHY selection

As the ESP32-S3 only has a single internal PHY, at first programming you may need to decide how that is going to be used in the intended application by burning eFuses to affect the initial USB configuration. This affects ROM download mode as well: while both USB-OTG as well as the USB Serial/JTAG controller allows serial programming, only USB-OTG supports the DFU protocol and only the USB Serial/JTAG controller supports JTAG debugging over USB. Even when not using USB, eFuse configuration is required when an external JTAG adapter will be used.

Table 29-6 indicates which eFuse to burn to get a certain boot-up configuration. Note that this is mostly relevant for the configuration in download mode and the bootloader as the configuration can be altered at runtime as soon as user code is running.

Table 29-6. Use cases and eFuse settings

Use case	eFuses	Note
USB serial/JTAG on internal PHY only	None	-
USB OTG on internal PHY only	EFUSE_USB_PHY_SEL + EFUSE_DIS_USB_JTAG	JTAG on GPIO pins
USB serial/JTAG on internal PHY, OTG on external PHY	None	-
USB OTG on internal PHY, USB serial/JTAG on external	EFUSE_USB_PHY_SEL	-

After the user program is running, it can modify the initial configuration by setting registers. Specifically, RTC_CNTL_SW_HW_USB_PHY_SEL can be used to have software override the effect of EFUSE_USB_PHY_SEL: if this bit is set, the USB PHY selection logic will use the value of the RTC_CNTL_SW_USB_PHY_SEL bit in place of that of EFUSE_USB_PHY_SEL.

29.4.2 Runtime operation

There is very little setup needed in order to use the USB Serial/JTAG Device. The USB-to-JTAG hardware itself does not need any setup aside from the standard USB initialization the host operating system already does. The CDC-ACM emulation, on the host side, also is plug-and-play.

On the firmware side, very little initialization should be needed either: the USB hardware is self-initializing and after boot-up, if a host is connected and listening on the CDC-ACM interface, data can be exchanged as described above without any specific setup aside from the firmware optionally setting up an interrupt service handler.

One thing to note is that there may be situations where the host is either not attached or the CDC-ACM virtual port is not opened. In this case, the packets that are flushed to the host will never be picked up and the transmit buffer will never be empty. It is important to detect this and time out, as this is the only way to reliably detect that the port on the host side is closed.

Another thing to note is that the USB device is dependent on both the PLL for the 48 MHz USB PHY clock, as well as APB_CLK. Specifically, an APB_CLK of 40 MHz or more is required for proper USB compliant operation, although the USB device will still function with most hosts with an APB_CLK as low as 10 MHz. Behaviour

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shown when this happens is dependent on the host USB hardware and drivers, and can include the device being unresponsive and it disappearing when first accessed.

More specifically, the APB_CLK will be affected by clock gating the USB Serial/JTAG Controller, which may happen in Light-sleep. Additionally, the USB serial/JTAG Controller (as well as the attached Xtensa CPUs) will be entirely powered down in Deep-sleep mode. If a device needs to be debugged in either of these two modes, it may be preferable to use an external JTAG debugger and serial interface instead.

The CDC-ACM interface can also be used to reset the SoC and take it into or out of download mode. Generating the correct sequence of handshake signals can be a bit complicated: Most operating systems only allow setting or resetting DTR and RTS separately, and not in tandem. Additionally, some drivers (e.g. the standard CDC-ACM driver on Windows) do not set DTR until RTS is set and the user needs to explicitly set RTS in order to 'propagate' the DTR value. These are the recommended procedures:

To reset the SoC into download mode:

Table 29-7. Reset SoC into Download Mode

Action	Internal state	Note
Clear DTR	RTS=?, DTR=0	Initialize to known values
Clear RTS	RTS=0, DTR=0	-
Set DTR	RTS=0, DTR=1	Set download mode flag
Clear RTS	RTS=0, DTR=1	Propagate DTR
Set RTS	RTS=1, DTR=1	-
Clear DTR	RTS=1, DTR=0	Reset SoC
Set RTS	RTS=1, DTR=0	Propagate DTR
Clear RTS	RTS=0, DTR=0	Clear download flag

To reset the SoC into booting from flash:

Table 29-8. Reset SoC into Booting

Action	Internal state	Note
Clear DTR	RTS=?, DTR=0	-
Clear RTS	RTS=0, DTR=0	Clear download flag
Set RTS	RTS=1, DTR=0	Reset SoC
Clear RTS	RTS=0, DTR=0	Exit reset

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29.5 Register Summary

The addresses in this section are relative to USB Serial/JTAG Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

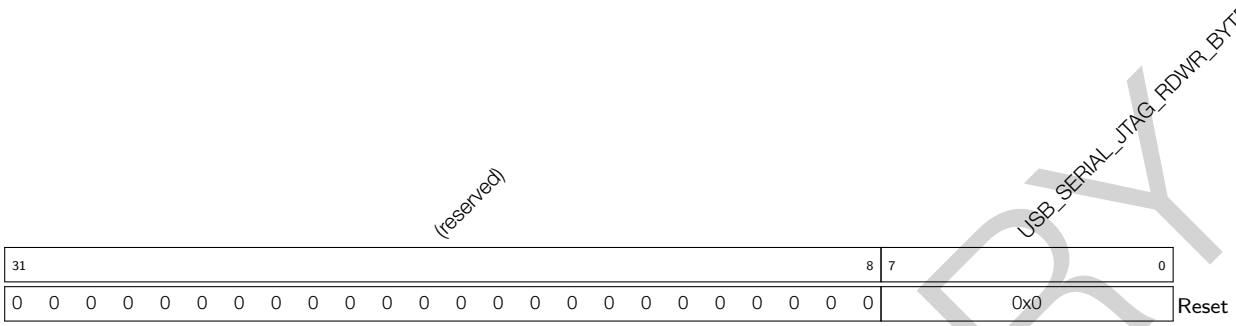
Name	Description	Address	Access
Configuration Registers			
USB_SERIAL_JTAG_EP1_REG	Endpoint 1 FIFO register	0x0000	R/W
USB_SERIAL_JTAG_EP1_CONF_REG	Endpoint 1 configure and status register	0x0004	varies
USB_SERIAL_JTAG_CONF0_REG	Configure 0 register	0x0018	R/W
USB_SERIAL_JTAG_MISC_CONF_REG	MISC register	0x0044	R/W
USB_SERIAL_JTAG_MEM_CONF_REG	Memory power control	0x0048	R/W
USB_SERIAL_JTAG_TEST_REG	USB Internal PHY test register	0x001C	varies
Interrupt Registers			
USB_SERIAL_JTAG_INT_RAW_REG	Raw status interrupt	0x0008	R/WTC/SS
USB_SERIAL_JTAG_INT_ST_REG	Masked interrupt	0x000C	RO
USB_SERIAL_JTAG_INT_ENA_REG	Interrupt enable bits	0x0010	R/W
USB_SERIAL_JTAG_INT_CLR_REG	Interrupt clear bits	0x0014	WT
Status Registers			
USB_SERIAL_JTAG_JFIFO_ST_REG	USB-JTAG FIFO status	0x0020	varies
USB_SERIAL_JTAG_FRAM_NUM_REG	SOF frame number	0x0024	RO
USB_SERIAL_JTAG_IN_EP0_ST_REG	IN Endpoint 0 status	0x0028	RO
USB_SERIAL_JTAG_IN_EP1_ST_REG	IN Endpoint 1 status	0x002C	RO
USB_SERIAL_JTAG_IN_EP2_ST_REG	IN Endpoint 2 status	0x0030	RO
USB_SERIAL_JTAG_IN_EP3_ST_REG	IN Endpoint 3 status	0x0034	RO
USB_SERIAL_JTAG_OUT_EP0_ST_REG	OUT Endpoint 0 status	0x0038	RO
USB_SERIAL_JTAG_OUT_EP1_ST_REG	OUT Endpoint 1 status	0x003C	RO
USB_SERIAL_JTAG_OUT_EP2_ST_REG	OUT Endpoint 2 status	0x0040	RO
Version Register			
USB_SERIAL_JTAG_DATE_REG	Version control register	0x0080	R/W

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29.6 Registers

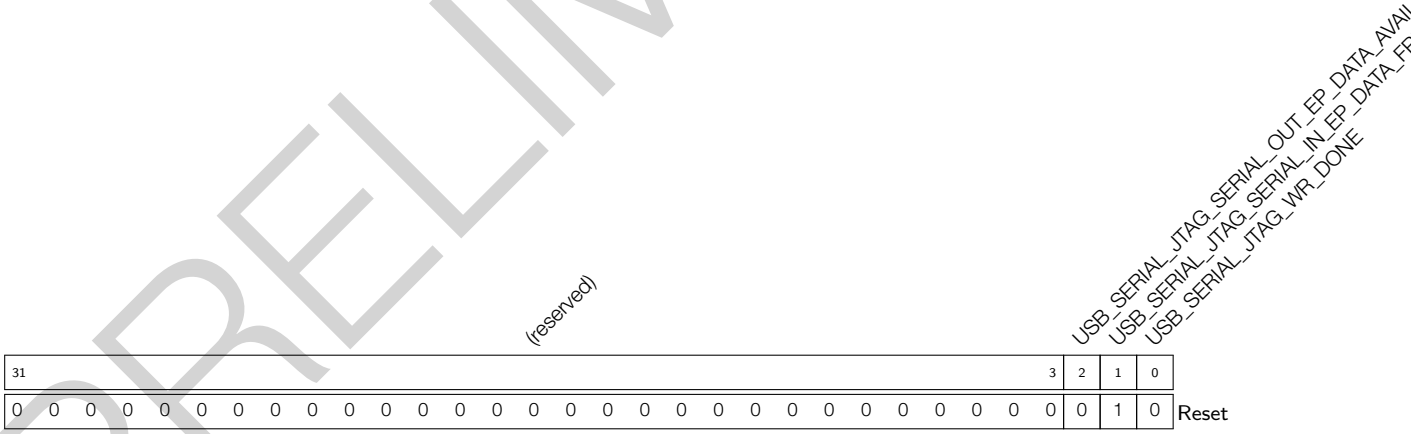
The addresses in this section are relative to USB Serial/JTAG Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 29.1. USB_SERIAL_JTAG_EP1_REG (0x0000)



USB_SERIAL_JTAG_RDWR_BYTE Write and read byte data to/from UART Tx/Rx FIFO through this field. When USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT is set, then user can write data (up to 64 bytes) into UART Tx FIFO. When USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT is set, user can check USB_SERIAL_JTAG_OUT_EP1_WR_ADDR USB_SERIAL_JTAG_OUT_EP0_RD_ADDR to know how many data is received, then read data from UART Rx FIFO. (R/W)

Register 29.2. USB_SERIAL_JTAG_EP1_CONF_REG (0x0004)



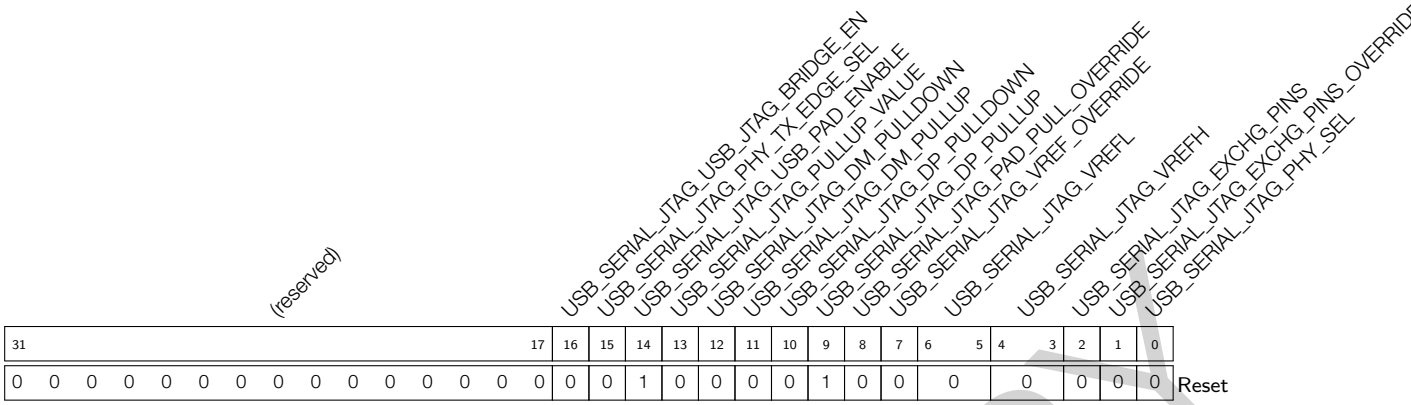
USB_SERIAL_JTAG_WR_DONE Set this bit to indicate writing byte data to UART Tx FIFO is done. (WT)

USB_SERIAL_JTAG_SERIAL_IN_EP_DATA_FREE 1'b1: Indicate UART Tx FIFO is not full and can write data into in. After writing USB_SERIAL_JTAG_WR_DONE, this bit would be 1'b0 until data in UART Tx FIFO is read by USB Host. (RO)

USB_SERIAL_JTAG_SERIAL_OUT_EP_DATA_AVAIL 1'b1: Indicate there is data in UART Rx FIFO. (RO)

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Register 29.3. USB_SERIAL_JTAG_CONF0_REG (0x0018)



USB_SERIAL_JTAG_PHY_SEL Select internal/external PHY. 1'b0: internal PHY, 1'b1: external PHY. (R/W)

USB_SERIAL_JTAG_EXCHG_PINS_OVERRIDE Enable software control USB D+ D- exchange. (R/W)

USB_SERIAL_JTAG_EXCHG_PINS USB D+ D- exchange. (R/W)

USB_SERIAL_JTAG_VREFH Control single-end input high threshold, 1.76 V to 2 V, step 80 mV. (R/W)

USB_SERIAL_JTAG_VREFL Control single-end input low threshold, 0.8 V to 1.04 V, step 80 mV. (R/W)

USB_SERIAL_JTAG_VREF_OVERRIDE Enable software control input threshold. (R/W)

USB_SERIAL_JTAG_PAD_PULL_OVERRIDE Enable software control USB D+ D- pullup pulldown. (R/W)

USB_SERIAL_JTAG_DP_PULLUP Control USB D+ pull up. (R/W)

USB_SERIAL_JTAG_DP_PULLDOWN Control USB D+ pull down. (R/W)

USB_SERIAL_JTAG_DM_PULLUP Control USB D- pull up. (R/W)

USB_SERIAL_JTAG_DM_PULLDOWN Control USB D- pull down. (R/W)

USB_SERIAL_JTAG_PULLUP_VALUE Control pull up value. (R/W)

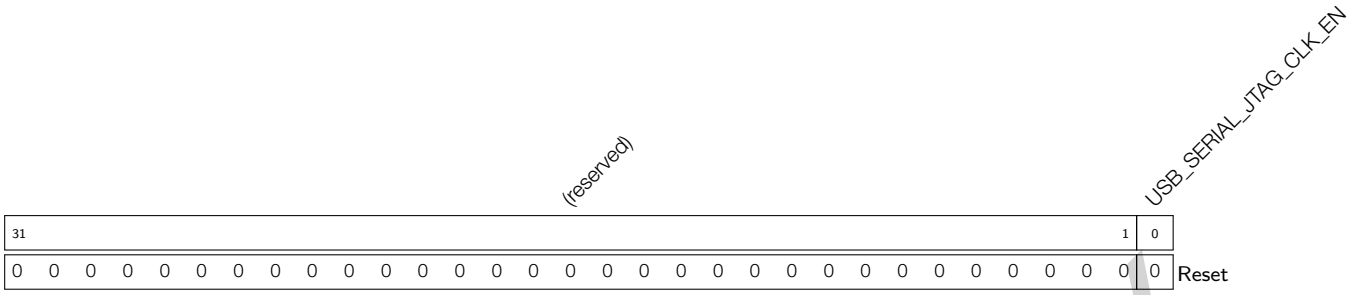
USB_SERIAL_JTAG_USB_PAD_ENABLE Enable USB pad function. (R/W)

USB_SERIAL_JTAG_PHY_TX_EDGE_SEL 0: TX output at clock negedge. 1: Tx output at clock posedge. (R/W)

USB_SERIAL_JTAG_USB_JTAG_BRIDGE_EN Set this bit usb_jtag, the connection between usb_jtag and internal JTAG is disconnected, and MTMS, MTDI, MTCK are output through GPIO Matrix, MTDO is input through GPIO Matrix. (R/W)

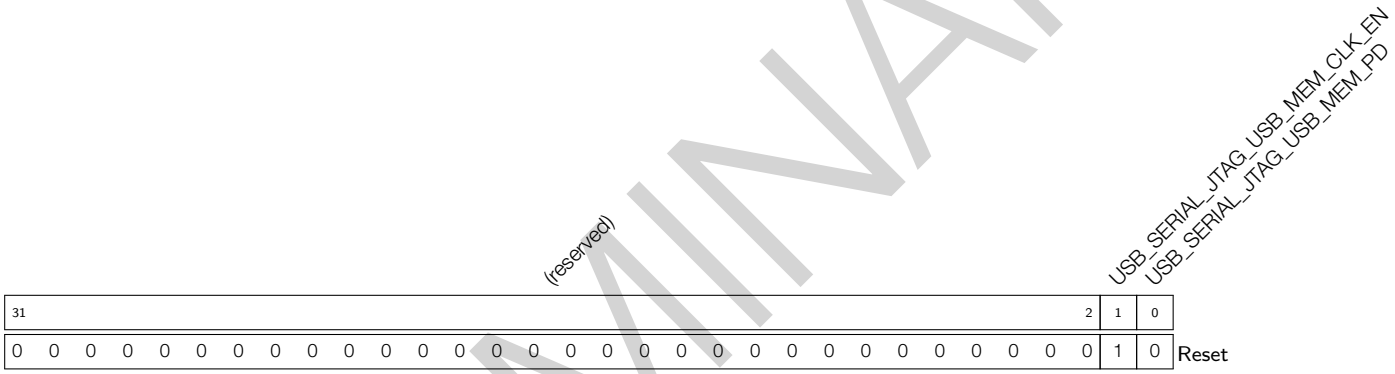
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Register 29.4. USB_SERIAL_JTAG_MISC_CONF_REG (0x0044)



USB_SERIAL_JTAG_CLK_EN 1'h1: Force clock on for register. 1'h0: Support clock only when application writes registers. (R/W)

Register 29.5. USB_SERIAL_JTAG_MEM_CONF_REG (0x0048)

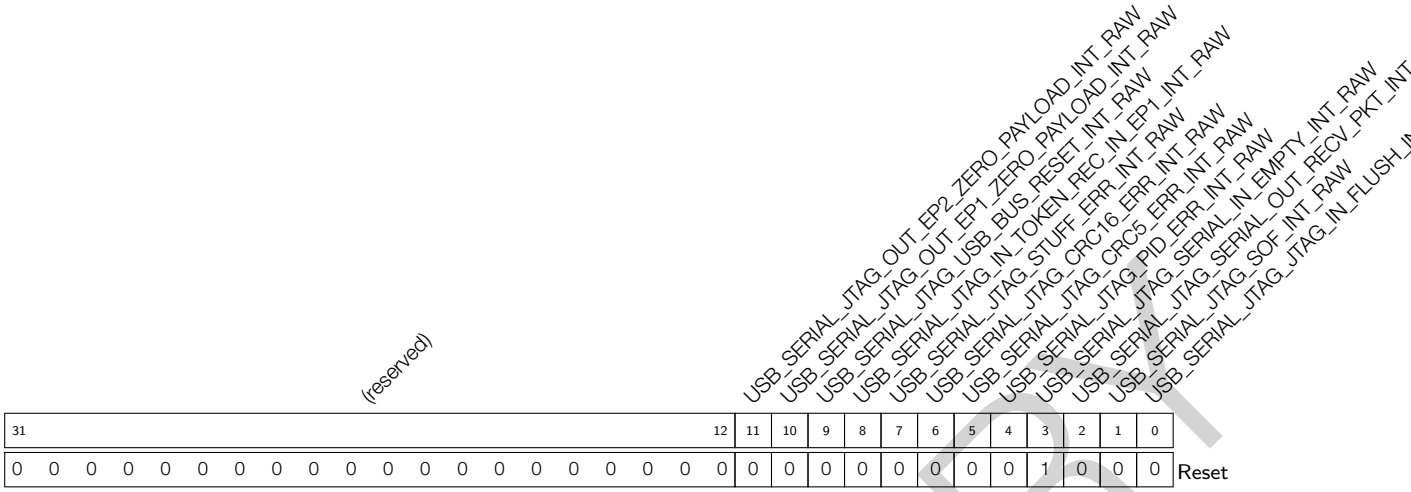


USB_SERIAL_JTAG_USB_MEM_PD 1: power down usb memory. (R/W)

USB_SERIAL_JTAG_USB_MEM_CLK_EN 1: Force clock on for usb memory. (R/W)

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Register 29.6. USB_SERIAL_JTAG_INT_RAW_REG (0x0008)



USB_SERIAL_JTAG_JTAG_IN_FLUSH_INT_RAW The raw interrupt bit turns to high level when flush cmd is received for IN endpoint 2 of JTAG. (R/WTC/SS)

USB_SERIAL_JTAG_SOF_INT_RAW The raw interrupt bit turns to high level when SOF frame is received. (R/WTC/SS)

USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT_RAW The raw interrupt bit turns to high level when Serial Port OUT Endpoint received one packet. (R/WTC/SS)

USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT_RAW The raw interrupt bit turns to high level when Serial Port IN Endpoint is empty. (R/WTC/SS)

USB_SERIAL_JTAG_PID_ERR_INT_RAW The raw interrupt bit turns to high level when pid error is detected. (R/WTC/SS)

USB_SERIAL_JTAG_CRC5_ERR_INT_RAW The raw interrupt bit turns to high level when CRC5 error is detected. (R/WTC/SS)

USB_SERIAL_JTAG_CRC16_ERR_INT_RAW The raw interrupt bit turns to high level when CRC16 error is detected. (R/WTC/SS)

USB_SERIAL_JTAG_STUFF_ERR_INT_RAW The raw interrupt bit turns to high level when stuff error is detected. (R/WTC/SS)

USB_SERIAL_JTAG_IN_TOKEN_REC_IN_EP1_INT_RAW The raw interrupt bit turns to high level when IN token for IN endpoint 1 is received. (R/WTC/SS)

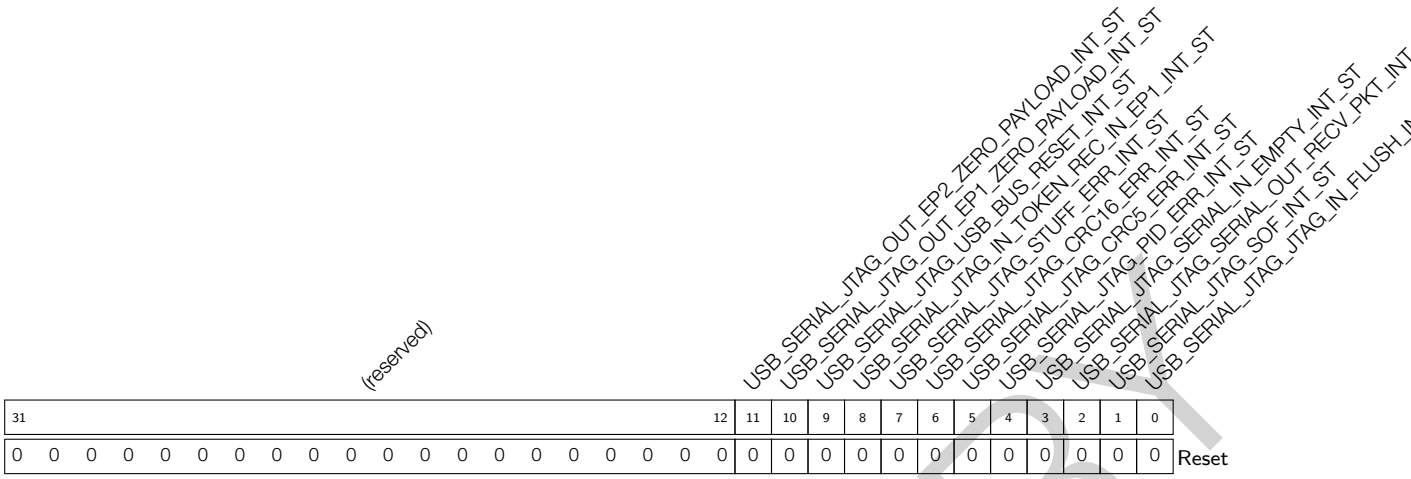
USB_SERIAL_JTAG_USB_BUS_RESET_INT_RAW The raw interrupt bit turns to high level when usb bus reset is detected. (R/WTC/SS)

USB_SERIAL_JTAG_OUT_EP1_ZERO_PAYLOAD_INT_RAW The raw interrupt bit turns to high level when OUT endpoint 1 received packet with zero palyload. (R/WTC/SS)

USB_SERIAL_JTAG_OUT_EP2_ZERO_PAYLOAD_INT_RAW The raw interrupt bit turns to high level when OUT endpoint 2 received packet with zero palyload. (R/WTC/SS)

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Register 29.7. USB_SERIAL_JTAG_INT_ST_REG (0x000C)



USB_SERIAL_JTAG_JTAG_IN_FLUSH_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_JTAG_IN_FLUSH_INT interrupt. (RO)

USB_SERIAL_JTAG_SOF_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_SOF_INT interrupt. (RO)

USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT interrupt. (RO)

USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT interrupt. (RO)

USB_SERIAL_JTAG_PID_ERR_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_PID_ERR_INT interrupt. (RO)

USB_SERIAL_JTAG_CRC5_ERR_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_CRC5_ERR_INT interrupt. (RO)

USB_SERIAL_JTAG_CRC16_ERR_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_CRC16_ERR_INT interrupt. (RO)

USB_SERIAL_JTAG_STUFF_ERR_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_STUFF_ERR_INT interrupt. (RO)

USB_SERIAL_JTAG_IN_TOKEN_REC_IN_EP1_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_IN_TOKEN_REC_IN_EP1_INT interrupt. (RO)

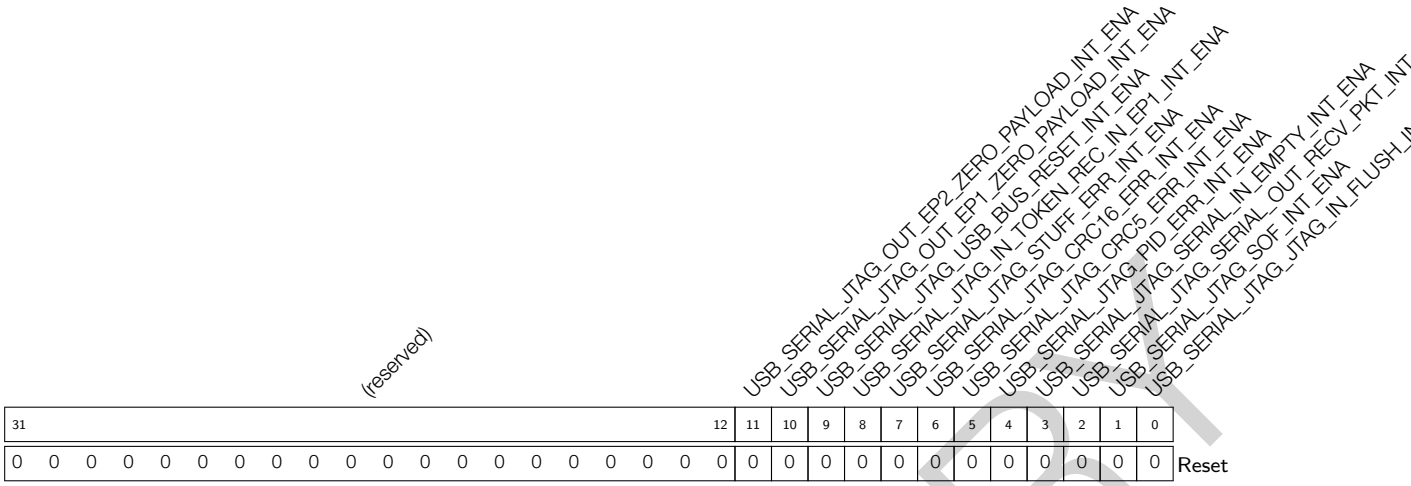
USB_SERIAL_JTAG_USB_BUS_RESET_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_USB_BUS_RESET_INT interrupt. (RO)

USB_SERIAL_JTAG_OUT_EP1_ZERO_PAYLOAD_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_OUT_EP1_ZERO_PAYLOAD_INT interrupt. (RO)

USB_SERIAL_JTAG_OUT_EP2_ZERO_PAYLOAD_INT_ST The raw interrupt status bit for the USB_SERIAL_JTAG_OUT_EP2_ZERO_PAYLOAD_INT interrupt. (RO)

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Register 29.8. USB_SERIAL_JTAG_INT_ENA_REG (0x0010)



USB_SERIAL_JTAG_JTAG_IN_FLUSH_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_JTAG_IN_FLUSH_INT interrupt. (R/W)

USB_SERIAL_JTAG_SOF_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_SOF_INT interrupt. (R/W)

USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT interrupt. (R/W)

USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT interrupt. (R/W)

USB_SERIAL_JTAG_PID_ERR_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_PID_ERR_INT interrupt. (R/W)

USB_SERIAL_JTAG_CRC5_ERR_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_CRC5_ERR_INT interrupt. (R/W)

USB_SERIAL_JTAG_CRC16_ERR_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_CRC16_ERR_INT interrupt. (R/W)

USB_SERIAL_JTAG_STUFF_ERR_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_STUFF_ERR_INT interrupt. (R/W)

USB_SERIAL_JTAG_IN_TOKEN_REC_IN_EP1_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_IN_TOKEN_REC_IN_EP1_INT interrupt. (R/W)

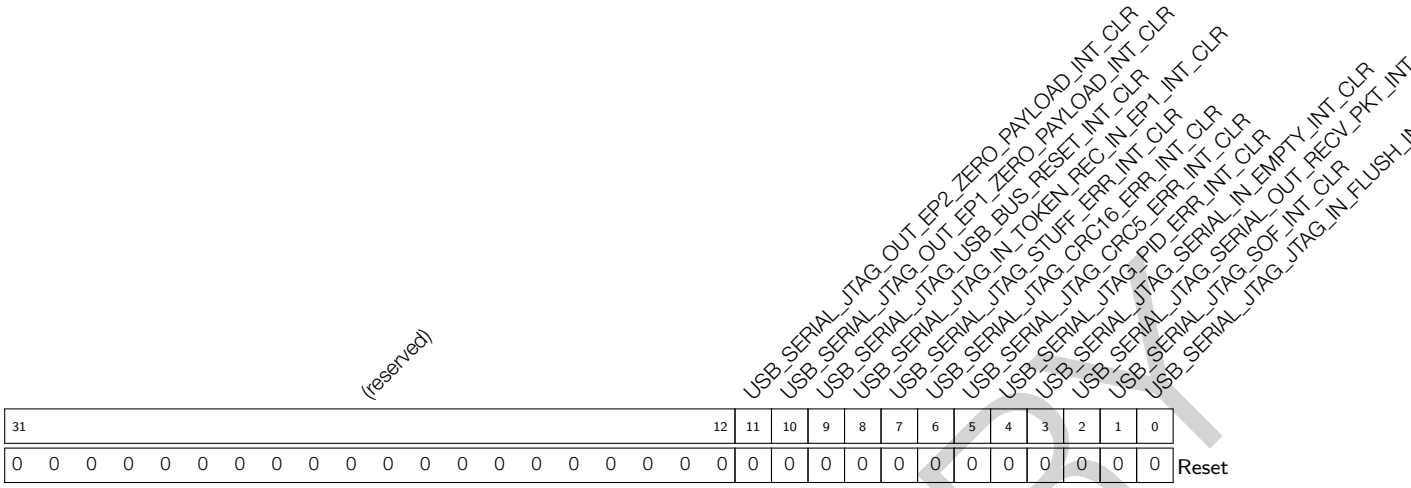
USB_SERIAL_JTAG_USB_BUS_RESET_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_USB_BUS_RESET_INT interrupt. (R/W)

USB_SERIAL_JTAG_OUT_EP1_ZERO_PAYLOAD_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_OUT_EP1_ZERO_PAYLOAD_INT interrupt. (R/W)

USB_SERIAL_JTAG_OUT_EP2_ZERO_PAYLOAD_INT_ENA The interrupt enable bit for the USB_SERIAL_JTAG_OUT_EP2_ZERO_PAYLOAD_INT interrupt. (R/W)

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Register 29.9. USB_SERIAL_JTAG_INT_CLR_REG (0x0014)



USB_SERIAL_JTAG_JTAG_IN_FLUSH_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_JTAG_IN_FLUSH_INT interrupt. (WT)

USB_SERIAL_JTAG_SOF_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_JTAG_SOF_INT interrupt. (WT)

USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT interrupt. (WT)

USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT interrupt. (WT)

USB_SERIAL_JTAG_PID_ERR_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_PID_ERR_INT interrupt. (WT)

USB_SERIAL_JTAG_CRC5_ERR_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_CRC5_ERR_INT interrupt. (WT)

USB_SERIAL_JTAG_CRC16_ERR_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_CRC16_ERR_INT interrupt. (WT)

USB_SERIAL_JTAG_STUFF_ERR_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_STUFF_ERR_INT interrupt. (WT)

USB_SERIAL_JTAG_IN_TOKEN_REC_IN_EP1_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_IN_TOKEN_IN_EP1_INT interrupt. (WT)

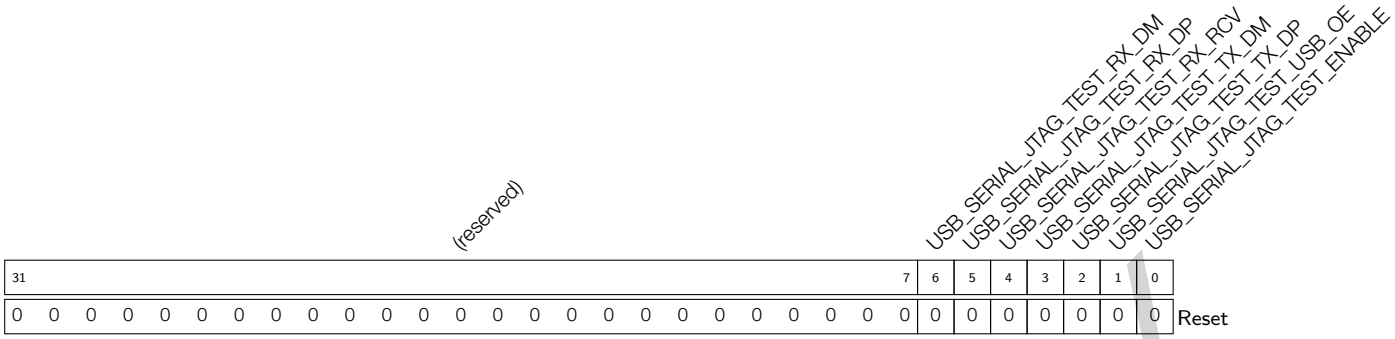
USB_SERIAL_JTAG_USB_BUS_RESET_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_USB_BUS_RESET_INT interrupt. (WT)

USB_SERIAL_JTAG_OUT_EP1_ZERO_PAYLOAD_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_OUT_EP1_ZERO_PAYLOAD_INT interrupt. (WT)

USB_SERIAL_JTAG_OUT_EP2_ZERO_PAYLOAD_INT_CLR Set this bit to clear the USB_SERIAL_JTAG_OUT_EP2_ZERO_PAYLOAD_INT interrupt. (WT)

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Register 29.10. USB_SERIAL_JTAG_TEST_REG (0x001C)



USB_SERIAL_JTAG_TEST_ENABLE Enable test of the USB pad. (R/W)

USB_SERIAL_JTAG_TEST_USB_OE USB pad oe in test. (R/W)

USB_SERIAL_JTAG_TEST_TX_DP USB D+ tx value in test. (R/W)

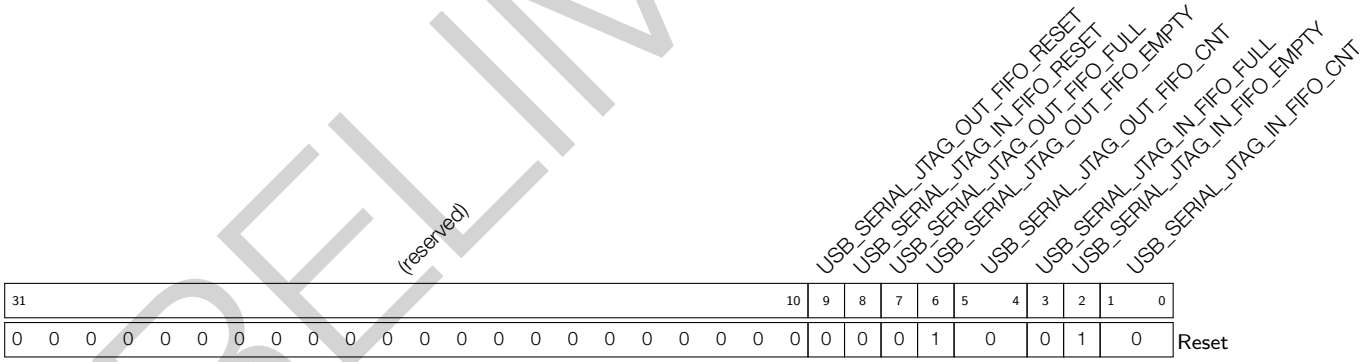
USB_SERIAL_JTAG_TEST_TX_DM USB D- tx value in test. (R/W)

USB_SERIAL_JTAG_TEST_RX_RCV USB differential rx value in test. (RO)

USB_SERIAL_JTAG_TEST_RX_DP USB D+ rx value in test. (RO)

USB_SERIAL_JTAG_TEST_RX_DM USB D- rx value in test. (RO)

Register 29.11. USB_SERIAL_JTAG_JFIFO_ST_REG (0x0020)



USB_SERIAL_JTAG_IN_FIFO_CNT JTAT in fifo counter. (RO)

USB_SERIAL_JTAG_IN_FIFO_EMPTY 1: JTAG in fifo is empty. (RO)

USB_SERIAL_JTAG_IN_FIFO_FULL 1: JTAG in fifo is full. (RO)

USB_SERIAL_JTAG_OUT_FIFO_CNT JTAG out fifo counter. (RO)

USB_SERIAL_JTAG_OUT_FIFO_EMPTY 1: JTAG out fifo is empty. (RO)

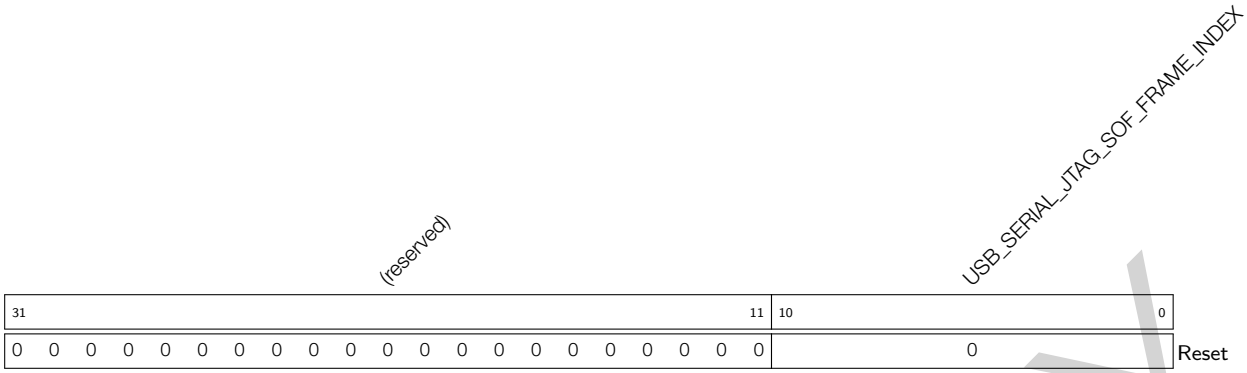
USB_SERIAL_JTAG_OUT_FIFO_FULL 1: JTAG out fifo is full. (RO)

USB_SERIAL_JTAG_IN_FIFO_RESET Write 1 to reset JTAG in fifo. (R/W)

USB_SERIAL_JTAG_OUT_FIFO_RESET Write 1 to reset JTAG out fifo. (R/W)

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Register 29.12. USB_SERIAL_JTAG_FRAM_NUM_REG (0x0024)



USB_SERIAL_JTAG_SOF_FRAME_INDEX Frame index of received SOF frame. (RO)

Register 29.13. USB_SERIAL_JTAG_IN_EP0_ST_REG (0x0028)



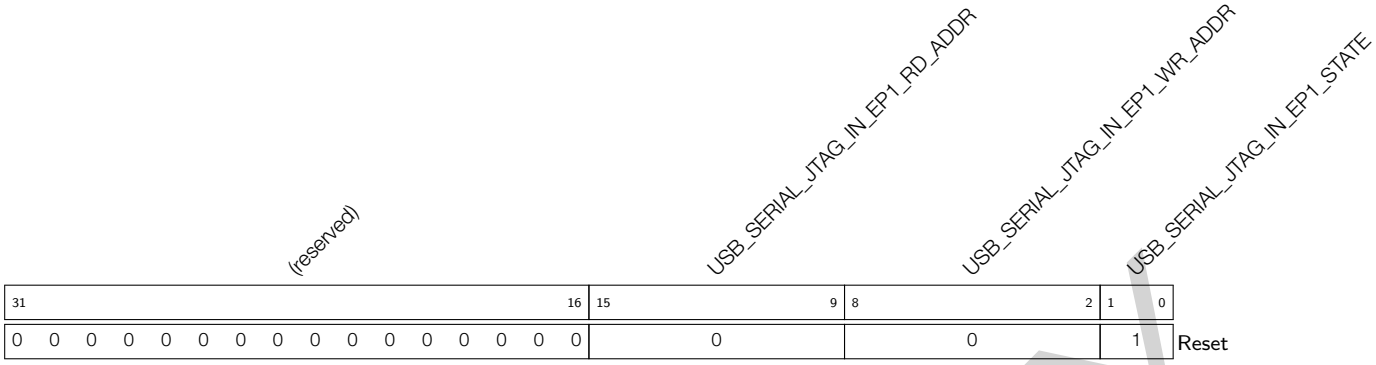
USB_SERIAL_JTAG_IN_EP0_STATE State of IN Endpoint 0. (RO)

USB_SERIAL_JTAG_IN_EP0_WR_ADDR Write data address of IN endpoint 0. (RO)

USB_SERIAL_JTAG_IN_EP0_RD_ADDR Read data address of IN endpoint 0. (RO)

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Register 29.14. USB_SERIAL_JTAG_IN_EP1_ST_REG (0x002C)

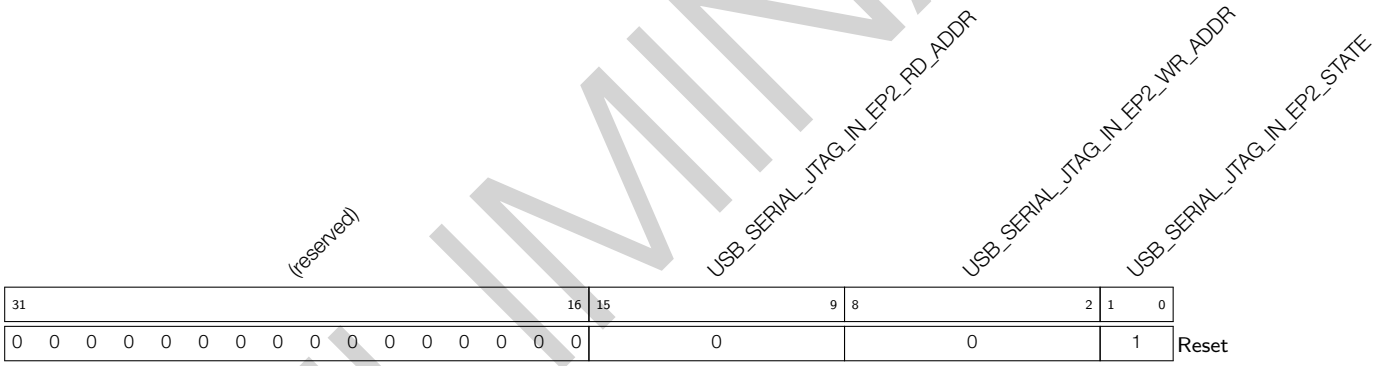


USB_SERIAL_JTAG_IN_EP1_STATE State of IN Endpoint 1. (RO)

USB_SERIAL_JTAG_IN_EP1_WR_ADDR Write data address of IN endpoint 1. (RO)

USB_SERIAL_JTAG_IN_EP1_RD_ADDR Read data address of IN endpoint 1. (RO)

Register 29.15. USB_SERIAL_JTAG_IN_EP2_ST_REG (0x0030)



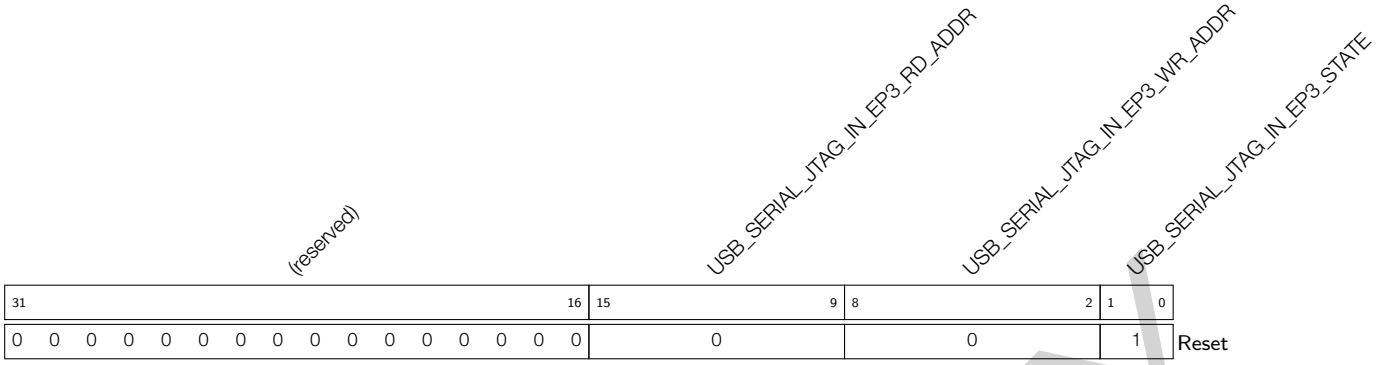
USB_SERIAL_JTAG_IN_EP2_STATE State of IN Endpoint 2. (RO)

USB_SERIAL_JTAG_IN_EP2_WR_ADDR Write data address of IN endpoint 2. (RO)

USB_SERIAL_JTAG_IN_EP2_RD_ADDR Read data address of IN endpoint 2. (RO)

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Register 29.16. USB_SERIAL_JTAG_IN_EP3_ST_REG (0x0034)

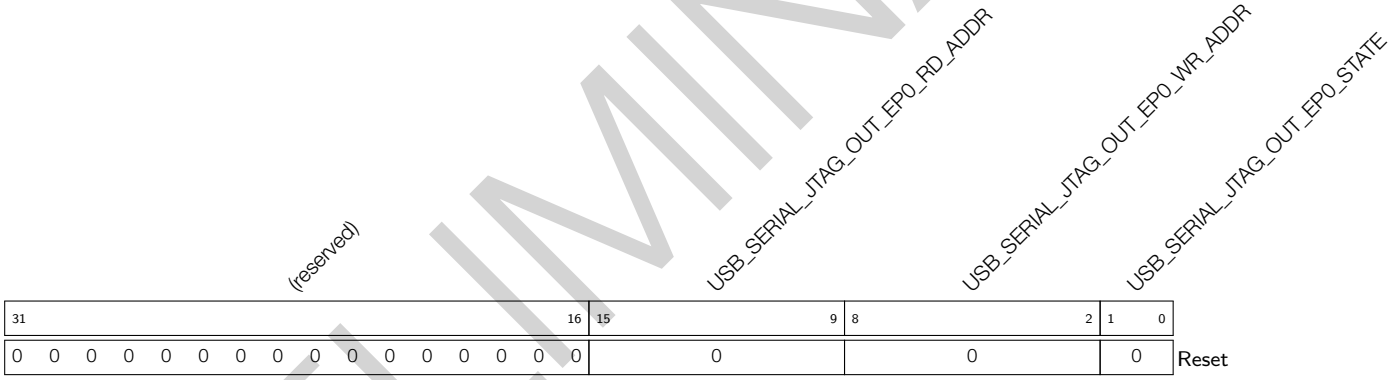


USB_SERIAL_JTAG_IN_EP3_STATE State of IN Endpoint 3. (RO)

USB_SERIAL_JTAG_IN_EP3_WR_ADDR Write data address of IN endpoint 3. (RO)

USB_SERIAL_JTAG_IN_EP3_RD_ADDR Read data address of IN endpoint 3. (RO)

Register 29.17. USB_SERIAL_JTAG_OUT_EP0_ST_REG (0x0038)



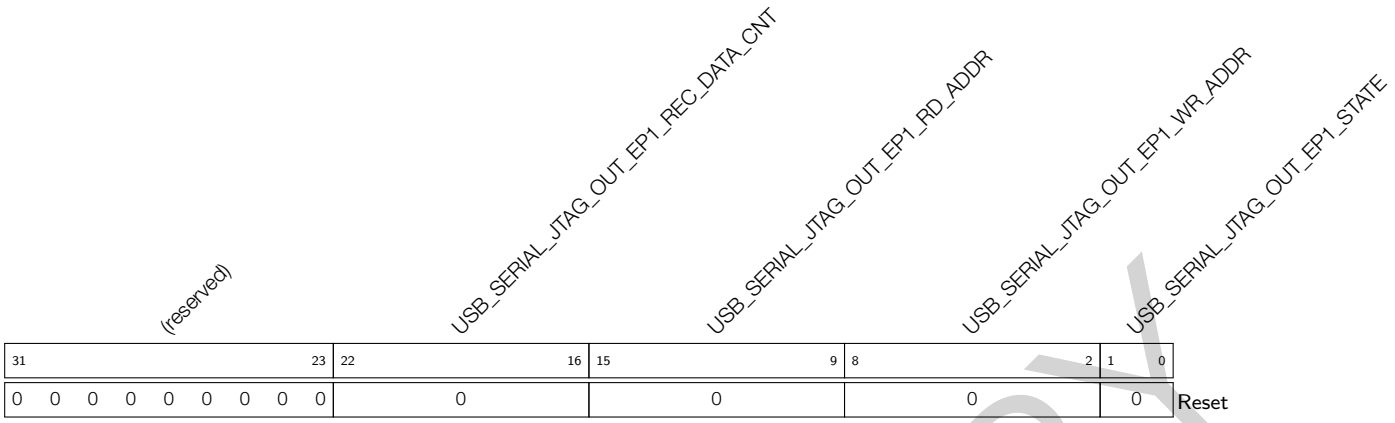
USB_SERIAL_JTAG_OUT_EP0_STATE State of OUT Endpoint 0. (RO)

USB_SERIAL_JTAG_OUT_EP0_WR_ADDR Write data address of OUT endpoint 0. When USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT is detected, there are USB_SERIAL_JTAG_OUT_EP0_WR_ADDR-2 bytes data in OUT EP0. (RO)

USB_SERIAL_JTAG_OUT_EP0_RD_ADDR Read data address of OUT endpoint 0. (RO)

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Register 29.18. USB_SERIAL_JTAG_OUT_EP1_ST_REG (0x003C)



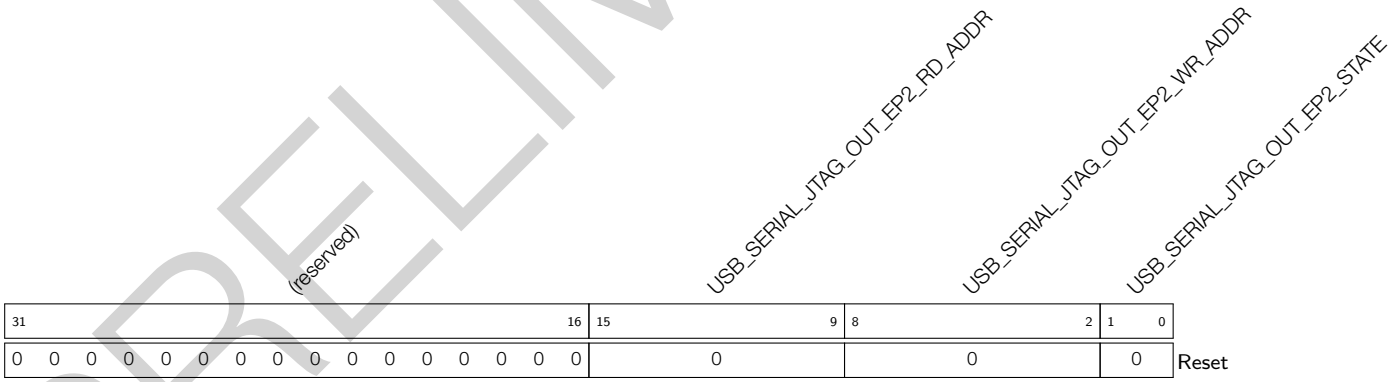
USB_SERIAL_JTAG_OUT_EP1_STATE State of OUT Endpoint 1. (RO)

USB_SERIAL_JTAG_OUT_EP1_WR_ADDR Write data address of OUT endpoint 1. When USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT is detected, there are USB_SERIAL_JTAG_OUT_EP1_WR_ADDR-2 bytes data in OUT EP1. (RO)

USB_SERIAL_JTAG_OUT_EP1_RD_ADDR Read data address of OUT endpoint 1. (RO)

USB_SERIAL_JTAG_OUT_EP1_REC_DATA_CNT Data count in OUT endpoint 1 when one packet is received. (RO)

Register 29.19. USB_SERIAL_JTAG_OUT_EP2_ST_REG (0x0040)



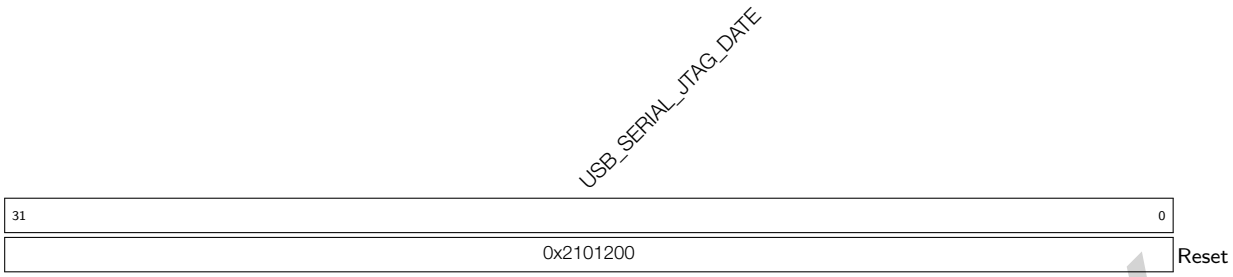
USB_SERIAL_JTAG_OUT_EP2_STATE State of OUT Endpoint 2. (RO)

USB_SERIAL_JTAG_OUT_EP2_WR_ADDR Write data address of OUT endpoint 2. When USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT is detected, there are USB_SERIAL_JTAG_OUT_EP2_WR_ADDR-2 bytes data in OUT EP2. (RO)

USB_SERIAL_JTAG_OUT_EP2_RD_ADDR Read data address of OUT endpoint 2. (RO)

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Register 29.20. USB_SERIAL_JTAG_DATE_REG (0x0080)



USB_SERIAL_JTAG_DATE register version. (R/W)

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30 SD/MMC Host Controller (SDHOST)

30.1 Overview

The ESP32-S3 memory card interface controller provides a hardware interface between the Advanced Peripheral Bus (APB) and an external memory device. The memory card interface allows the ESP32-S3 to be connected to SDIO memory cards, MMC cards and devices with a CE-ATA interface. It supports two external cards (Card0 and Card1). And all SD/MMC module interface signal only connect to GPIO pad by GPIO matrix.

30.2 Features

This module supports the following features:

- Two external cards
- SD Memory Card standard: V3.0 and V3.01
- MMC: V4.41, V4.5, and V4.51
- CE-ATA: V1.1
- 1-bit, 4-bit, and 8-bit modes

The SD/MMC controller topology is shown in Figure 30-1. The controller supports two peripherals which cannot be functional at the same time.

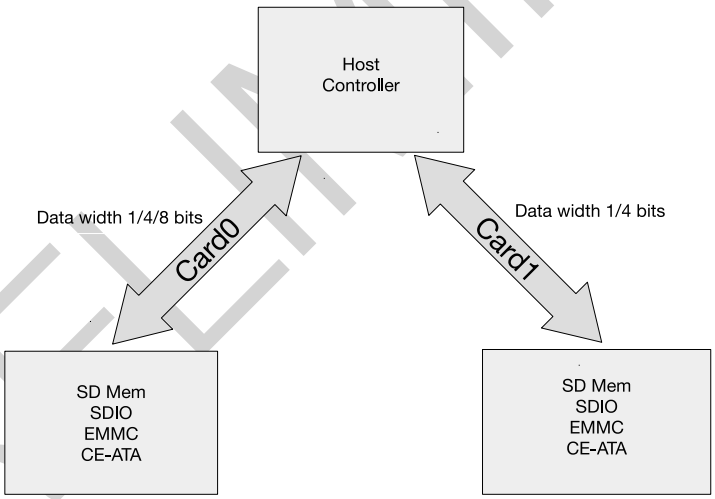


Figure 30-1. SD/MMC Controller Topology

30.3 SD/MMC External Interface Signals

The primary external interface signals, which enable the SD/MMC controller to communicate with an external device, are clock (sdhost_cclk_out_1.eg:card1), command (sdhost_ccmd_out_1) and data signals (sdhost_cdata_in_1[7:0]/sdhost_cdata_out_1[7:0]). Additional signals include the card interrupt, card detect, and write-protect signals. The direction of each signal is shown in Figure 30-2. The direction and description of each pin are listed in Table 30-1.

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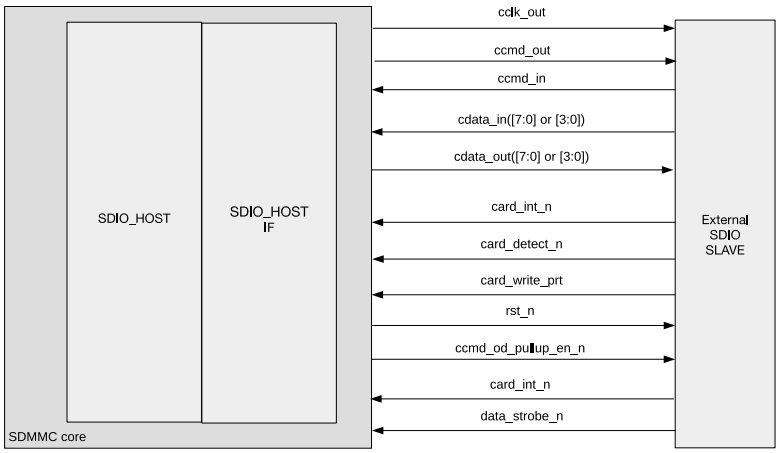


Figure 30-2. SD/MMC Controller External Interface Signals

Table 30-1. SD/MMC Signal Description

Pin	Direction	Description
sdhost_cclk_out	Output	Clock signals for slave device
sdhost_ccmd	Duplex	Duplex command/response lines
sdhost_cdata	Duplex	Duplex data read/write lines
sdhost_card_detect_n	Input	Card detection input line
sdhost_card_write_prt	Input	Card write protection status input
sdhost_rst_n	Output	Hardware reset for MMC4.4 cards
sdhost_ccmd_od_pullup_en_n	output	Card Cmd Open-Drain Pullup
sdhost_card_int_n	Input	Interrupt pin for eSDIO devices
sdhost_data_strobe_n	Input	Card HS400 Data Strobe

30.4 Functional Description

30.4.1 SD/MMC Host Controller Architecture

The SD/MMC host controller consists of two main functional blocks, as shown in Figure 30-3:

- Bus Interface Unit (BIU): It provides APB interfaces for registers, data access method for RMA, and data read and write operation by DMA.
- Card Interface Unit (CIU): It handles external memory card interface protocols. It also provides clock control.

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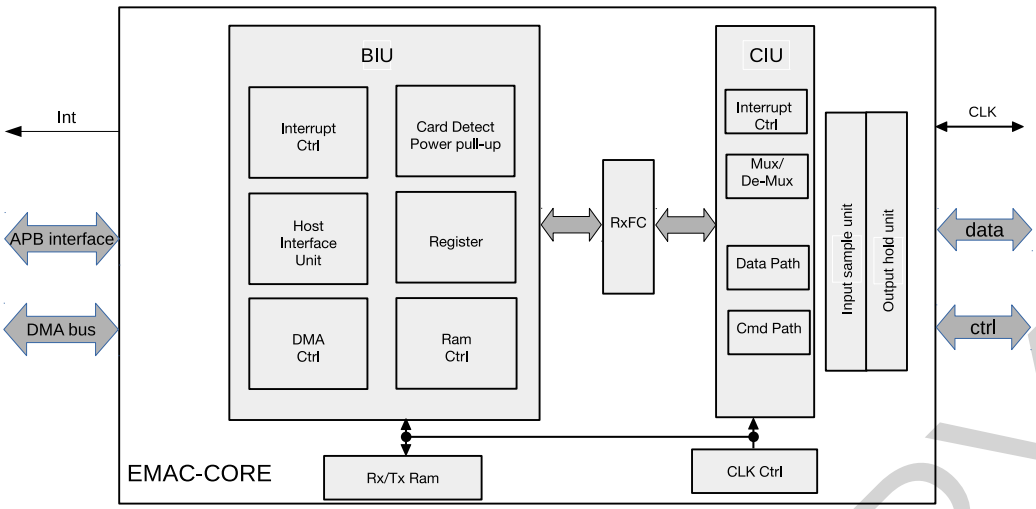


Figure 30-3. SDIO Host Block Diagram

30.4.1.1 Bus Interface Unit (BIU)

The BIU provides the access to registers and RAM data through the Host Interface Unit (HIU). Additionally, it provides a method to access to memory data through a DMA interface. Figure 30-3 illustrates the internal components of the BIU. Figure 30-9 illustrates the clcok slection. The BIU provides the following functions:

- Host interface
- DMA interface
- Interrupt control
- Register access
- FIFO access
- Power/pull-up control and card detection

30.4.1.2 Card Interface Unit (CIU)

The CIU module implements the card-specific protocols. Within the CIU, the command path control unit and data path control unit are used to interface with the command and data ports, respectively, of the SD/MMC/CE-ATA cards. The CIU also provides clock control. Figure 30-3 illustrates the internal structure of the CIU, which consists of the following primary functional blocks:

- Command path
- Data path
- SDIO interrupt control
- Clock control
- Mux/De-Mux unit

30.4.2 Command Path

The command path performs the following functions:

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- Configures clock parameters
- Configures card command parameters
- Sends commands to card bus (sdhost_ccmd_out line)
- Receives responses from card bus (sdhost_ccmd_in line)
- Sends responses to BIU
- Drives the P-bit on the command line

The command path State Machine is shown in Figure 30-4.

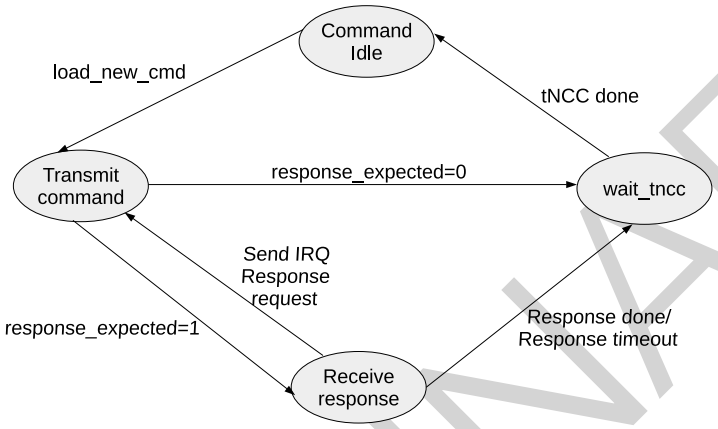


Figure 30-4. Command Path State Machine

30.4.3 Data Path

The data path block pops RAM data and transmits them on sdhost_cdata_out during a write-data transfer, or it receives data on sdhost_cdata_in and pushes them into RAM during a read-data transfer. The data path loads new data parameters, i.e., expected data, read/write data transfer, stream/block transfer, block size, byte count, card type, timeout registers, etc., whenever a data transfer command is not in progress.

If the SDHOST_DATA_EXPECTED bit is set in SDHOST_CMD_REG register, the new command is a data-transfer command and the data path starts one of the following operations:

- Transmitting data if the SDHOST_READ_WRITE bit is 1
- Receiving data if the SDHOST_READ_WRITE bit is 0

30.4.3.1 Data Transmit Operation

The module starts data transmission two clock cycles after a response for the data-write command is received. This occurs even if the command path detects a response error or a cyclic redundancy check (CRC) error in a response. If no response is received from the card until the response timeout, no data are transmitted. Depending on the value of the SDHOST_TRANSFER_MODE bit in SDHOST_CMD_REG register, the data-transmit state machine adds data to the card's data bus in a stream or in block(s). The data transmit state machine is shown in Figure 30-5.

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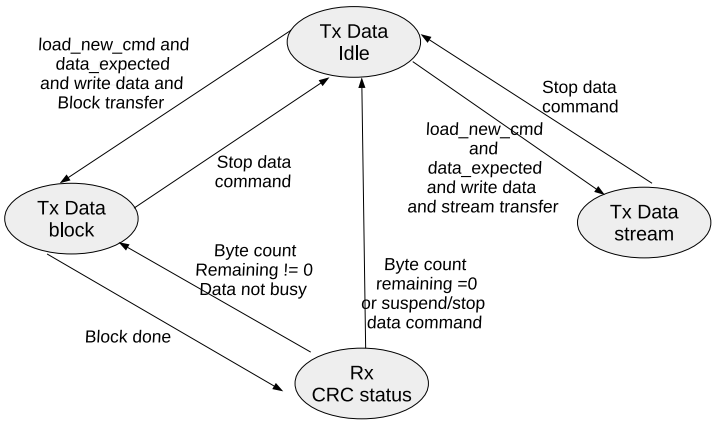


Figure 30-5. Data Transmit State Machine

30.4.3.2 Data Receive Operation

The module receives data two clock cycles after the end bit of a data-read command, even if the command path detects a response error or a CRC error. If no response is received from the card and a response timeout occurs, the BIU does not receive a signal about the completion of the data transfer. If the command sent by the CIU is an illegal operation for the card, it would prevent the card from starting a read-data transfer, and the BIU will not receive a signal about the completion of the data transfer.

If no data is received by the data timeout, the data path signals a data timeout to the BIU, which marks an end to the data transfer. Based on the value of the SDHOST_TRANSFER_MODE bit in SDHOST_CMD_REG register, the data-receive state machine gets data from the card's data bus in a stream or block(s). The data receive state machine is shown in Figure 30-6.

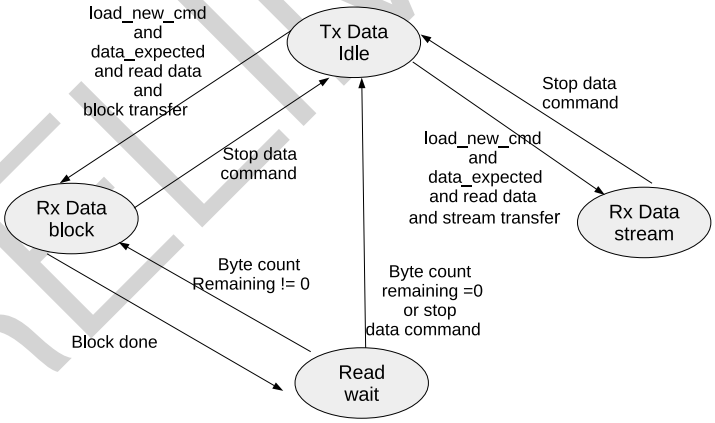


Figure 30-6. Data Receive State Machine

30.5 Software Restrictions for Proper CIU Operation

- Only one card at a time can be selected to execute a command or data transfer. For example, when data are being transferred to or from a card, a new command must not be issued to another card. A new command, however, can be issued to the same card, allowing it to read the device status or stop the transfer.
- Only one command at a time can be issued for data transfers.

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- During an open-ended card-write operation, if the card clock is stopped due to RAM being empty, the software must fill RAM with data first, and then start the card clock. Only then can it issue a stop/abort command to the card.
- During an SDIO/Combo card transfer, if the card function is suspended and the software wants to resume the suspended transfer, it must first reset RAM, setting SDHOST_FIFO_RESET bits and then issue the resume command as if it were a new data-transfer command.
- When issuing card reset commands (CMD0, CMD15 or CMD52_reset), while a card data transfer is in progress, the software must set the SDHOST_STOP_ABORT_CMD bit in SDHOST_CMD_REG register, so that the CIU can stop the data transfer after issuing the card reset command.
- When the data's end bit error is set in the SDHOST_RINTSTS_REG register, the CIU does not guarantee SDIO interrupts. In such a case, the software ignores SDIO interrupts and issues a stop/abort command to the card, so that the card stops sending read-data.
- If the card clock is stopped due to RAM being full during a card read, the software will read at least two RAM locations to restart the card clock.
- Only one CE-ATA device at a time can be selected for a command or data transfer. For example, when data are transferred from a CE-ATA device, a new command should not be sent to another CE-ATA device.
- If a CE-ATA device's interrupts are enabled (nIEN=0), a new SDHOST_RW_BLK command should not be sent to the same device if the execution of a SDHODT_RW_BLK command is already in progress. Only the CCSD can be sent while waiting for the CCS.
- If, however, a CE-ATA device's interrupts are disabled (nIEN=1), a new command can be issued to the same device, allowing it to read status information.
- Open-ended transfers are not supported in CE-ATA devices.
- The sdhost_send_auto_stop signal is not supported (software should not set the sdhost_send_auto_stop bit) in CE-ATA transfers.

After configuring the command start bit to 1, the values of the following registers cannot be changed before a command has been issued:

- CMD - command
- CMDARG - command argument
- BYTCNT - byte count
- BLKSIZ - block size
- CLKDIV - clock divider
- CKLENA - clock enable
- CLKSRC - clock source
- TMOUT - timeout
- CTYPE - card type

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30.6 RAM for Receiving and Sending Data

The submodule RAM is a buffer area for sending and receiving data. It can be divided into two units: the one is for sending data, and the other is for receiving data. The process of sending and receiving data can also be achieved by the CPU and DMA for reading and writing. The latter method is described in detail in Section 30.8.

30.6.1 TX RAM Module

There are two ways to enable a write operation: DMA and CPU read/write.

If SDIO-sending is enabled, data can be written to the TX RAM module by APB interface. Data will be written to register SDHOST_BUFFIFO_REG from the CPU, directly, by an APB interface.

Another way of data transmission is by DMA.

30.6.2 RX RAM Module

There are two ways to enable a read operation: DMA and CPU read/write.

When the data path receives data, the data will be written to the RX RAM. Then, these data can be read with the APB method at the reading end. Register SDHOST_BUFFIFO_REG can be read by the APB directly.

Another way of receiving data is by DMA.

30.7 DMA Descriptor Chain

Each linked list module consists of two parts: the linked list itself and a data buffer. In other words, each module points to a unique data buffer and the linked list that follows the module. Figure 30-7 shows the descriptor chain.

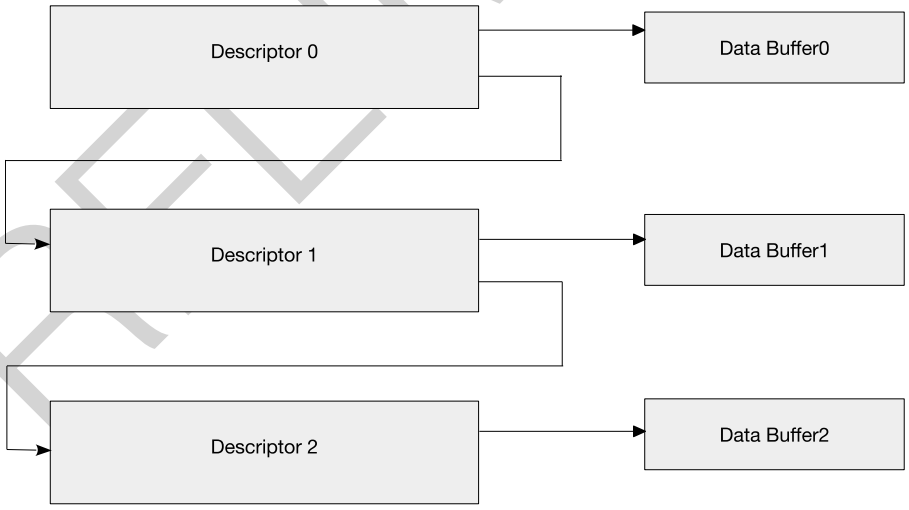


Figure 30-7. Descriptor Chain

30.8 The Structure of DMA descriptor chain

Each linked list consists of four words. As is shown below, Figure 30-8 demonstrates the linked list's structure, and Table 30-2, Table 30-3, Table 30-4, Table 30-5 provide the descriptions of linked lists.

PRELIMINARY

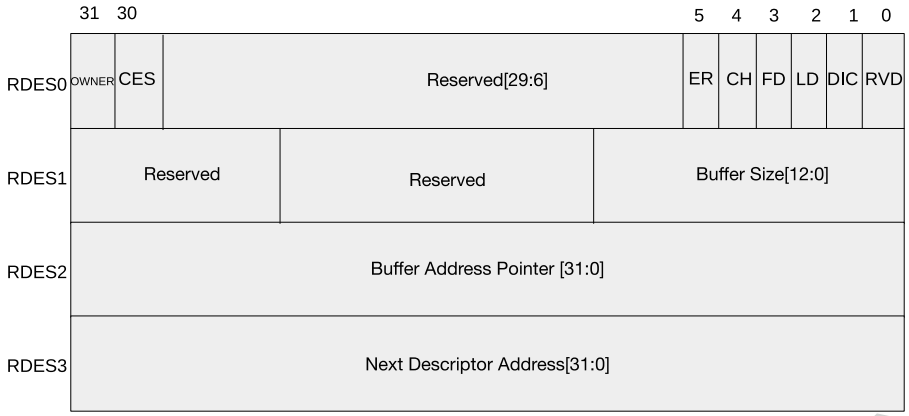


Figure 30-8. The Structure of a Linked List

The DES0 element contains control and status information.

Table 30-2. Word DES0 of SD/MMC GDMA Linked List

Bits	Name	Description
31	OWNER	When set, this bit indicates that the descriptor is owned by the DMA Controller. When reset, it indicates that the descriptor is owned by the Host. The DMA clears this bit when it completes the data transfer.
30	CES (Card Error Summary)	These error bits indicate the status of the transition to or from the card. The following bits are also present in SDHOST_RINTSTS_REG, which indicates their digital logic OR gate. • EBE: End Bit Error • RTO: Response Time out • RCRC: Response CRC • SBE: Start Bit Error • DRTO: Data Read Timeout • DCRC: Data CRC for Receive • RE: Response Error
29:6	Reserved	Reserved
5	ER (End of Ring)	When set, this bit indicates that the descriptor list has reached its final descriptor. The DMA Controller then returns to the base address of the list, creating a Descriptor Chain.
4	CH (Second Address Chained)	When set, this bit indicates that the second address in the descriptor is the Next Descriptor address. When this bit is set, BS2 (DES1[25:13]) should be all zeros.

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Bits	Name	Description
3	FD (First Descriptor)	When set, this bit indicates that this descriptor contains the first buffer of the data. If the size of the first buffer is 0, the Next Descriptor contains the beginning of the data.
2	LD (Last Descriptor)	This bit is associated with the last block of a DMA transfer. When set, the bit indicates that the buffers pointed by this descriptor are the last buffers of the data. After this descriptor is completed, the remaining byte count is 0. In other words, after the descriptor with the LD bit set is completed, the remaining byte count should be 0.
1	DIC (Disable Interrupt on Completion)	When set, this bit will prevent the setting of the TI/RI bit of the DMA Status Register (IDSTS) for the data that ends in the buffer pointed by this descriptor.
0	Reserved	Reserved

The DES1 element contains the buffer size.

Table 30-3. Word DES1 of SD/MMC GDMA Linked List

Bits	Name	Description
31:26	Reserved	Reserved
25:13	Reserved	Reserved
12:0	BS (Buffer Size)	Indicates the size of the data buffer (in Byte), which must be a multiple of four. In the case where the buffer size is not a multiple of four, the resulting behavior is undefined. This field should not be zero.

The DES2 element contains the address pointer to the data buffer.

Table 30-4. Word DES2 of SD/MMC GDMA Linked List

Bits	Name	Description
31:0	Buffer Address Pointer	These bits indicate the physical address of the data buffer. And the buffer address must be word-aligned.

The DES3 element contains the address pointer to the next descriptor if the present descriptor is not the last one in a chained descriptor structure.

Table 30-5. Word DES3 of SD/MMC GDMA Linked List

Bits	Name	Description
31:0	Next Descriptor Address	If CH (DES0[4]) is set, this bit contains the address pointer to the next descriptor.

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Bits	Name	Description
		If this is not the last descriptor in a chained descriptor structure, the address pointer to the next descriptor should be: DES3[1:0] = 0.

30.9 Initialization

30.9.1 DMA Initialization

The DMA Controller initialization should proceed as follows:

1. Write to the DMA Bus Mode Register (SDHOST_BMOD_REG) will set the Host bus's access parameters.
2. Write to the DMA Interrupt Enable Register (SDHOST_IDINTEN_REG) will mask any unnecessary interrupt causes.
3. The software driver creates either the inlink or the outlink descriptors. Then, it writes to the DMA Descriptor List Base Address Register (SDHOST_DBADDR_REG), providing the DMA Controller with the starting address of the list.
4. The DMA Controller engine attempts to acquire descriptors from descriptor lists.

30.9.2 DMA Transmission Initialization

The DMA transmission occurs as follows:

1. The Host sets up the elements (DES0-DES3) for transmission, and sets the OWNER bit (DES0[31]). The Host also prepares the data buffer.
2. The Host programs the write-data command in the CMD register in BIU.
3. The Host also programs the required transmit threshold (SDHOST_TX_WMARK field in SDHOST_FIFOTH_REG register).
4. The DMA Controller engine fetches the descriptor and checks the OWNER bit. If the OWNER bit is not set, it means that the host owns the descriptor. In this case, the DMA Controller enters a suspend-state and asserts the Descriptor Unable interrupt in the SDHOST_IDSTS_REG register. In such a case, the host needs to release the DMA Controller by writing any value to SDHOST_PLDMND_REG.
5. It then waits for the Command Done (CD) bit in DHOST_RINTSTS_REG register and no errors from BIU, which indicates that a transfer has completed.
6. Subsequently, the DMA Controller engine waits for a DMA interface request from BIU. This request will be generated, based on the programmed transmit-threshold value. For the last bytes of data which cannot be accessed using a burst, single transfers are performed on the AHB Master Interface.
7. The DMA Controller fetches the transmit data from the data buffer in the Host memory and transfers them to RAM for transmission to card.
8. When data span across multiple descriptors, the DMA Controller fetches the next descriptor and extends its operation using the following descriptor. The last descriptor bit indicates whether the data span multiple descriptors or not.

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9. When data transmission is complete, the status information is updated in the SDHOST_IDSTS_REG register by setting the SDHOST_IDSTS_TI, if it has already been enabled. Also, the OWNER bit is cleared by the DMA Controller by performing a write transaction to DES0.

30.9.3 DMA Reception Initialization

The DMA reception occurs as follows:

1. The Host sets up the element (DES0-DES3) for reception, and sets the OWNER bit (DES0[31]).
2. The Host programs the read-data command in the CMD register in BIU.
3. Then, the Host programs the required level of the receive-threshold (SDHOST_RX_WMARK field in SDHOST_FIFOTH_REG register).
4. The DMA Controller engine fetches the descriptor and checks the OWNER bit. If the OWNER bit is not set, it means that the host owns the descriptor. In this case, the DMA enters a suspend-state and asserts the Descriptor Unable interrupt in the SDHOST_IDSTS_REG register. In such a case, the host needs to release the DMA Controller by writing any value to SDHOST_PLDMND_REG.
5. It then waits for the Command Done (CD) bit and no errors from BIU, which indicates that a reception can be done.
6. The DMA Controller engine then waits for a DMA interface request from BIU. This request will be generated, based on the programmed receive-threshold value. For the last bytes of the data which cannot be accessed using a burst, single transfers are performed on the AHB.
7. The DMA Controller fetches the data from RAM and transfers them to the Host memory.
8. When data span across multiple descriptors, the DMA Controller will fetch the next descriptor and extend its operation using the following descriptor. The last descriptor bit indicates whether the data span multiple descriptors or not.
9. When data reception is complete, the status information is updated in the SDHOST_IDSTS_REG register by setting SDHOST_IDSTS_RI, if it has already been enabled. Also, the OWNER bit is cleared by the DMA Controller by performing a write-transaction to DES0.

30.10 Clock Phase Selection

If the setup time requirements for the input or output data signal are not met, users can specify the clock phase, as shown in the figure 30-9.

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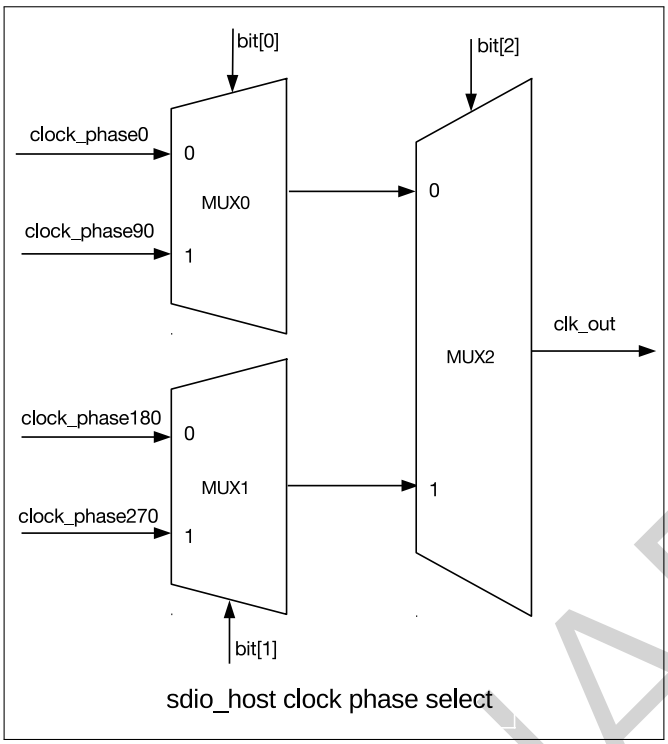


Figure 30-9. Clock Phase Selection

This issue can be fixed by configuring register SDHOST_CLK_DIV_EDGE_REG. For example, set CCLKIN_EDGE_DRV_SEL bit to 0 to drive the output data in phase0, and set the CCLKIN_EDGE_SAM_SEL bit to 1 to select phase90 to sample the data from SDIO slave, if there are still timing issue, please set bit 4 or 6 to use phase180 or phase 270 to sample the data from SDIO slave.

Please find detailed information on the clock phase selection register SDHOST_CLK_DIV_EDGE_REG in Section Registers.

Table 30-6. SDHOST Clk Phase Selection

Clock phase	phase_select value
0	0
90	1
180	4
270	6

30.11 Interrupt

Interrupts can be generated as a result of various events. The SDHOST_IDSTS_REG register contains all the bits that might cause an interrupt. The SDHOST_IDINTEN_REG register contains an enable bit for each of the events that can cause an interrupt.

There are two groups of summary interrupts, ”Normal” ones (bit8 SDHOST_IDSTS_NIS) and ”Abnormal” ones (bit9 SDHOST_IDSTS_AIS), as outlined in the SDHOST_IDSTS_REG register. Interrupts are cleared by writing 1 to the position of the corresponding bit. When all the enabled interrupts within a group are cleared, the corresponding summary bit is also cleared. When both summary bits are cleared, the interrupt signal connected to CPU is de-asserted (stops signalling).

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Interrupts are not queued up, and if a new interrupt-event occurs before the driver has responded to it, no additional interrupts are generated. For example, the SDHOST_IDSTS_RI indicates that one or more data were transferred to the Host buffer.

An interrupt is generated only once for concurrent events. The driver must scan the SDHOST_IDSTS_REG register for the interrupt cause.

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30.12 Register Summary

The addresses in this section are relative to SD/MMC Host Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
SDHOST_CTRL_REG	Control register	0x0000	R/W
SDHOST_CLKDIV_REG	Clock divider configuration register	0x0008	R/W
SDHOST_CLKSRC_REG	Clock source selection register	0x000C	R/W
SDHOST_CLKENA_REG	Clock enable register	0x0010	R/W
SDHOST_TMOUT_REG	Data and response timeout configuration register	0x0014	R/W
SDHOST_CTYPE_REG	Card bus width configuration register	0x0018	R/W
SDHOST_BLKSIZ_REG	Card data block size configuration register	0x001C	R/W
SDHOST_BYTCNT_REG	Data transfer length configuration register	0x0020	R/W
SDHOST_INTMASK_REG	SDIO interrupt mask register	0x0024	R/W
SDHOST_CMDARG_REG	Command argument data register	0x0028	R/W
SDHOST_CMD_REG	Command and boot configuration register	0x002C	R/W
SDHOST_RESP0_REG	Response data register	0x0030	RO
SDHOST_RESP1_REG	Long response data register	0x0034	RO
SDHOST_RESP2_REG	Long response data register	0x0038	RO
SDHOST_RESP3_REG	Long response data register	0x003C	RO
SDHOST_MINTSTS_REG	Masked interrupt status register	0x0040	RO
SDHOST_RINTSTS_REG	Raw interrupt status register	0x0044	R/W
SDHOST_STATUS_REG	SD/MMC status register	0x0048	RO
SDHOST_FIFOTH_REG	FIFO configuration register	0x004C	R/W
SDHOST_CDETECT_REG	Card detect register	0x0050	RO
SDHOST_WRTPRT_REG	Card write protection (WP) status register	0x0054	RO
SDHOST_TCBCNT_REG	Transferred byte count register	0x005C	RO
SDHOST_TBBCNT_REG	Transferred byte count register	0x0060	RO
SDHOST_DEBNCE_REG	Debounce filter time configuration register	0x0064	R/W
SDHOST_USRID_REG	User ID (scratchpad) register	0x0068	R/W
SDHOST_VERID_REG	Version ID (scratchpad) register	0x006C	RO
SDHOST_HCON_REG	Hardware feature register	0x0070	RO
SDHOST_UHS_REG	UHS-1 register	0x0074	R/W
SDHOST_RST_N_REG	Card reset register	0x0078	R/W
SDHOST_BMOD_REG	Burst mode transfer configuration register	0x0080	R/W
SDHOST_PLDMND_REG	Poll demand configuration register	0x0084	WO
SDHOST_DBADDR_REG	Descriptor base address register	0x0088	R/W
SDHOST_IDSTS_REG	IDMAC status register	0x008C	R/W
SDHOST_IDINTEN_REG	IDMAC interrupt enable register	0x0090	R/W
SDHOST_DSCADDR_REG	Host descriptor address pointer	0x0094	RO
SDHOST_BUFADDR_REG	Host buffer address pointer register	0x0098	RO
SDHOST_CARDTHRCTL_REG	Card Threshold Control register	0x0100	R/W
SDHOST_EMMCDDR_REG	eMMC DDR register	0x010C	R/W
SDHOST_ENSHIFT_REG	Enable Phase Shift register	0x0110	R/W

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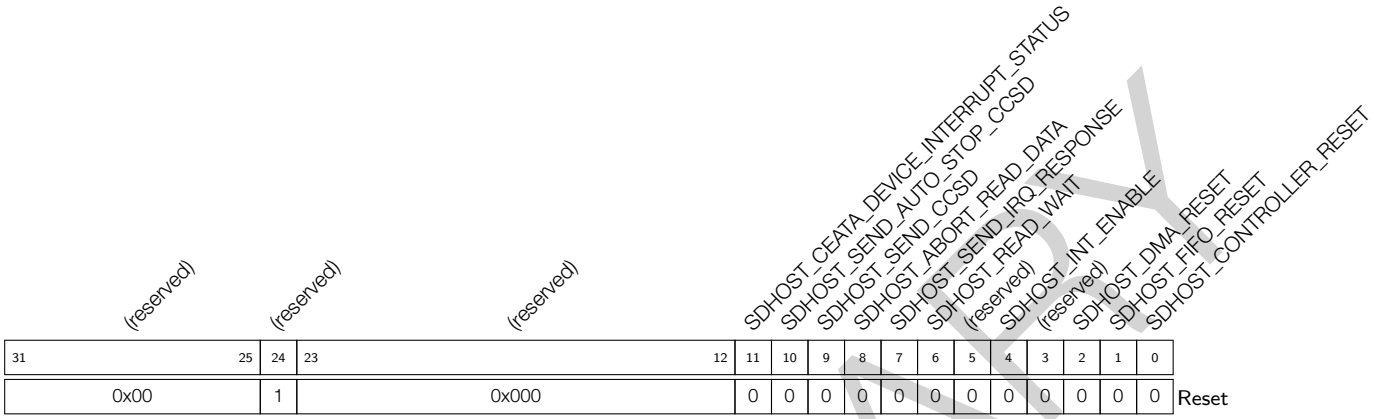
Name	Description	Address	Access
SDHOST_BUFFIFO_REG	CPU write and read transmit data by FIFO	0x0200	R/W
SDHOST_CLK_DIV_EDGE_REG	Clock phase selection register	0x0800	R/W

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30.13 Registers

The addresses in this section are relative to SD/MMC Host Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 30.1. SDHOST_CTRL_REG (0x0000)



SDHOST_CEATA_DEVICE_INTERRUPT_STATUS Software should appropriately write to this bit after the power-on reset or any other reset to the CE-ATA device. After reset, the CE-ATA device's interrupt is usually disabled (nIEN = 1). If the host enables the CE-ATA device's interrupt, then software should set this bit. (R/W)

SDHOST_SEND_AUTO_STOP_CCSD Always set SDHOST_SEND_AUTO_STOP_CCSD and SDHOST_SEND_CCSD bits together; SDHOST_SEND_AUTO_STOP_CCSD should not be set independently of send_ccsd. When set, SD/MMC automatically sends an internally-generated STOP command (CMD12) to the CE-ATA device. After sending this internally-generated STOP command, the Auto Command Done (ACD) bit in SDHOST_RINTSTS_REG is set and an interrupt is generated for the host, in case the ACD interrupt is not masked. After sending the Command Completion Signal Disable (CCSD), SD/MMC automatically clears the SDHOST_SEND_AUTO_STOP_CCSD bit. (R/W)

SDHOST_SEND_CCSD When set, SD/MMC sends CCSD to the CE-ATA device. Software sets this bit only if the current command is expecting CCS (that is, RW_BLK), and if interrupts are enabled for the CE-ATA device. Once the CCSD pattern is sent to the device, SD/MMC automatically clears the SDHOST_SEND_CCSD bit. It also sets the Command Done (CD) bit in the SDHOST_RINTSTS_REG register, and generates an interrupt for the host, in case the Command Done interrupt is not masked.

NOTE: Once the SDHOST_SEND_CCSD bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, within the boundary conditions the CCSD may be sent to the CE-ATA device, even if the device has signalled CCS. (R/W)

Continued on the next page...

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Register 30.1. SDHOST_CTRL_REG (0x0000)

Continued from the previous page...

SDHOST_ABORT_READ_DATA After a suspend-command is issued during a read-operation, software polls the card to find when the suspend-event occurred. Once the suspend-event has occurred, software sets the bit which will reset the data state machine that is waiting for the next block of data. This bit is automatically cleared once the data state machine is reset to idle. (R/W)

SDHOST_SEND_IRQ_RESPONSE Bit automatically clears once response is sent. To wait for MMC card interrupts, host issues CMD40 and waits for interrupt response from MMC card(s). In the meantime, if host wants SD/MMC to exit waiting for interrupt state, it can set this bit, at which time SD/MMC command state-machine sends CMD40 response on bus and returns to idle state. (R/W)

SDHOST_READ_WAIT For sending read-wait to SDIO cards. (R/W)

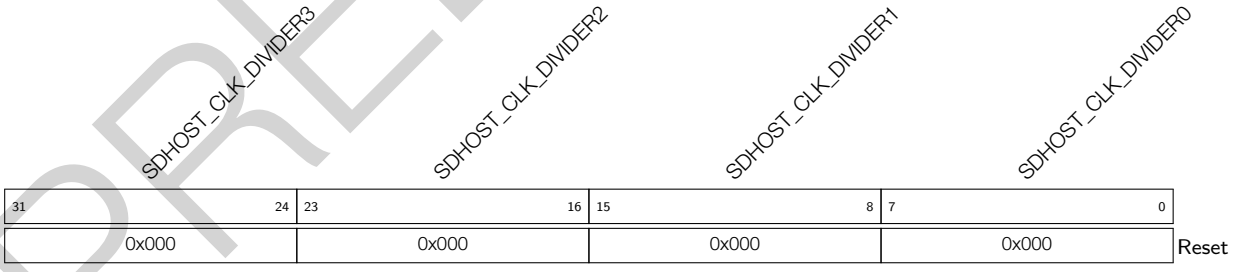
SDHOST_INT_ENABLE Global interrupt enable/disable bit. 0: Disable; 1: Enable. (R/W)

SDHOST_DMA_RESET To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks. (R/W)

SDHOST_FIFO_RESET To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation.
Note: FIFO pointers will be out of reset after 2 cycles of system clocks in addition to synchronization delay (2 cycles of card clock), after the fifo_reset is cleared. (R/W)

SDHOST_CONTROLLER_RESET To reset controller, firmware should set this bit. This bit is auto-cleared after two AHB and two sdhost_cclk_in clock cycles. (R/W)

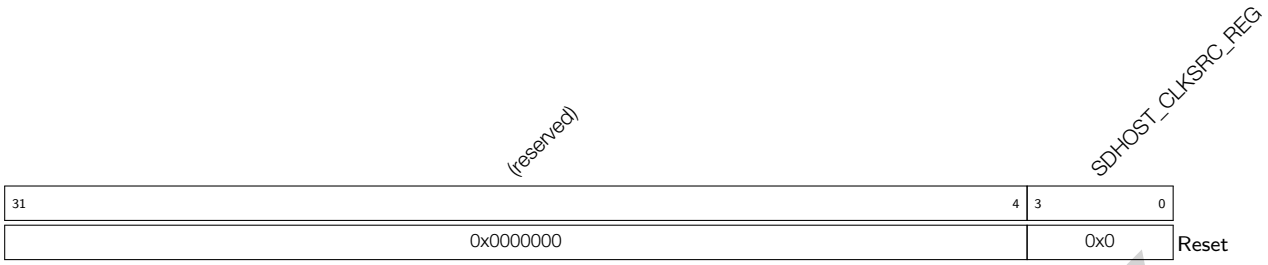
Register 30.2. SDHOST_CLKDIV_REG (0x0008)



SDHOST_CLK_DIVIDER*m* Clock divider (*m*) value. Clock divisor is 2**n*, where *n* = 0 bypasses the divider (divisor of 1). For example, a value of 1 means divided by 2*1 = 2, a value of 0xFF means divided by 2*255 = 510, and so on. The range of *m* is 0 ~ 3. (R/W)

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Register 30.3. SDHOST_CLKSRC_REG (0x000C)



SDHOST_CLKSRC_REG Clock divider source for two SD cards is supported. Each card has two bits assigned to it. For example, bit[1:0] are assigned for card 0, bit[3:2] are assigned for card 1. Card 0 maps and internally routes clock divider[0:3] outputs to cclk_out[1:0] pins, depending on bit value. (R/W)

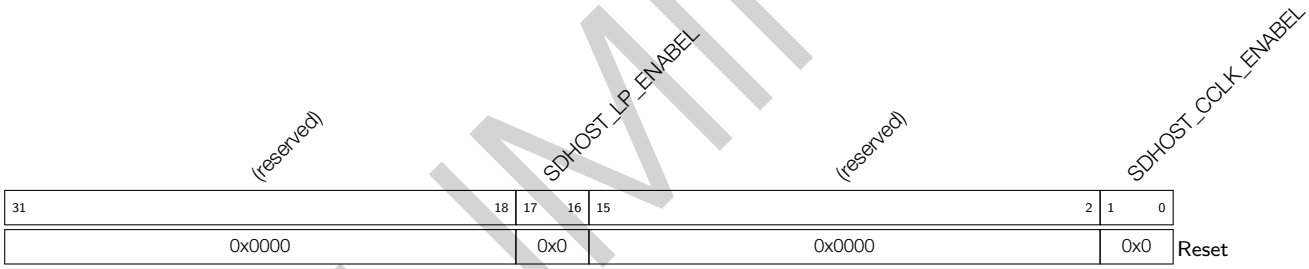
00 : Clock divider 0;

01 : Clock divider 1;

10 : Clock divider 2;

11 : Clock divider 3.

Register 30.4. SDHOST_CLKENA_REG (0x0010)



SDHOST_LP_ENABLE Disable clock when the card is in IDLE state. One bit per card. (R/W)

0: clock disabled;

1: clock enabled.

SDHOST_CCLK_ENABLE Clock-enable control for two SD card clocks and one MMC card clock is supported. One bit per card. (R/W)

0: Clock disabled;

1: Clock enabled.

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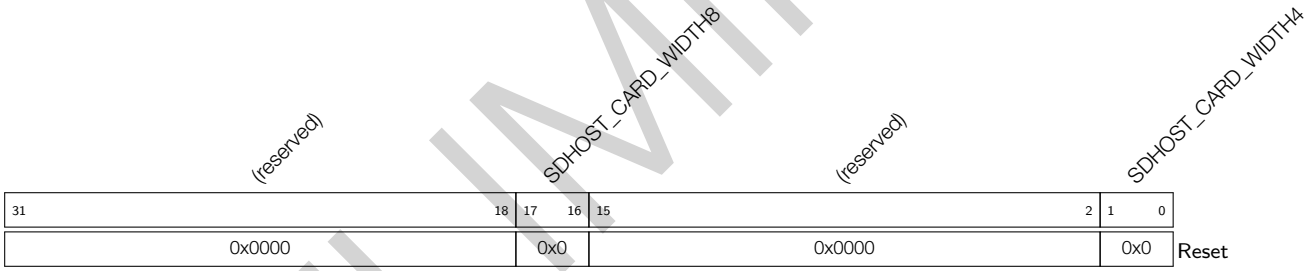
Register 30.5. SDHOST_TMOUT_REG (0x0014)



SDHOST_DATA_TIMEOUT Value for card data read timeout. This value is also used for data starvation by host timeout. The timeout counter is started only after the card clock is stopped. This value is specified in number of card output clocks, i.e. sdhost_cclk_out of the selected card. (R/W)
NOTE: The software timer should be used if the timeout value is in the order of 100 ms. In this case, read data timeout interrupt needs to be disabled.

SDHOST_RESPONSE_TIMEOUT Response timeout value. Value is specified in terms of number of card output clocks, i.e., sdhost_cclk_out. (R/W)

Register 30.6. SDHOST_CTYPE_REG (0x0018)

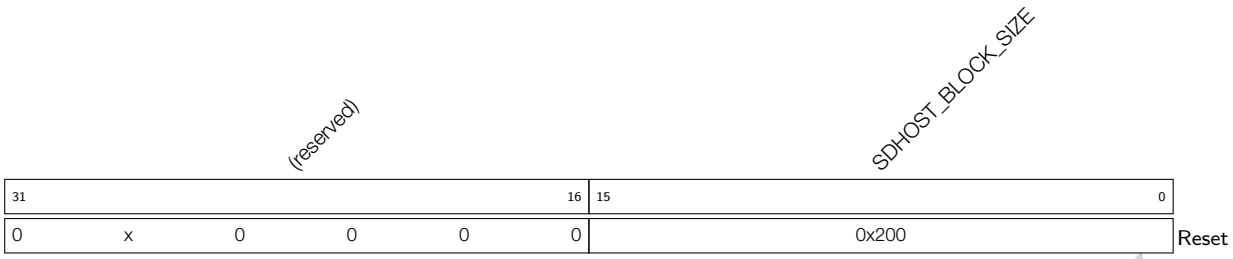


SDHOST_CARD_WIDTH8 One bit per card indicates if card is in 8-bit mode. (R/W)
0: Non 8-bit mode;
1: 8-bit mode.
Bit[17:16] correspond to card[1:0] respectively.

SDHOST_CARD_WIDTH4 One bit per card indicates if card is 1-bit or 4-bit mode. (R/W)
0: 1-bit mode;
1: 4-bit mode.
Bit[1:0] correspond to card[1:0] respectively.

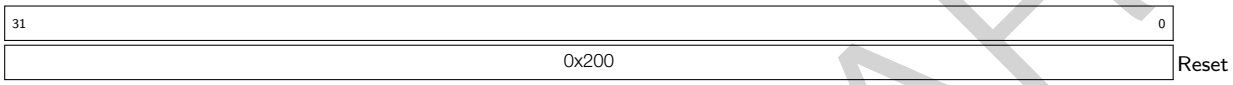
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Register 30.7. SDHOST_BLKSIZ_REG (0x001C)



SDHOST_BLOCK_SIZE Block size. (R/W)

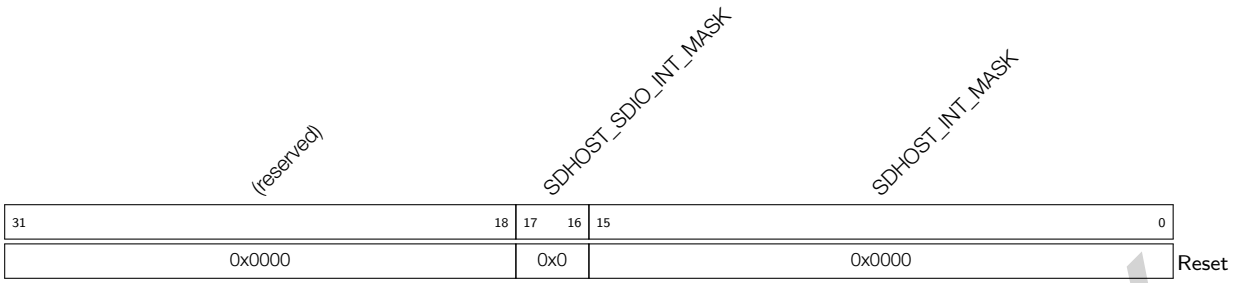
Register 30.8. SDHOST_BYTCNT_REG (0x0020)



SDHOST_BYTCNT_REG Number of bytes to be transferred, should be an integral multiple of Block Size for block transfers. For data transfers of undefined byte lengths, byte count should be set to 0. When byte count is set to 0, it is the responsibility of host to explicitly send stop/abort command to terminate data transfer. (R/W)

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Register 30.9. SDHOST_INTMASK_REG (0x0024)

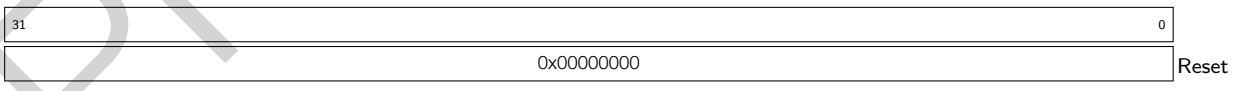


SDHOST_SDIO_INT_MASK SDIO interrupt mask, one bit for each card. Bit[17:16] correspond to card[15:0] respectively. When masked, SDIO interrupt detection for that card is disabled. 0 masks an interrupt, and 1 enables an interrupt. (R/W)

SDHOST_INT_MASK These bits used to mask unwanted interrupts. A value of 0 masks interrupt, and a value of 1 enables the interrupt. (R/W)

Bit 15 (EBE): End-bit error/no CRC error;
Bit 14 (ACD): Auto command done;
Bit 13 (SBE/BCI): Rx Start Bit Error;
Bit 12 (HLE): Hardware locked write error;
Bit 11 (FRUN): FIFO underrun/overrun error;
Bit 10 (HTO): Data starvation-by-host timeout;
Bit 9 (DRTO): Data read timeout;
Bit 8 (RTO): Response timeout;
Bit 7 (DCRC): Data CRC error;
Bit 6 (RCRC): Response CRC error;
Bit 5 (RXDR): Receive FIFO data request;
Bit 4 (TXDR): Transmit FIFO data request;
Bit 3 (DTO): Data transfer over;
Bit 2 (CD): Command done;
Bit 1 (RE): Response error;
Bit 0 (CD): Card detect.

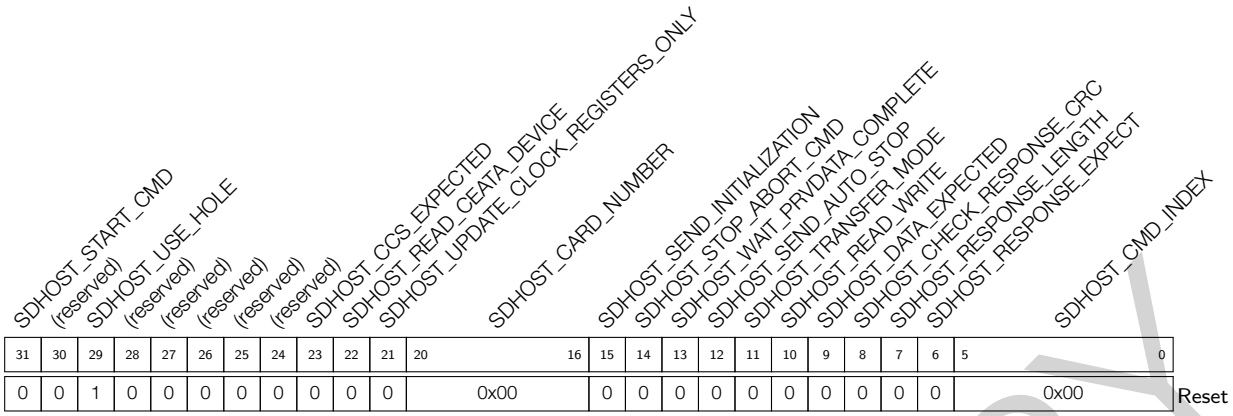
Register 30.10. SDHOST_CMDARG_REG (0x0028)



SDHOST_CMDARG_REG Value indicates command argument to be passed to the card. (R/W)

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Register 30.11. SDHOST_CMD_REG (0x002C)



SDHOST_START_CMD Start command. Once command is served by the CIU, this bit is automatically cleared. When this bit is set, host should not attempt to write to any command registers. If a write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and a response is received from SD_MMC_CEATA cards, Command Done bit is set in the raw interrupt Register. (R/W)

SDHOST_USE_HOLE Use Hold Register. (R/W)

0: CMD and DATA sent to card bypassing HOLD Register;

1: CMD and DATA sent to card through the HOLD Register.

SDHOST_CCS_EXPECTED Expected Command Completion Signal (CCS) configuration. (R/W)

0: Interrupts are not enabled in CE-ATA device (nIEN = 1 in ATA control register), or command does not expect CCS from device;

1: Interrupts are enabled in CE-ATA device (nIEN = 0), and RW_BLK command expects command completion signal from CE-ATA device.

If the command expects Command Completion Signal (CCS) from the CE-ATA device, the software should set this control bit. SD/MMC sets Data Transfer Over (DTO) bit in RINTSTS register and generates interrupt to host if Data Transfer Over interrupt is not masked.

SDHOST_READ_CEATA_DEVICE Read access flag. (R/W)

0: Host is not performing read access (RW_REG or RW_BLK)towards CE-ATA device;

1: Host is performing read access (RW_REG or RW_BLK) towards CE-ATA device.

Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. SD/MMC should not indicate read data timeout while waiting for data from CE-ATA device.

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Register 30.11. SDHOST_CMD_REG (0x002C)

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SDHOST_UPDATE_CLOCK_REGISTERS_ONLY 0: Normal command sequence; 1: Do not send commands, just update clock register value into card clock domain. (R/W)
Following register values are transferred into card clock domain: CLKDIV, CLRSRC, and CLKENA. Changes card clocks (change frequency, truncate off or on, and set low-frequency mode). This is provided in order to change clock frequency or stop clock without having to send command to cards.
During normal command sequence, when sdhost_update_clock_registers_only = 0, following control registers are transferred from BIU to CIU: CMD, CMDARG, TMOUT, CTYPE, BLKSIZ, and BYTCNT. CIU uses new register values for new command sequence to card(s). When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards.

SDHOST_CARD_NUMBER Card number in use. Represents physical slot number of card being accessed. In SD-only mode, up to two cards are supported. (R/W)

SDHOST_SEND_INITIALIZATION 0: Do not send initialization sequence (80 clocks of 1) before sending this command; 1: Send initialization sequence before sending this command. (R/W)
After powered on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card.

SDHOST_STOP_ABORT_CMD 0: Neither stop nor abort command can stop current data transfer. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0; 1: Stop or abort command intended to stop current data transfer in progress. (R/W)
When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state.

SDHOST_WAIT_PRVDATA_COMPLETE 0: Send command at once, even if previous data transfer has not completed; 1: Wait for previous data transfer to complete before sending Command. (R/W)
The SDHOST_WAIT_PRVDATA_COMPLETE] = 0 option is typically used to query status of card during data transfer or to stop current data transfer. SDHOST_CARD_NUMBERr should be same as in previous command.

SDHOST_SEND_AUTO_STOP 0: No stop command is sent at the end of data transfer; 1: Send stop command at the end of data transfer. (R/W)

Continued on the next page...

PRELIMINARY

Register 30.11. SDHOST_CMD_REG (0x002C)

Continued from the previous page ...

SDHOST_TRANSFER_MODE 0: Block data transfer command; 1: Stream data transfer command. (R/W)
Don't care if no data expected.

SDHOST_READ_WRITE 0: Read from card; 1: Write to card.
Don't care if no data is expected from card. (R/W)

SDHOST_DATA_EXPECTED 0: No data transfer expected; 1: Data transfer expected. (R/W)

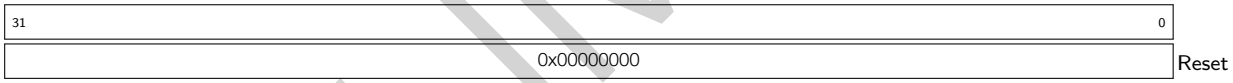
SDHOST_CHECK_RESPONSE_CRC 0: Do not check; 1: Check response CRC.
Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller. (R/W)

SDHOST_RESPONSE_LENGTH 0: Short response expected from card; 1: Long response expected from card. (R/W)

SDHOST_RESPONSE_EXPECT 0: No response expected from card; 1: Response expected from card. (R/W)

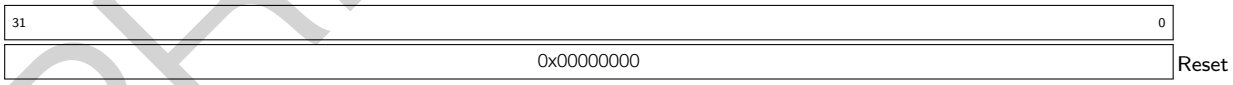
SDHOST_CMD_INDEX Command index. (R/W)

Register 30.12. SDHOST_RESP0_REG (0x0030)



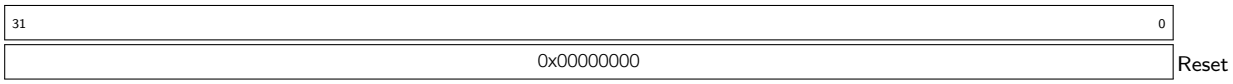
SDHOST_RESP0_REG Bit[31:0] of response. (RO)

Register 30.13. SDHOST_RESP1_REG (0x0034)



SDHOST_RESP1_REG Bit[63:32] of long response. (RO)

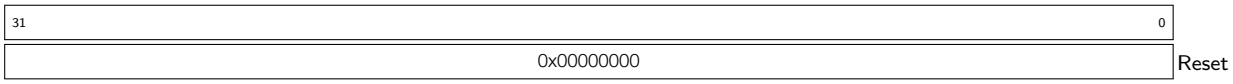
Register 30.14. SDHOST_RESP2_REG (0x0038)



SDHOST_RESP2_REG Bit[95:64] of long response. (RO)

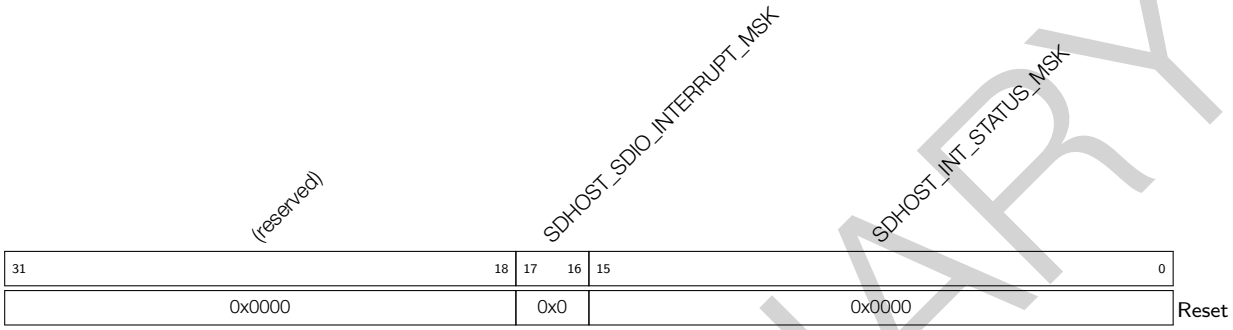
PRELIMINARY

Register 30.15. SDHOST_RESP3_REG (0x003C)



SDHOST_RESP3_REG Bit[127:96] of long response. (RO)

Register 30.16. SDHOST_MINTSTS_REG (0x0040)



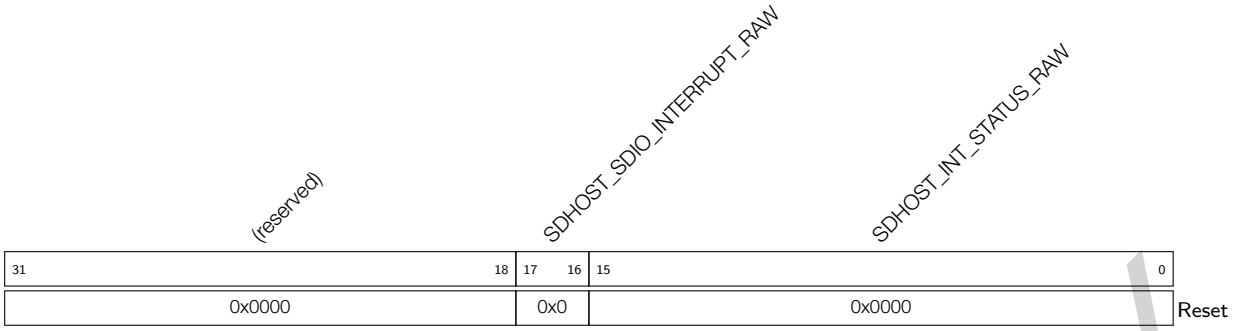
SDHOST_SDIO_INTERRUPT_MSK Interrupt from SDIO card, one bit for each card. Bit[17:16] correspond to card1 and card0, respectively. SDIO interrupt for card is enabled only if corresponding sdhost_sdio_int_mask bit is set in Interrupt mask register (Setting mask bit enables interrupt). (RO)

SDHOST_INT_STATUS_MSK Interrupt enabled only if corresponding bit in interrupt mask register is set. (RO)

Bit 15 (EBE): End-bit error/no CRC error;
Bit 14 (ACD): Auto command done;
Bit 13 (SBE/BCI): RX Start Bit Error;
Bit 12 (HLE): Hardware locked write error;
Bit 11 (FRUN): FIFO underrun/overrun error;
Bit 10 (HTO): Data starvation by host timeout (HTO);
Bit 9 (DTRO): Data read timeout;
Bit 8 (RTO): Response timeout;
Bit 7 (DCRC): Data CRC error;
Bit 6 (RCRC): Response CRC error;
Bit 5 (RXDR): Receive FIFO data request;
Bit 4 (TXDR): Transmit FIFO data request;
Bit 3 (DTO): Data transfer over;
Bit 2 (CD): Command done;
Bit 1 (RE): Response error;
Bit 0 (CD): Card detect.

PRELIMINARY

Register 30.17. SDHOST_RINTSTS_REG (0x0044)



SDHOST_SDIO_INTERRUPT_RAW Interrupt from SDIO card, one bit for each card. Bit[17:16] correspond to card1 and card0, respectively. Setting a bit clears the corresponding interrupt bit and writing 0 has no effect. (R/W)

0: No SDIO interrupt from card;

1: SDIO interrupt from card.

SDHOST_INT_STATUS_RAW Setting a bit clears the corresponding interrupt and writing 0 has no effect. Bits are logged regardless of interrupt mask status. (R/W)

Bit 15 (EBE): End-bit error/no CRC error;

Bit 14 (ACD): Auto command done;

Bit 13 (SBE/BCI): RX Start Bit Error;

Bit 12 (HLE): Hardware locked write error;

Bit 11 (FRUN): FIFO underrun/overrun error;

Bit 10 (HTO): Data starvation by host timeout (HTO);

Bit 9 (DTRO): Data read timeout;

Bit 8 (RTO): Response timeout;

Bit 7 (DCRC): Data CRC error;

Bit 6 (RCRC): Response CRC error;

Bit 5 (RXDR): Receive FIFO data request;

Bit 4 (TXDR): Transmit FIFO data request;

Bit 3 (DTO): Data transfer over;

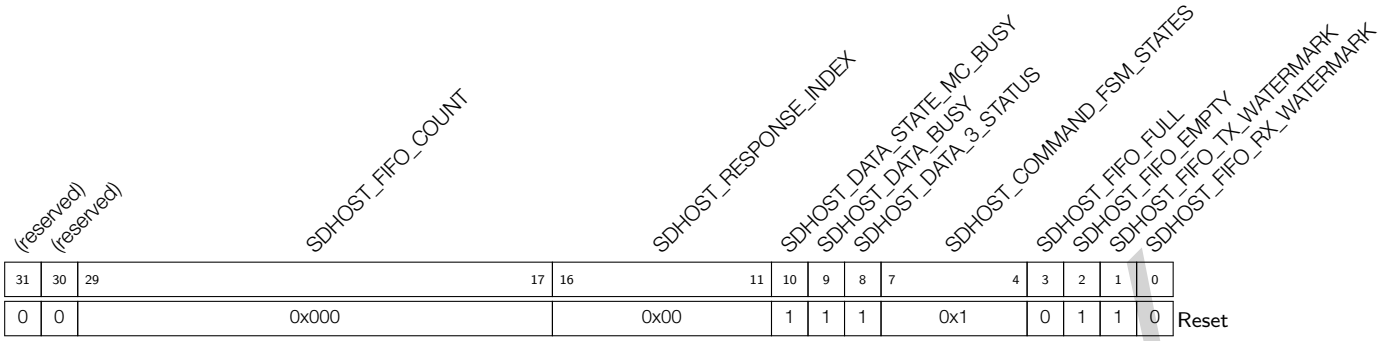
Bit 2 (CD): Command done;

Bit 1 (RE): Response error;

Bit 0 (CD): Card detect.

PRELIMINARY

Register 30.18. SDHOST_STATUS_REG (0x0048)



SDHOST_FIFO_COUNT FIFO count, number of filled locations in FIFO. (RO)

SDHOST_RESPONSE_INDEX Index of previous response, including any auto-stop sent by core. (RO)

SDHOST_DATA_STATE_MC_BUSY Data transmit or receive state-machine is busy. (RO)

SDHOST_DATA_BUSY Inverted version of raw selected sdhost_card_data[0].

0: Card data not busy;

1: Card data busy. (RO)

SDHOST_DATA_3_STATUS Raw selected sdhost_card_data[3], checks whether card is present.

0: card not present;

1: card present. (RO)

SDHOST_COMMAND_FSM_STATES Command FSM states. (RO)

0: Idle;

1: Send init sequence;

2: Send cmd start bit;

3: Send cmd tx bit;

4: Send cmd index + arg;

5: Send cmd crc7;

6: Send cmd end bit;

7: Receive resp start bit;

8: Receive resp IRQ response;

9: Receive resp tx bit;

10: Receive resp cmd idx;

11: Receive resp data;

12: Receive resp crc7;

13: Receive resp end bit;

14: Cmd path wait NCC;

15: Wait, cmd-to-response turnaround.

Continued on the next page...

PRELIMINARY

Register 30.18. SDHOST_STATUS_REG (0x0048)

Continued from the previous page ...

SDHOST_FIFO_FULL FIFO is full status. (RO)

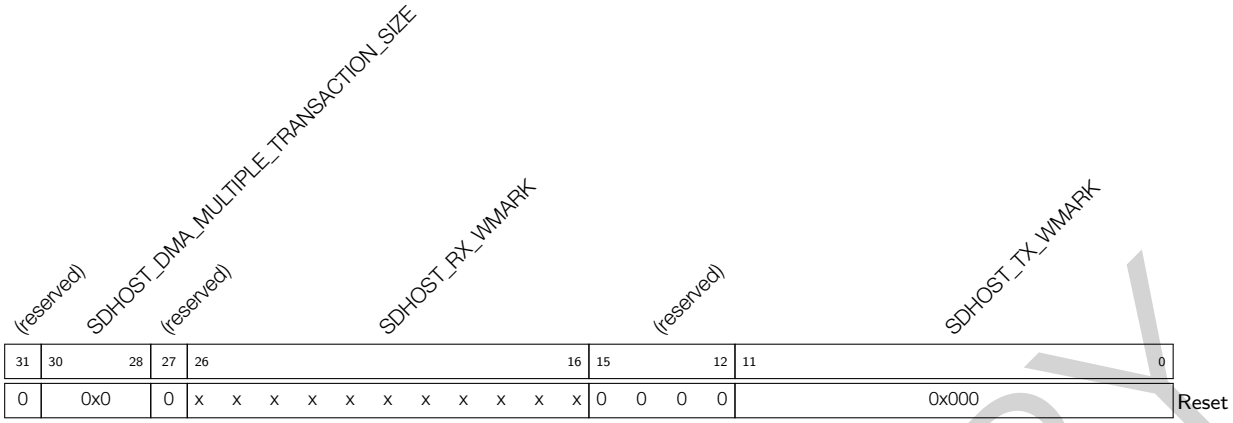
SDHOST_FIFO_EMPTY FIFO is empty status. (RO)

SDHOST_FIFO_TX_WATERMARK FIFO reached Transmit watermark level, not qualified with data transfer. (RO)

SDHOST_FIFO_RX_WATERMARK FIFO reached Receive watermark level, not qualified with data transfer. (RO)

PRELIMINARY

Register 30.19. SDHOST_FIFOTH_REG (0x004C)



SDHOST_DMA_MULTIPLE_TRANSACTION_SIZE Burst size of multiple transaction, should be programmed same as DMA controller multiple-transaction-size SDHOST_SRC/DEST_MSIZE. (R/W)

000: 1-byte transfer;

001: 4-byte transfer;

010: 8-byte transfer;

011: 16-byte transfer;

100: 32-byte transfer;

101: 64-byte transfer;

110: 128-byte transfer;

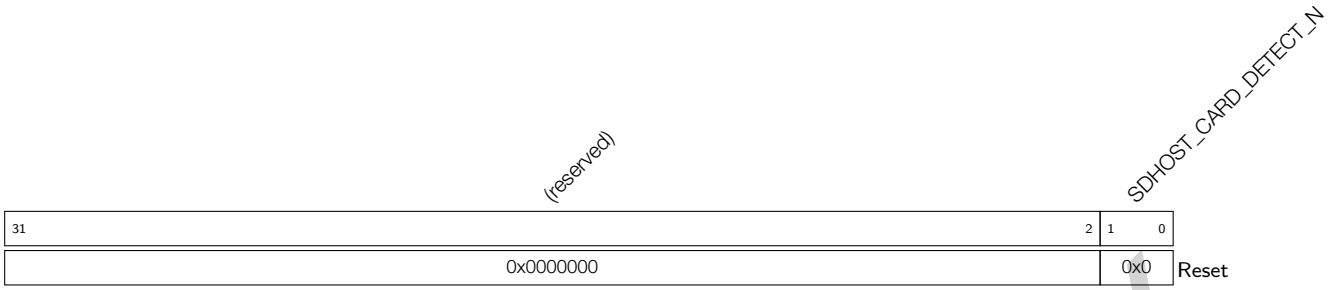
111: 256-byte transfer.

SDHOST_RX_WMARK FIFO threshold watermark level when receiving data to card.When FIFO data count reaches greater than this number , DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data.In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request.During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt.In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. (R/W)

SDHOST_TX_WMARK FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming.In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. (R/W)

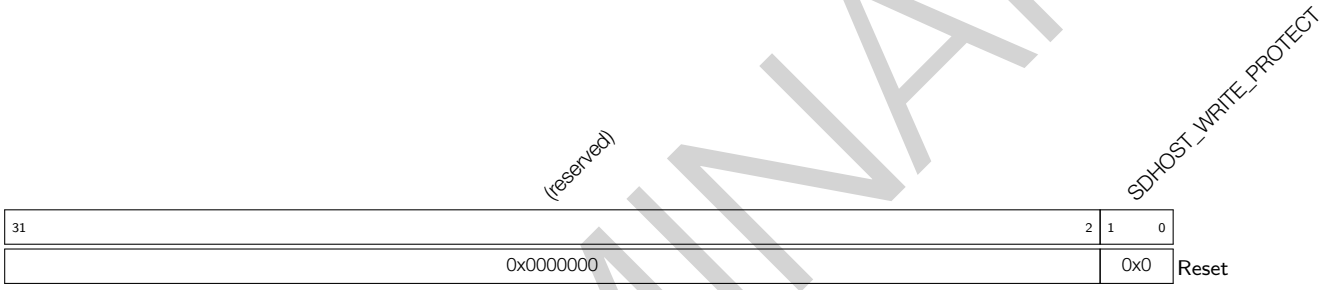
PRELIMINARY

Register 30.20. SDHOST_CDETECT_REG (0x0050)



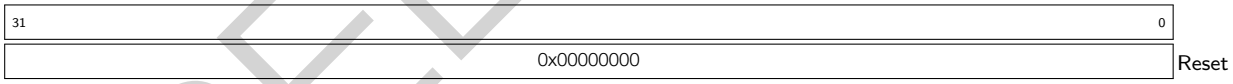
SDHOST_CARD_DETECT_N Value on sdhost_card_detect_n input ports (1 bit per card), read-only bits. 0 represents presence of card. Only NUM_CARDS number of bits are implemented. (RO)

Register 30.21. SDHOST_WRTPRT_REG (0x0054)



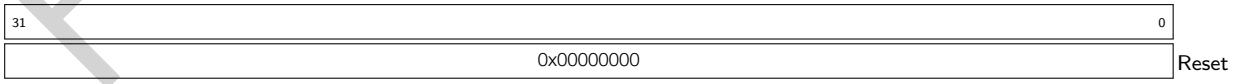
SDHOST_WRITE_PROTECT Value on sdhost_card_write_prt input ports (1 bit per card). 1 represents write protection. Only NUM_CARDS number of bits are implemented. (RO)

Register 30.22. SDHOST_TCBCNT_REG (0x005C)



SDHOST_TCBCNT_REG Number of bytes transferred by CIU unit to card. (RO)

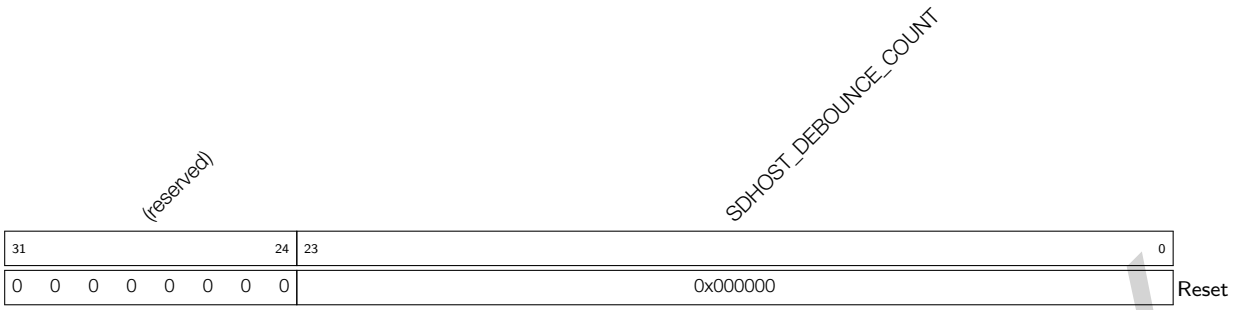
Register 30.23. SDHOST_TBBCNT_REG (0x0060)



SDHOST_TBBCNT_REG Number of bytes transferred between Host/DMA memory and BIU FIFO. (RO)

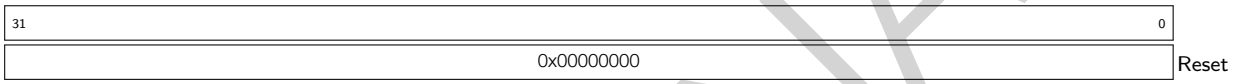
PRELIMINARY

Register 30.24. SDHOST_DEBNCE_REG (0x0064)



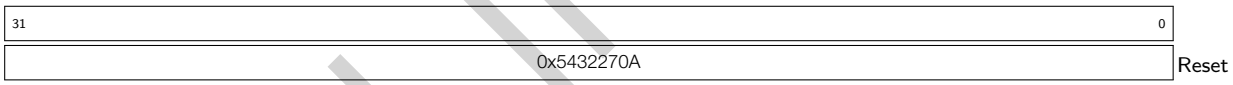
SDHOST_DEBOUNCE_COUNT Number of host clocks (clk) used by debounce filter logic. The typical debounce time is 5 ~ 25 ms to prevent the card instability when the card is inserted or removed. (R/W)

Register 30.25. SDHOST_USRID_REG (0x0068)



SDHOST_USRID_REG User identification register, value set by user. Can also be used as a scratch-pad register by user. (R/W)

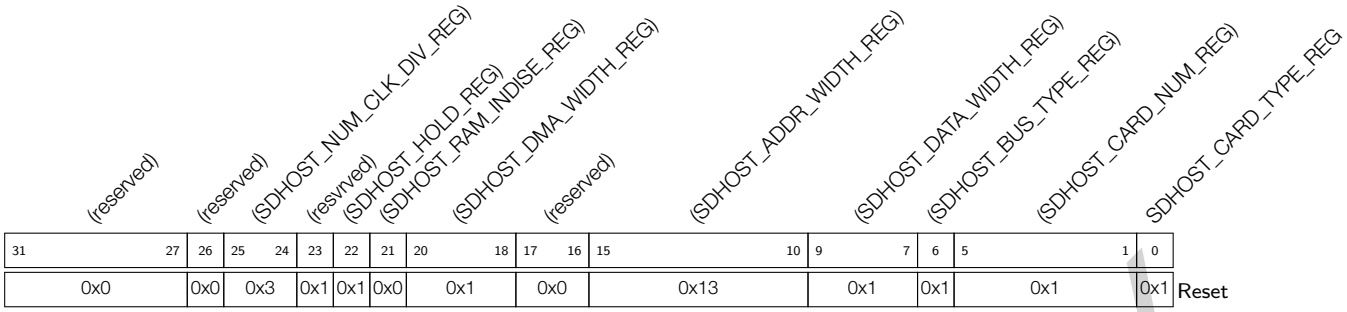
Register 30.26. SDHOST_VERID_REG (0x006C)



SDHOST_VERSIONID_REG Hardware version register. Can also be read by fireware. (RO)

PRELIMINARY

Register 30.27. SDHOST_HCON_REG (0x0070)



SDHOST_NUM_CLK_DIV_REG Have 4 clk divider in design . (RO)

SDHOST_HOLD_REG Have a hold regiser in data path . (RO)

SDHOST_RAM_INDISE_REG Inside RAM in SDMMC module. (RO)

SDHOST_DMA_WIDTH_REG DMA data witdth is 32. (RO)

SDHOST_ADDR_WIDTH_REG Register address width is 32. (RO)

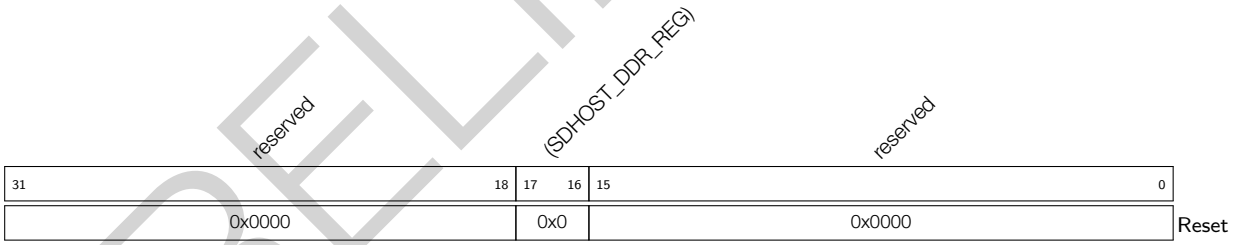
SDHOST_DATA_WIDTH_REG Regisger data widht is 32. (RO)

SDHOST_BUS_TYPE_REG Register config is APB bus. (RO)

SDHOST_CARD_NUM_REG Support card number is 2. (RO)

SDHOST_CARD_TYPE_REG Hardware support SDIO and MMC. (RO)

Register 30.28. SDHOST_UHS_REG (0x0074)



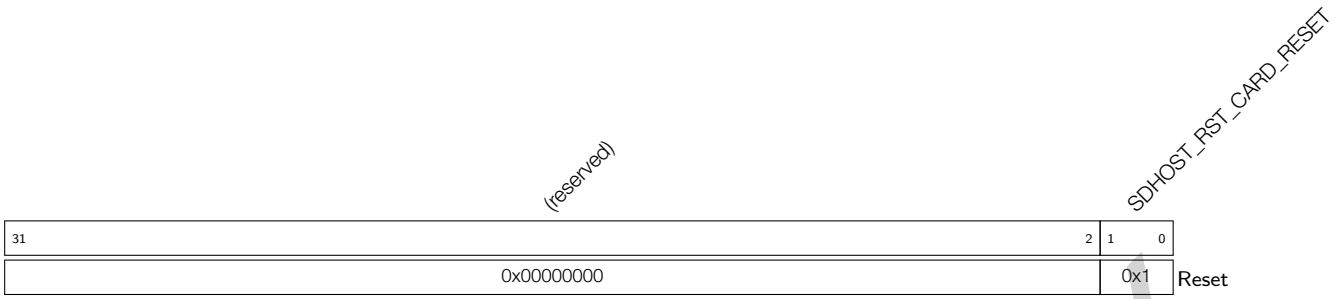
SDHOST_DDR_REG DDR mode selecton,1 bit for each card. (R/W)

0-Non-DDR mdoe.

1-DDR mdoe.

PRELIMINARY

Register 30.29. SDHOST_RST_N_REG (0x0078)



SDHOST_RST_CARD_RESET Hardware reset.

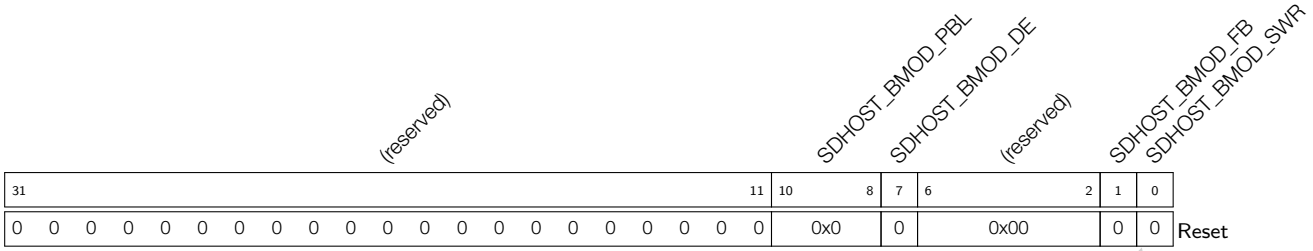
1: Active mode;

0: Reset.

These bits cause the cards to enter pre-idle state, which requires them to be re-initialized. SDHOST_RST_CARD_RESET[0] should be set to 1'b0 to reset card0, SDHOST_RST_CARD_RESET[1] should be set to 1'b0 to reset card1. (R/W)

PRELIMINARY

Register 30.30. SDHOST_BMOD_REG (0x0080)



SDHOST_BMOD_PBL Programmable Burst Length. These bits indicate the maximum number of beats to be performed in one IDMAC Internal DMA Control transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of FIFOTH register. In order to change this value, write the required value to FIFOTH register. This is an encode value as follows: (RO)

000: 1-byte transfer;

001: 4-byte transfer;

010: 8-byte transfer;

011: 16-byte transfer;

100: 32-byte transfer;

101: 64-byte transfer;

110: 128-byte transfer;

111: 256-byte transfer.

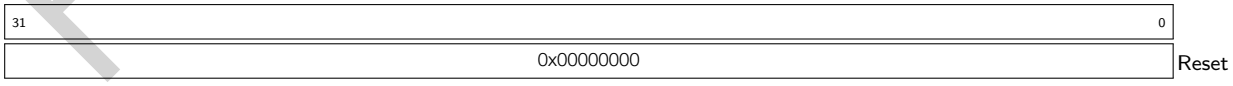
PBL is a read-only value and is applicable only for data access, it does not apply to descriptor access.

SDHOST_BMOD_DE IDMAC Enable. When set, the IDMAC is enabled. (RO)

SDHOST_BMOD_FB Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations. (R/W)

SDHOST_BMOD_SWR Software Reset. When set, the DMA Controller resets all its internal registers. It is automatically cleared after one clock cycle. (R/W)

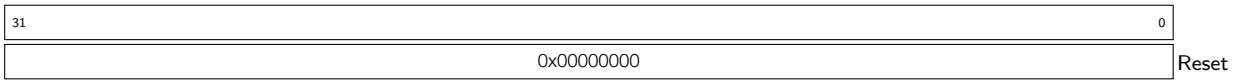
Register 30.31. SDHOST_PLDMND_REG (0x0080)



SDHOST_PLDMND_REG Poll Demand. If the OWNER bit of a descriptor is not set, the FSM goes to the Suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation. This is a write only . (WO)

PRELIMINARY

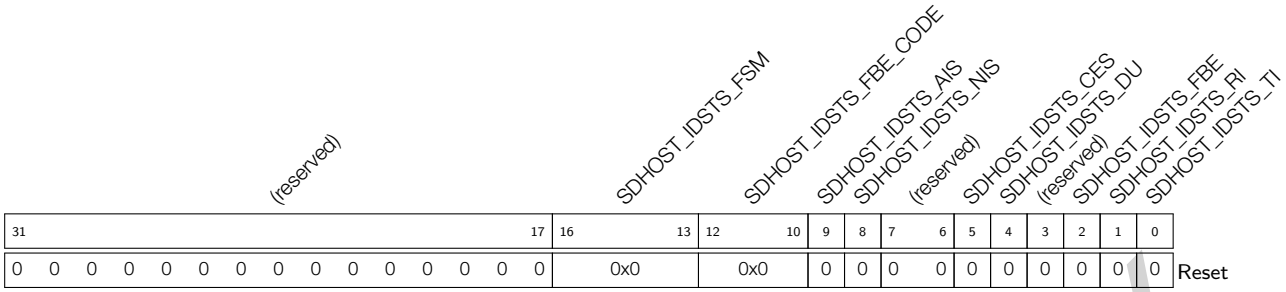
Register 30.32. SDHOST_DBADDR_REG (0x0088)



SDHOST_DBADDR_REG Start of Descriptor List. Contains the base address of the First Descriptor. The LSB bits [1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits may be treated as read-only. (R/W)

PRELIMINARY

Register 30.33. SDHOST_IDSTS_REG (0x008C)



SDHOST_IDSTS_FSM DMAC FSM present state. (RO)

0: DMA_IDLE (idle state);
1: DMA_SUSPEND (suspend state);
2: DESC_RD (descriptor reading state);
3: DESC_CHK (descriptor checking state);
4: DMA_RD_REQ_WAIT (read-data request waiting state);
5: DMA_WR_REQ_WAIT (write-data request waiting state);
6: DMA_RD (data-read state);
7: DMA_WR (data-write state);
8: DESC_CLOSE (descriptor close state).

SDHOST_IDSTS_FBE_CODE Fatal Bus Error Code. Indicates the type of error that caused a Bus Error. Valid only when the Fatal Bus Error bit IDSTS[2] is set. This field does not generate an interrupt. (RO)

001: Host Abort received during transmission;
010: Host Abort received during reception;
Others: Reserved.

SDHOST_IDSTS_AIS Abnormal Interrupt Summary. Logical OR of the following: IDSTS[2] : Fatal Bus Interrupt, IDSTS[4] : DU bit Interrupt. Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing 1 clears this bit. (R/W)

SDHOST_IDSTS_NIS Normal Interrupt Summary. Logical OR of the following: IDSTS[0] : Transmit Interrupt, IDSTS[1] : Receive Interrupt. Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing 1 clears this bit. (R/W)

Continued on the next page...

PRELIMINARY

Register 30.33. SDHOST_IDSTS_REG (0x008C)

Continued from the previous page...

SDHOST_IDSTS_CES Card Error Summary. Indicates the status of the transaction to/from the card, also present in RINTSTS. Indicates the logical OR of the following bits: (R/W)
EBE : End Bit Error;
RTO : Response Timeout/Boot Ack Timeout;
RCRC : Response CRC;
SBE : Start Bit Error;
DRTO : Data Read Timeout/BDS timeout;
DCRC : Data CRC for Receive;
RE : Response Error.
Writing 1 clears this bit. The abort condition of the IDMAC depends on the setting of this CES bit. If the CES bit is enabled, then the IDMAC aborts on a response error.

SDHOST_IDSTS_DU Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWNER bit = 0 (DES0[31] = 0). Writing 1 clears this bit. (R/W)

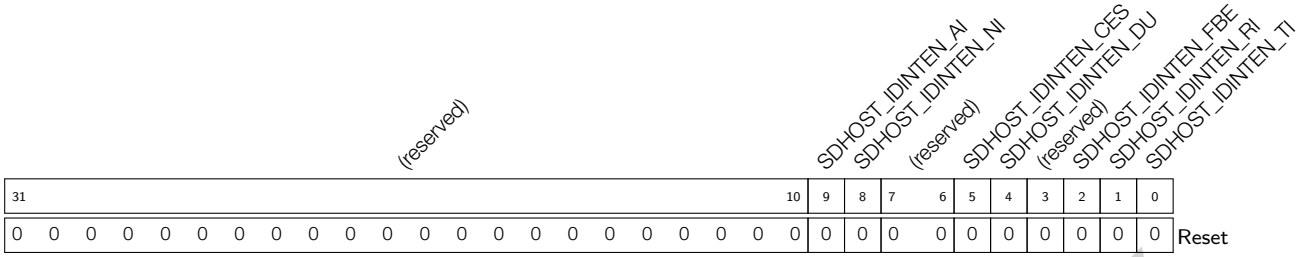
SDHOST_IDSTS_FBE Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (IDSTS[12:10]) . When this bit is set, the DMA disables all its bus accesses. Writing 1 clears this bit. (R/W)

SDHOST_IDSTS_RI Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing 1 clears this bit. (R/W)

SDHOST_IDSTS_TI Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing 1 clears this bit. (R/W)

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Register 30.34. SDHOST_IDINTEN_REG (0x0090)



SDHOST_IDINTEN_AI Abnormal Interrupt Summary Enable. When set, an abnormal interrupt is enabled. This bit enables the following bits:
IDINTEN[2]: Fatal Bus Error Interrupt; (R/W)
IDINTEN[4]: DU Interrupt.

SDHOST_IDINTEN_NI Normal Interrupt Summary Enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: (R/W)
IDINTEN[0]: Transmit Interrupt;
IDINTEN[1]: Receive Interrupt.

SDHOST_IDINTEN_CES Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary. (R/W)

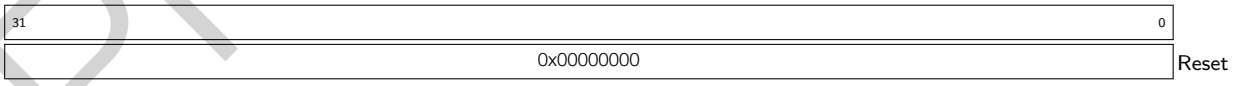
SDHOST_IDINTEN_DU Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the DU interrupt is enabled. (R/W)

SDHOST_IDINTEN_FBE Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled. (R/W)

SDHOST_IDINTEN_RI Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled. (R/W)

SDHOST_IDINTEN_TI Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled. (R/W)

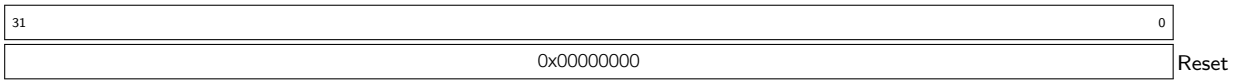
Register 30.35. SDHOST_DSCADDR_REG (0x0094)



SDHOST_DSCADDR_REG Host Descriptor Address Pointer, updated by IDMAC during operation and cleared on reset. This register points to the start address of the current descriptor read by the IDMAC. (RO)

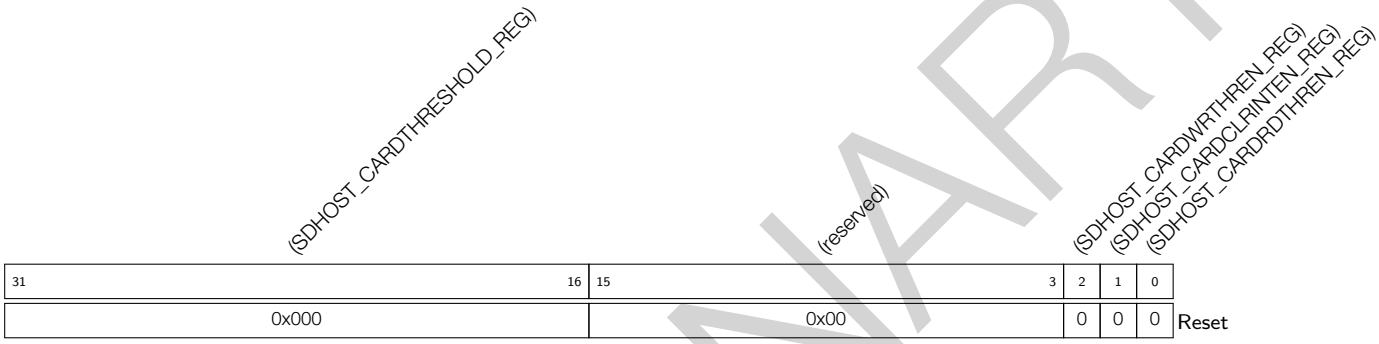
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Register 30.36. SDHOST_BUFADDR_REG (0x0098)



SDHOST_BUFADDR_REG Host Buffer Address Pointer, updated by IDMAC during operation and cleared on reset. This register points to the current Data Buffer Address being accessed by the IDMAC. (RO)

Register 30.37. SDHOST_CARDTHRCTL_REG (0x0100)



SDHOST_CARDTHRESHOLD_REG The inside FIFO size is 512,This register is applicable when SDHOST_CARDERTHREN_REG is set to 1 or SDHOST_CARDRDTHREN_REG set to 1. (R/W)

SDHOST_CARDWRTHREN_REG Applicable when HS400 mode is enabled. (R/W)

1'b0-Card write Threshold disabled.

1'b1-Card write Threshold enabled.

SDHOST_CARDCLRINTEN_REG Busy clear interrupt generation: (R/W)

1'b0-Busy clear interrypt disabled.

1'b1-Busy clear interrypt enabled.

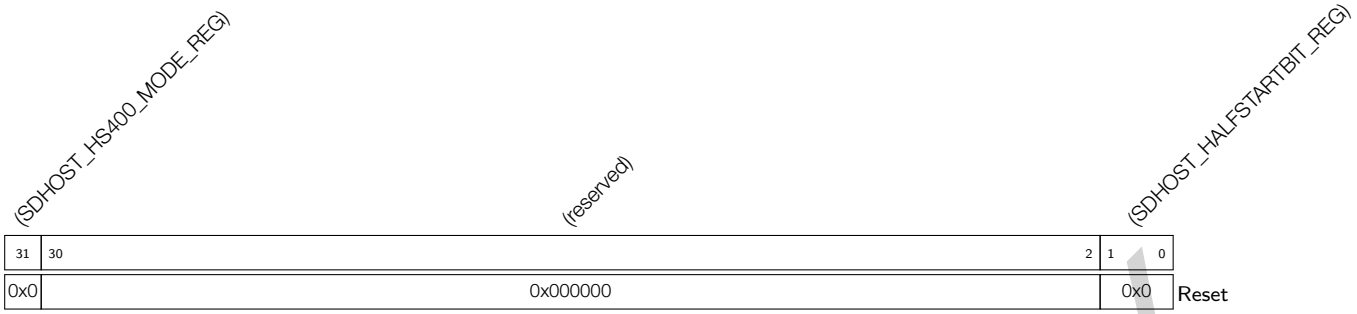
SDHOST_CARDRDTHREN_REG Card read threshold enable. (R/W)

1'b0-Card read threshold disabled.

1'b1-Card read threshold enabled.

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Register 30.38. SDHOST_EMMC_DDR_REG (0x010C)



SDHOST_HS400_MODE_REG Set 1 to enable HS400 mode. (R/W)

SDHOST_HALFSTARTBIT_REG Control for start bit detection mechanism duration of start bit.Each bit refers to one slot.Set this bit to 1 for eMMC4.5 and above,set to 0 for SD applications.For eMMC4.5,start bit can be: (R/W)

1'b0-Full cycle.

1'b1-less than one full cycle.

Register 30.39. SDHOST_ENSHIFT_REG (0x0110)



DHOST_ENABLE_SHIFT_REG Control for the amount of phase shift provided on the default enables in the design.Two bits assigned for each card. (R/W)

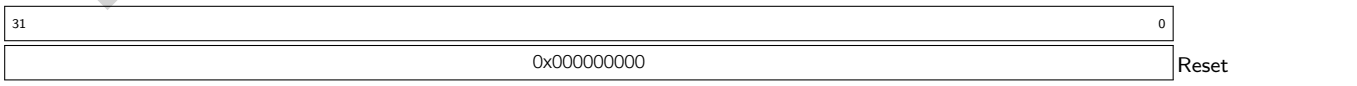
2'b00-Default phase shift.

2'b01-Enables shifted to next immediate positive edge.

2'b10-Enables shifted to next immediate negative edge.

2'b11-Reserved.

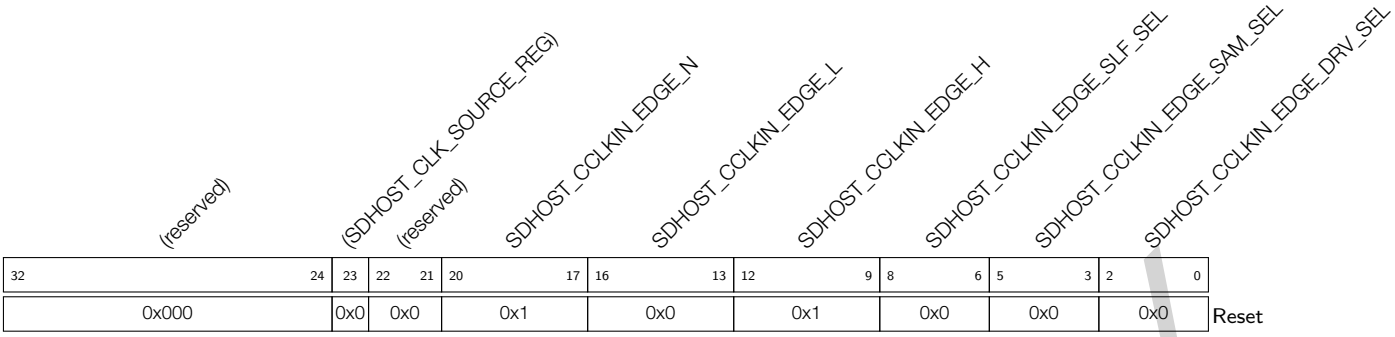
Register 30.40. SDHOST_BUFFIFO_REG (0x0200)



SDHOST_BUFFIFO_REG CPU write and read transmit data by FIFO. This register points to the current Data FIFO . (RO)

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Register 30.41. SDHOST_CLK_DIV_EDGE_REG (0x0800)



SDHOST_CLK_SOURCE_REG Set to 1 to use 160M PLL clock ,Set to 0 to use 40M XLTAL clock. (R/W)

CCLKIN_EDGE_N This value should be equal to CCLKIN_EDGE_L. (R/W)

CCLKIN_EDGE_L The low level of the divider clock. The value should be larger than CCLKIN_EDGE_H. (R/W)

CCLKIN_EDGE_H The high level of the divider clock. The value should be smaller than CCLKIN_EDGE_L. (R/W)

CCLKIN_EDGE_SLF_SEL It is used to select the clock phase of the internal signal from phase90, phase180, or phase270. (R/W)

CCLKIN_EDGE_SAM_SEL It is used to select the clock phase of the input signal from phase90, phase180, or phase270. (R/W)

CCLKIN_EDGE_DRV_SEL It is used to select the clock phase of the output signal from phase90, phase180, or phase270. (R/W)

Note: SD/MMC use this register to divide the 160M clock(CCLKIN_EDGE_H/CCLKIN_EDGE_L). The output clock connect to sdio slave divider by this register and SDHOST_CLKDIV_REG,there are 4 clock source to seleced by SDHOST_CLKSRC_REG register.

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31 LED PWM Controller (LEDC)

31.1 Overview

The LED PWM Controller is a peripheral designed to generate PWM signals for LED control. It has specialized features such as automatic duty cycle fading. However, the LED PWM Controller can also be used to generate PWM signals for other purposes.

31.2 Features

The LED PWM Controller has the following features:

- Eight independent PWM generators (i.e. eight channels)
- Four independent timers that support division by fractions
- Automatic duty cycle fading (i.e. gradual increase/decrease of a PWM's duty cycle without interference from the processors) with interrupt generation on fade completion
- Adjustable phase of PWM signal output
- PWM signal output in low-power mode (Light-sleep mode)
- Maximum PWM resolution: 14 bits

Note that the four timers are identical regarding their features and operation. The following sections refer to the timers collectively as Timer*x* (where *x* ranges from 0 to 3). Likewise, the eight PWM generators are also identical in features and operation, and thus are collectively referred to as PWM*n* (where *n* ranges from 0 to 7).

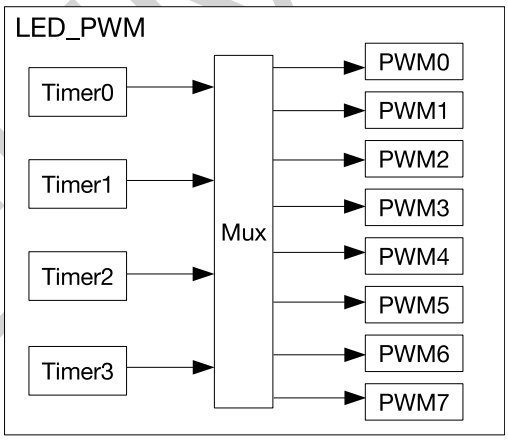


Figure 31-1. LED PWM Architecture

31.3 Functional Description

31.3.1 Architecture

Figure 31-1 shows the architecture of the LED PWM Controller.

The four timers can be independently configured (i.e. clock divider, and counter overflow value) and each internally maintains a timebase counter (i.e. a counter that counts on cycles of a reference clock). Each PWM

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generator will select one of the timers and uses the timer's counter value as a reference to generate its PWM signal.

Figure 31-2 illustrates the main functional blocks of the timer and the PWM generator.

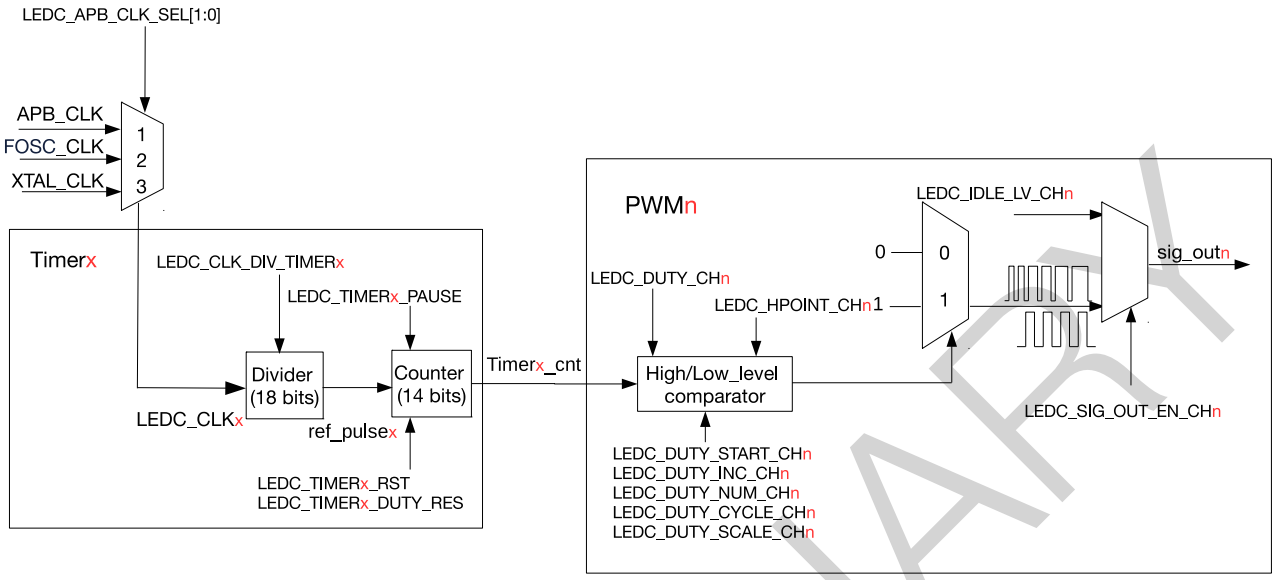


Figure 31-2. LED PWM Generator Diagram

31.3.2 Timers

Each timer in LED PWM Controller internally maintains a timebase counter. Referring to Figure 31-2, this clock signal used by the timebase counter is named ref_pulse*x*. All timers use the same clock source LEDC_CLK*x*, which is then passed through a clock divider to generate ref_pulse*x* for the counter.

31.3.2.1 Clock Source

Software configuring registers for LED PWM is clocked by APB_CLK. For more information about APB_CLK, see Chapter 6 *Reset and Clock*. To use the LED PWM pheripheral, the APB_CLK signal to the LED PWM has to be enabled. The APB_CLK signal to LED PWM can be enabled by setting the SYSTEM_LEDC_CLK_EN field in the register SYSTEM_PERIP_CLK_EN0_REG and be reset via software by setting the SYSTEM_LEDC_RST field in the register SYSTEM_PERIP_RST_EN0_REG. For more information, please refer to Table 15-1 in Chapter 15 *System Registers*.

Timers in the LED PWM Controller choose their common clock source from one of the following clock signals: APB_CLK, FOSC_CLK and XTAL_CLK (see Chapter 6 *Reset and Clock* for more details about each clock signal). The procedure for selecting a clock source signal for LEDC_CLK*x* is described below:

- APB_CLK: Set LEDC_APB_CLK_SEL[1:0] to 1
- FOSC_CLK: Set LEDC_APB_CLK_SEL[1:0] to 2
- XTAL_CLK: Set LEDC_APB_CLK_SEL[1:0] to 3

The LEDC_CLK*x* signal will then be passed through the clock divider.

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31.3.2.2 Clock Divider Configuration

The LEDC_CLK*x* signal is passed through a clock divider to generate the ref_pulse*x* signal for the counter. The frequency of ref_pulse*x* is equal to the frequency of LEDC_CLK*x* divided by the LEDC_CLK_DIV_TIMER*x* divider value (see Figure 31-2).

The LEDC_CLK_DIV_TIMER*x* divider value is a fractional clock divider. Thus, it supports non-integer divider values. LEDC_CLK_DIV_TIMER*x* is configured according to the following equation.

$$LEDC\_CLK\_DIV\_TIMERx = A + \frac{B}{256}$$

- *A* corresponds to the most significant 10 bits of LEDC_CLK_DIV_TIMER*x* (i.e. LEDC_TIMER*x*_CONF_REG[21:12])
- The fractional part *B* corresponds to the least significant 8 bits of LEDC_CLK_DIV_TIMER*x* (i.e. LEDC_TIMER*x*_CONF_REG[11:4])

When the fractional part *B* is zero, LEDC_CLK_DIV_TIMER*x* is equivalent to an integer divider value (i.e. an integer prescaler). In other words, a ref_pulse*x* clock pulse is generated after every *A* number of LEDC_CLK*x* clock pulses.

However, when *B* is nonzero, LEDC_CLK_DIV_TIMER*x* becomes a non-integer divider value. The clock divider implements non-integer frequency division by alternating between *A* and (*A*+1) LEDC_CLK*x* clock pulses per ref_pulse*x* clock pulse. This will result in the average frequency of ref_pulse*x* clock pulse being the desired frequency (i.e. the non-integer divided frequency). For every 256 ref_pulse*x* clock pulses:

- A number of *B* ref_pulse*x* clock pulses will consist of (*A*+1) LEDC_CLK*x* clock pulses
- A number of (256-*B*) ref_pulse*x* clock pulses will consist of *A* LEDC_CLK*x* clock pulses
- The ref_pulse*x* clock pulses consisting of (*A*+1) pulses are evenly distributed amongst those consisting of *A* pulses

Figure 31-3 illustrates the relation between LEDC_CLK*x* clock pulses and ref_pulse*x* clock pulses when dividing by a non-integer LEDC_CLK_DIV_TIMER*x*.

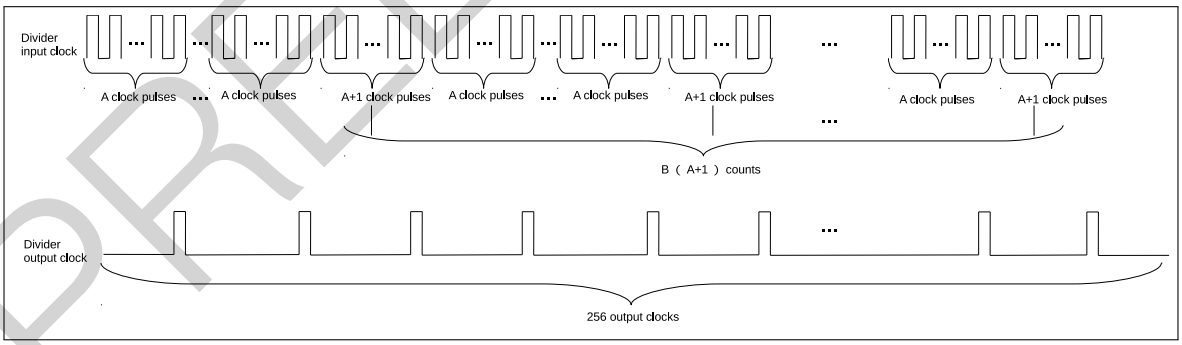


Figure 31-3. Frequency Division When LEDC_CLK_DIV_TIMER*x* is a Non-Integer Value

To change the timer's clock divider value at runtime, first set the LEDC_CLK_DIV_TIMER*x* field, and then set the LEDC_TIMER*x*_PARA_UP field to apply the new configuration. This will cause the newly configured values to take effect upon the next overflow of the counter. LEDC_TIMER*x*_PARA_UP field will be automatically cleared by hardware.

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31.3.2.3 14-bit Counter

Each timer contains a 14-bit timebase counter that uses ref_pulse*x* as its reference clock (see Figure 31-2). The LEDC_TIMER*x*_DUTY_RES field configures the overflow value of this 14-bit counter. Hence, the maximum resolution of the PWM signal is 14 bits. The counter counts up to $2^{LEDC\_TIMERx\_DUTY\_RES} - 1$, overflows and begins counting from 0 again. The counter's value can be read, reset, and suspended by software.

The counter can trigger LEDC_TIMER*x*_OVF_INT interrupt (generated automatically by hardware without configuration) every time the counter overflows. It can also be configured to trigger LEDC_OVF_CNT_CH*n*_INT interrupt after the counter overflows $LEDC\_OVF\_NUM\_CHn + 1$ times. To configure LEDC_OVF_CNT_CH*n*_INT interrupt, please:

1. Configure LEDC_TIMER_SEL_CH*n* as the counter for the PWM generator
2. Enable the counter by setting LEDC_OVF_CNT_EN_CH*n*
3. Set LEDC_OVF_NUM_CH*n* to the number of counter overflows to generate an interrupt, minus 1
4. Enable the overflow interrupt by setting LEDC_OVF_CNT_CH*n*_INT_ENA
5. Set LEDC_TIMER*x*_DUTY_RES to enable the timer and wait for a LEDC_OVF_CNT_CH*n*_INT interrupt

Referring to Figure 31-2, the frequency of a PWM generator output signal (sig_out*n*) is dependent on the frequency of the timer's clock source (LEDC_CLK*x*), the clock divider value (LEDC_CLK_DIV_TIMER*x*), and the range of the counter (LEDC_TIMER*x*_DUTY_RES):

$$f_{\text{PWM}} = \frac{f_{\text{LEDC\_CLK}x}}{\text{LEDC\_CLK\_DIV\_TIMER}x \cdot 2^{\text{LEDC\_TIMER}x\text{\_DUTY\_RES}}}$$

To change the overflow value at runtime, first set the LEDC_TIMER*x*_DUTY_RES field, and then set the LEDC_TIMER*x*_PARA_UP field. This will cause the newly configured values to take effect upon the next overflow of the counter. If LEDC_OVF_CNT_EN_CH*n* field is reconfigured, LEDC_PARA_UP_CH*n* should be set to apply the new configuration. In summary, these configuration values need to be updated by setting LEDC_TIMER*x*_PARA_UP or LEDC_PARA_UP_CH*n*. LEDC_TIMER*x*_PARA_UP and LEDC_PARA_UP_CH*n* will be automatically cleared by hardware.

31.3.3 PWM Generators

To generate a PWM signal, a PWM generator (PWM*n*) selects a timer (Timer*x*). Each PWM generator can be configured separately by setting LEDC_TIMER_SEL_CH*n* to use one of four timers to generate the PWM output.

As shown in Figure 31-2, each PWM generator has a comparator and two multiplexers. A PWM generator compares the timer's 14-bit counter value (Timer*x*_cnt) to two trigger values Hpoint*n* and Lpoint*n*. When the timer's counter value is equal to Hpoint*n* or Lpoint*n*, the PWM signal is high or low, respectively, as described below:

- If Timer*x*_cnt == Hpoint*n*, sig_out*n* is 1.
- If Timer*x*_cnt == Lpoint*n*, sig_out*n* is 0.

Figure 31-4 illustrates how Hpoint*n* or Lpoint*n* are used to generate a fixed duty cycle PWM output signal.

For a particular PWM generator (PWM*n*), its Hpoint*n* is sampled from the LEDC_HPOINT_CH*n* field each time the selected timer's counter overflows. Likewise, Lpoint*n* is also sampled on every counter overflow and is calculated

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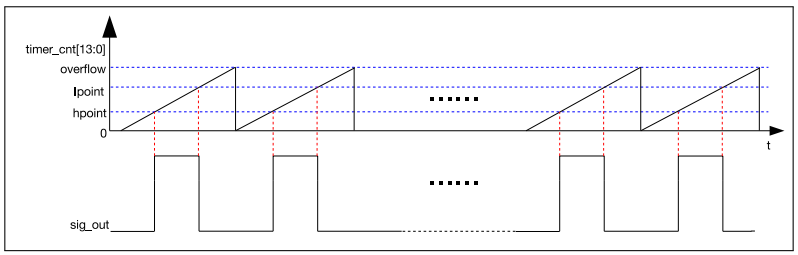


Figure 31-4. LED_PWM Output Signal Diagram

from the sum of the LEDC_DUTY_CH*n*[18:4] and LEDC_HPOINT_CH*n* fields. By setting Hpoint*n* and Lpoint*n* via the LEDC_HPOINT_CH*n* and LEDC_DUTY_CH*n*[18:4] fields, the relative phase and duty cycle of the PWM output can be set.

The PWM output signal (sig_out*n*) is enabled by setting LEDC_SIG_OUT_EN_CH*n*. When LEDC_SIG_OUT_EN_CH*n* is cleared, PWM signal output is disabled, and the output signal (sig_out*n*) will output a constant level as specified by LEDC_IDLE_LV_CH*n*.

The bits LEDC_DUTY_CH*n*[3:0] are used to dither the duty cycles of the PWM output signal (sig_out*n*) by periodically altering the duty cycle of sig_out*n*. When LEDC_DUTY_CH*n*[3:0] is set to a non-zero value, then for every 16 cycles of sig_out*n*, LEDC_DUTY_CH*n*[3:0] of those cycles will have PWM pulses that are one timer tick longer than the other (16- LEDC_DUTY_CH*n*[3:0]) cycles. For instance, if LEDC_DUTY_CH*n*[18:4] is set to 10 and LEDC_DUTY_CH*n*[3:0] is set to 5, then 5 of 16 cycles will have a PWM pulse with a duty value of 11 and the rest of the 16 cycles will have a PWM pulse with a duty value of 10. The average duty cycle after 16 cycles is 10.3125.

If fields LEDC_TIMER_SEL_CH*n*, LEDC_HPOINT_CH*n*, LEDC_DUTY_CH*n*[18:4] and LEDC_SIG_OUT_EN_CH*n* are reconfigured, LEDC_PARA_UP_CH*n* must be set to apply the new configuration. This will cause the newly configured values to take effect upon the next overflow of the counter. LEDC_PARA_UP_CH*n* field will be automatically cleared by hardware.

31.3.4 Duty Cycle Fading

The PWM generators can fade the duty cycle of a PWM output signal (i.e. gradually change the duty cycle from one value to another). If Duty Cycle Fading is enabled, the value of Lpoint*n* will be incremented/decremented after a fixed number of counter overflows occurs. Figure 31-5 illustrates Duty Cycle Fading.

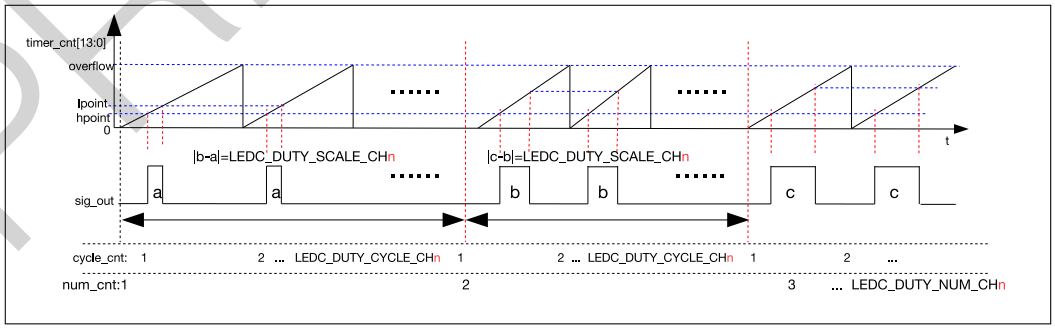


Figure 31-5. Output Signal Diagram of Fading Duty Cycle

Duty Cycle Fading is configured using the following register fields:

- LEDC_DUTY_CH*n* is used to set the initial value of Lpoint*n*.

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- LEDC_DUTY_START_CH*n* will enable/disable duty cycle fading when set/cleared.
- LEDC_DUTY_CYCLE_CH*n* sets the number of counter overflow cycles for every Lpoint*n* increment/decrement. In other words, Lpoint*n* will be incremented/decremented after LEDC_DUTY_CYCLE_CH*n* counter overflows.
- LEDC_DUTY_INC_CH*n* configures whether Lpoint*n* is incremented/decremented if set/cleared.
- LEDC_DUTY_SCALE_CH*n* sets the amount that Lpoint*n* is incremented/decremented.
- LEDC_DUTY_NUM_CH*n* sets the maximum number of increments/decrements before duty cycle fading stops.

If the fields LEDC_DUTY_CH*n*, LEDC_DUTY_START_CH*n*, LEDC_DUTY_CYCLE_CH*n*, LEDC_DUTY_INC_CH*n*, LEDC_DUTY_SCALE_CH*n*, and LEDC_DUTY_NUM_CH*n* are reconfigured, LEDC_PARA_UP_CH*n* must be set to apply the new configuration. After this field is set, the values for duty cycle fading will take effect at once. LEDC_PARA_UP_CH*n* field will be automatically cleared by hardware.

31.3.5 Interrupts

- LEDC_OVF_CNT_CH*n*_INT: Triggered when the timer counter overflows for (LEDC_OVF_NUM_CH*n* + 1) times and the register LEDC_OVF_CNT_EN_CH*n* is set to 1.
- LEDC_DUTY_CHNG_END_CH*n*_INT: Triggered when a fade on an LED PWM generator has finished.
- LEDC_TIMER*x*_OVF_INT: Triggered when an LED PWM timer has reached its maximum counter value.

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31.4 Register Summary

The addresses in this section are relative to LED PWM Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
Configuration Register			
LEDC_CH0_CONF0_REG	Configuration register 0 for channel 0	0x0000	varies
LEDC_CH0_CONF1_REG	Configuration register 1 for channel 0	0x000C	R/W
LEDC_CH1_CONF0_REG	Configuration register 0 for channel 1	0x0014	varies
LEDC_CH1_CONF1_REG	Configuration register 1 for channel 1	0x0020	R/W
LEDC_CH2_CONF0_REG	Configuration register 0 for channel 2	0x0028	varies
LEDC_CH2_CONF1_REG	Configuration register 1 for channel 2	0x0034	R/W
LEDC_CH3_CONF0_REG	Configuration register 0 for channel 3	0x003C	varies
LEDC_CH3_CONF1_REG	Configuration register 1 for channel 3	0x0048	R/W
LEDC_CH4_CONF0_REG	Configuration register 0 for channel 4	0x0050	varies
LEDC_CH4_CONF1_REG	Configuration register 1 for channel 4	0x005C	R/W
LEDC_CH5_CONF0_REG	Configuration register 0 for channel 5	0x0064	varies
LEDC_CH5_CONF1_REG	Configuration register 1 for channel 5	0x0070	R/W
LEDC_CH6_CONF0_REG	Configuration register 0 for channel 6	0x0078	varies
LEDC_CH6_CONF1_REG	Configuration register 1 for channel 6	0x0084	R/W
LEDC_CH7_CONF0_REG	Configuration register 0 for channel 7	0x008C	varies
LEDC_CH7_CONF1_REG	Configuration register 1 for channel 7	0x0098	R/W
LEDC_CONF_REG	Global ledc configuration register	0x00D0	R/W
Hpoint Register			
LEDC_CH0_HPOINT_REG	High point register for channel 0	0x0004	R/W
LEDC_CH1_HPOINT_REG	High point register for channel 1	0x0018	R/W
LEDC_CH2_HPOINT_REG	High point register for channel 2	0x002C	R/W
LEDC_CH3_HPOINT_REG	High point register for channel 3	0x0040	R/W
LEDC_CH4_HPOINT_REG	High point register for channel 4	0x0054	R/W
LEDC_CH5_HPOINT_REG	High point register for channel 5	0x0068	R/W
LEDC_CH6_HPOINT_REG	High point register for channel 6	0x007C	R/W
LEDC_CH7_HPOINT_REG	High point register for channel 7	0x0090	R/W
Duty Cycle Register			
LEDC_CH0_DUTY_REG	Initial duty cycle for channel 0	0x0008	R/W
LEDC_CH0_DUTY_R_REG	Current duty cycle for channel 0	0x0010	RO
LEDC_CH1_DUTY_REG	Initial duty cycle for channel 1	0x001C	R/W
LEDC_CH1_DUTY_R_REG	Current duty cycle for channel 1	0x0024	RO
LEDC_CH2_DUTY_REG	Initial duty cycle for channel 2	0x0030	R/W
LEDC_CH2_DUTY_R_REG	Current duty cycle for channel 2	0x0038	RO
LEDC_CH3_DUTY_REG	Initial duty cycle for channel 3	0x0044	R/W
LEDC_CH3_DUTY_R_REG	Current duty cycle for channel 3	0x004C	RO
LEDC_CH4_DUTY_REG	Initial duty cycle for channel 4	0x0058	R/W
LEDC_CH4_DUTY_R_REG	Current duty cycle for channel 4	0x0060	RO
LEDC_CH5_DUTY_REG	Initial duty cycle for channel 5	0x006C	R/W

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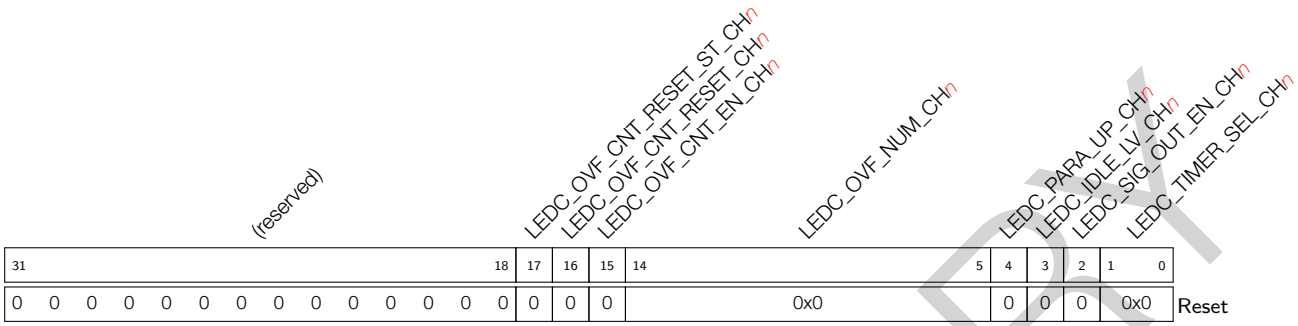
Name	Description	Address	Access
LEDC_CH5_DUTY_R_REG	Current duty cycle for channel 5	0x0074	RO
LEDC_CH6_DUTY_REG	Initial duty cycle for channel 6	0x0080	R/W
LEDC_CH6_DUTY_R_REG	Current duty cycle for channel 6	0x0088	RO
LEDC_CH7_DUTY_REG	Initial duty cycle for channel 7	0x0094	R/W
LEDC_CH7_DUTY_R_REG	Current duty cycle for channel 7	0x009C	RO
Timer Register			
LEDC_TIMER0_CONF_REG	Timer 0 configuration	0x00A0	varies
LEDC_TIMER0_VALUE_REG	Timer 0 current counter value	0x00A4	RO
LEDC_TIMER1_CONF_REG	Timer 1 configuration	0x00A8	varies
LEDC_TIMER1_VALUE_REG	Timer 1 current counter value	0x00AC	RO
LEDC_TIMER2_CONF_REG	Timer 2 configuration	0x00B0	varies
LEDC_TIMER2_VALUE_REG	Timer 2 current counter value	0x00B4	RO
LEDC_TIMER3_CONF_REG	Timer 3 configuration	0x00B8	varies
LEDC_TIMER3_VALUE_REG	Timer 3 current counter value	0x00BC	RO
Interrupt Register			
LEDC_INT_RAW_REG	Raw interrupt status	0x00C0	RO
LEDC_INT_ST_REG	Masked interrupt status	0x00C4	RO
LEDC_INT_ENA_REG	Interrupt enable bits	0x00C8	R/W
LEDC_INT_CLR_REG	Interrupt clear bits	0x00CC	WO
Version Register			
LEDC_DATE_REG	Version control register	0x00FC	R/W

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31.5 Registers

The addresses in this section are relative to LED PWM Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 31.1. LEDC_CH*n*_CONF0_REG (*n*: 0-7) (0x0000+0x14n*)**



LEDC_TIMER_SEL_CH*n* This field is used to select one of timers for channel *n*.

0: select timer0

1: select timer1

2: select timer2

3: select timer3 (R/W)

LEDC_SIG_OUT_EN_CH*n* Set this bit to enable signal output on channel *n*. (R/W)

LEDC_IDLE_LV_CH*n* This bit is used to control the output value when channel *n* is inactive (when LEDC_SIG_OUT_EN_CH*n* is 0). (R/W)

LEDC_PARA_UP_CH*n* This bit is used to update the listed fields below for channel *n*, and will be automatically cleared by hardware. (WO)

- LEDC_HPOINT_CH*n*
- LEDC_DUTY_START_CH*n*
- LEDC_SIG_OUT_EN_CH*n*
- LEDC_TIMER_SEL_CH*n*
- LEDC_DUTY_NUM_CH*n*
- LEDC_DUTY_CYCLE_CH*n*
- LEDC_DUTY_SCALE_CH*n*
- LEDC_DUTY_INC_CH*n*
- LEDC_OVF_CNT_EN_CH*n*

Continued on the next page...

PRELIMINARY

Register 31.1. LEDC_CH*n*_CONF0_REG (*n*: 0-7) (0x0000+0x14n*)**

Continued from the previous page...

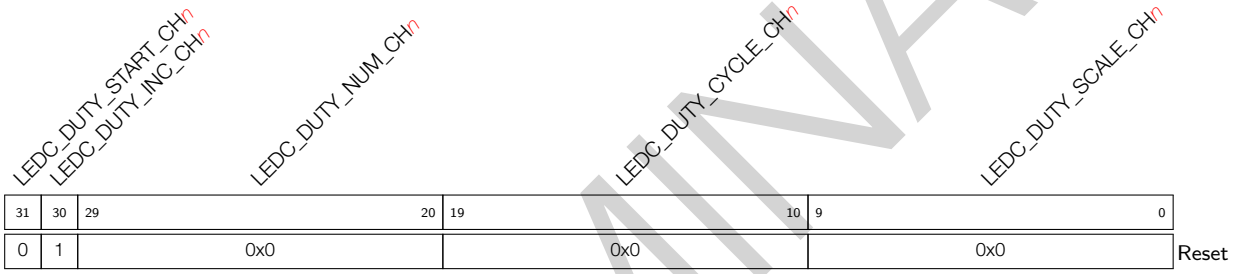
LEDC_OVF_NUM_CH*n* This register is used to configure the maximum times of overflow minus 1. The LEDC_OVF_CNT_CH*n*_INT interrupt will be triggered when channel *n* overflows for (LEDC_OVF_NUM_CH*n* + 1) times. (R/W)

LEDC_OVF_CNT_EN_CH*n* This bit is used to count the number of times when the timer selected by channel *n* overflows.(R/W)

LEDC_OVF_CNT_RESET_CH*n* Set this bit to reset the timer-overflow counter of channel *n*. (WO)

LEDC_OVF_CNT_RESET_ST_CH*n* This is the status bit of LEDC_OVF_CNT_RESET_CH*n*. (RO)

Register 31.2. LEDC_CH*n*_CONF1_REG (*n*: 0-7) (0x000C+0x14n*)**



LEDC_DUTY_SCALE_CH*n* This register is used to configure the changing step scale of duty on channel *n*. (R/W)

LEDC_DUTY_CYCLE_CH*n* The duty will change every LEDC_DUTY_CYCLE_CH*n* on channel *n*. (R/W)

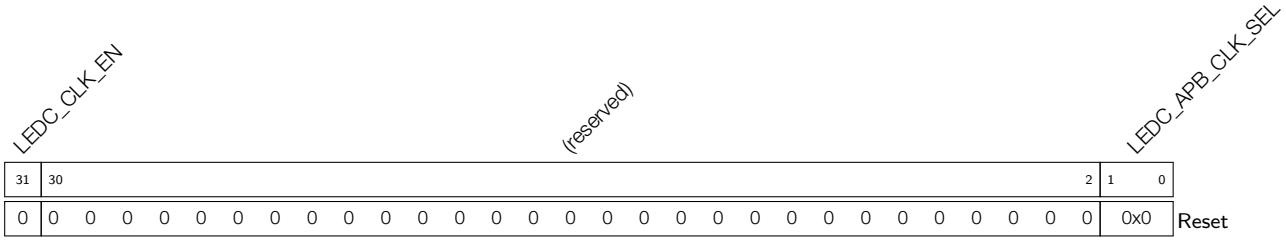
LEDC_DUTY_NUM_CH*n* This register is used to control the number of times the duty cycle will be changed. (R/W)

LEDC_DUTY_INC_CH*n* This register is used to increase or decrease the duty of output signal on channel *n*. 1: Increase; 0: Decrease. (R/W)

LEDC_DUTY_START_CH*n* Other configured fields in LEDC_CH*n*_CONF1_REG will start to take effect upon the next timer overflow when this bit is set to 1. (R/W)

PRELIMINARY

Register 31.3. LEDC_CONF_REG (0x00D0)



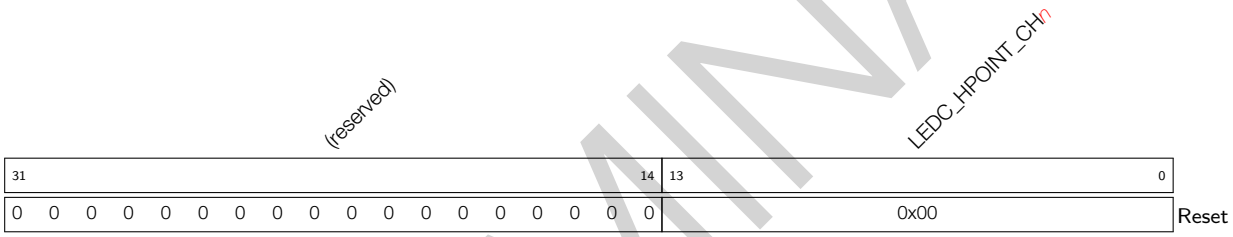
LEDC_APB_CLK_SEL This field is used to select the common clock source for all the 4 timers.

1: APB_CLK; 2: FOSC_CLK; 3: XTAL_CLK. (R/W)

LEDC_CLK_EN This bit is used to control clock.

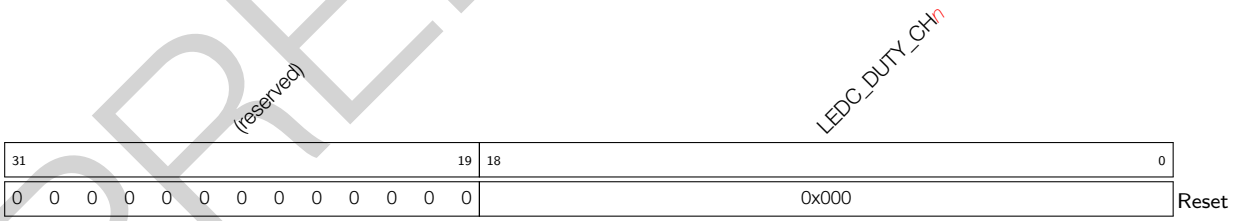
1: Force clock on for register. 0: Support clock only when application writes registers. (R/W)

Register 31.4. LEDC_CH*n*_HPOINT_REG (*n*: 0-7) (0x0004+0x14n*)**



LEDC_HPOINT_CH*n* The output value changes to high when the selected timers has reached the value specified by this register. (R/W)

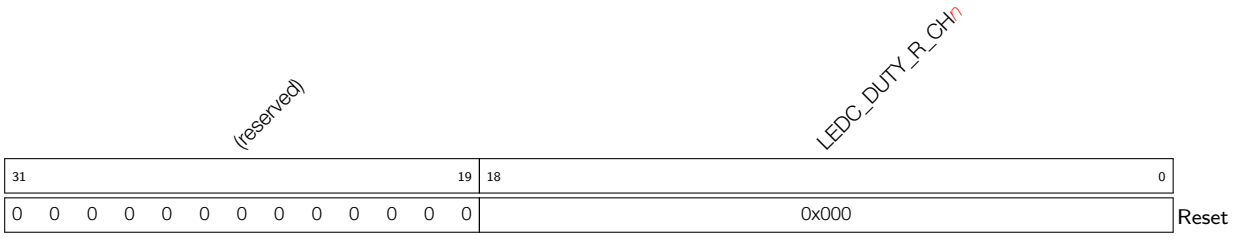
Register 31.5. LEDC_CH*n*_DUTY_REG (*n*: 0-7) (0x0008+0x14n*)**



LEDC_DUTY_CH*n* This register is used to change the output duty by controlling the Lpoint. The output value turns to low when the selected timers has reached the Lpoint. (R/W)

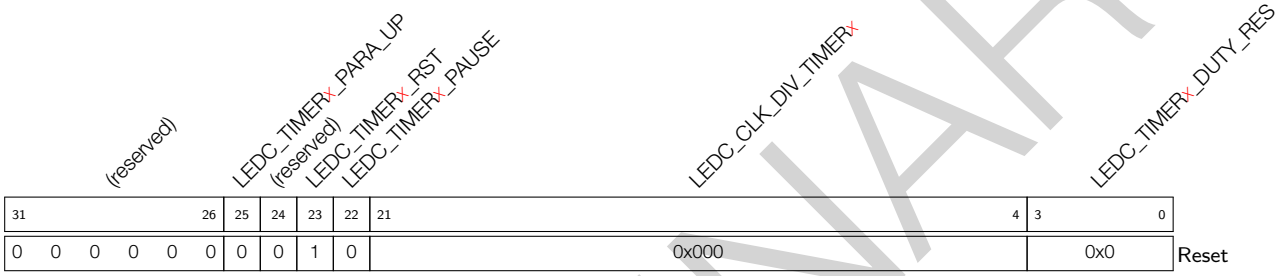
PRELIMINARY

Register 31.6. LEDC_CH*n*_DUTY_R_REG (*n*: 0-7) (0x0010+0x14n*)**



LEDC_DUTY_R_CH*n* This register stores the current duty of output signal on channel *n*. (RO)

Register 31.7. LEDC_TIMER*x*_CONF_REG (*x*: 0-3) (0x00A0+0x8x*)**



LEDC_TIMER*x*_DUTY_RES This register is used to control the range of the counter in timer *x*. (R/W)

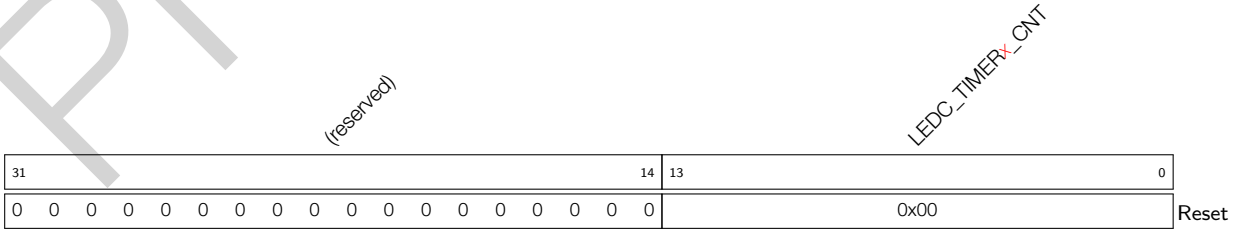
LEDC_CLK_DIV_TIMER*x* This register is used to configure the divisor for the divider in timer *x*. The least significant eight bits represent the fractional part. (R/W)

LEDC_TIMER*x*_PAUSE This bit is used to suspend the counter in timer *x*. (R/W)

LEDC_TIMER*x*_RST This bit is used to reset timer *x*. The counter will show 0 after reset. (R/W)

LEDC_TIMER*x*_PARA_UP Set this bit to update LEDC_CLK_DIV_TIMER*x* and LEDC_TIMER*x*_DUTY_RES. (WO)

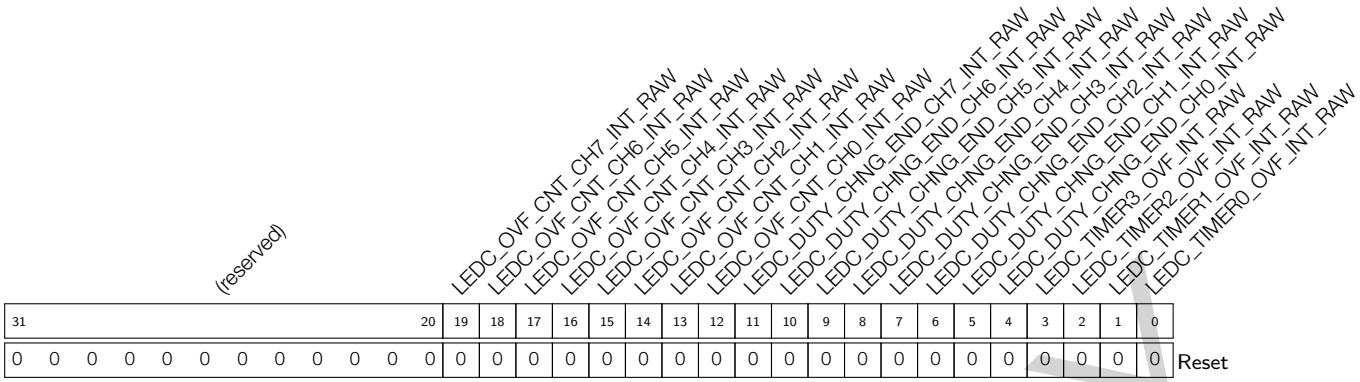
Register 31.8. LEDC_TIMER*x*_VALUE_REG (*x*: 0-3) (0x00A4+0x8x*)**



LEDC_TIMER*x*_CNT This register stores the current counter value of timer *x*. (RO)

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Register 31.9. LEDC_INT_RAW_REG (0x00C0)

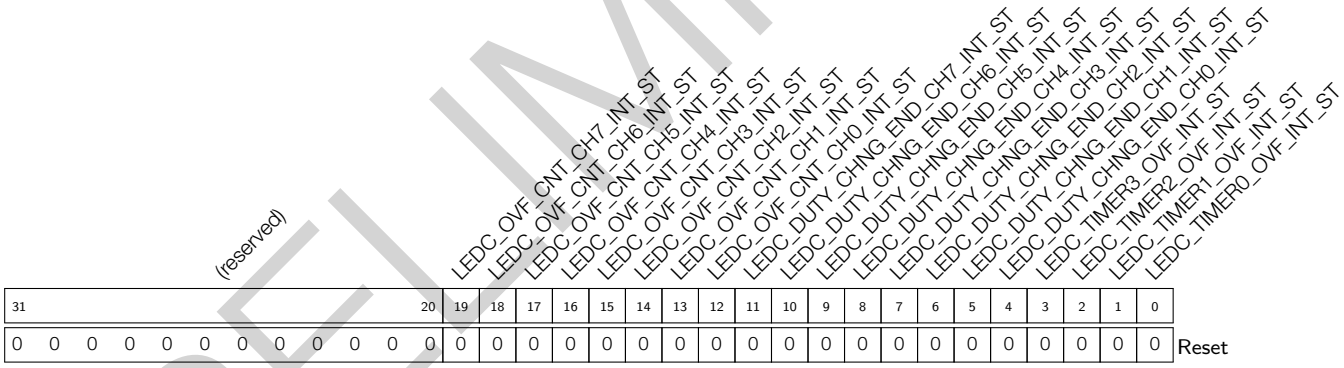


LEDC_TIMER*x*_OVF_INT_RAW Triggered when the timer*x* has reached its maximum counter value. (RO)

LEDC_DUTY_CHNG_END_CH*n*_INT_RAW Interrupt raw bit for channel *n*. Triggered when the gradual change of duty has finished. (RO)

LEDC_OVF_CNT_CH*n*_INT_RAW Interrupt raw bit for channel *n*. Triggered when the ovf_cnt has reached the value specified by LEDC_OVF_NUM_CH*n*. (RO)

Register 31.10. LEDC_INT_ST_REG (0x00C4)



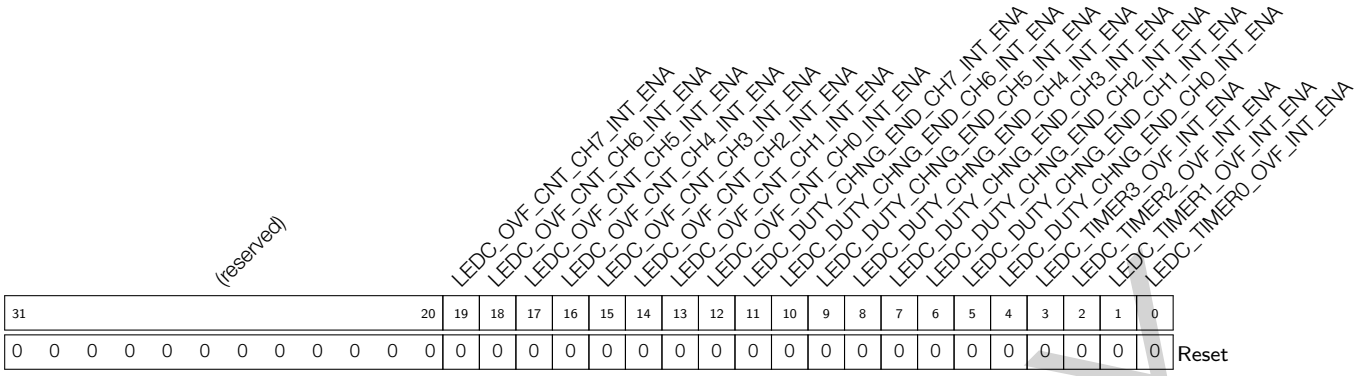
LEDC_TIMER*x*_OVF_INT_ST This is the masked interrupt status bit for the LEDC_TIMER*x*_OVF_INT interrupt when LEDC_TIMER*x*_OVF_INT_ENA is set to 1. (RO)

LEDC_DUTY_CHNG_END_CH*n*_INT_ST This is the masked interrupt status bit for the LEDC_DUTY_CHNG_END_CH*n*_INT interrupt when LEDC_DUTY_CHNG_END_CH*n*_INT_ENAIS set to 1. (RO)

LEDC_OVF_CNT_CH*n*_INT_ST This is the masked interrupt status bit for the LEDC_OVF_CNT_CH*n*_INT interrupt when LEDC_OVF_CNT_CH*n*_INT_ENA is set to 1. (RO)

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Register 31.11. LEDC_INT_ENA_REG (0x00C8)

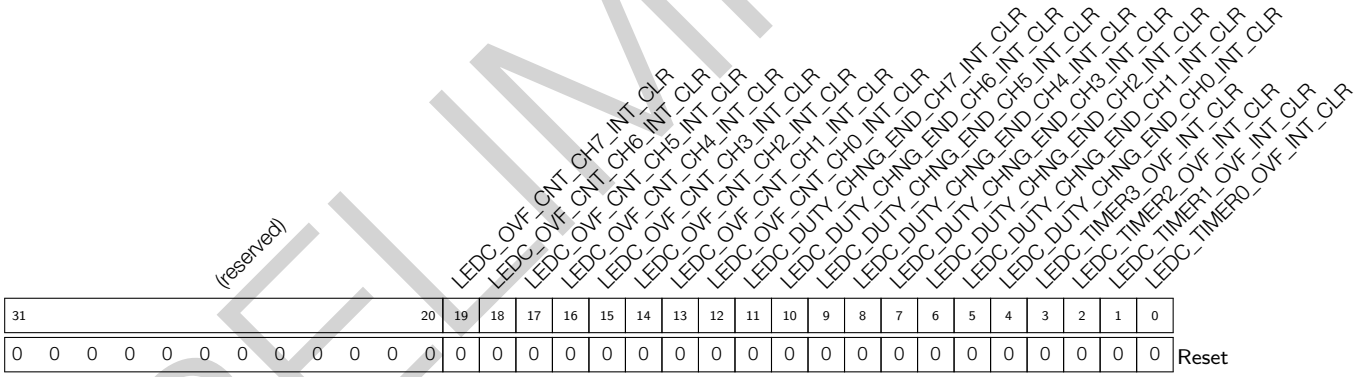


LEDC_TIMER*x*_OVF_INT_ENA The interrupt enable bit for the LEDC_TIMER*x*_OVF_INT interrupt. (R/W)

LEDC_DUTY_CHNG_END_CH*n*_INT_ENA The interrupt enable bit for the LEDC_DUTY_CHNG_END_CH*n*_INT interrupt. (R/W)

LEDC_OVF_CNT_CH*n*_INT_ENA The interrupt enable bit for the LEDC_OVF_CNT_CH*n*_INT interrupt. (R/W)

Register 31.12. LEDC_INT_CLR_REG (0x00CC)



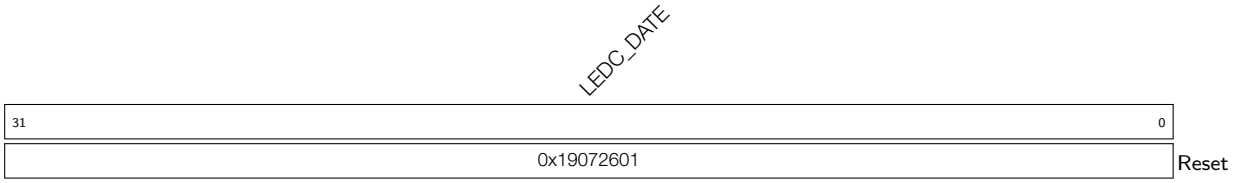
LEDC_TIMER*x*_OVF_INT_CLR Set this bit to clear the LEDC_TIMER*x*_OVF_INT interrupt. (WO)

LEDC_DUTY_CHNG_END_CH*n*_INT_CLR Set this bit to clear the LEDC_DUTY_CHNG_END_CH*n*_INT interrupt. (WO)

LEDC_OVF_CNT_CH*n*_INT_CLR Set this bit to clear the LEDC_OVF_CNT_CH*n*_INT interrupt. (WO)

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Register 31.13. LEDC_DATE_REG (0x00FC)



LEDC_DATE This is the version control register. (R/W)

PRELIMINARY

32 Motor Control PWM (MCPWM)

32.1 Overview

The **M**otor **C**ontrol **P**ulse **W**idth **M**odulator (MCPWM) peripheral is intended for motor and power control. It provides six PWM outputs that can be set up to operate in several topologies. One common topology uses a pair of PWM outputs driving an H-bridge to control motor rotation speed and rotation direction.

The timing and control resources inside are allocated into two major types of submodules: PWM timers and PWM operators. Each PWM timer provides timing references that can either run freely or be synced to other timers or external sources. Each PWM operator has all necessary control resources to generate waveform pairs for one PWM channel. The MCPWM peripheral also contains a dedicated capture submodule that is used in systems where accurate timing of external events is important.

ESP32-S3 contains two MCPWM peripherals: MCPWM0 and MCPWM1.

32.2 Features

Each MCPWM peripheral has one clock divider (prescaler), three PWM timers, three PWM operators, and a capture module. Figure 32-1 shows the submodules inside and the signals on the interface. PWM timers are used for generating timing references. The PWM operators generate desired waveform based on the timing references. Any PWM operator can be configured to use the timing references of any PWM timers. Different PWM operators can use the same PWM timer's timing references to produce related PWM signals. PWM operators can also use different PWM timers' values to produce the PWM signals that work alone. Different PWM timers can also be synchronized together.

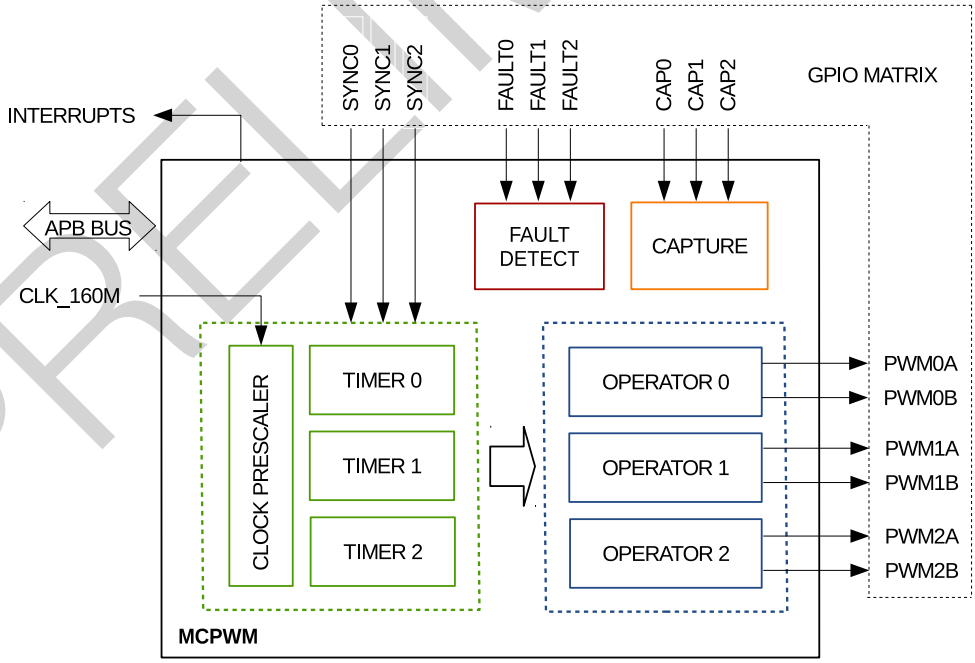


Figure 32-1. MCPWM Module Overview

An overview of the submodules' function in Figure 32-1 is shown below:

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- PWM Timers 0, 1 and 2
  - Every PWM timer has a dedicated 8-bit clock prescaler.
  - The 16-bit counter in the PWM timer can work in count-up mode, count-down mode or count-up-down mode.
  - A hardware sync or software sync can trigger a reload on the PWM timer with a phase register. It will also trigger the prescaler's restart, so that the timer's clock can also be synced. The source of the hard sync can come from any GPIO or any other PWM timer's sync_out. The source of the soft sync comes from writing toggle value to the MCPWM_TIMER*x*_SYNC_SW bit.
- PWM Operators 0, 1 and 2
  - Every PWM operator has two PWM outputs: PWM*x*A and PWM*x*B. They can work independently, in symmetric and asymmetric configuration.
  - Software, asynchronously override control of PWM signals.
  - Configurable dead-time on rising and falling edges; each set up independently.
  - All events can trigger CPU interrupts.
  - Modulating of PWM output by high-frequency carrier signals, useful when gate drivers are insulated with a transformer.
  - Period, time stamps and important control registers have shadow registers with flexible updating methods.
- Fault Detection Module
  - Programmable fault handling allocated on fault condition in both cycle-by-cycle mode and one-shot mode.
  - A fault condition can force the PWM output to either high or low logic levels.
- Capture Module
  - Speed measurement of rotating machinery (for example, toothed sprockets sensed with Hall sensors)
  - Measurement of elapsed time between position sensor pulses
  - Period and duty-cycle measurement of pulse train signals
  - Decoding current or voltage amplitude derived from duty-cycle-encoded signals of current/voltage sensors
  - Three individual capture channels, each of which has a time-stamp register (32 bits)
  - Selection of edge polarity and prescaling of input capture signal
  - The capture timer can sync with a PWM timer or external signals.
  - Interrupt on each of the three capture channels

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32.3 Submodules

32.3.1 Overview

This section lists the configuration parameters of key submodules. For information on adjusting a specific parameter, e.g. synchronization source of PWM timer, please refer to Section 32.3.2 for details.

32.3.1.1 Prescaler Submodule



Figure 32-2. Prescaler Submodule

Configuration option:

- Scale the CRYPTO_PWM_CLK.

32.3.1.2 Timer Submodule

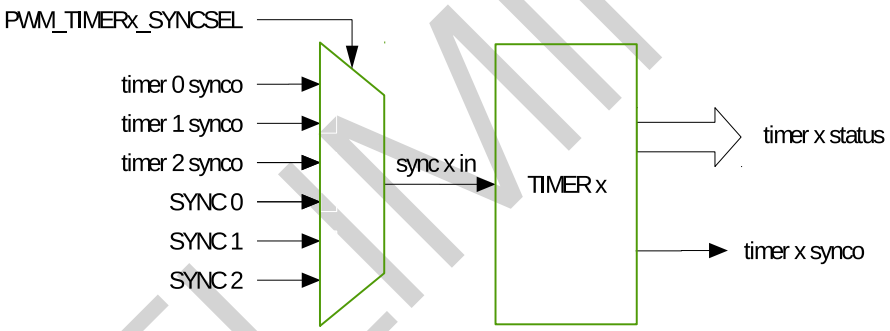


Figure 32-3. Timer Submodule

Configuration options:

- Set the PWM timer frequency or period.
- Configure the working mode for the timer:
  - Count-Up Mode: for asymmetric PWM outputs
  - Count-Down Mode: for asymmetric PWM outputs
  - Count-Up-Down Mode: for symmetric PWM outputs
- Configure the the reloading phase (including the value and the direction) used during software and hardware synchronization.
- Synchronize the PWM timers with each other. Either hardware or software synchronization may be used.
- Configure the source of the PWM timer's the synchronization input to one of the seven sources below:

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  - The three PWM timer's synchronization outputs.
  - Three synchronization signals from the GPIO matrix: PWMn_SYNC0_IN, PWMn_SYNC1_IN, PWMn_SYNC2_IN.
  - No synchronization input signal selected
- Configure the source of the PWM timer's synchronization output to one of the four sources below:
  - Synchronization input signal
  - Event generated when value of the PWM timer is equal to zero
  - Event generated when value of the PWM timer is equal to period
  - Event generated when writing toggling value to MCPWM_TIMER*x*_SYNC_SW bit
- Configure the method of period updating.

32.3.1.3 Operator Submodule

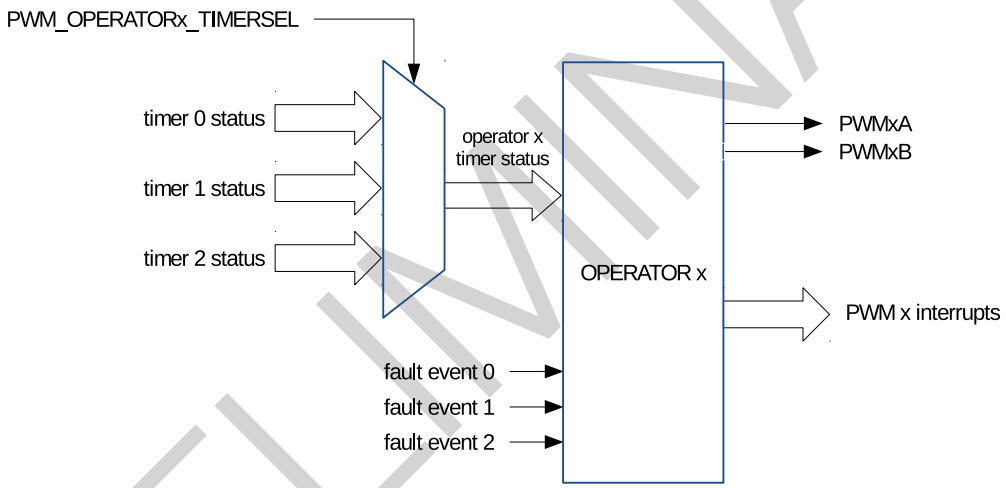


Figure 32-4. Operator Submodule

The configuration parameters of the operator submodule are shown in Table 32-1.

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Table 32-1. Configuration Parameters of the Operator Submodule

Submodule	Configuration Parameter or Option
PWM Generator	• Set up the PWM duty cycle for PWM*x*A and/or PWM*x*B output. • Set up at which time the timing events occur. • Define what action should be taken on timing events: – Switch high or low of PWM*x*A and/or PWM*x*B outputs – Toggle PWM*x*A and/or PWM*x*B outputs – Take no action on outputs • Use direct s/w control to force the state of PWM outputs • Add a dead time to raising edge and/or failing edge on PWM outputs. • Configure update method for this submodule.
Dead Time Generator	• Control of complementary dead time relationship between upper and lower switches. • Specify the dead time on rising edge. • Specify the dead time on falling edge. • Bypass the dead time generator module. The PWM waveform will pass through without inserting dead time. • Allow PWM*x*B phase shifting with respect to the PWM*x*A output. • Configure updating method for this submodule.
PWM Carrier	• Enable carrier and set up carrier frequency. • Configure duration of the first pulse in the carrier waveform. • Set up the duty cycle of the following pulses. • Bypass the PWM carrier module. The PWM waveform will be passed through without modification.
Fault Handler	• Configure if and how the PWM module should react the fault event signals. • Specify the action taken when a fault event occurs: – Force PWM*x*A and/or PWM*x*B high. – Force PWM*x*A and/or PWM*x*B low. – Configure PWM*x*A and/or PWM*x*B to ignore any fault event. • Configure how often the PWM should react to fault events: – One-shot – Cycle-by-cycle • Generate interrupts. • Bypass the fault handler submodule entirely. • Set up an option for cycle-by-cycle actions clearing. • If desired, independently-configured actions can be taken when time-base counter is counting down or up.

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32.3.1.4 Fault Detection Submodule

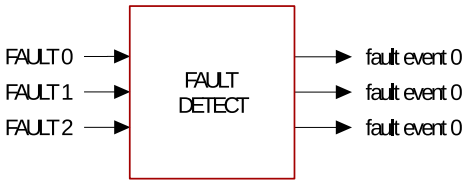


Figure 32-5. Fault Detection Submodule

Configuration options:

- Enable fault event generation and configure the polarity of fault event generation for every fault signal
- Generate fault event interrupts

32.3.1.5 Capture Submodule

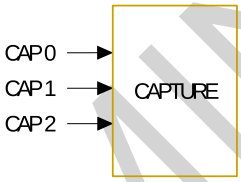


Figure 32-6. Capture Submodule

Configuration options:

- Select the edge polarity and prescaling of the capture input.
- Set up a software-triggered capture.
- Configure the capture timer's sync trigger and sync phase.
- Software syncs the capture timer.

32.3.2 PWM Timer Submodule

Each MCPWM module has three PWM timer submodules. Any of them can determine the necessary event timing for any of the three PWM operator submodules. Built-in synchronization logic allows multiple PWM timer submodules, in one or more MCPWM modules, to work together as a system, when using synchronization signals from the GPIO matrix.

32.3.2.1 Configurations of the PWM Timer Submodule

Users can configure the following functions of the PWM timer submodule:

- Control how often events occur by specifying the PWM timer frequency or period.
- Configure a particular PWM timer to synchronize with other PWM timers or modules.

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- Get a PWM timer in phase with other PWM timers or modules.
- Set one of the following timer counting modes: count-up, count-down, count-up-down.
- Change the rate of the PWM timer clock (PT_clk) with a prescaler. Each timer has its own prescaler configured with MCPWM_TIMER*x*_PRESCALE of the register MCPWM_TIMER0_CFG0_REG. The PWM timer increments or decrements at a slower pace, depending on the setting of this field.

32.3.2.2 PWM Timer's Working Modes and Timing Event Generation

The PWM timer has three working modes, selected by the PWM*x* timer mode field:

- Count-Up Mode:
  In this mode, the PWM timer increments from zero until reaching the value configured in the period field. Once done, the PWM timer returns to zero and starts increasing again. PWM period is equal to the value of the period field + 1.
  Note: The period field is MCPWM_TIMER*x*_PERIOD (*x* = 0, 1, 2), i.e., MCPWM_TIMER0_PERIOD, MCPWM_TIMER1_PERIOD, MCPWM_TIMER2_PERIOD.
- Count-Down Mode:
  The PWM timer decrements to zero, starting from the value configured in the period field. After reaching zero, it is set back to the period value. Then it starts to decrement again. In this case, the PWM period is also equal to the value of period field + 1.
- Count-Up-Down Mode:
  This is a combination of the two modes mentioned above. The PWM timer starts increasing from zero until the period value is reached. Then, the timer decreases back to zero. This pattern is then repeated. The PWM period is the result of (the value of the period field × 2 + 1).

Figures 32-7 to 32-10 show PWM timer waveforms in different modes, including timer behavior during synchronization events. In Count-Up mode, the counting direction after synchronization is always counting up. while in Count-Down mode, the counting direction after synchronization is always counting down. In Count-Up-Down Mode, the counting direction after synchronization can be chosen by setting the MCPWM_TIMER*x*_PHASE_DIRECTION.

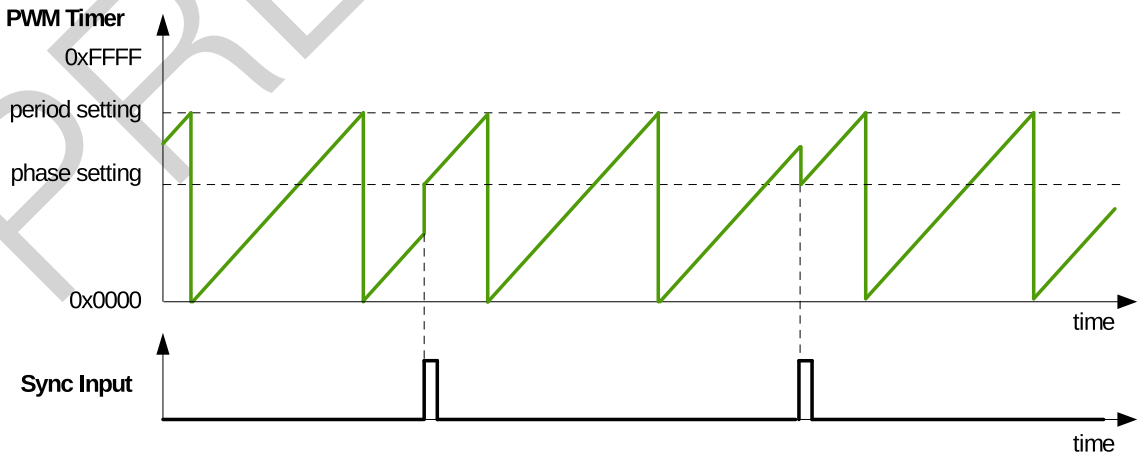


Figure 32-7. Count-Up Mode Waveform

PRELIMINARY

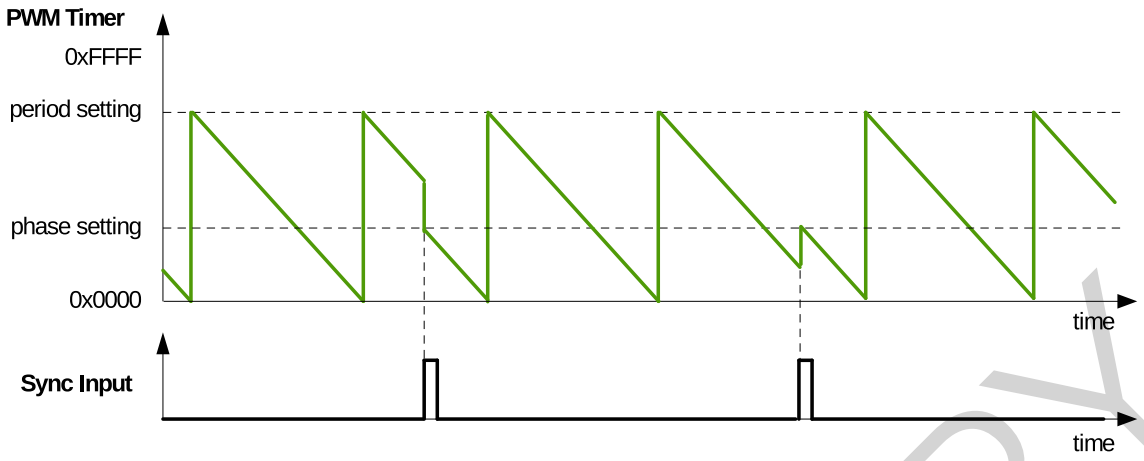


Figure 32-8. Count-Down Mode Waveforms

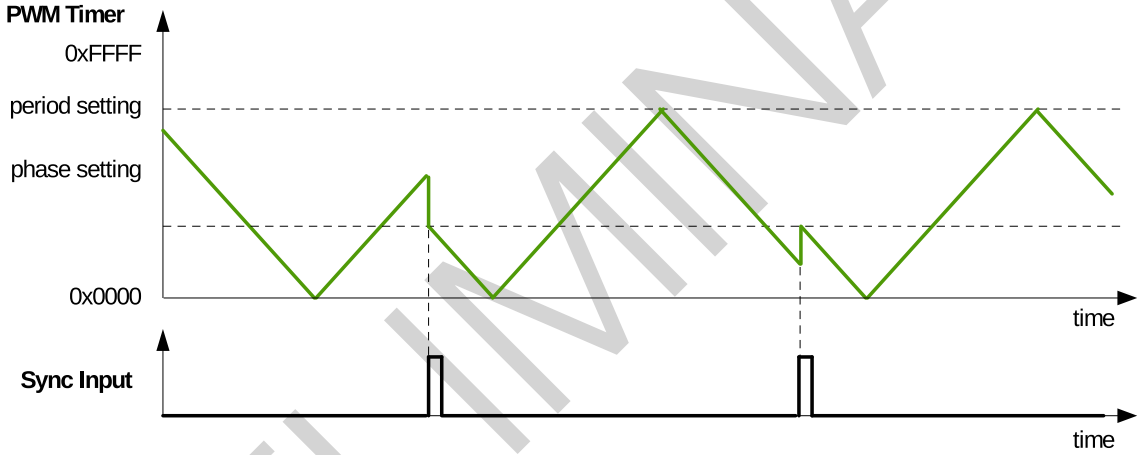


Figure 32-9. Count-Up-Down Mode Waveforms, Count-Down at Synchronization Event

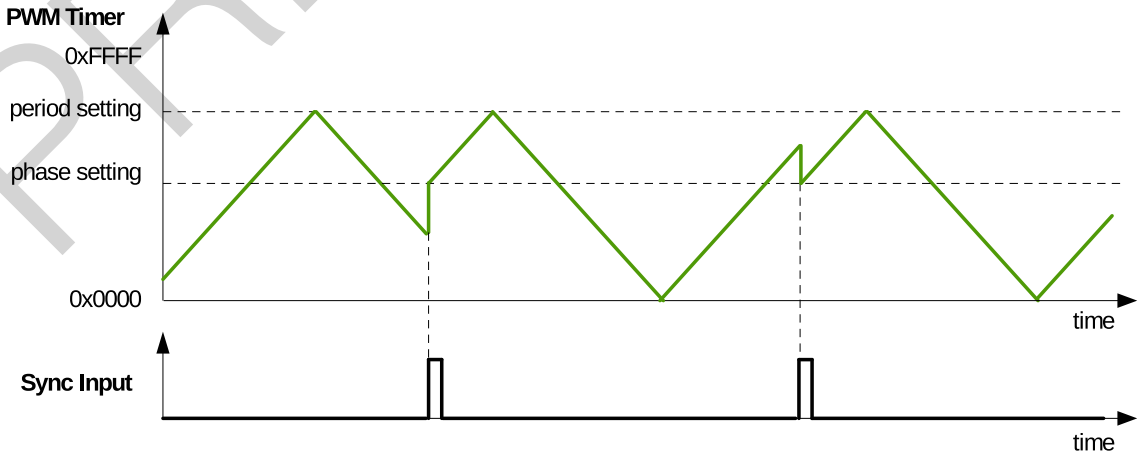


Figure 32-10. Count-Up-Down Mode Waveforms, Count-Up at Synchronization Event

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When the PWM timer is running, it generates the following timing events periodically and automatically:

- UTEP
  The timing event generated when the PWM timer's value equals to the value of the period field (MCPWM_TIMER*x*_PERIOD) and when the PWM timer is increasing.
- UTEZ
  The timing event generated when the PWM timer's value equals to zero and when the PWM timer is increasing.
- DTEP
  The timing event generated when the PWM timer's value equals to the value of the period field (MCPWM_TIMER*x*_PERIOD) and when the PWM timer is decreasing.
- DTEZ
  The timing event generated when the PWM timer's value equals to zero and when the PWM timer is decreasing.

Figures 32-11 to 32-13 show the timing waveforms of U/DTEP and U/DTEZ.

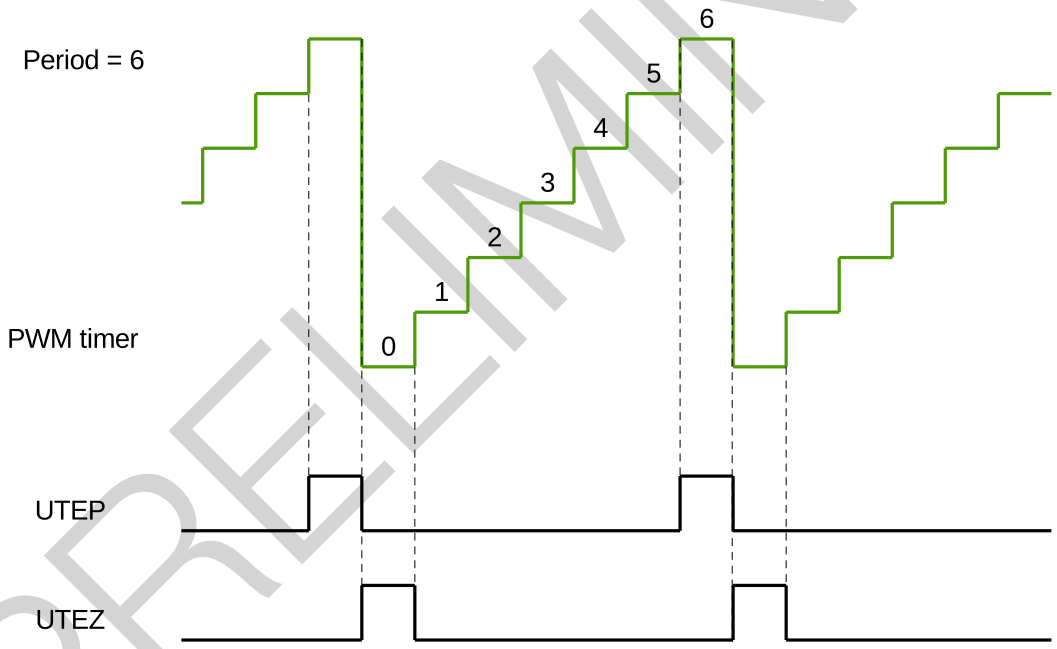


Figure 32-11. UTEP and UTEZ Generation in Count-Up Mode

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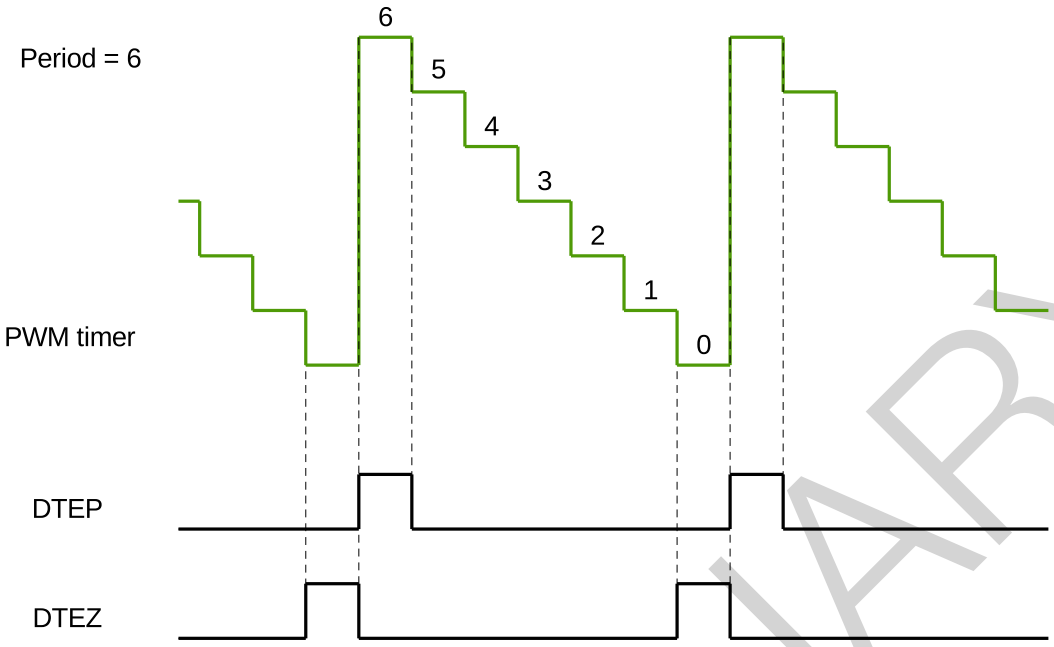


Figure 32-12. DTEP and DTEZ Generation in Count-Down Mode

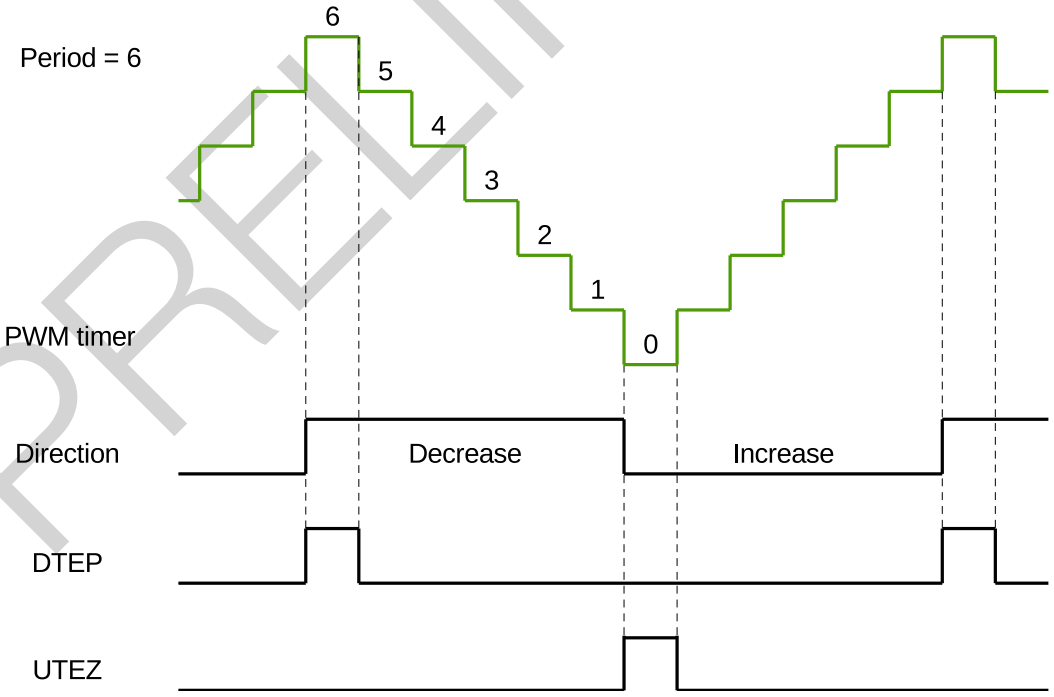


Figure 32-13. DTEP and UTEZ Generation in Count-Up-Down Mode

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32.3.2.3 PWM Timer Shadow Register

The PWM timer's period register and the PWM timer's clock prescaler register have shadow registers. The purpose of a shadow register is to save a copy of the value to be written into the active register at a specific moment synchronized with the hardware. Both register types are defined as follows:

- Active Register
  This register is directly responsible for controlling all actions performed by hardware.
- Shadow Register
  It acts as a temporary buffer for a value to be written to the active register. At a specific, user-configured point in time, the value saved in the shadow register is copied to the active register. Before this happens, the content of the shadow register has no direct effect on the controlled hardware. This helps to prevent spurious operation of the hardware, which may happen when a register is asynchronously modified by software. Both the shadow register and the active register have the same memory address. The software always writes into, or reads from the shadow register.

  The moment of updating the clock prescaler's active register is at the time when the timer starts operating. When MCPWM_GLOBAL_UP_EN is set to 1, the moment of updating the period active register can be selected by the following ways. By setting the update method register of MCPWM_TIMER*x*_PERIOD_UPMETHOD, the update can start when the PWM timer is equal to zero, when the PWM timer is equal to period, at a synchronization moment, or immediately. Software can also trigger a globally forced update bit MCPWM_GLOBAL_FORCE_UP which will prompt all registers in the module to be updated according to shadow registers.

32.3.2.4 PWM Timer Synchronization and Phase Locking

The PWM modules adopt a flexible synchronization method. Each PWM timer has a synchronization input and a synchronization output. The synchronization input can be selected from three synchronization outputs and three synchronization signals from the GPIO matrix. The synchronization output can be generated from the synchronization input signal, when the PWM timer's value is equal to period or zero, or software synchronization. Thus, the PWM timers can be chained together with their phase locked. During synchronization, the PWM timer clock prescaler will reset its counter in order to synchronize the PWM timer clock.

32.3.3 PWM Operator Submodule

The PWM Operator submodule has the following functions:

- Generates a PWM signal pair, based on timing references obtained from the corresponding PWM timer.
- Each signal out of the PWM signal pair includes a specific pattern of dead time.
- Superimposes a carrier on the PWM signal, if configured to do so.
- Handles response under fault conditions.

Figure 32-14 shows the block diagram of a PWM operator.

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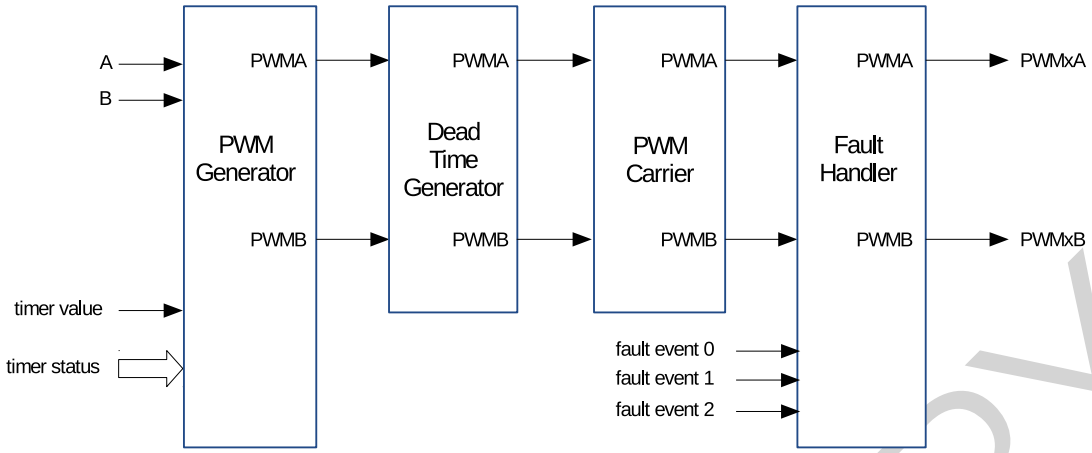


Figure 32-14. Submodules Inside the PWM Operator

32.3.3.1 PWM Generator Submodule

Purpose of the PWM Generator Submodule

In this submodule, important timing events are generated or imported. The events are then converted into specific actions to generate the desired waveforms at the PWM*x*A and PWM*x*B outputs.

The PWM generator submodule performs the following actions:

- Generation of timing events based on time stamps configured using the A and B registers. Events happen when the following conditions are satisfied:
  - UTEA: the PWM timer is counting up and its value is equal to register A.
  - UTEB: the PWM timer is counting up and its value is equal to register B.
  - DTEA: the PWM timer is counting down and its value is equal to register A.
  - DTEB: the PWM timer is counting down and its value is equal to register B.
- Generation of U/DT1, U/DT2 timing events based on fault or synchronization events.
- Management of priority when these timing events occur concurrently.
- Qualification and generation of set, clear and toggle actions, based on the timing events.
- Controlling of the PWM duty cycle, depending on configuration of the PWM generator submodule.
- Handling of new time stamp values, using shadow registers to prevent glitches in the PWM cycle.

PWM Operator Shadow Registers

The time stamp registers A and B, as well as action configuration registers MCPWM_GEN*x*_A_REG and MCPWM_GEN*x*_B_REG are shadowed. Shadowing provides a way of updating registers in sync with the hardware.

When MCPWM_GLOBAL_UP_EN is set to 1, the shadow registers can be written to the active register at a

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specified time. The update method fields for time stamp registers A and B are MCPWM_GEN_A_UPMETHOD and MCPWM_GEN_B_UPMETHOD. The update method field for MCPWM_GEN*x*_A_REG and MCPWM_GEN*x*_B_REG is MCPWM_GEN_CFG_UPMETHOD. Software can also trigger a globally forced update bit
MCPWM_GLOBAL_FORCE_UP which will prompt all registers in the module to be updated according to shadow registers. For a description of the shadow registers, please see 32.3.2.3.

Timing Events

For convenience, all timing signals and events are summarized in Table 32-2.

Table 32-2. Timing Events Used in PWM Generator

Signal	Event Description	PWM Timer Operation
DTEP	PWM timer value is equal to the period register value	PWM timer counts down.
DTEZ	PWM timer value is equal to zero	
DTEA	PWM timer value is equal to A register	
DTEB	PWM timer value is equal to B register	
DT0 event	Based on fault or synchronization events	
DT1 event	Based on fault or synchronization events	
UTEP	PWM timer value is equal to the period register value	PWM timer counts up.
UTEZ	PWM timer value is equal to zero	
UTEA	PWM timer value is equal to A register	
UTEB	PWM timer value is equal to B register	
UT0 event	Based on fault or synchronization events	
UT1 event	Based on fault or synchronization events	
Software-force event	Software-initiated asynchronous event	N/A

The purpose of a software-force event is to impose non-continuous or continuous changes on the PWM*x*A and PWM*x*B outputs. The change is done asynchronously. Software-force control is handled by the MCPWM_GEN*x*_FORCE_REG registers.

The selection and configuration of T0/T1 in the PWM generator submodule is independent of the configuration of fault events in the fault handler submodule. A particular trip event may or may not be configured to cause trip action in the fault handler submodule, but the same event can be used by the PWM generator to trigger T0/T1 for controlling PWM waveforms.

It is important to know that when the PWM timer is in count-up-down mode, it will always decrement after a TEP event, and will always increment after a TEZ event. So when the PWM timer is in count-up-down mode, DTEP and UTEZ events will occur, while the events UTEP and DTEZ will never occur.

The PWM generator can handle multiple events at the same time. Events are prioritized by the hardware and relevant details are provided in Table 32-3 and Table 32-4. Priority levels range from 1 (the highest) to 7 (the lowest). Please note that the priority of TEP and TEZ events depends on the PWM timer's direction.

If the value of A or B is set to be greater than the period, then U/DTEA and U/DTEB will never occur.

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Table 32-3. Timing Events Priority When PWM Timer Increments

Priority Level	Event
1 (highest)	Software-force event
2	UTEP
3	UT0
4	UT1
5	UTEB
6	UTEA
7 (lowest)	UTEZ

Table 32-4. Timing Events Priority when PWM Timer Decrements

Priority level	Event
1 (highest)	Software-force event
2	DTEZ
3	DT0
4	DT1
5	DTEB
6	DTEA
7 (lowest)	DTEP

Notes:

1. UTEP and UTEZ do not happen simultaneously. When the PWM timer is in count-up mode, UTEP will always happen one cycle earlier than UTEZ, as demonstrated in Figure 32-11, so their action on PWM signals will not interrupt each other. When the PWM timer is in count-up-down mode, UTEP will not occur.
2. DTEP and DTEZ do not happen simultaneously. When the PWM timer is in count-down mode, DTEZ will always happen one cycle earlier than DTEP, as demonstrated in Figure 32-12, so their action on PWM signals will not interrupt each other. When the PWM timer is in count-up-down mode, DTEZ will not occur.

PWM Signal Generation

The PWM generator submodule controls the behavior of outputs PWM*x*A and PWM*x*B when a particular timing event occurs. The timing events are further qualified by the PWM timer's counting direction (up or down). Knowing the counting direction, the submodule may then perform an independent action at each stage of the PWM timer counting up or down.

The following actions may be configured on outputs PWM*x*A and PWM*x*B:

- Set High:
  Set the output of PWM*x*A or PWM*x*B to a high level.
- Clear Low:
  Clear the output of PWM*x*A or PWM*x*B by setting it to a low level.
- Toggle:

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Change the current output level of PWM*x*A or PWM*x*B to the opposite value. If it is currently pulled high, pull it low, or vice versa.

- Do Nothing:
  Keep both outputs PWM*x*A and PWM*x*B unchanged. In this state, interrupts can still be triggered.

The configuration of actions on outputs is done by using registers MCPWN_GEN*x*_A_REG and MCPWN_GEN*x*_B_REG. So, the action to be taken on each output is set independently. Also there is great flexibility in selecting actions to be taken on a given output based on events. More specifically, any event listed in Table 32-2 can operate on either output PWM*x*A or PWM*x*B. To check out registers for particular generator 0, 1 or 2, please refer to register description in Section 32.4.

Waveforms for Common Configurations

Figure 32-15 presents the symmetric PWM waveform generated when the PWM timer is counting up and down. DC 0%–100% modulation can be calculated via the formula below:

$$Duty = (Period - A) \div Period$$

If A matches the PWM timer value and the PWM timer is incrementing, then the PWM output is pulled up. If A matches the PWM timer value while the PWM timer is decrementing, then the PWM output is pulled low.

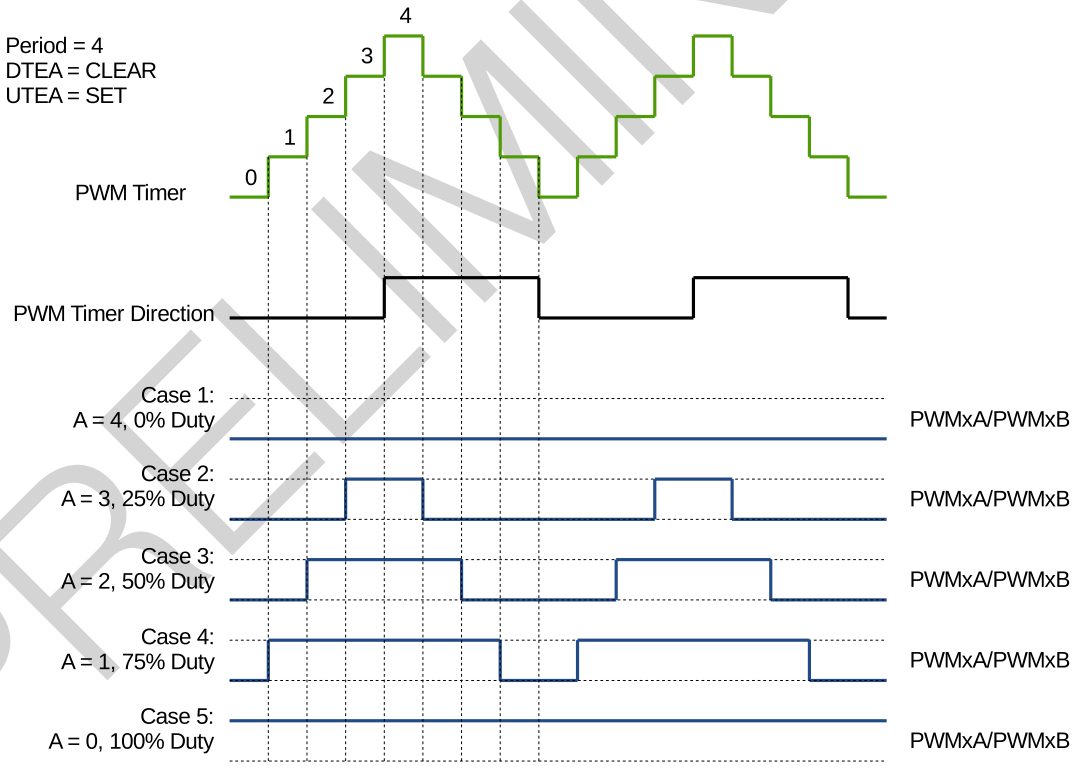


Figure 32-15. Symmetrical Waveform in Count-Up-Down Mode

The PWM waveforms in Figures 32-16 to 32-19 show some common PWM operator configurations. The following conventions are used in the figures:

- Period A and B refer to the values written in the corresponding registers.
- PWM*x*A and PWM*x*B are the output signals of PWM Operator *x*.

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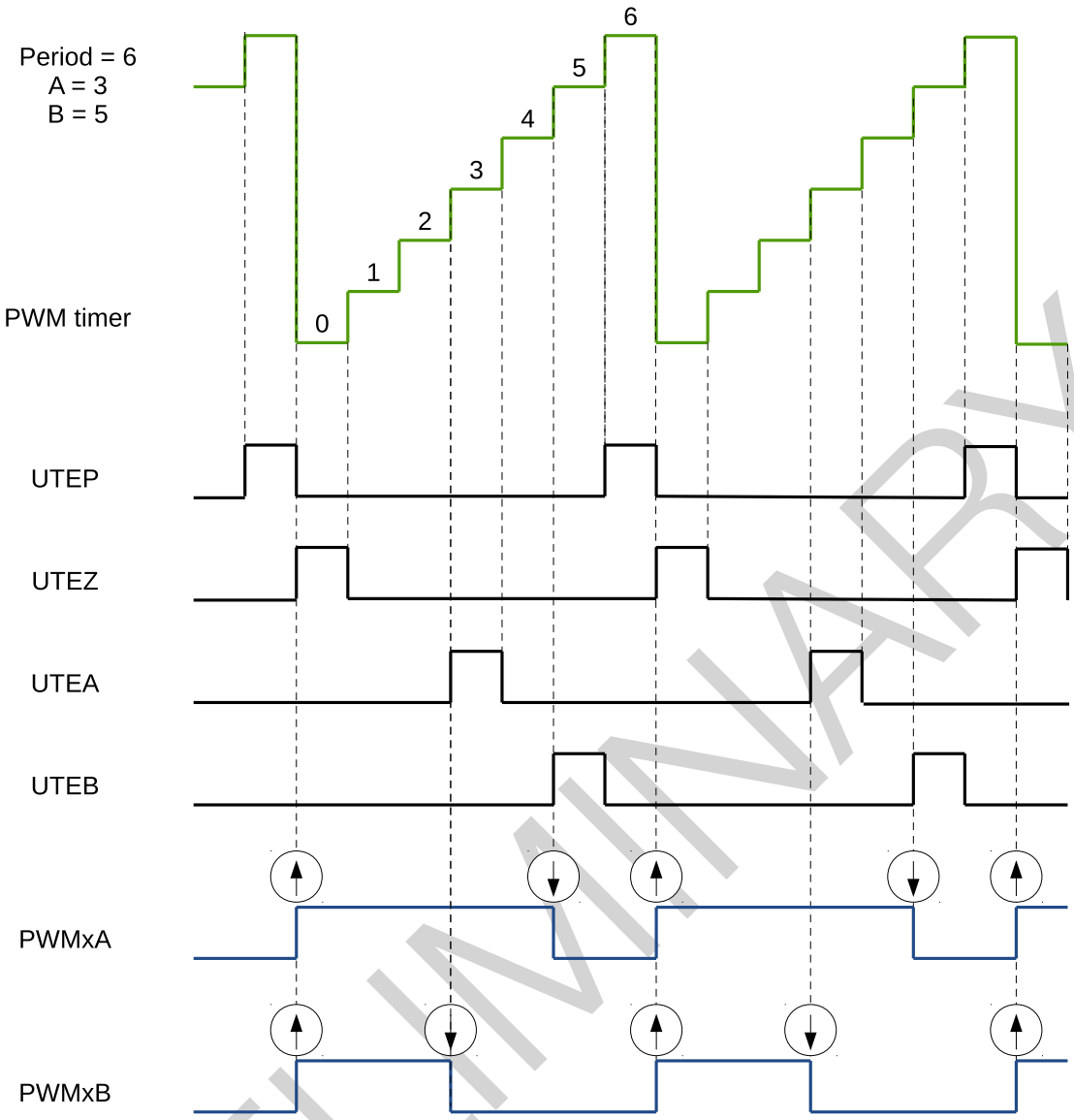


Figure 32-16. Count-Up, Single Edge Asymmetric Waveform, with Independent Modulation on PWM*x*A and PWM*x*B — Active High

The duty modulation for PWM*x*A is set by B, active high and proportional to B.
The duty modulation for PWM*x*B is set by A, active high and proportional to A.

$$Period = (MCPWM\_TIMERx\_PERIOD + 1) \times T_{PT\_clk}$$

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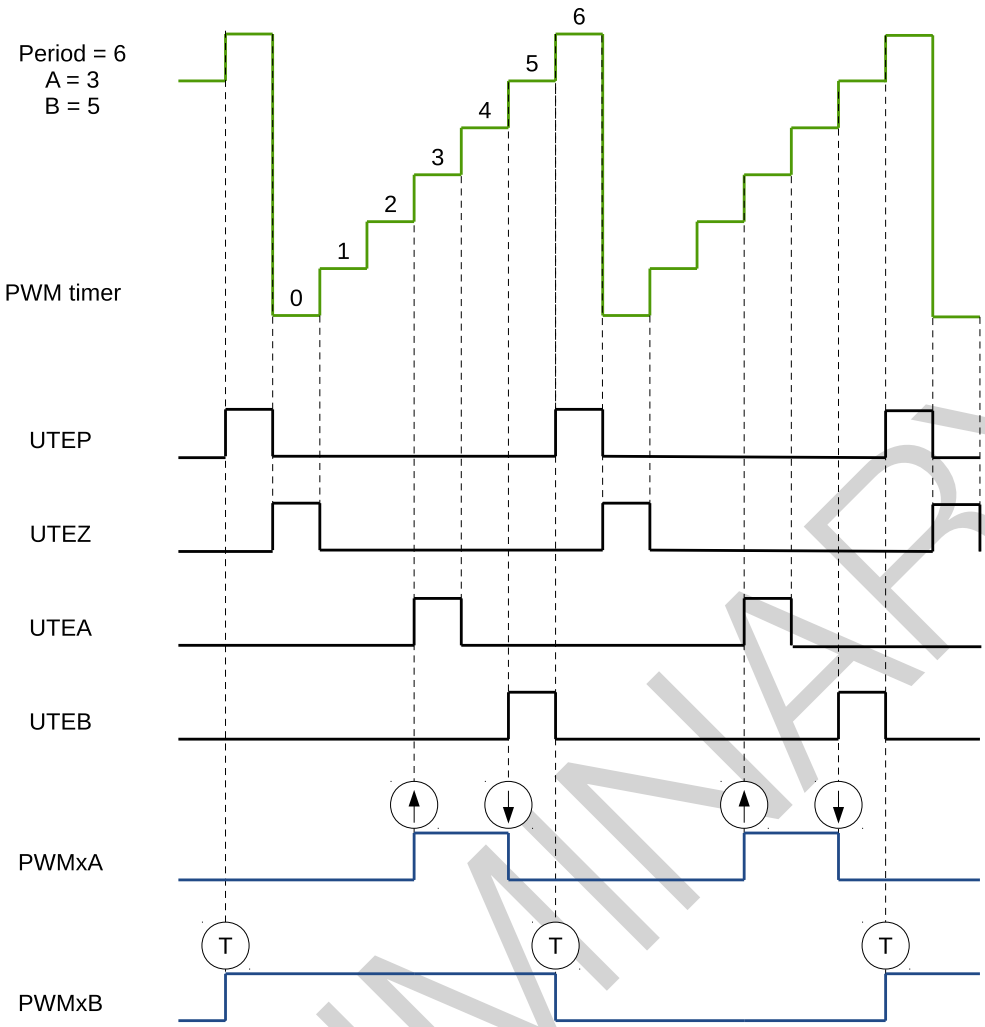


Figure 32-17. Count-Up, Pulse Placement Asymmetric Waveform with Independent Modulation on PWMxA

Pulses may be generated anywhere within the PWM cycle (zero – period).

PWMxA's high time duty is proportional to (B – A).

$$Period = (MCPWM\_TIMERx\_PERIOD + 1) \times T_{PT\_clk}$$

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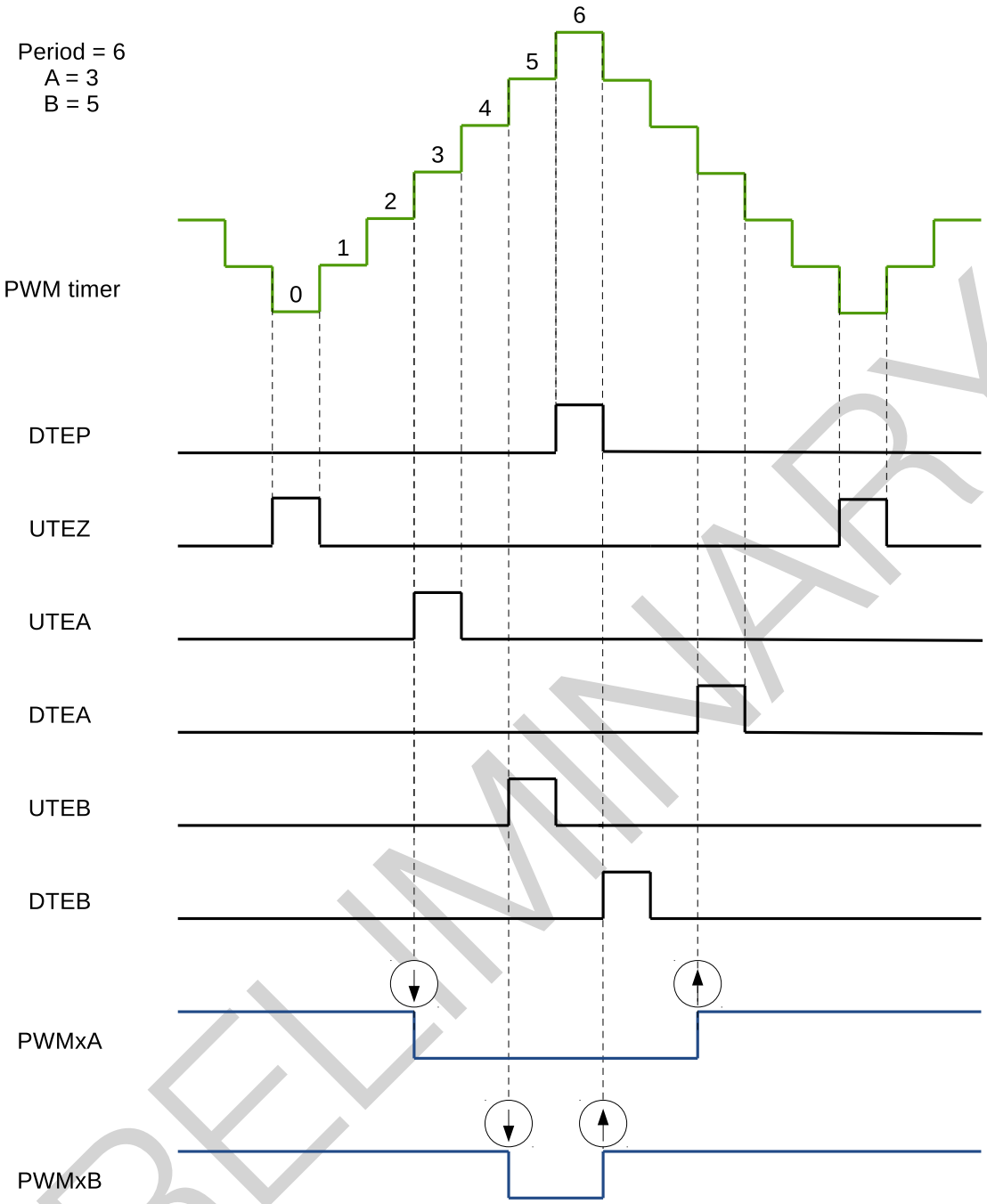


Figure 32-18. Count-Up-Down, Dual Edge Symmetric Waveform, with Independent Modulation on PWM*x*A and PWM*x*B — Active High

The duty modulation for PWM*x*A is set by A, active high and proportional to A.
The duty modulation for PWM*x*B is set by B, active high and proportional to B.
Outputs PWM*x*A and PWM*x*B can drive independent switches.

$$Period = (2 \times MCPWM\_TIMERx\_PERIOD) \times T_{PT\_clk}$$

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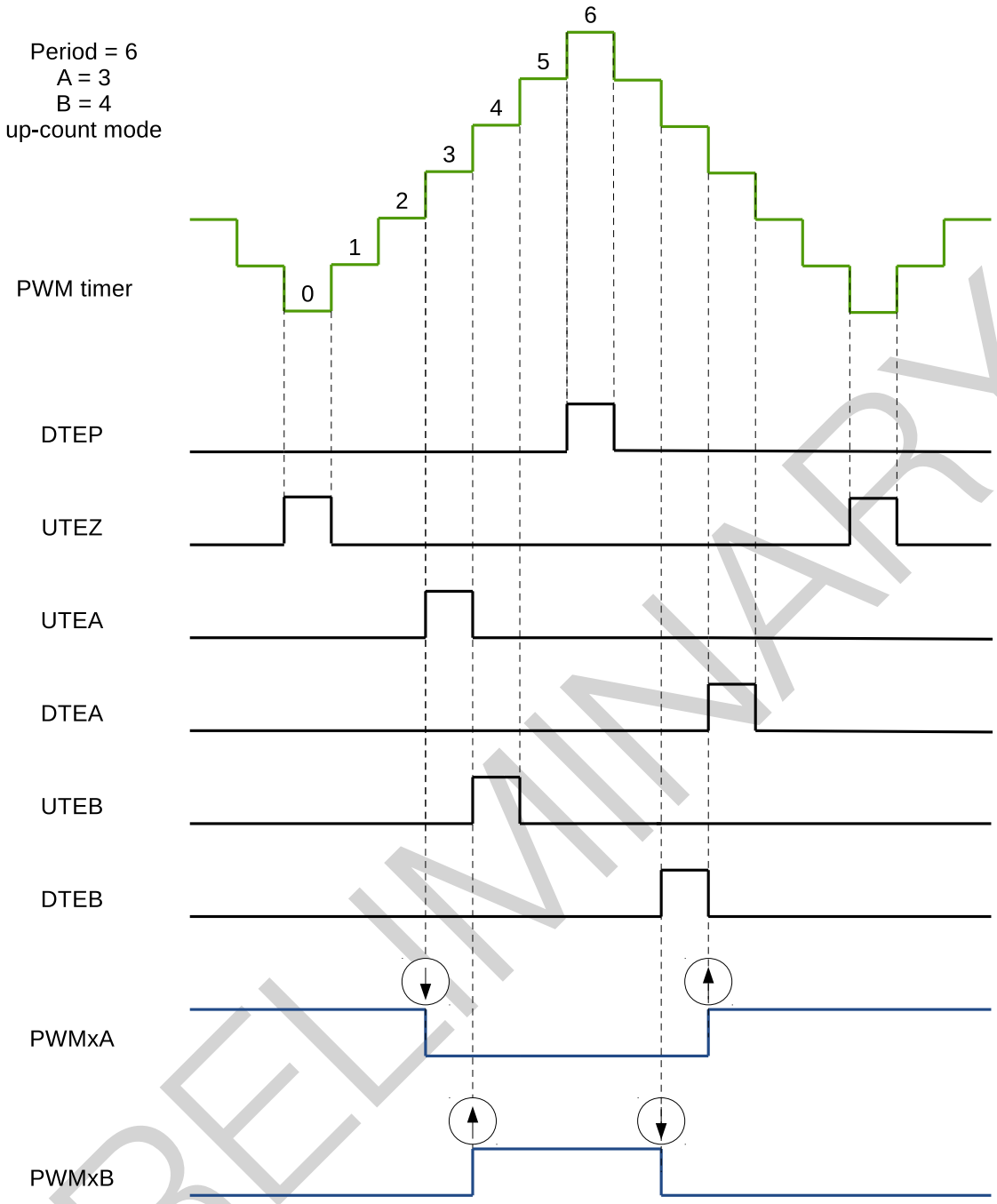


Figure 32-19. Count-Up-Down, Dual Edge Symmetric Waveform, with Independent Modulation on PWM*x*A and PWM*x*B — Complementary

The duty modulation of PWM*x*A is set by A, is active high and proportional to A.
The duty modulation of PWM*x*B is set by B, is active low and proportional to B.
Outputs PWM*x* can drive upper/lower (complementary) switches.
Dead-time = B – A; Edge placement is fully programmable by software. Use the dead-time generator module if another edge delay method is required.

$$Period = (2 \times MCPWM\_TIMERx\_PERIOD) \times T_{PT\_clk}$$

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Software-Force Events

There are two types of software-force events inside the PWM generator:

- Non-continuous-immediate (NCI) software-force events
  Such types of events are immediately effective on PWM outputs when triggered by software. The forcing is non-continuous, meaning the next active timing events will be able to alter the PWM outputs.
- Continuous (CNTU) software-force events
  Such types of events are continuous. The forced PWM outputs will continue until they are released by software. The events' triggers are configurable. They can be timing events or immediate events.

Figure 32-20 shows a waveform of NCI software-force events. NCI events are used to force PWMxA output low. Forcing on PWMxB is disabled in this case.

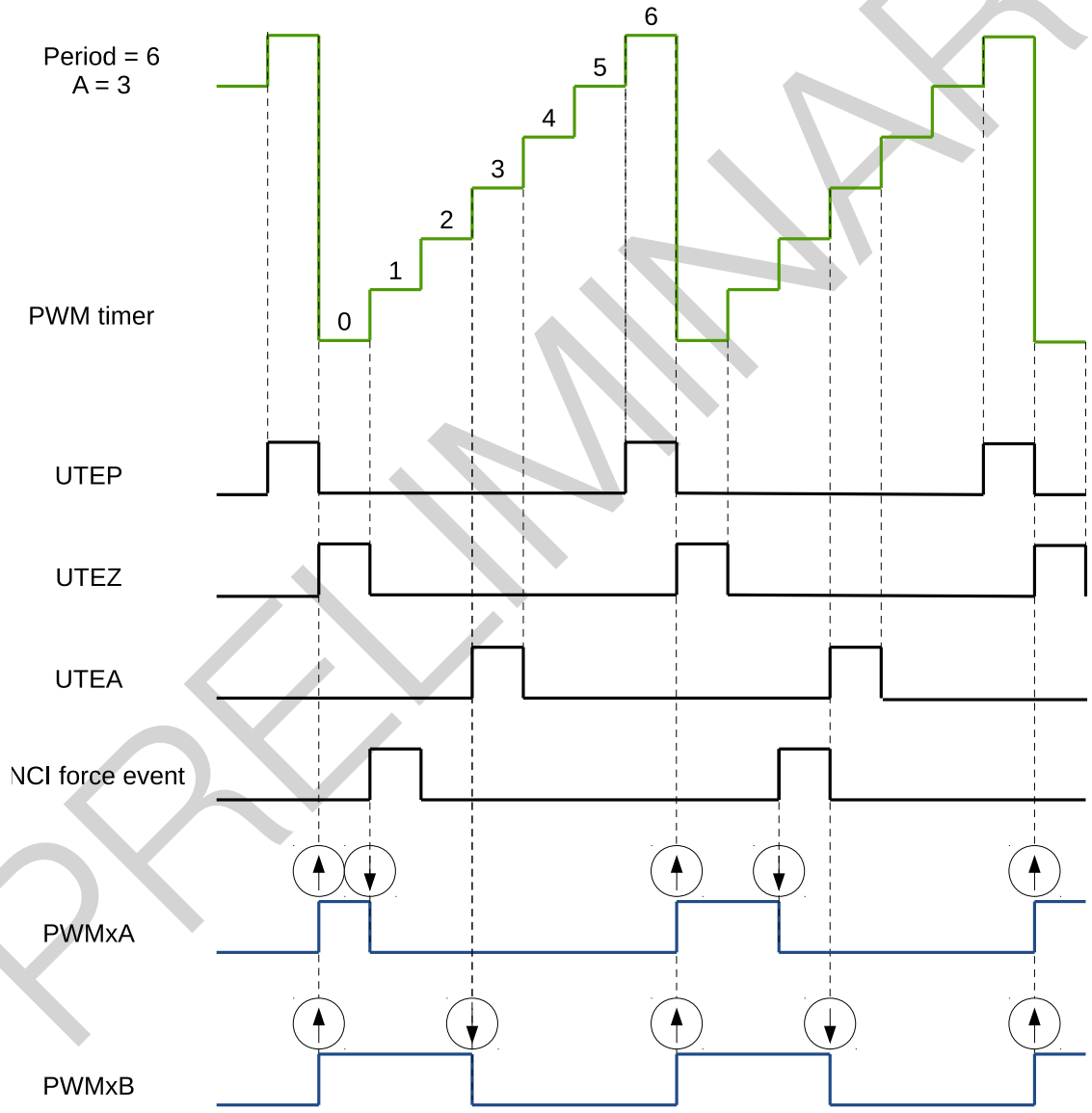


Figure 32-20. Example of an NCI Software-Force Event on PWMxA

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Figure 32-21 shows a waveform of CNTU software-force events. UTEZ events are selected as triggers for CNTU software-force events. CNTU is used to force the PWM*x*B output low. Forcing on PWM*x*A is disabled.

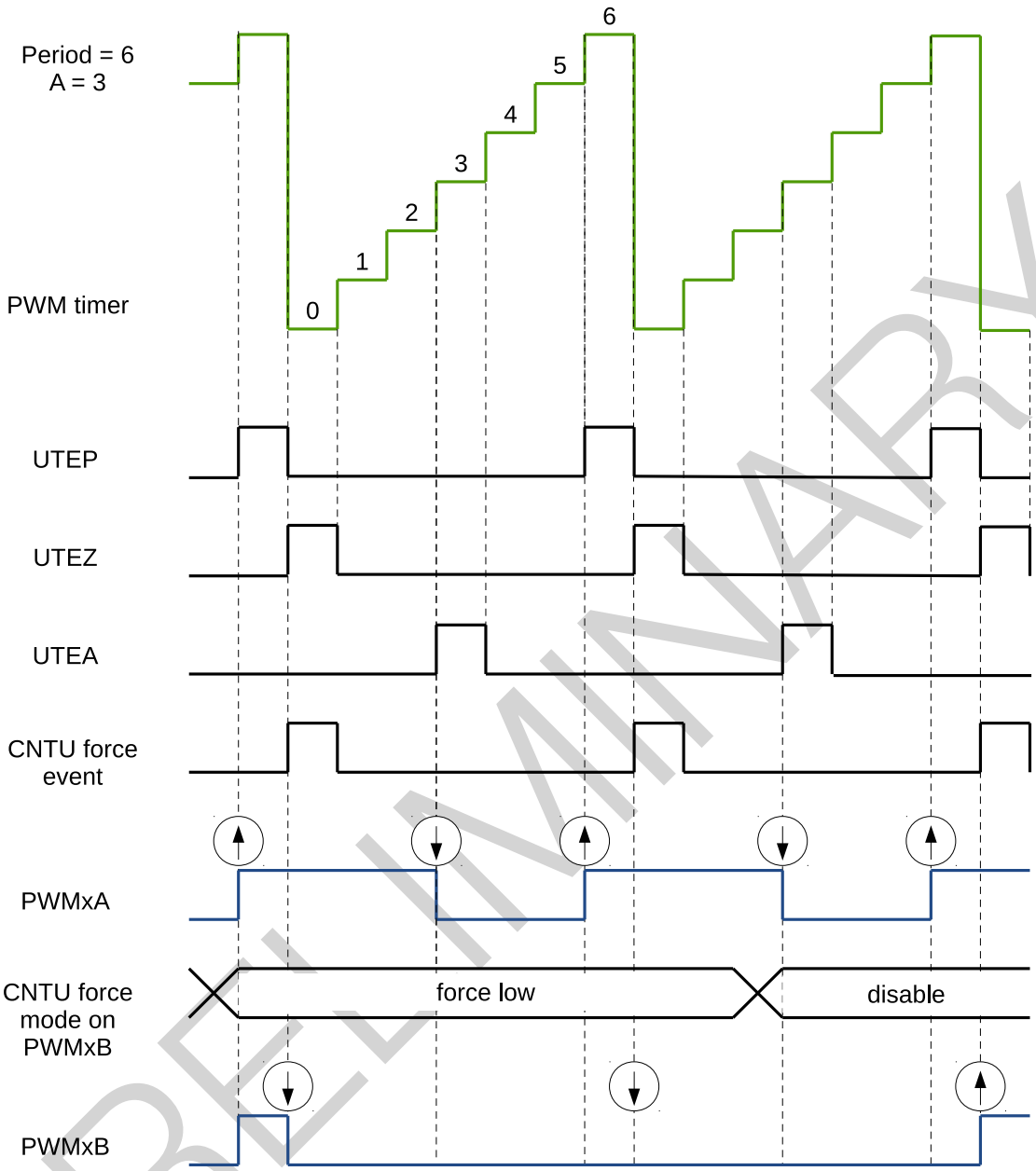


Figure 32-21. Example of a CNTU Software-Force Event on PWM*x*B

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32.3.3.2 Dead Time Generator Submodule

Purpose of the Dead Time Generator Submodule

Several options to generate signals on PWM*x*A and PWM*x*B outputs, with a specific placement of signal edges, have been discussed in section 32.3.3.1. The required dead time is obtained by altering the edge placement between signals and by setting the signal's duty cycle. Another option is to control the dead time using a specialized submodule – the Dead Time Generator.

The key functions of the dead time generator submodule are as follows:

- Generating signal pairs (PWM*x*A and PWM*x*B) with a dead time from a single PWM*x*A input
- Creating a dead time by adding delay to signal edges:
  - Rising edge delay (RED)
  - Falling edge delay (FED)
- Configuring the signal pairs to be:
  - Active high complementary (AHC)
  - Active low complementary (ALC)
  - Active high (AH)
  - Active low (AL)
- This submodule may also be bypassed, if the dead time is configured directly in the generator submodule.

Dead Time Generator's Shadow Registers

Delay registers RED and FED are shadowed with registers MCPWM_DT*x*_RED_CFG_REG and MCPWM_DT*x*_FED_CFG_REG. When MCPWM_GLOBAL_UP_EN is set to 1, the shadow registers can be written to the active register at specified time. The update method register for MCPWM_DT*x*_RED_CFG_REG is MCPWM_DT_RED_UPMETHOD. The update method register for MCPWM_DT*x*_FED_CFG_REG is MCPWM_DT_FED_UPMETHOD. The Software can also trigger a globally forced update bit MCPWM_GLOBAL_FORCE_UP which will prompt all registers in the module to be updated according to shadow registers.For the description of shadow registers, please see section 32.3.2.3.

Highlights for Operation of the Dead Time Generator

Options for setting up the dead-time submodule are shown in Figure 32-22.

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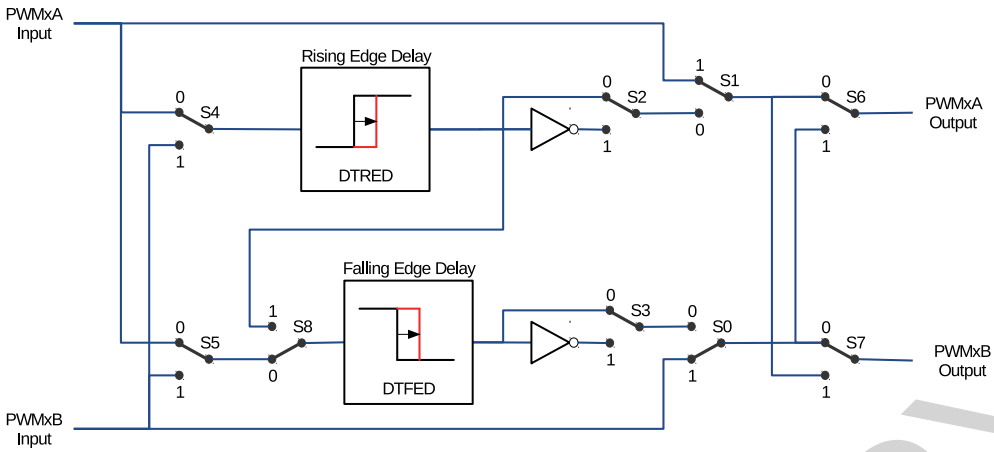


Figure 32-22. Options for Setting up the Dead Time Generator Submodule

S0-S8 in the figure above are switches controlled by fields in register MCPWM_DTx_CFG_REG shown in Table 32-5.

Table 32-5. Dead Time Generator Switches Control Fields

Switch	Field
S0	MCPWM_DTx_B_OUTBYPASS
S1	MCPWM_DTx_A_OUTBYPASS
S2	MCPWM_DTx_RED_OUTINVERT
S3	MCPWM_DTx_FED_OUTINVERT
S4	MCPWM_DTx_RED_INSEL
S5	MCPWM_DTx_FED_INSEL
S6	MCPWM_DTx_A_OUTSWAP
S7	MCPWM_DTx_B_OUTSWAP
S8	MCPWM_DTx_DEB_MODE

All switch combinations are supported, but not all of them represent the typical modes of use. Table 32-6 documents some typical dead time configurations. In these configurations the position of S4 and S5 sets PWMxA as the common source of both falling-edge and rising-edge delay. The modes presented in table 32-6 may be categorized as follows:

Table 32-6. Typical Dead Time Generator Operating Modes

Mode	Mode Description	S0	S1	S2	S3
1	PWMxA and PWMxB Pass Through/No Delay	1	1	X	X
2	Active High Complementary (AHC), see Figure 32-23	0	0	0	1
3	Active Low Complementary (ALC), see Figure 32-24	0	0	1	0
4	Active High (AH), see Figure 32-25	0	0	0	0
5	Active Low (AL), see Figure 32-26	0	0	1	1
6	PWMxA Output = PWMxA In (No Delay) PWMxB Output = PWMxA Input with Falling Edge Delay	0	1	0 or 1	0 or 1
7	PWMxA Output = PWMxA Input with Rising Edge Delay PWMxB Output = PWMxB Input with No Delay	1	0	0 or 1	0 or 1

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Note:
For all the modes above, the position of the binary switches S4 to S8 is set to 0.

- **Mode 1: Bypass delays on both falling (FED) as well as raising edge (RED)**
  In this mode the dead time submodule is disabled. Signals PWM*x*A and PWM*x*B pass through without any modifications.
- **Mode 2-5: Classical Dead Time Polarity Settings**
  These modes represent typical configurations of polarity and should cover the active-high/low modes in available industry power switch gate drivers. The typical waveforms are shown in Figures 32-23 to 32-26.
- **Modes 6 and 7: Bypass delay on falling edge (FED) or rising edge (RED)**
  In these modes, either RED (Rising Edge Delay) or FED (Falling Edge Delay) is bypassed. As a result, the corresponding delay is not applied.

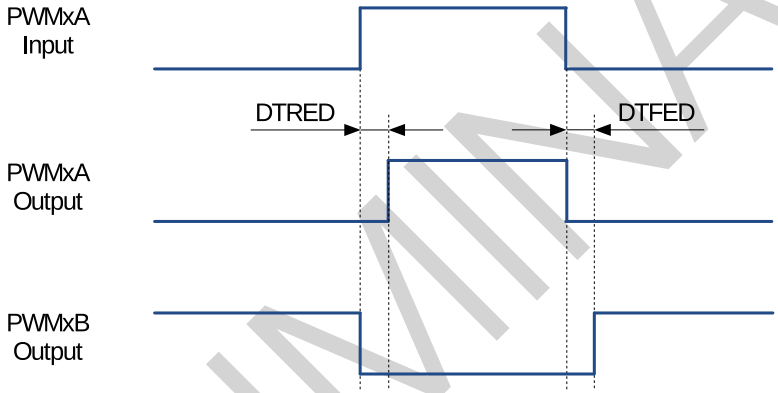


Figure 32-23. Active High Complementary (AHC) Dead Time Waveforms

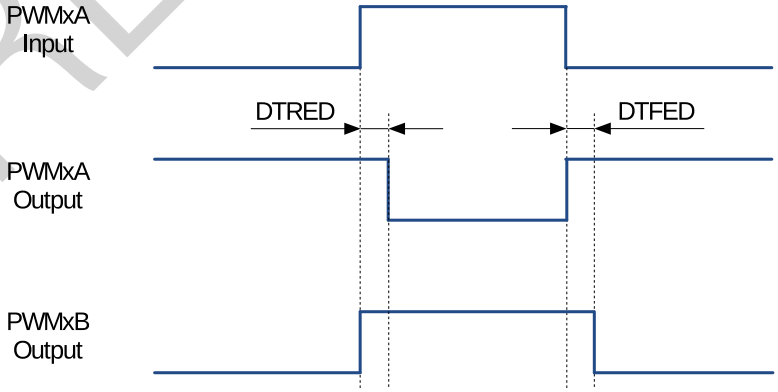


Figure 32-24. Active Low Complementary (ALC) Dead Time Waveforms

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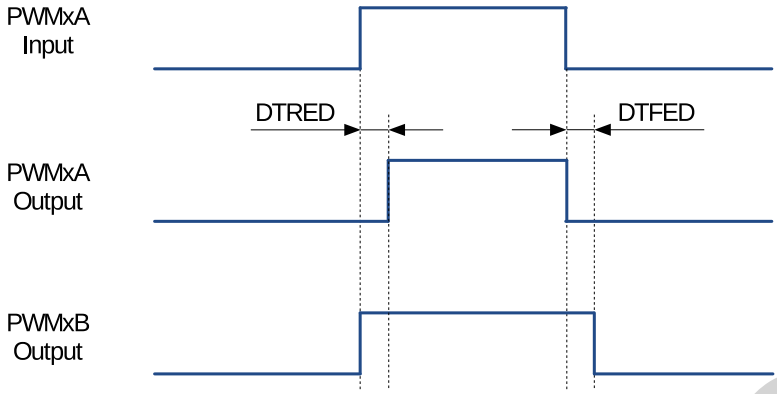


Figure 32-25. Active High (AH) Dead Time Waveforms

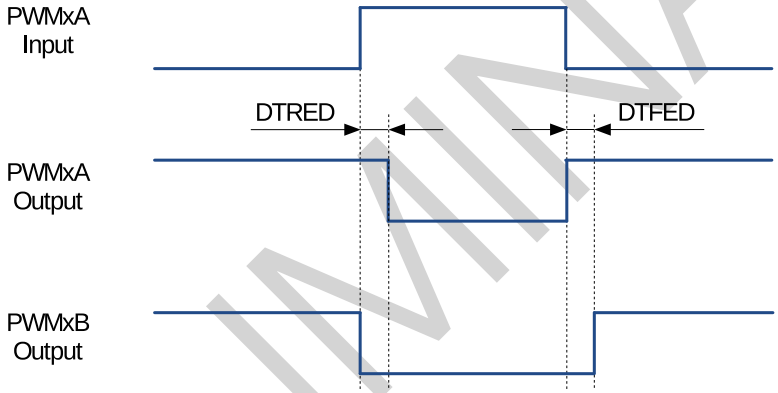


Figure 32-26. Active Low (AL) Dead Time Waveforms

Rising edge (RED) and falling edge (FED) delays may be set up independently. The delay value is programmed using the 16-bit registers MCPWM_DT*x*_RED and MCPWM_DT*x*_FED. The register value represents the number of clock (DT_clk) periods by which a signal edge is delayed. DT_CLK can be selected from PWM_clk or PT_clk through register MCPWM_DT*x*_CLK_SEL.

To calculate the delay on falling edge (FED) and rising edge (RED), use the following formulas:

$$FED = MCPWM\_DTx\_FED \times T_{DT\_clk}$$

$$RED = MCPWM\_DTx\_RED \times T_{DT\_clk}$$

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32.3.3.3 PWM Carrier Submodule

The coupling of PWM output to a motor driver may need isolation with a transformer. Transformers deliver only AC signals, while the duty cycle of a PWM signal may range anywhere from 0% to 100%. The PWM carrier submodule passes such a PWM signal through a transformer by using a high frequency carrier to modulate the signal.

Function Overview

The following key characteristics of this submodule are configurable:

- Carrier frequency
- Pulse width of the first pulse
- Duty cycle of the second and the subsequent pulses
- Enabling/disabling the carrier function

Operational Highlights

The PWM carrier clock (PC_clk) is derived from PWM_clk. The frequency and duty cycle are configured by the MCPWM_CARRIER*x*_PRESCALE and MCPWM_CARRIER*x*_DUTY bits in the MCPWM_CARRIER*x*_CFG_REG register. The purpose of one-shot pulses is to provide high-energy impulse to reliably turn on the power switch. Subsequent pulses sustain the power-on status. The width of a one-shot pulse is configurable with the MCPWM_CARRIER*x*_OSHTWTH bits. Enabling/disabling of the carrier submodule is done with the MCPWM_CARRIER*x*_EN bit.

Waveform Examples

Figure 32-27 shows an example of waveforms, where a carrier is superimposed on original PWM pulses. This figure do not show the first one-shot pulse and the duty-cycle control. Related details are covered in the following two sections.

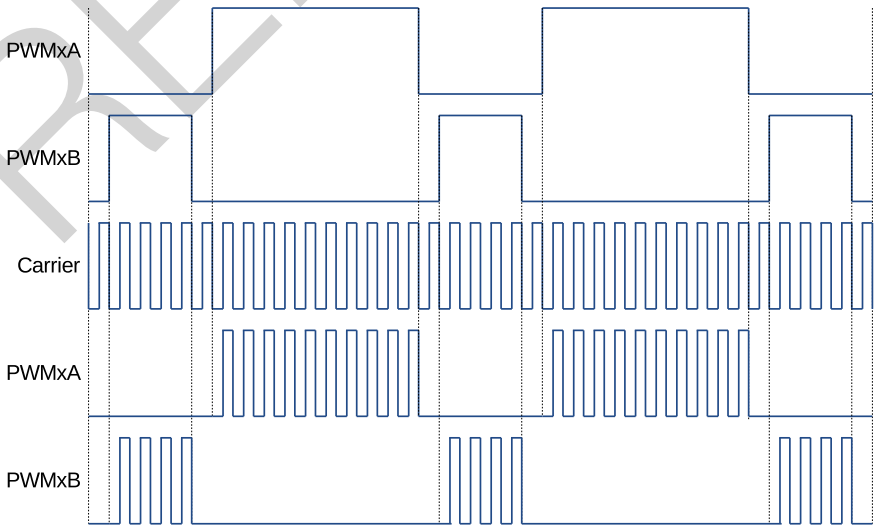


Figure 32-27. Example of Waveforms Showing PWM Carrier Action

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One-Shot Pulse

The width of the first pulse is configurable. It may assume one of 16 possible values and is described by the formula below:

$$T_{1stpulse} = T_{PWM\_clk} \times 8 \times (MCPWM\_CARRIERx\_PRESCALE + 1) \times (MCPWM\_CARRIERx\_OSHTWTH + 1)$$

Where:

- T_{PMW_clk} is the period of the PWM clock (PWM_clk).
- $(MCPWM\_CARRIERx\_OSHTWTH + 1)$ is the width of the first pulse (whose value ranges from 1 to 16).
- $(MCPWM\_CARRIERx\_PRESCALE + 1)$ is the PWM carrier clock's (PC_clk) prescaler value.

The first one-shot pulse and subsequent sustaining pulses are shown in Figure 32-28.

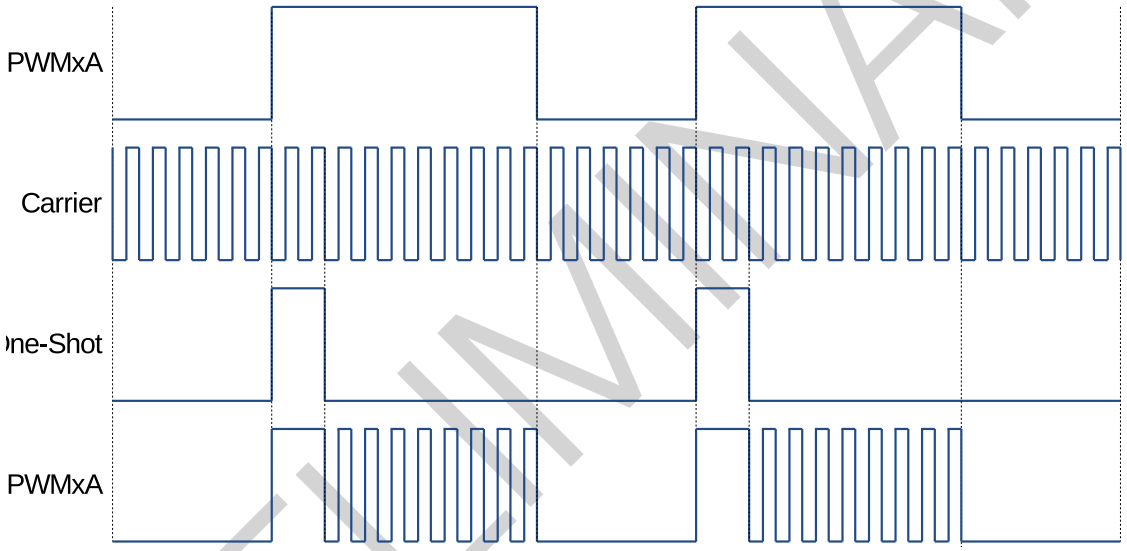


Figure 32-28. Example of the First Pulse and the Subsequent Sustaining Pulses of the PWM Carrier Sub-module

Duty Cycle Control

After issuing the first one-shot pulse, the remaining PWM signal is modulated according to the carrier frequency. Users can configure the duty cycle of this signal. Tuning of duty may be required, so that the signal passes through the isolating transformer and can still operate (turn on/off) the motor drive, changing rotation speed and direction.

The duty cycle may be set to one of seven values, using MCPWM_CARRIERx_DUTY, or bits [7:5] of register MCPWM_CARRIERx_CFG_REG.

Below is the formula for calculating the duty cycle:

$$Duty = MCPWM\_CARRIERx\_DUTY \div 8$$

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All seven settings of the duty cycle are shown in Figure 32-29.

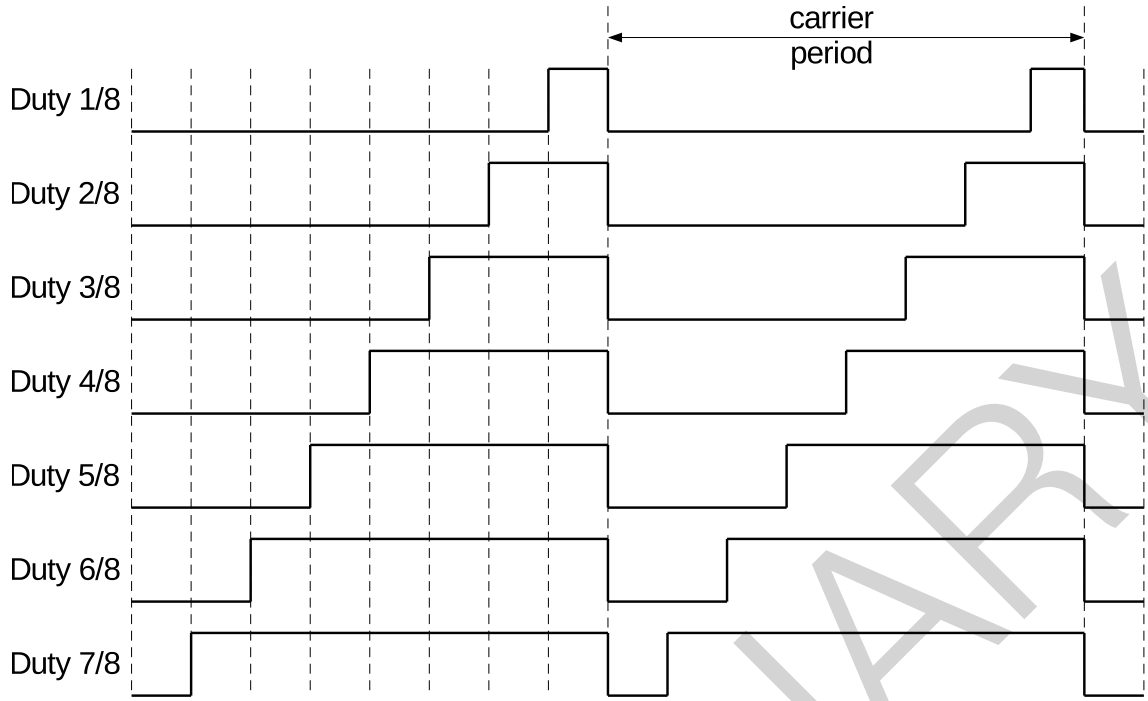


Figure 32-29. Possible Duty Cycle Settings for Sustaining Pulses in the PWM Carrier Submodule

32.3.3.4 Fault Handler Submodule

Each MCPWM peripheral is connected to three fault signals (FAULT0, FAULT1 and FAULT2) which are sourced from the GPIO matrix. These signals are intended to indicate external fault conditions, and may be preprocessed by the fault detection submodule to generate fault events. Fault events can then execute the user code to control MCPWM outputs in response to specific faults.

Function of Fault Handler Submodule

The key actions performed by the fault handler submodule are:

- Forcing outputs PWM*x*A and PWM*x*B, upon detected fault, to one of the following states:
  - High
  - Low
  - Toggle
  - No action taken
- Execution of one-shot trip (OST) upon detection of over-current conditions/short circuits.
- Cycle-by-cycle tripping (CBC) to provide current-limiting operation.
- Allocation of either one-shot or cycle-by-cycle operation for each fault signal.
- Generation of interrupts for each fault input.
- Support for software-force tripping.
- Enabling or disabling of submodule function as required.

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Operation and Configuration Tips

This section provides the operational tips and set-up options for the fault handler submodule.

Fault signals coming from pins are sampled and synced in the GPIO matrix. In order to guarantee the successful sampling of fault pulses, each pulse duration must be at least two APB clock cycles. The fault detection submodule will then sample fault signals by using PWM_clk. So, the duration of fault pulses coming from GPIO matrix must be at least one PWM_clk cycle. Differently put, regardless of the period relation between APB clock and PWM_clk, the width of fault signal pulses on pins must be at least equal to the sum of two APB clock cycles and one PWM_clk cycle.

Each level of fault signals, FAULT0 to FAULT2, can be used by the fault handler submodule to generate fault events (fault_event0 to fault_event2). Every fault event can be configured individually to provide CBC action, OST action, or none.

- **Cycle-by-Cycle (CBC) action:**
  When CBC action is triggered, the state of PWM*x*A and PWM*x*B will be changed immediately according to the configuration of fields MCPWM_FH*x*_A_CBC_U/D and MCPWM_FH*x*_B_CBC_U/D. Different actions can be indicted when the PWM timer is incrementing or decrementing. Different CBC action interrupts can be triggered for different fault events. Status field MCPWM_FH*x*_CBC_ON indicates whether a CBC action is on or off. When the fault event is no longer present, CBC actions on PWM*x*A/B will be cleared at a specified point, which is either a D/UTEP or D/UTEZ event. Field MCPWM_FH*x*_CBCPULSE determines at which event PWM*x*A and PWM*x*B will be able to resume normal actions. Therefore, in this mode, the CBC action is cleared or refreshed upon every PWM cycle.
- **One-Shot (OST) action:**
  When OST action is triggered, the state of PWM*x*A and PWM*x*B will be changed immediately, depending on the setting of fields MCPWM_FH*x*_A_OST_U/D and MCPWM_FH*x*_B_OST_U/D. Different actions can be configured when PWM timer is incrementing or decrementing. Different OST action interrupts can be triggered form different fault events. Status field MCPWM_FH*x*_OST_ON indicates whether an OST action is on or off. The OST actions on PWM*x*A/B are not automatically cleared when the fault event is no longer present. One-shot actions must be cleared manually by setting the rising edge of the MCPWM_FH*x*_CLR_OST bit.

32.3.4 Capture Submodule

32.3.4.1 Introduction

The capture submodule contains three complete capture channels. Channel inputs CAP0, CAP1 and CAP2 are sourced from the GPIO matrix. Thanks to the flexibility of the GPIO matrix, CAP0, CAP1 and CAP2 can be configured from any pin input. Multiple capture channels can be sourced from the same pin input, while prescaling for each channel can be set differently. Also, capture channels are sourced from different pins. This provides several options for handling capture signals by hardware in the background, instead of having them processed directly by the CPU. A capture submodule has the following independent key resources:

- One 32-bit timer (counter) which can be synchronized with the PWM timer, another submodule or software.
- Three capture channels, each equipped with a 32-bit time-stamp and a capture prescaler.
- Independent edge polarity (rising/falling edge) selection for any capture channel.
- Input capture signal prescaling (from 1 to 256).

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- Interrupt capabilities on any of the three capture events.

32.3.4.2 Capture Timer

The capture timer is a 32-bit counter incrementing continuously. It is enabled by setting MCPWM_CAP_TIMER_EN to 1. Its operating clock source is APB_CLK. When MCPWM_CAP_SYNCI_EN is configured, the counter will be loaded with phase stored in register MCPWM_CAP_TIMER_PHASE_REG at the time of a sync event. Sync events can select from PWM timers sync-out, PWM module sync-in by configuring MCPWM_CAP_SYNCI_SEL. Sync event can also generate by setting MCPWM_CAP_SYNC_SW. The capture timer provides timing references for all three capture channels.

32.3.4.3 Capture Channel

The capture signal coming to a capture channel will be inverted first, if needed, and then prescaled. Each capture channel has a prescaler register of MCPWM_CAP*x*_PRESCALE. Finally, specified edges of preprocessed capture signal will trigger capture events. Setting MCPWM_CAP*x*_EN to enable a capture channel. The capture event occurs at the time selected by the MCPWM_CAP*x*_MODE. When a capture event occurs, the capture timer's value is stored in time-stamp register MCPWM_CAP_CH*x*_REG. Different interrupts can be generated for different capture channels at capture events. The edge that triggers a capture event is recorded in register MCPWM_CAP*x*_EDGE. The capture event can be also forced by software setting MCPWM_CAP*x*_SW.

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32.4 Register Summary

The addresses in this section are relative to Motor Control PWM0 and Motor Control PWM1 base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Name	Description	Address	Access
Prescaler configuration			
MCPWM_CLK_CFG_REG	PWM clock prescaler register	0x0000	R/W
PWM Timer 0 Configuration and status			
MCPWM_TIMER0_CFG0_REG	PWM timer0 period and update method configuration register	0x0004	R/W
MCPWM_TIMER0_CFG1_REG	PWM timer0 working mode and start/stop control configuration register	0x0008	R/W
MCPWM_TIMER0_SYNC_REG	PWM timer0 sync function configuration register	0x000C	R/W
MCPWM_TIMER0_STATUS_REG	PWM timer0 status register	0x0010	RO
PWM Timer 1 Configuration and Status			
MCPWM_TIMER1_CFG0_REG	PWM timer1 period and update method configuration register	0x0014	R/W
MCPWM_TIMER1_CFG1_REG	PWM timer1 working mode and start/stop control configuration register	0x0018	varies
MCPWM_TIMER1_SYNC_REG	PWM timer1 sync function configuration register	0x001C	R/W
MCPWM_TIMER1_STATUS_REG	PWM timer1 status register	0x0020	RO
PWM Timer 2 Configuration and status			
MCPWM_TIMER2_CFG0_REG	PWM timer2 period and update method configuration register	0x0024	R/W
MCPWM_TIMER2_CFG1_REG	PWM timer2 working mode and start/stop control configuration register	0x0028	varies
MCPWM_TIMER2_SYNC_REG	PWM timer2 sync function configuration register	0x002C	R/W
MCPWM_TIMER2_STATUS_REG	PWM timer2 status register	0x0030	RO
Common configuration for PWM timers			
MCPWM_TIMER_SYNCI_CFG_REG	Synchronization input selection for three PWM timers	0x0034	R/W
MCPWM_OPERATOR_TIMERSEL_REG	Select specific timer for PWM operators	0x0038	R/W
PWM Operator 0 Configuration and Status			
MCPWM_GEN0_STMP_CFG_REG	Transfer status and update method for time stamp registers A and B	0x003C	varies
MCPWM_GEN0_TSTMP_A_REG	PWM generator 0 shadow register for timer stamp A	0x0040	R/W
MCPWM_GEN0_TSTMP_B_REG	PWM generator 0 shadow register for timer stamp B	0x0044	R/W
MCPWM_GEN0_CFG0_REG	PWM generator 0 event T0 and T1 handling	0x0048	R/W
MCPWM_GEN0_FORCE_REG	Permissive to force PWM0A and PWM0B outputs by software	0x004C	R/W
MCPWM_GEN0_A_REG	Actions triggered by events on PWM0A	0x0050	R/W
MCPWM_GEN0_B_REG	Actions triggered by events on PWM0B	0x0054	R/W

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Name	Description	Address	Access
MCPWM_DT0_CFG_REG	PWM generator 0 dead time type selection and configuration	0x0058	R/W
MCPWM_DT0_FED_CFG_REG	PWM generator 0 shadow register for falling edge delay (FED)	0x005C	R/W
MCPWM_DT0_RED_CFG_REG	PWM generator 0 shadow register for rising edge delay (RED)	0x0060	R/W
MCPWM_CARRIER0_CFG_REG	PWM generator 0 carrier enable and configuration	0x0064	R/W
MCPWM_FH0_CFG0_REG	Actions on PWM0A and PWM0B on trip events	0x0068	R/W
MCPWM_FH0_CFG1_REG	Software triggers for fault handler actions	0x006C	R/W
MCPWM_FH0_STATUS_REG	Status of fault events	0x0070	RO
PWM Operator 1 Configuration and Status			
MCPWM_GEN1_STMP_CFG_REG	Transfer status and update method for time stamp registers A and B	0x0074	varies
MCPWM_GEN1_TSTMP_A_REG	PWM generator 1 shadow register for timer stamp A	0x0078	R/W
MCPWM_GEN1_TSTMP_B_REG	PWM generator 1 shadow register for timer stamp B	0x007C	R/W
MCPWM_GEN1_CFG0_REG	PWM generator 1 event T0 and T1 handling	0x0080	R/W
MCPWM_GEN1_FORCE_REG	Permissive to force PWM1A and PWM1B outputs by software	0x0084	R/W
MCPWM_GEN1_A_REG	Actions triggered by events on PWM1A	0x0088	R/W
MCPWM_GEN1_B_REG	Actions triggered by events on PWM1B	0x008C	R/W
MCPWM_DT1_CFG_REG	PWM generator 1 dead time type selection and configuration	0x0090	R/W
MCPWM_DT1_FED_CFG_REG	PWM generator 1 shadow register for falling edge delay (FED)	0x0094	R/W
MCPWM_DT1_RED_CFG_REG	PWM generator 1 shadow register for rising edge delay (RED)	0x0098	R/W
MCPWM_CARRIER1_CFG_REG	PWM generator 1 carrier enable and configuration	0x009C	R/W
MCPWM_FH1_CFG0_REG	Actions on PWM1A and PWM1B trip events	0x00A0	R/W
MCPWM_FH1_CFG1_REG	Software triggers for fault handler actions	0x00A4	R/W
MCPWM_FH1_STATUS_REG	Status of fault events	0x00A8	RO
PWM Operator 2 Configuration and Status			
MCPWM_GEN2_STMP_CFG_REG	Transfer status and update method for time stamp registers A and B	0x00AC	varies
MCPWM_GEN2_TSTMP_A_REG	PWM generator 2 shadow register for timer stamp A	0x00B0	R/W
MCPWM_GEN2_TSTMP_B_REG	PWM generator 2 shadow register for timer stamp B	0x00B4	R/W
MCPWM_GEN2_CFG0_REG	PWM generator 2 event T0 and T1 handling	0x00B8	R/W
MCPWM_GEN2_FORCE_REG	Permissive to force PWM2A and PWM2B outputs by software	0x00BC	R/W

PRELIMINARY

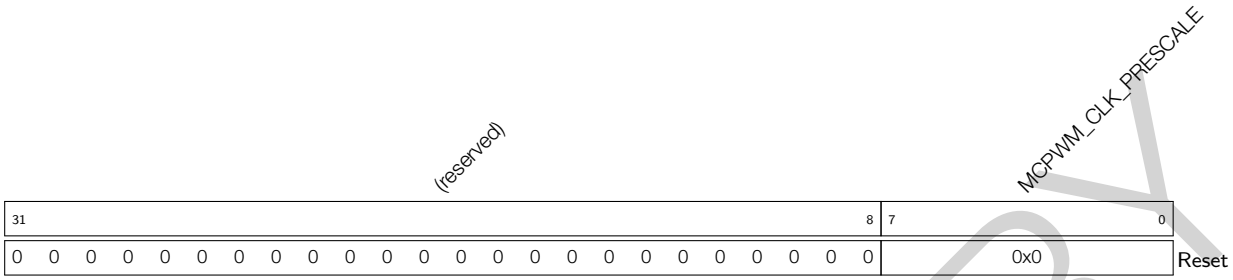
Name	Description	Address	Access
MCPWM_GEN2_A_REG	Actions triggered by events on PWM2A	0x00C0	R/W
MCPWM_GEN2_B_REG	Actions triggered by events on PWM2B	0x00C4	R/W
MCPWM_DT2_CFG_REG	PWM generator 2 dead time type selection and configuration	0x00C8	R/W
MCPWM_DT2_FED_CFG_REG	PWM generator 2 shadow register for falling edge delay (FED)	0x00CC	R/W
MCPWM_DT2_RED_CFG_REG	PWM generator 2 shadow register for rising edge delay (RED)	0x00D0	R/W
MCPWM_CARRIER2_CFG_REG	PWM generator 2 carrier enable and configuration	0x00D4	R/W
MCPWM_FH2_CFG0_REG	Actions on PWM2A and PWM2B trip events	0x00D8	R/W
MCPWM_FH2_CFG1_REG	Software triggers for fault handler actions	0x00DC	R/W
MCPWM_FH2_STATUS_REG	Status of fault events	0x00E0	RO
Fault Detection Configuration and Status			
MCPWM_FAULT_DETECT_REG	Fault detection configuration and status	0x00E4	varies
Capture Configuration and Status			
MCPWM_CAP_TIMER_CFG_REG	Configure capture timer	0x00E8	varies
MCPWM_CAP_TIMER_PHASE_REG	Phase for capture timer sync	0x00EC	R/W
MCPWM_CAP_CH0_CFG_REG	Capture channel 0 configuration and enable	0x00F0	varies
MCPWM_CAP_CH1_CFG_REG	Capture channel 1 configuration and enable	0x00F4	varies
MCPWM_CAP_CH2_CFG_REG	Capture channel 2 configuration and enable	0x00F8	varies
MCPWM_CAP_CH0_REG	Ch0 capture value status register	0x00FC	RO
MCPWM_CAP_CH1_REG	Ch1 capture value status register	0x0100	RO
MCPWM_CAP_CH2_REG	ch2 capture value status register	0x0104	RO
MCPWM_CAP_STATUS_REG	Edge of last capture trigger	0x0108	RO
Enable update of active registers			
MCPWM_UPDATE_CFG_REG	Enable update	0x010C	R/W
Manage Interrupts			
MCPWM_INT_ENA_REG	Interrupt enable bits	0x0110	R/W
MCPWM_INT_RAW_REG	Raw interrupt status	0x0114	R/WTC/SS
MCPWM_INT_ST_REG	Masked interrupt status	0x0118	RO
MCPWM_INT_CLR_REG	Interrupt clear bits	0x011C	WT
MCPWM APB Configuration Register			
MCPWM_CLK_REG	MCPWM APB configuration register	0x0120	R/W
Version Register			
MCPWM_VERSION_REG	Version control register	0x0124	R/W

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32.5 Registers

The addresses in this section are relative to Motor Control PWM0 and Motor Control PWM1 base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 32.1. MCPWM_CLK_CFG_REG (0x0000)



MCPWM_CLK_PRESCALE Period of PWM_clk = 6.25ns * (PWM_CLK_PRESCALE + 1). (R/W)

Register 32.2. MCPWM_TIMER0_CFG0_REG (0x0004)



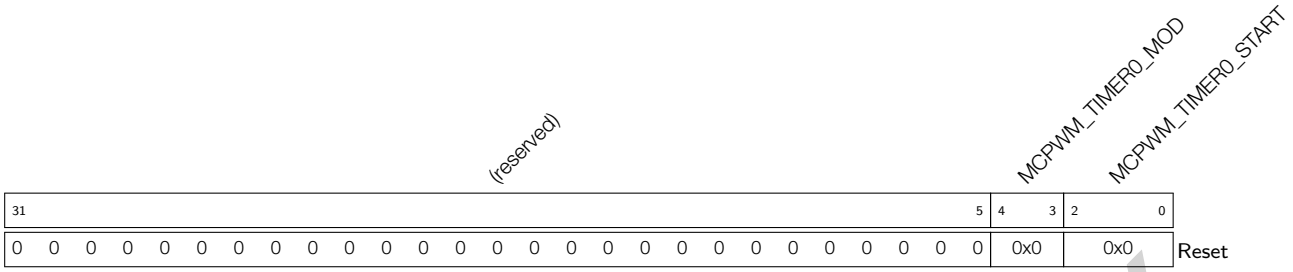
MCPWM_TIMER0_PRESCALE Period of PT0_clk = Period of PWM_clk * (PWM_TIMER0_PRESCALE + 1). (R/W)

MCPWM_TIMER0_PERIOD Period shadow register of PWM timer0. (R/W)

MCPWM_TIMER0_PERIOD_UPMETHOD Update method for active register of PWM timer0 period. 0: immediate; 1: TEZ; 2: sync; 3: TEZ | sync. TEZ here and below means timer equal zero event. (R/W)

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Register 32.3. MCPWM_TIMER0_CFG1_REG (0x0008)



MCPWM_TIMER0_START PWM timer0 start and stop control. (R/W/SC)

- 0: if PWM timer0 starts, then stops at TEZ;
- 1: if timer0 starts, then stops at TEP;
- 2: PWM timer0 starts and runs on;
- 3: timer0 starts and stops at the next TEZ;
- 4: timer0 starts and stops at the next TEP.

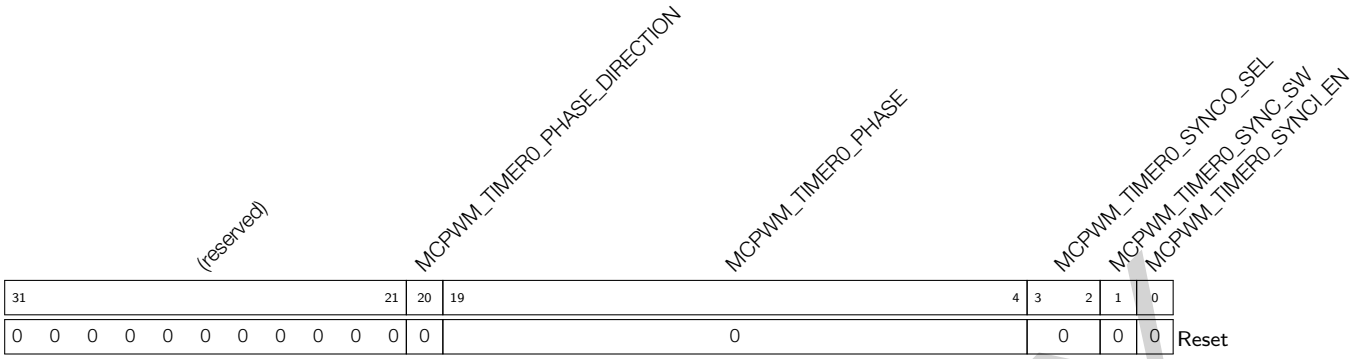
TEP here and below means the event that happens when the timer equals to period.

MCPWM_TIMER0_MOD PWM timer0 working mode. (R/W)

- 0: freeze;
- 1: increase mode
- 2: decrease mode
- 3: up-down mode.

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Register 32.4. MCPWM_TIMER0_SYNC_REG (0x000C)



MCPWM_TIMER0_SYNCI_EN When set, timer reloading with phase on sync input event is enabled. (R/W)

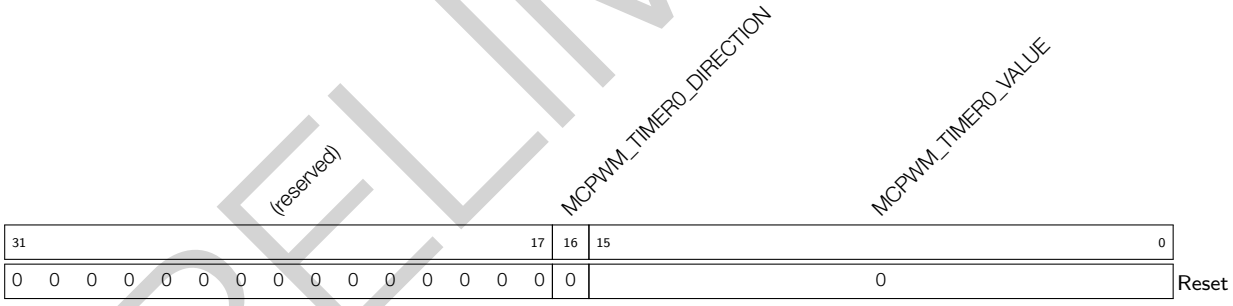
MCPWM_TIMER0_SYNC_SW Toggling this bit will trigger a software sync. (R/W)

MCPWM_TIMER0_SYNCO_SEL PWM timer0 sync_out selection, 0: sync_in; 1: TEZ; 2: TEP. The sync_out will always generate when toggling the MCPWM_TIMER0_SYNC_SW bit. (R/W)

MCPWM_TIMER0_PHASE Phase for timer reload on sync event. (R/W)

MCPWM_TIMER0_PHASE_DIRECTION Configure the PWM timer0's direction when timer0 mode is up-down mode. 0: increase; 1: decrease. (R/W)

Register 32.5. MCPWM_TIMER0_STATUS_REG (0x0010)

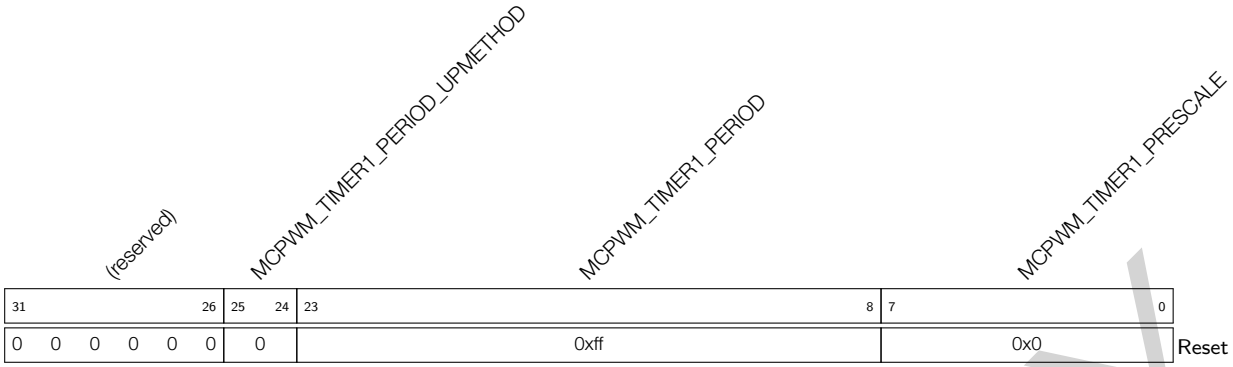


MCPWM_TIMER0_VALUE Current PWM timer0 counter value. (RO)

MCPWM_TIMER0_DIRECTION Current PWM timer0 counter direction. 0: increment; 1: decrement. (RO)

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Register 32.6. MCPWM_TIMER1_CFG0_REG (0x0014)

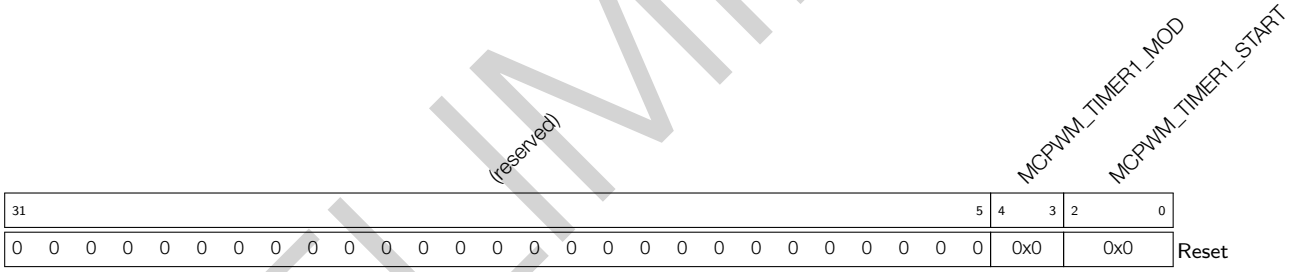


MCPWM_TIMER1_PRESCALE Period of PT0_clk = Period of PWM_clk * (PWM_timer1_PRESCALE + 1). (R/W)

MCPWM_TIMER1_PERIOD Period shadow register of PWM timer1. (R/W)

MCPWM_TIMER1_PERIOD_UPMETHOD Update method for active register of PWM timer1 period, 0: immediate, 1: TEZ, 2: sync, 3: TEZ | sync. TEZ here and below means timer equal zero event. (R/W)

Register 32.7. MCPWM_TIMER1_CFG1_REG (0x0018)



MCPWM_TIMER1_START PWM timer1 start and stop control. (R/W/SC)

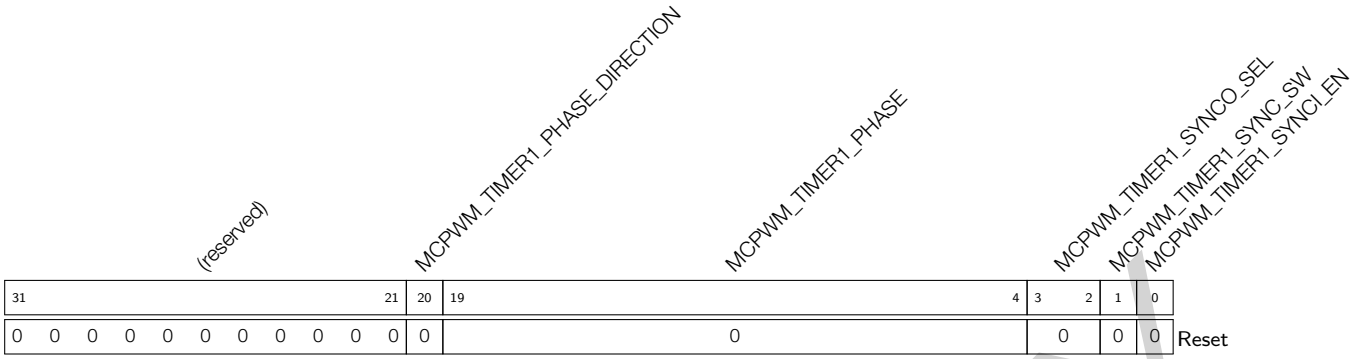
- 0: if PWM timer1 starts, then stops at TEZ;
- 1: if timer1 starts, then stops at TEP;
- 2: PWM timer1 starts and runs on;
- 3: timer1 starts and stops at the next TEZ;
- 4: timer1 starts and stops at the next TEP.

TEP here and below means the event that happens when the timer equals to period.

MCPWM_TIMER1_MOD PWM timer1 working mode. 0: freeze; 1: increase mode; 2: decrease mode; 3: up-down mode. (R/W)

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Register 32.8. MCPWM_TIMER1_SYNC_REG (0x001C)



MCPWM_TIMER1_SYNCI_EN When set, timer reloading with phase on sync input event is enabled. (R/W)

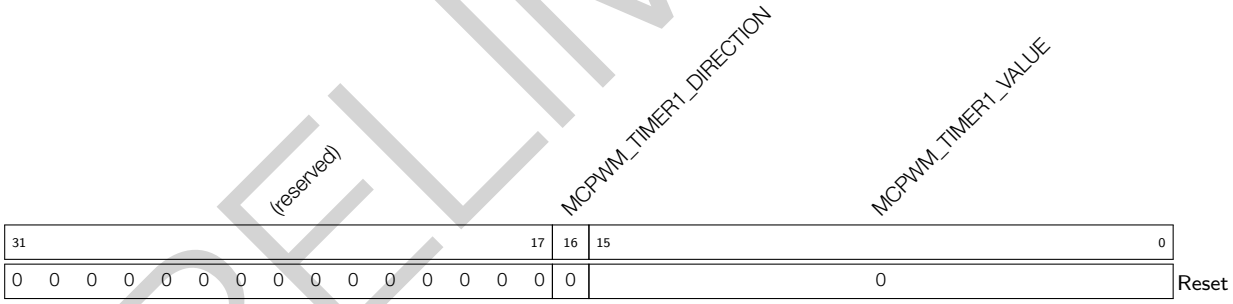
MCPWM_TIMER1_SYNC_SW Toggling this bit will trigger a software sync. (R/W)

MCPWM_TIMER1_SYNCO_SEL PWM timer1 sync_out selection. 0: sync_in; 1: TEZ; 2: TEP. The sync_out will always generate when toggling the reg_timer1_sync_sw bit. (R/W)

MCPWM_TIMER1_PHASE Phase for timer reload on sync event. (R/W)

MCPWM_TIMER1_PHASE_DIRECTION Configure the PWM timer1's direction when timer1 is in up-down mode. 0: increase; 1: decrease. (R/W)

Register 32.9. MCPWM_TIMER1_STATUS_REG (0x0020)

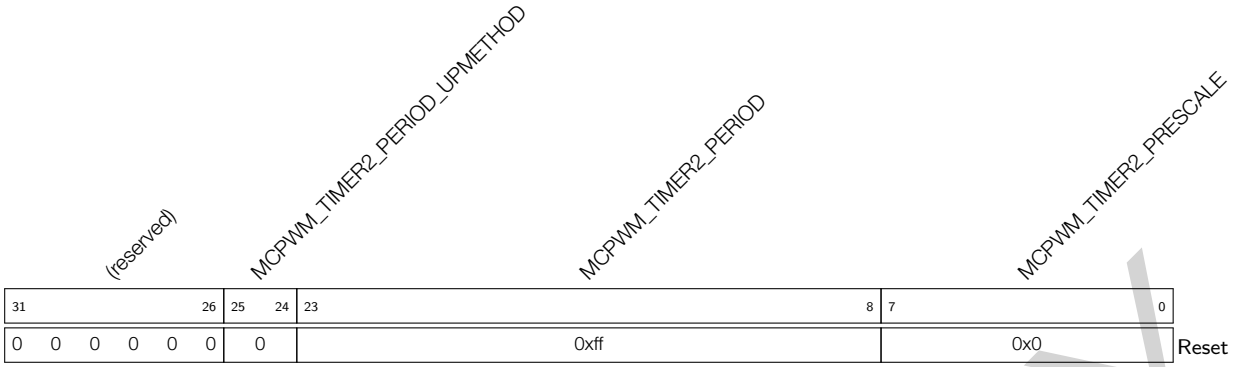


MCPWM_TIMER1_VALUE Current value of PWM timer1 counter. (RO)

MCPWM_TIMER1_DIRECTION Current direction of PWM timer1 counter. 0: increment; 1: decrement. (RO)

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Register 32.10. MCPWM_TIMER2_CFG0_REG (0x0024)



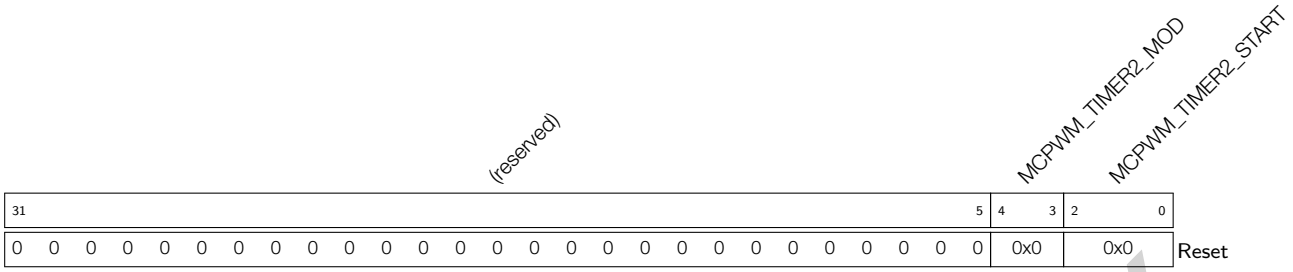
MCPWM_TIMER2_PRESCALE Period of PT0_clk = Period of PWM_clk * (PWM_timer2_PRESCALE + 1). (R/W)

MCPWM_TIMER2_PERIOD Period shadow register of PWM timer2. (R/W)

MCPWM_TIMER2_PERIOD_UPMETHOD Update method for active register of PWM timer2 period. 0: immediate; 1: TEZ; 2: sync; 3: TEZ | sync. TEZ here and below means timer equal zero event. (R/W)

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Register 32.11. MCPWM_TIMER2_CFG1_REG (0x0028)



MCPWM_TIMER2_START PWM timer2 start and stop control. (R/W/SC)

- 0: if PWM timer2 starts, then stops at TEZ;
- 1: if timer2 starts, then stops at TEP;
- 2: PWM timer2 starts and runs on;
- 3: timer2 starts and stops at the next TEZ;
- 4: timer2 starts and stops at the next TEP.

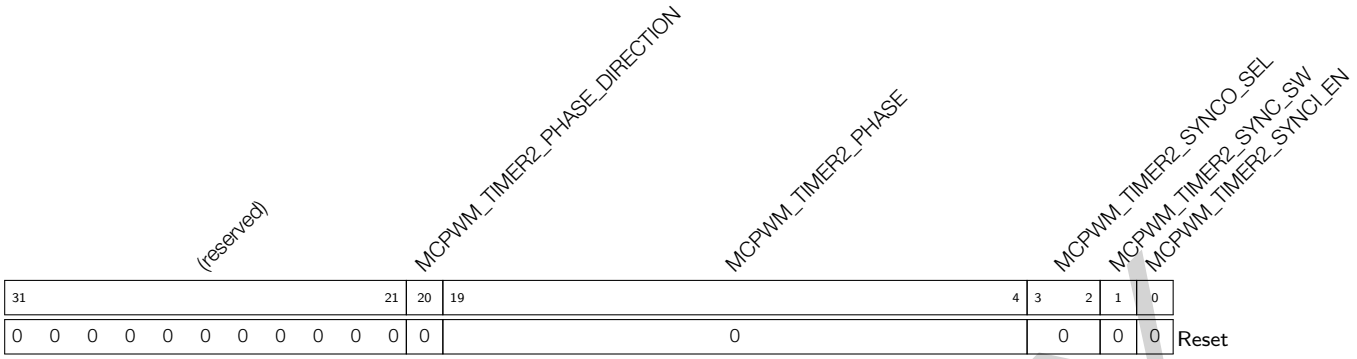
TEP here and below means the event that happens when the timer equals to period.

MCPWM_TIMER2_MOD PWM timer2 working mode. (R/W)

- 0: freeze;
- 1: increase mode;
- 2: decrease mode;
- 3: up-down mode.

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Register 32.12. MCPWM_TIMER2_SYNC_REG (0x002C)



MCPWM_TIMER2_SYNCI_EN When set, timer reloading with phase on sync input event is enabled. (R/W)

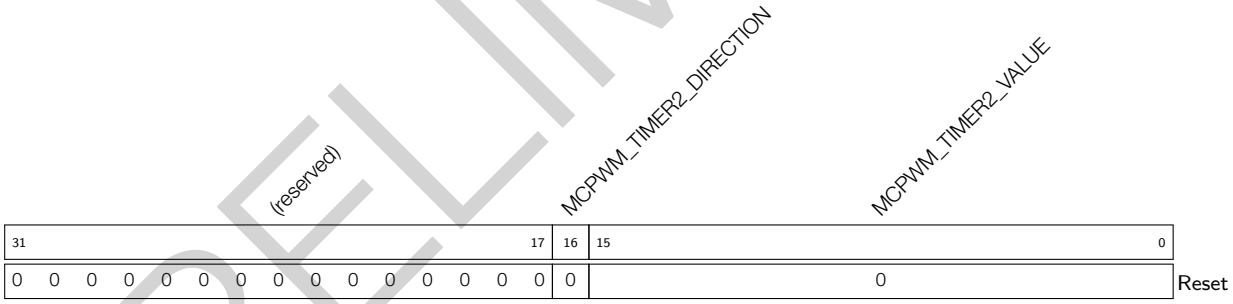
MCPWM_TIMER2_SYNC_SW Toggling this bit will trigger a software sync. (R/W)

MCPWM_TIMER2_SYNCO_SEL PWM timer2 sync_out selection. 0: sync_in; 1: TEZ; 2: TEP. The sync_out will always generate when toggling the reg_timer2_sync_sw bit. (R/W)

MCPWM_TIMER2_PHASE Phase for timer reload on sync event. (R/W)

MCPWM_TIMER2_PHASE_DIRECTION Configure the PWM timer2's direction when timer2 mode is up-down mode. 0: increase; 1: decrease. (R/W)

Register 32.13. MCPWM_TIMER2_STATUS_REG (0x0030)

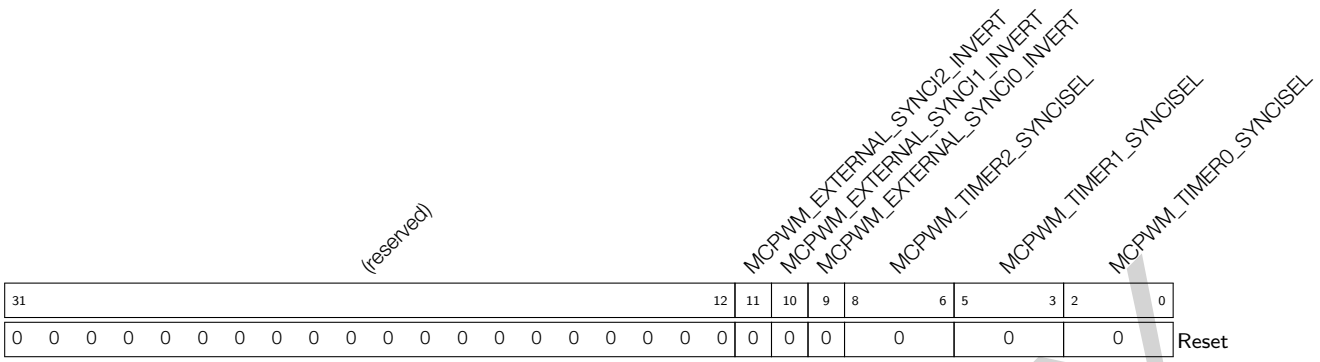


MCPWM_TIMER2_VALUE Current value of PWM timer2 counter. (RO)

MCPWM_TIMER2_DIRECTION Current direction of PWM timer2 counter. 0: increment; 1: decrement. (RO)

PRELIMINARY

Register 32.14. MCPWM_TIMER_SYNCI_CFG_REG (0x0034)



MCPWM_TIMER0_SYNCISEL Select sync input for PWM timer0. (R/W)

- 1: PWM timer0 sync_out;
- 2: PWM timer1 sync_out;
- 3: PWM timer2 sync_out;
- 4: SYNC0 from GPIO matrix;
- 5: SYNC1 from GPIO matrix;
- 6: SYNC2 from GPIO matrix;
- Other values: no sync input selected.

MCPWM_TIMER1_SYNCISEL Select sync input for PWM timer1. (R/W)

- 1: PWM timer0 sync_out;
- 2: PWM timer1 sync_out;
- 3: PWM timer2 sync_out;
- 4: SYNC0 from GPIO matrix;
- 5: SYNC1 from GPIO matrix;
- 6: SYNC2 from GPIO matrix;
- Other values: no sync input selected.

Continued on the next page...

PRELIMINARY

Register 32.14. MCPWM_TIMER_SYNCI_CFG_REG (0x0034)

Continued from the previous page...

MCPWM_TIMER2_SYNCISEL Select sync input for PWM timer2. (R/W)

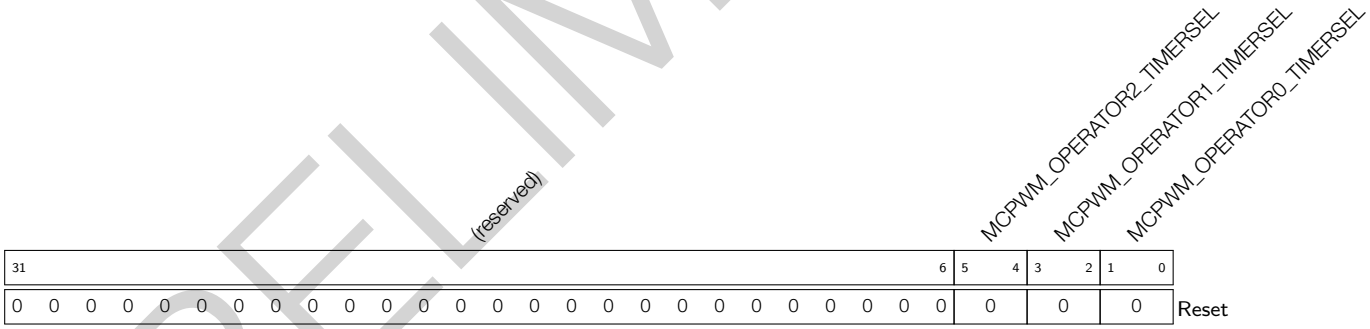
- 1: PWM timer0 sync_out;
- 2: PWM timer1 sync_out;
- 3: PWM timer2 sync_out;
- 4: SYNC0 from GPIO matrix;
- 5: SYNC1 from GPIO matrix;
- 6: SYNC2 from GPIO matrix
- Other values: no sync input selected.

MCPWM_EXTERNAL_SYNCI0_INVERT Invert SYNC0 from GPIO matrix. (R/W)

MCPWM_EXTERNAL_SYNCI1_INVERT Invert SYNC1 from GPIO matrix. (R/W)

MCPWM_EXTERNAL_SYNCI2_INVERT Invert SYNC2 from GPIO matrix. (R/W)

Register 32.15. MCPWM_OPERATOR_TIMERSEL_REG (0x0038)



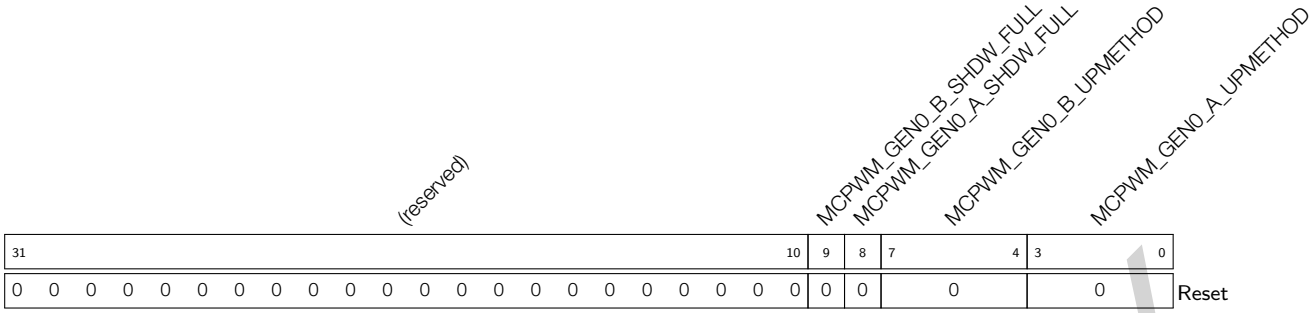
MCPWM_OPERATOR0_TIMERSEL Select which PWM timer's is the timing reference for PWM operator0. 0: timer0; 1: timer1; 2: timer2. (R/W)

MCPWM_OPERATOR1_TIMERSEL Select which PWM timer's is the timing reference for PWM operator1. 0: timer0; 1: timer1; 2: timer2. (R/W)

MCPWM_OPERATOR2_TIMERSEL Select which PWM timer's is the timing reference for PWM operator2. 0: timer0; 1: timer1; 2: timer2. (R/W)

PRELIMINARY

Register 32.16. MCPWM_GEN0_STMP_CFG_REG (0x003C)



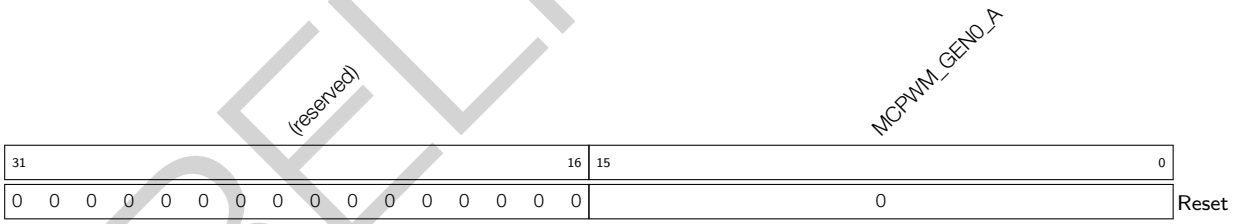
MCPWM_GEN0_A_UPMETHOD Update method for PWM generator 0 time stamp A's active register. When all bits are set to 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1: TEP; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_GEN0_B_UPMETHOD Update method for PWM generator 0 time stamp B's active register. When all bits are set to 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1: TEP; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_GEN0_A_SHDW_FULL Set and reset by hardware. If set, PWM generator 0 time stamp A's shadow reg is filled and waiting to be transferred to A's active reg; if cleared, A's active reg has been updated with shadow register latest value. (R/WTC/SC)

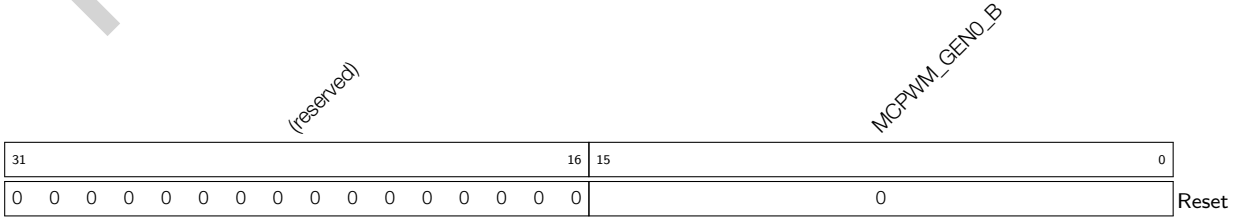
MCPWM_GEN0_B_SHDW_FULL Set and reset by hardware. If set, PWM generator 0 time stamp B's shadow reg is filled and waiting to be transferred to B's active reg; if cleared, B's active reg has been updated with shadow register latest value. (R/WTC/SC)

Register 32.17. MCPWM_GEN0_TSTMP_A_REG (0x0040)



MCPWM_GEN0_A PWM generator 0 time stamp A's shadow register. (R/W)

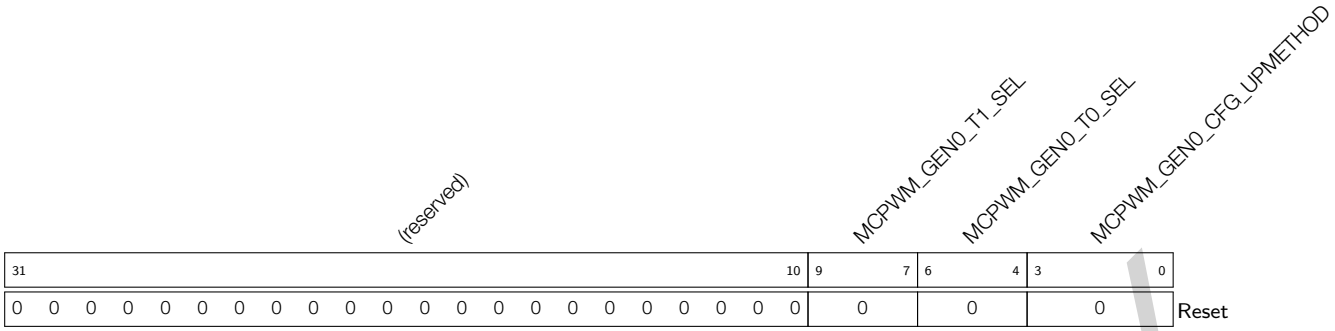
Register 32.18. MCPWM_GEN0_TSTMP_B_REG (0x0044)



MCPWM_GEN0_B PWM generator 0 time stamp B's shadow register. (R/W)

PRELIMINARY

Register 32.19. MCPWM_GEN0_CFG0_REG (0x0048)



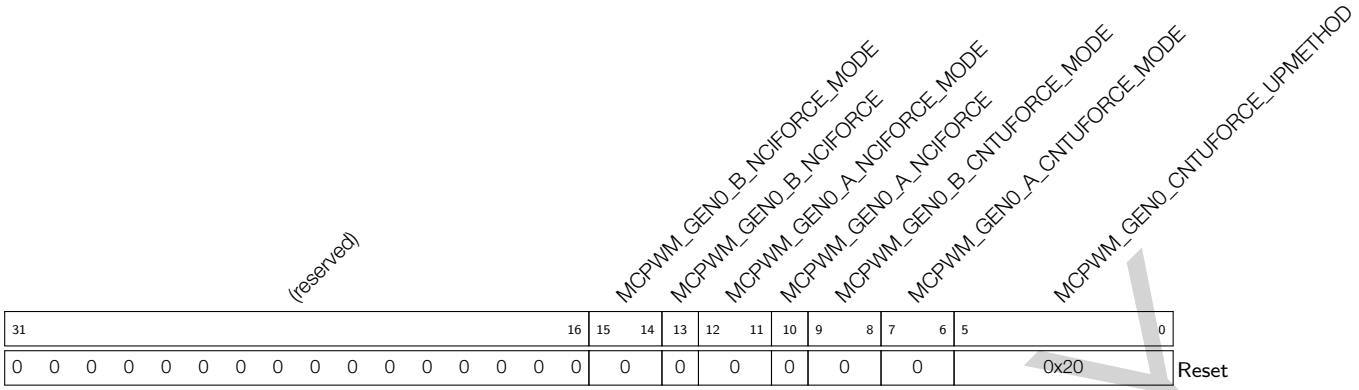
MCPWM_GEN0_CFG_UPMETHOD Update method for PWM generator 0's active register of configuration. When all bits are set to 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1:TEP; when bit2 is set to 1:sync; when bit3 is set to 1:disable the update. (R/W)

MCPWM_GEN0_T0_SEL Source selection for PWM generator 0 event_t0, take effect immediately, 0: fault_event0, 1: fault_event1, 2: fault_event2, 3: sync_taken, 4: none. (R/W)

MCPWM_GEN0_T1_SEL Source selection for PWM generator 0 event_t1, take effect immediately, 0: fault_event0, 1: fault_event1, 2: fault_event2, 3: sync_taken, 4: none. (R/W)

PRELIMINARY

Register 32.20. MCPWM_GEN0_FORCE_REG (0x004C)



MCPWM_GEN0_CNTUFORCE_UPMETHOD Updating method for continuous software force of PWM generator0. When all bits are set to 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1: TEP; when bit2 is set to 1: TEA; when bit3 is set to 1: TEB; when bit4 is set to 1: sync; when bit5 is set to 1: disable update. (TEA/B here and below means an event generated when the timer's value equals to that of register A/B.) (R/W)

MCPWM_GEN0_A_CNTUFORCE_MODE Continuous software force mode for PWM0A. 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

MCPWM_GEN0_B_CNTUFORCE_MODE Continuous software force mode for PWM0B. 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

MCPWM_GEN0_A_NCIFORCE Trigger of non-continuous immediate software-force event for PWM0A, a toggle will trigger a force event. (R/W)

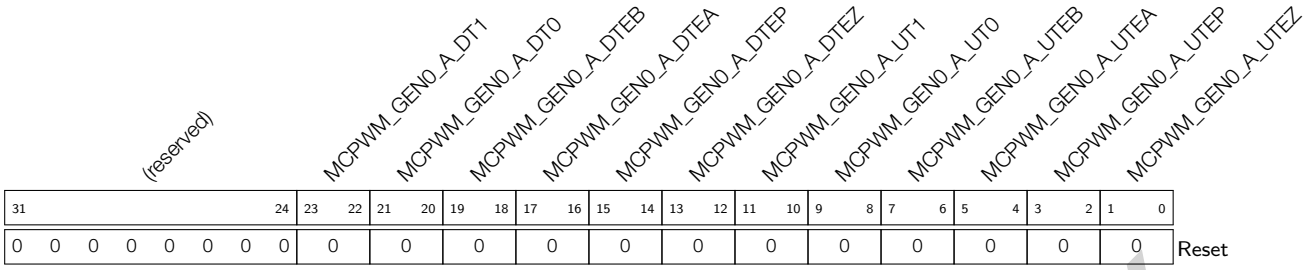
MCPWM_GEN0_A_NCIFORCE_MODE Non-continuous immediate software force mode for PWM0A. 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

MCPWM_GEN0_B_NCIFORCE Trigger of non-continuous immediate software-force event for PWM0B, a toggle will trigger a force event. (R/W)

MCPWM_GEN0_B_NCIFORCE_MODE Non-continuous immediate software force mode for PWM0B. 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

PRELIMINARY

Register 32.21. MCPWM_GEN0_A_REG (0x0050)



MCPWM_GEN0_A_UTEZ Action on PWM0A triggered by event TEZ when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_A_UTEP Action on PWM0A triggered by event TEP when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_A_UTEA Action on PWM0A triggered by event TEA when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_A_UTEB Action on PWM0A triggered by event TEB when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_A_UT0 Action on PWM0A triggered by event_t0 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_A_UT1 Action on PWM0A triggered by event_t1 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_A_DTEZ Action on PWM0A triggered by event TEZ when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_A_DTEP Action on PWM0A triggered by event TEP when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_A_DTEA Action on PWM0A triggered by event TEA when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

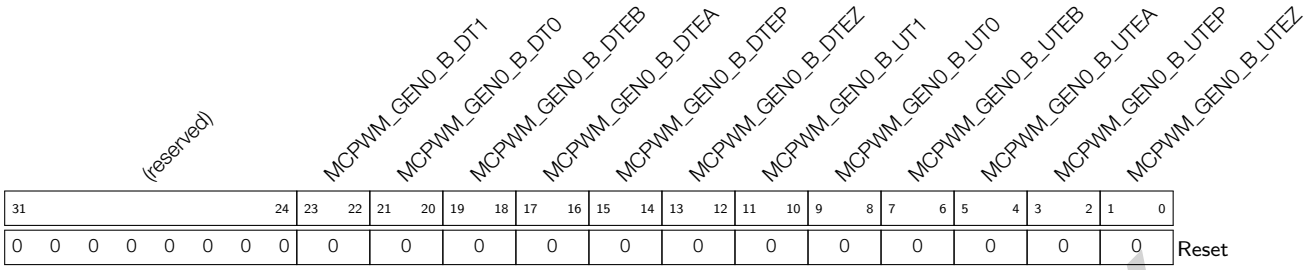
MCPWM_GEN0_A_DTEB Action on PWM0A triggered by event TEB when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_A_DT0 Action on PWM0A triggered by event_t0 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_A_DT1 Action on PWM0A triggered by event_t1 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

PRELIMINARY

Register 32.22. MCPWM_GEN0_B_REG (0x0054)



MCPWM_GEN0_B_UTEZ Action on PWM0B triggered by event TEZ when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_B_UTEP Action on PWM0B triggered by event TEP when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_B_UTEA Action on PWM0B triggered by event TEA when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_B_UTEB Action on PWM0B triggered by event TEB when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_B_UT0 Action on PWM0B triggered by event_t0 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_B_UT1 Action on PWM0B triggered by event_t1 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_B_DTEZ Action on PWM0B triggered by event TEZ when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_B_DTEP Action on PWM0B triggered by event TEP when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_B_DTEA Action on PWM0B triggered by event TEA when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

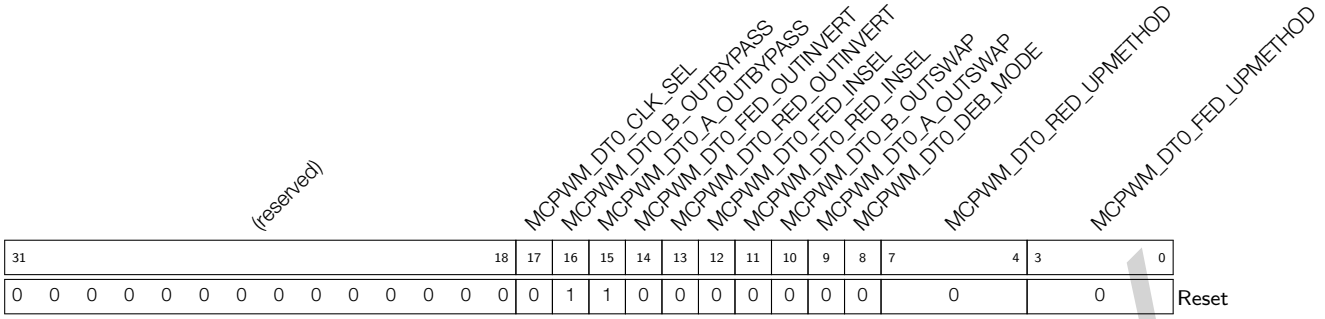
MCPWM_GEN0_B_DTEB Action on PWM0B triggered by event TEB when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_B_DT0 Action on PWM0B triggered by event_t0 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN0_B_DT1 Action on PWM0B triggered by event_t1 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

PRELIMINARY

Register 32.23. MCPWM_DT0_CFG_REG (0x0058)



MCPWM_DT0_FED_UPMETHOD Update method for FED (rising edge delay) active register. 0: immediate; when bit0 is set to 1: tez; when bit1 is set to 1: tep; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_DT0_RED_UPMETHOD Update method for RED (rising edge delay) active register. 0: immediate; when bit0 is set to 1: tez; when bit1 is set to 1: tep; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_DT0_DEB_MODE S8 in table 32-5, dual-edge B mode, 0: fed/red take effect on different path separately, 1: fed/red take effect on B path, A out is in bypass or dulpB mode (R/W)

MCPWM_DT0_A_OUTSWAP S6 in table 32-5. (R/W)

MCPWM_DT0_B_OUTSWAP S7 in table 32-5. (R/W)

MCPWM_DT0_RED_INSEL S4 in table 32-5. (R/W)

MCPWM_DT0_FED_INSEL S5 in table 32-5. (R/W)

MCPWM_DT0_RED_OUTINVERT S2 in table 32-5. (R/W)

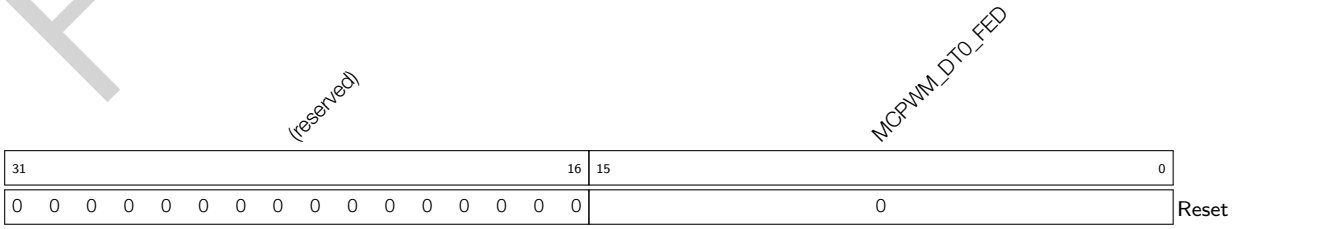
MCPWM_DT0_FED_OUTINVERT S3 in table 32-5. (R/W)

MCPWM_DT0_A_OUTBYPASS S1 in table 32-5. (R/W)

MCPWM_DT0_B_OUTBYPASS S0 in table 32-5. (R/W)

MCPWM_DT0_CLK_SEL Dead time generator 0 clock selection. 0: PWM_clk, 1: PT_clk. (R/W)

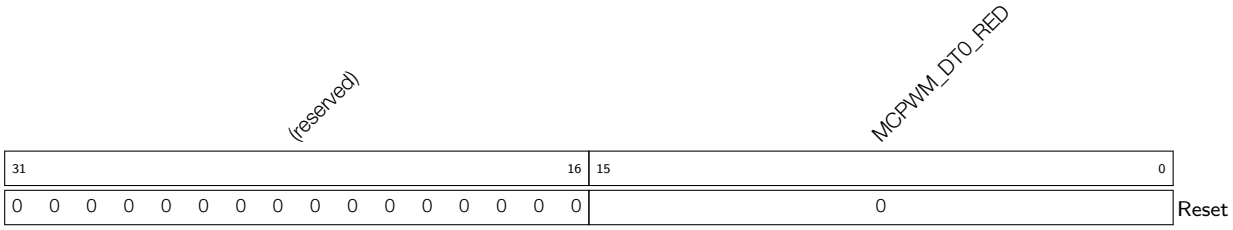
Register 32.24. MCPWM_DT0_FED_CFG_REG (0x005C)



MCPWM_DT0_FED Shadow register for FED. (R/W)

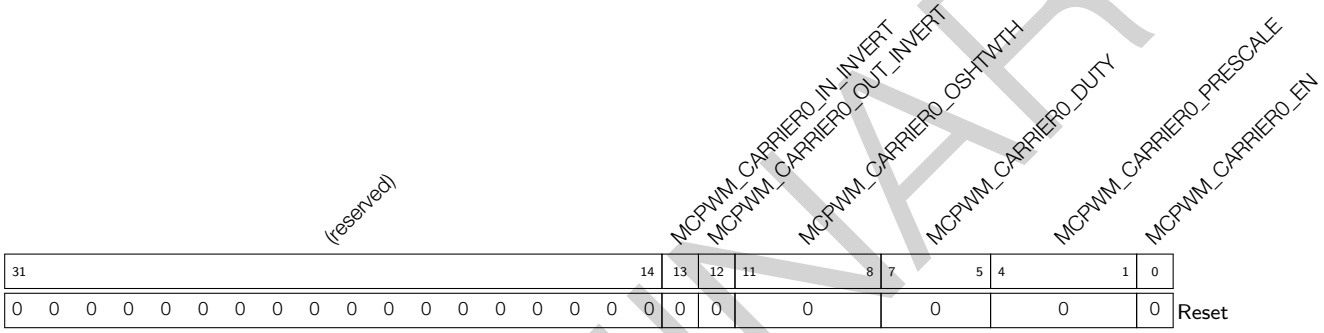
PRELIMINARY

Register 32.25. MCPWM_DT0_RED_CFG_REG (0x0060)



MCPWM_DT0_RED Shadow register for RED. (R/W)

Register 32.26. MCPWM_CARRIER0_CFG_REG (0x0064)



MCPWM_CARRIER0_EN When set, carrier0 function is enabled. When cleared, carrier0 is bypassed. (R/W)

MCPWM_CARRIER0_PRESCALE PWM carrier0 clock (PC_clk) prescale value. Period of PC_clk = period of PWM_clk * (PWM_CARRIER0_PRESCALE + 1). (R/W)

MCPWM_CARRIER0_DUTY Carrier duty selection. Duty = PWM_CARRIER0_DUTY / 8. (R/W)

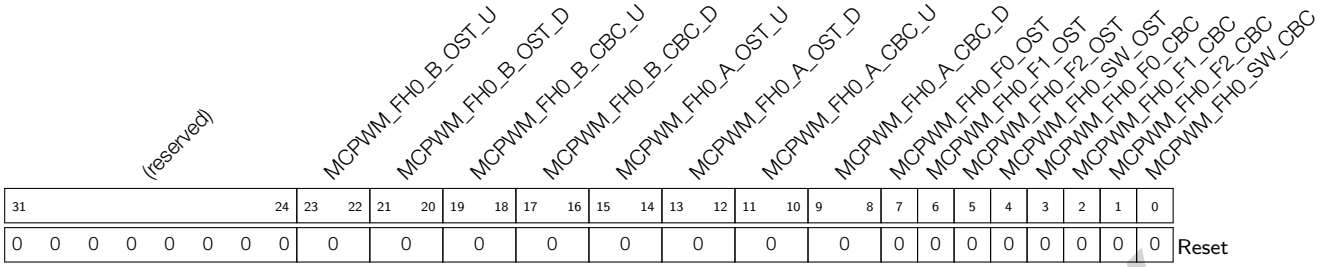
MCPWM_CARRIER0_OSHTWTH Width of the first pulse in number of periods of the carrier. (R/W)

MCPWM_CARRIER0_OUT_INVERT When set, invert the output of PWM0A and PWM0B for this submodule. (R/W)

MCPWM_CARRIER0_IN_INVERT When set, invert the input of PWM0A and PWM0B for this submodule. (R/W)

PRELIMINARY

Register 32.27. MCPWM_FH0_CFG0_REG (0x0068)



MCPWM_FH0_SW_CBC Enable register for software force cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH0_F2_CBC event_f2 will trigger cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH0_F1_CBC event_f1 will trigger cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH0_F0_CBC event_f0 will trigger cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH0_SW_OST Enable register for software force one-shot mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH0_F2_OST event_f2 will trigger one-shot mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH0_F1_OST event_f1 will trigger one-shot mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH0_F0_OST event_f0 will trigger one-shot mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH0_A_CBC_D Cycle-by-cycle mode action on PWM0A when fault event occurs and timer is decreasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH0_A_CBC_U Cycle-by-cycle mode action on PWM0A when fault event occurs and timer is increasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH0_A_OST_D One-shot mode action on PWM0A when fault event occurs and timer is decreasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH0_A_OST_U One-shot mode action on PWM0A when fault event occurs and timer is increasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH0_B_CBC_D Cycle-by-cycle mode action on PWM0B when fault event occurs and timer is decreasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

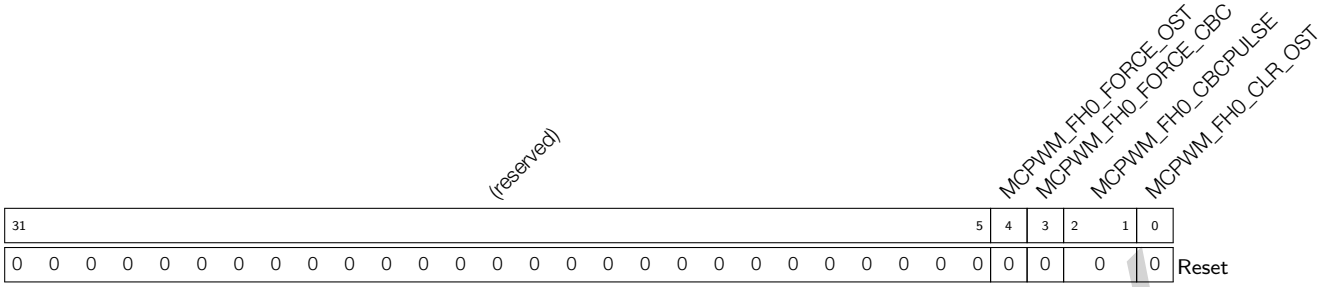
MCPWM_FH0_B_CBC_U Cycle-by-cycle mode action on PWM0B when fault event occurs and timer is increasing. 0: do nothing,1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH0_B_OST_D One-shot mode action on PWM0B when fault event occurs and timer is decreasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH0_B_OST_U One-shot mode action on PWM0B when fault event occurs and timer is increasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

PRELIMINARY

Register 32.28. MCPWM_FH0_CFG1_REG (0x006C)



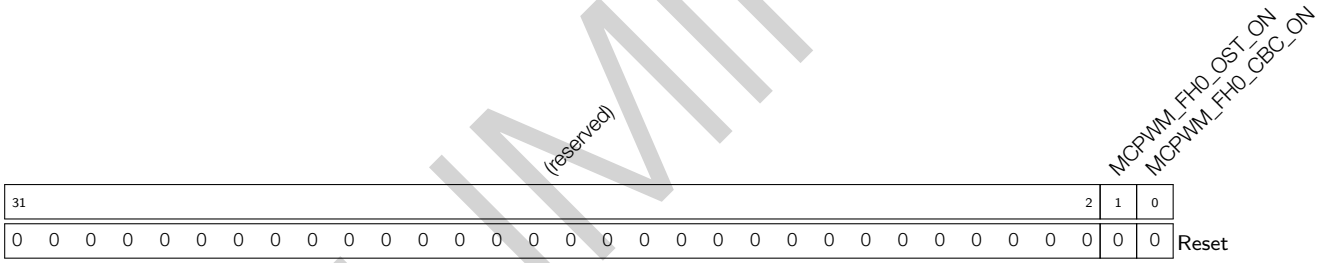
MCPWM_FH0_CLR_OST A rising edge will clear on going one-shot mode action. (R/W)

MCPWM_FH0_CBCPULSE Cycle-by-cycle mode action refresh moment selection. When bit0 is set to 1: TEZ; when bit1 is set to 1: TEP. (R/W)

MCPWM_FH0_FORCE_CBC A toggle triggers a cycle-by-cycle mode action. (R/W)

MCPWM_FH0_FORCE_OST A toggle (software negate its value) triggers a one-shot mode action. (R/W)

Register 32.29. MCPWM_FH0_STATUS_REG (0x0070)

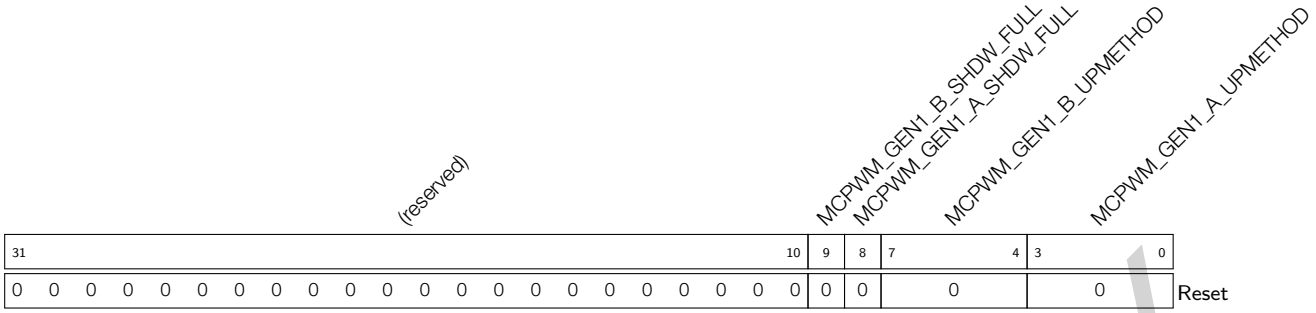


MCPWM_FH0_CBC_ON Set and reset by hardware. If set, a cycle-by-cycle mode action is on-going. (RO)

MCPWM_FH0_OST_ON Set and reset by hardware. If set, an one-shot mode action is on-going. (RO)

PRELIMINARY

Register 32.30. MCPWM_GEN1_STMP_CFG_REG (0x0074)



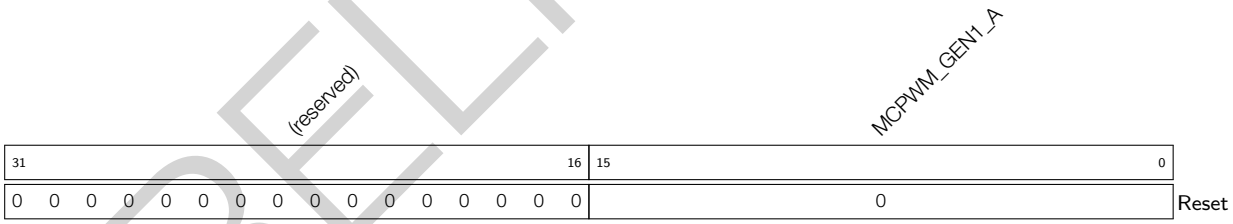
MCPWM_GEN1_A_UPMETHOD Update method for PWM generator 1 time stamp A's active register. When all bits are set to 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1: TEP; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_GEN1_B_UPMETHOD Update method for PWM generator 1 time stamp B's active register. When all bits are set to 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1: TEP; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_GEN1_A_SHDW_FULL Set and reset by hardware. If set, PWM generator 1 time stamp A's shadow reg is filled and waiting to be transferred to A's active reg. If cleared, A's active reg has been updated with shadow register latest value. (R/WTC/SC)

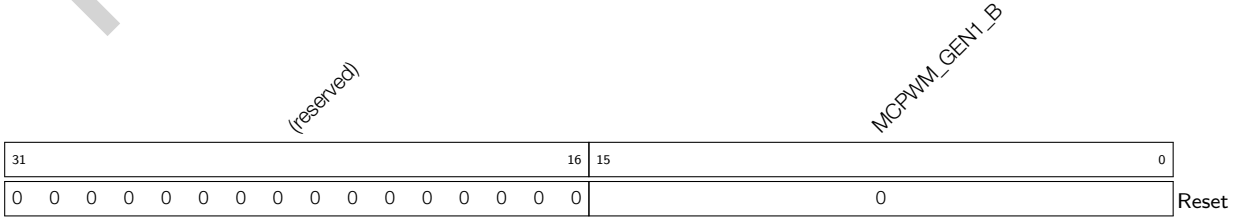
MCPWM_GEN1_B_SHDW_FULL Set and reset by hardware. If set, PWM generator 1 time stamp B's shadow reg is filled and waiting to be transferred to B's active reg. If cleared, B's active reg has been updated with shadow register latest value. (R/WTC/SC)

Register 32.31. MCPWM_GEN1_TSTMP_A_REG (0x0078)



MCPWM_GEN1_A PWM generator 1 time stamp A's shadow register. (R/W)

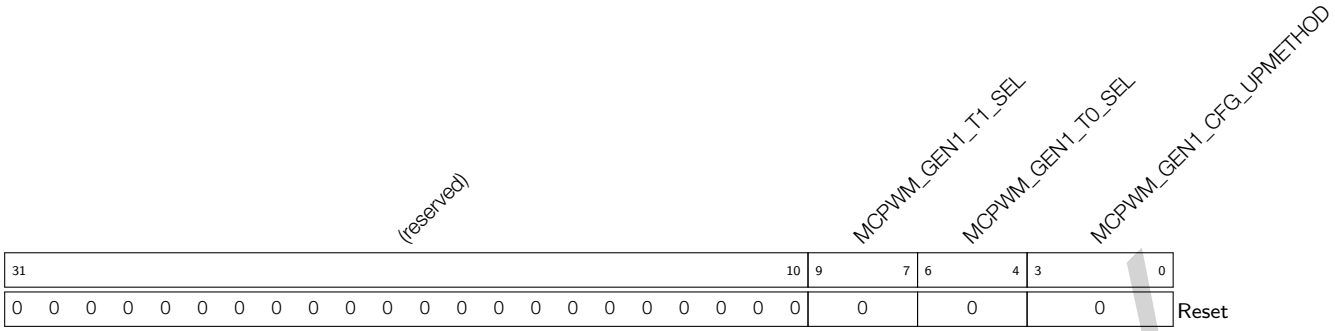
Register 32.32. MCPWM_GEN1_TSTMP_B_REG (0x007C)



MCPWM_GEN1_B PWM generator 1 time stamp B's shadow register. (R/W)

PRELIMINARY

Register 32.33. MCPWM_GEN1_CFG0_REG (0x0080)



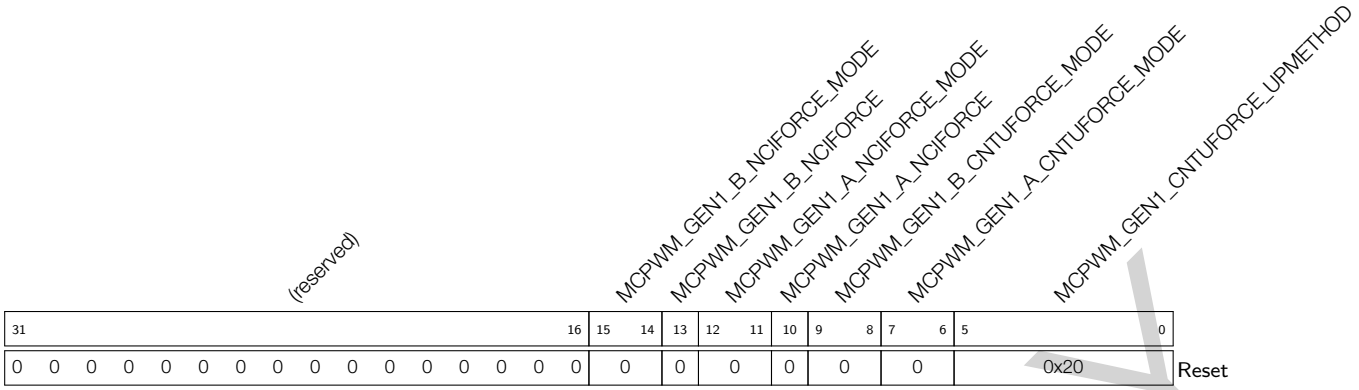
MCPWM_GEN1_CFG_UPMETHOD Update method for PWM generator 1's active register of configuration. When all bits are set to 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1:sync; when bit3 is set to 1:disable the update. (R/W)

MCPWM_GEN1_T0_SEL Source selection for PWM generator 1 event_t0, take effect immediately, 0: fault_event0, 1: fault_event1, 2: fault_event2, 3: sync_taken, 4: none. (R/W)

MCPWM_GEN1_T1_SEL Source selection for PWM generator 1 event_t1, take effect immediately, 0: fault_event0, 1: fault_event1, 2: fault_event2, 3: sync_taken, 4: none. (R/W)

PRELIMINARY

Register 32.34. MCPWM_GEN1_FORCE_REG (0x0084)



MCPWM_GEN1_CNTUFORCE_UPMETHOD Updating method for continuous software force of PWM generator 1. When all bits are set to 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1: TEP; when bit2 is set to 1: TEA; when bit3 is set to 1: TEB; when bit4 is set to 1: sync; when bit5 is set to 1: disable update. (TEA/B here and below means an event generated when the timer's value equals to that of register A/B.) (R/W)

MCPWM_GEN1_A_CNTUFORCE_MODE Continuous software force mode for PWM1A. 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

MCPWM_GEN1_B_CNTUFORCE_MODE Continuous software force mode for PWM1B. 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

MCPWM_GEN1_A_NCIFORCE Trigger of non-continuous immediate software-force event for PWM1A, a toggle will trigger a force event. (R/W)

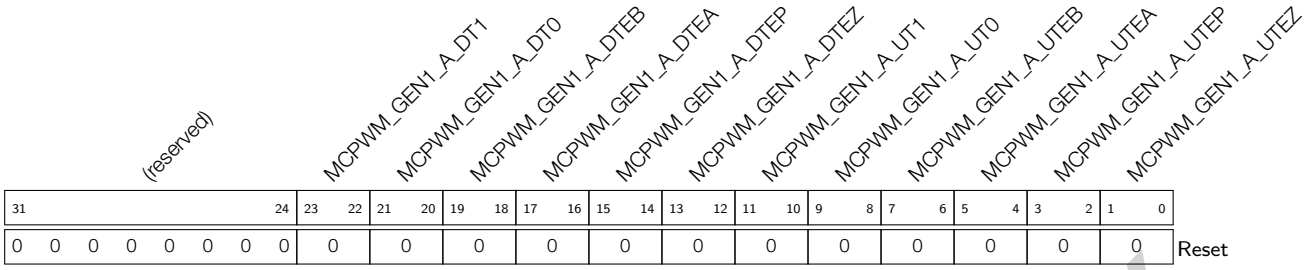
MCPWM_GEN1_A_NCIFORCE_MODE Non-continuous immediate software force mode for PWM1A. 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

MCPWM_GEN1_B_NCIFORCE Trigger of non-continuous immediate software-force event for PWM1B, a toggle will trigger a force event. (R/W)

MCPWM_GEN1_B_NCIFORCE_MODE Non-continuous immediate software force mode for PWM1B. 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

PRELIMINARY

Register 32.35. MCPWM_GEN1_A_REG (0x0088)



MCPWM_GEN1_A_UTEZ Action on PWM1A triggered by event TEZ when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_A_UTEP Action on PWM1A triggered by event TEP when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_A_UTEA Action on PWM1A triggered by event TEA when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_A_UTEB Action on PWM1A triggered by event TEB when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_A_UT0 Action on PWM1A triggered by event_t0 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_A_UT1 Action on PWM1A triggered by event_t1 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_A_DTEZ Action on PWM1A triggered by event TEZ when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_A_DTEP Action on PWM1A triggered by event TEP when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_A_DTEA Action on PWM1A triggered by event TEA when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

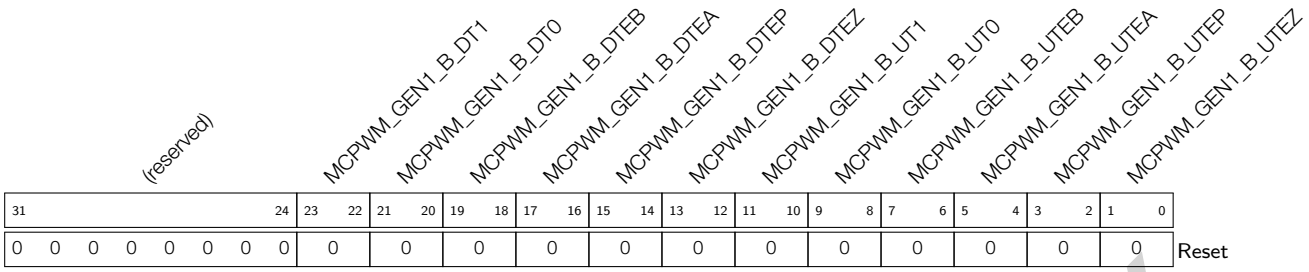
MCPWM_GEN1_A_DTEB Action on PWM1A triggered by event TEB when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_A_DT0 Action on PWM1A triggered by event_t0 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_A_DT1 Action on PWM1A triggered by event_t1 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

PRELIMINARY

Register 32.36. MCPWM_GEN1_B_REG (0x008C)



MCPWM_GEN1_B_UTEZ Action on PWM1B triggered by event TEZ when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_B_UTEP Action on PWM1B triggered by event TEP when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_B_UTEA Action on PWM1B triggered by event TEA when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_B_UTEB Action on PWM1B triggered by event TEB when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_B_UT0 Action on PWM1B triggered by event_t0 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_B_UT1 Action on PWM1B triggered by event_t1 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_B_DTEZ Action on PWM1B triggered by event TEZ when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_B_DTEP Action on PWM1B triggered by event TEP when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_B_DTEA Action on PWM1B triggered by event TEA when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

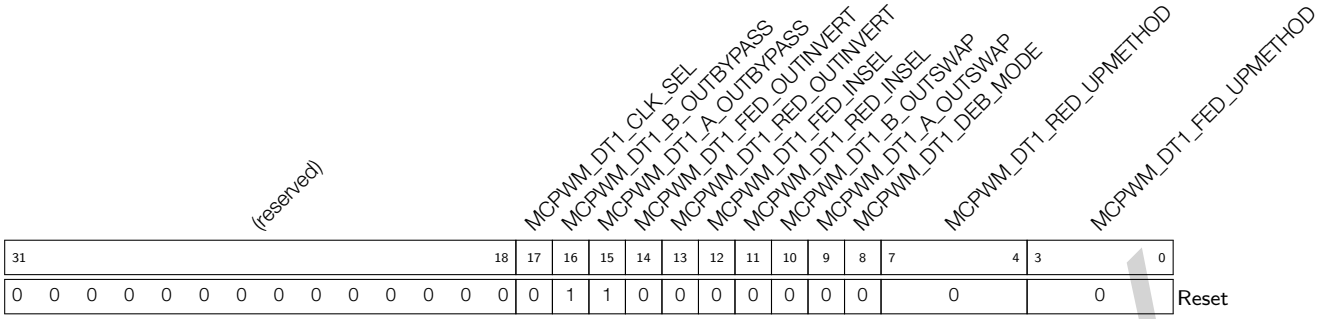
MCPWM_GEN1_B_DTEB Action on PWM1B triggered by event TEB when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_B_DT0 Action on PWM1B triggered by event_t0 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN1_B_DT1 Action on PWM1B triggered by event_t1 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

PRELIMINARY

Register 32.37. MCPWM_DT1_CFG_REG (0x0090)



MCPWM_DT1_FED_UPMETHOD Update method for FED (falling edge delay) active register. 0: immediate; when bit0 is set to 1: tez; when bit1 is set to 1: tep; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_DT1_RED_UPMETHOD Update method for RED (rising edge delay) active register. 0: immediate; when bit0 is set to 1: tez; when bit1 is set to 1: tep; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_DT1_DEB_MODE S8 in table 32-5, dual-edge B mode. 0: fed/red take effect on different path separately; 1: fed/red take effect on B path, A out is in bypass or dulpB mode. (R/W)

MCPWM_DT1_A_OUTSWAP S6 in table 32-5. (R/W)

MCPWM_DT1_B_OUTSWAP S7 in table 32-5. (R/W)

MCPWM_DT1_RED_INSEL S4 in table 32-5. (R/W)

MCPWM_DT1_FED_INSEL S5 in table 32-5. (R/W)

MCPWM_DT1_RED_OUTINVERT S2 in table 32-5. (R/W)

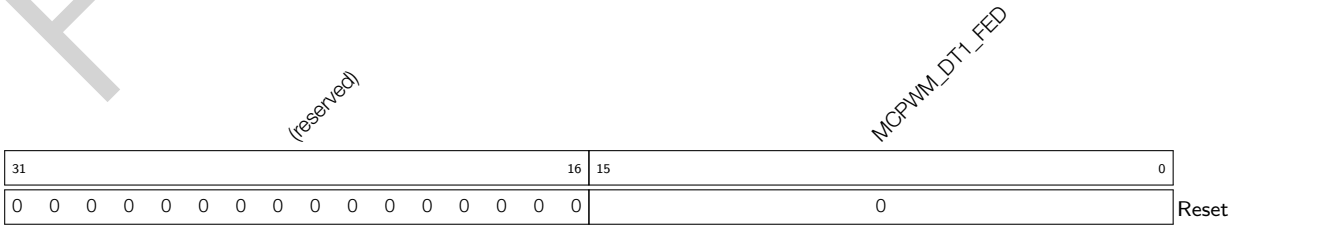
MCPWM_DT1_FED_OUTINVERT S3 in table 32-5. (R/W)

MCPWM_DT1_A_OUTBYPASS S1 in table 32-5. (R/W)

MCPWM_DT1_B_OUTBYPASS S0 in table 32-5. (R/W)

MCPWM_DT1_CLK_SEL Dead time generator 1 clock selection. 0: PWM_clk, 1: PT_clk. (R/W)

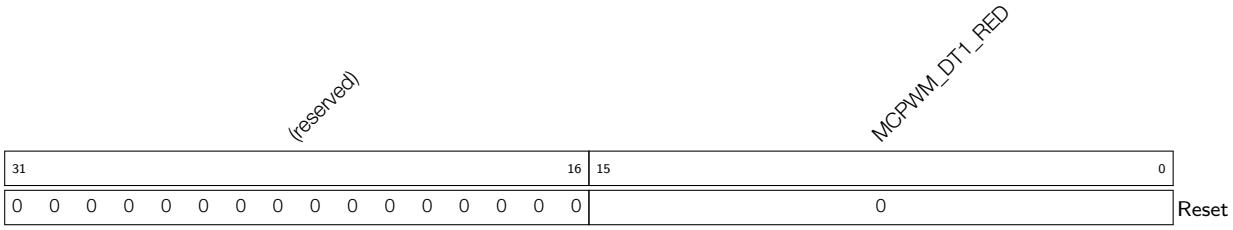
Register 32.38. MCPWM_DT1_FED_CFG_REG (0x0094)



MCPWM_DT1_FED Shadow register for FED. (R/W)

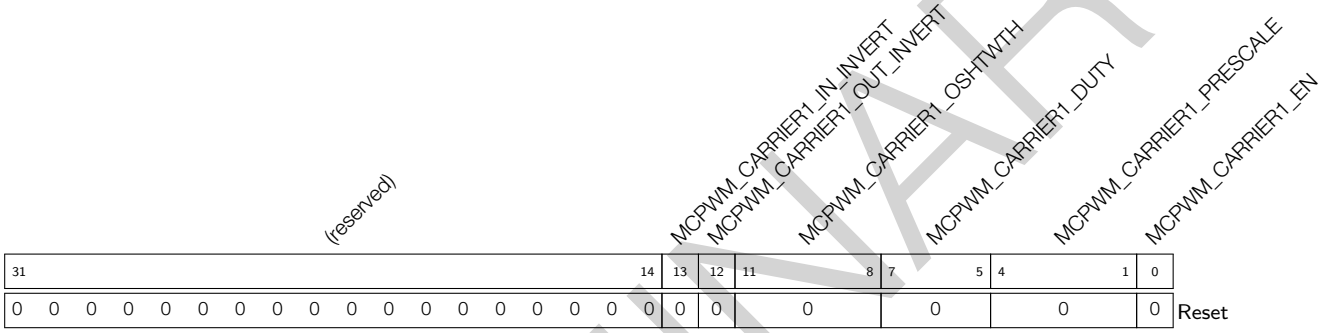
PRELIMINARY

Register 32.39. MCPWM_DT1_RED_CFG_REG (0x0098)



MCPWM_DT1_RED Shadow register for RED. (R/W)

Register 32.40. MCPWM_CARRIER1_CFG_REG (0x009C)



MCPWM_CARRIER1_EN When set, carrier1 function is enabled. When cleared, carrier1 is bypassed. (R/W)

MCPWM_CARRIER1_PRESCALE PWM carrier1 clock (PC_clk) prescale value. Period of PC_clk = period of PWM_clk * (PWM_CARRIER0_PRESCALE + 1). (R/W)

MCPWM_CARRIER1_DUTY Carrier duty selection. Duty = PWM_CARRIER0_DUTY / 8. (R/W)

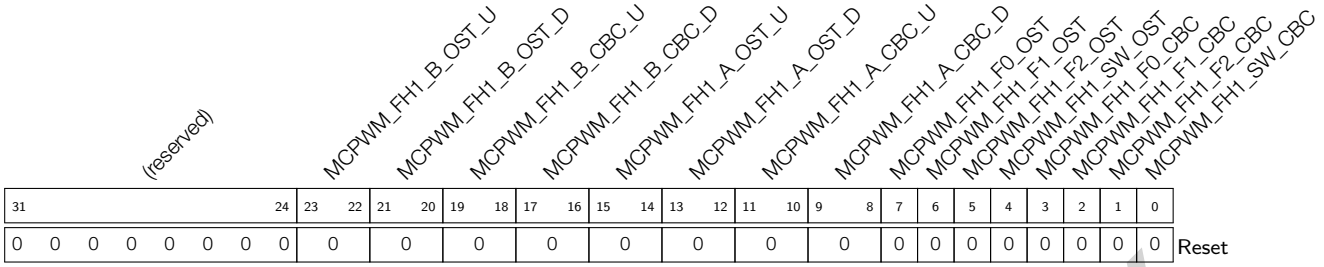
MCPWM_CARRIER1_OSHTWTH Width of the first pulse in number of periods of the carrier. (R/W)

MCPWM_CARRIER1_OUT_INVERT When set, invert the output of PWM1A and PWM1B for this submodule. (R/W)

MCPWM_CARRIER1_IN_INVERT When set, invert the input of PWM1A and PWM1B for this submodule. (R/W)

PRELIMINARY

Register 32.41. MCPWM_FH1_CFG0_REG (0x00A0)



MCPWM_FH1_SW_CBC Enable register for software force cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH1_F2_CBC event_f2 will trigger cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH1_F1_CBC event_f1 will trigger cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH1_F0_CBC event_f0 will trigger cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH1_SW_OST Enable register for software force one-shot mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH1_F2_OST event_f2 will trigger one-shot mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH1_F1_OST event_f1 will trigger one-shot mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH1_F0_OST event_f0 will trigger one-shot mode action. 0: disable, 1: enable (R/W)

MCPWM_FH1_A_CBC_D Cycle-by-cycle mode action on PWM1A when fault event occurs and timer is decreasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH1_A_CBC_U Cycle-by-cycle mode action on PWM1A when fault event occurs and timer is increasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH1_A_OST_D One-shot mode action on PWM1A when fault event occurs and timer is decreasing. 0: do nothing,1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH1_A_OST_U One-shot mode action on PWM1A when fault event occurs and timer is increasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH1_B_CBC_D Cycle-by-cycle mode action on PWM1B when fault event occurs and timer is decreasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

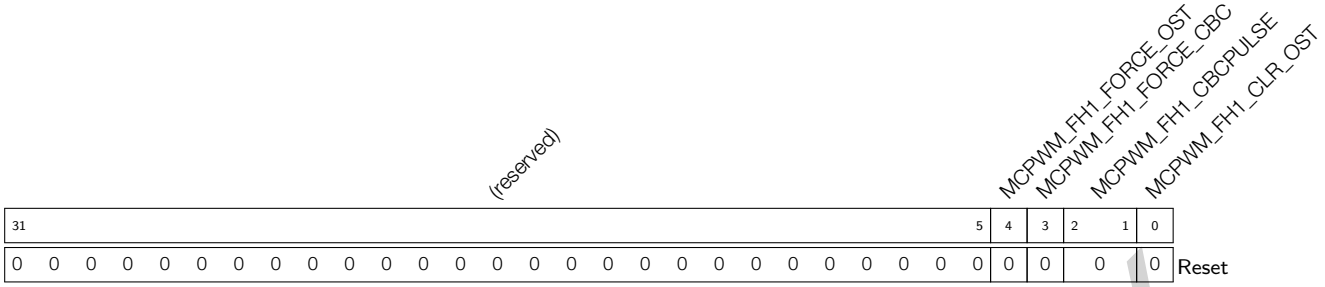
MCPWM_FH1_B_CBC_U Cycle-by-cycle mode action on PWM1B when fault event occurs and timer is increasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH1_B_OST_D One-shot mode action on PWM1B when fault event occurs and timer is decreasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH1_B_OST_U One-shot mode action on PWM1B when fault event occurs and timer is increasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

PRELIMINARY

Register 32.42. MCPWM_FH1_CFG1_REG (0x00A4)



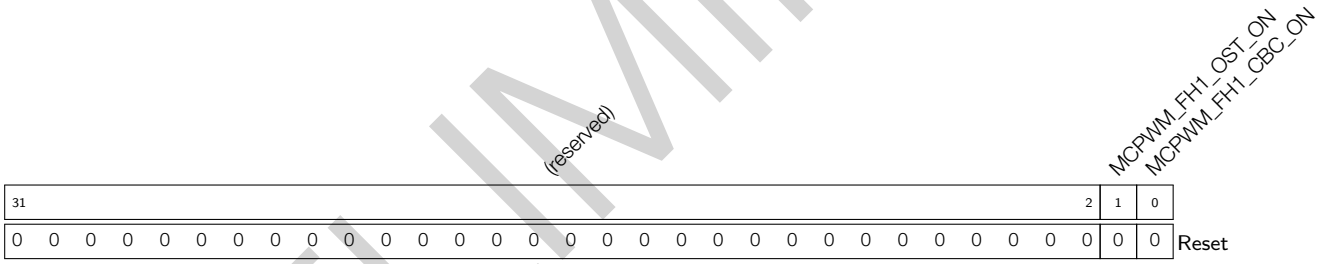
MCPWM_FH1_CLR_OST A rising edge will clear on going one-shot mode action. (R/W)

MCPWM_FH1_CBCPULSE Cycle-by-cycle mode action refresh moment selection. When all bits are 0: refresh disabled; when bit0 is set to 1: TEZ; when bit1 is set to 1: TEP; when all bits are 1: TEZ/TEP. (R/W)

MCPWM_FH1_FORCE_CBC A toggle triggers a cycle-by-cycle mode action. (R/W)

MCPWM_FH1_FORCE_OST A toggle (software negate its value) triggers a one-shot mode action. (R/W)

Register 32.43. MCPWM_FH1_STATUS_REG (0x00A8)

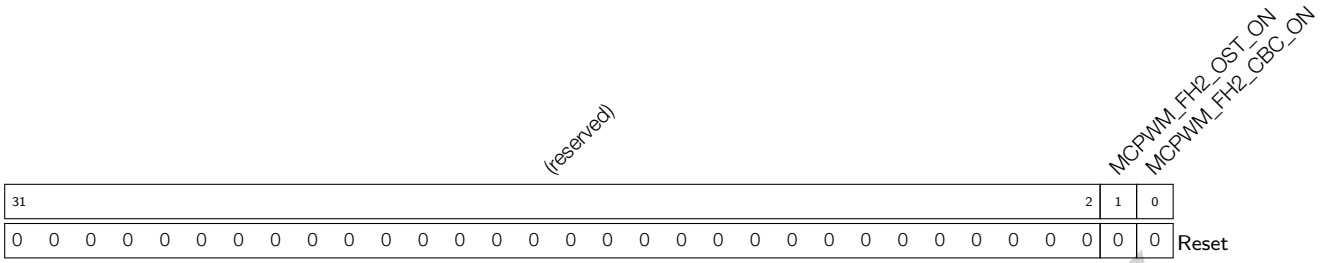


MCPWM_FH1_CBC_ON Set and reset by hardware. If set, a cycle-by-cycle mode action is on-going. (RO)

MCPWM_FH1_OST_ON Set and reset by hardware. If set, an one-shot mode action is on-going. (RO)

PRELIMINARY

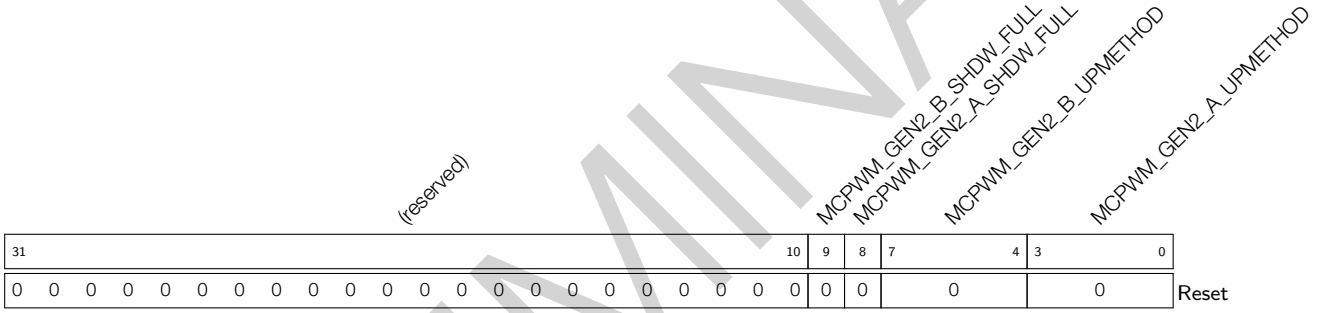
Register 32.44. MCPWM_FH2_STATUS_REG (0x00E0)



MCPWM_FH2_CBC_ON Set and reset by hardware. If set, a cycle-by-cycle mode action is on-going. (RO)

MCPWM_FH2_OST_ON Set and reset by hardware. If set, an one-shot mode action is on-going. (RO)

Register 32.45. MCPWM_GEN2_STMP_CFG_REG (0x00AC)



MCPWM_GEN2_A_UPMETHOD Update method for PWM generator 2 time stamp A's active register. When all bits are set to 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1: TEP; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

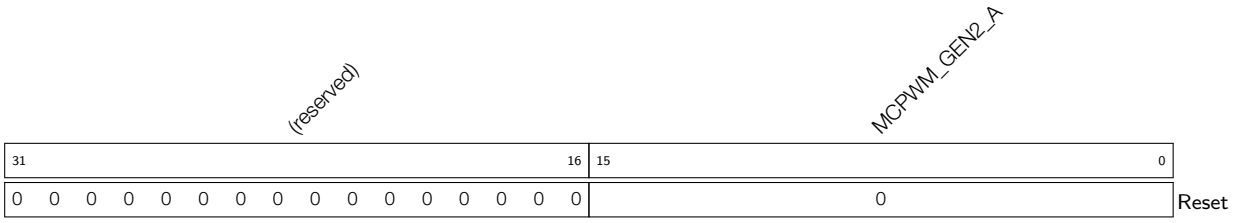
MCPWM_GEN2_B_UPMETHOD Update method for PWM generator 2 time stamp B's active register. When all bits are set to 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1: TEP; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_GEN2_A_SHDW_FULL Set and reset by hardware. If set, PWM generator 2 time stamp A's shadow reg is filled and waiting to be transferred to A's active reg. If cleared, A's active reg has been updated with shadow register latest value. (R/WTC/SC)

MCPWM_GEN2_B_SHDW_FULL Set and reset by hardware. If set, PWM generator 2 time stamp B's shadow reg is filled and waiting to be transferred to B's active reg. If cleared, B's active reg has been updated with shadow register latest value. (R/WTC/SC)

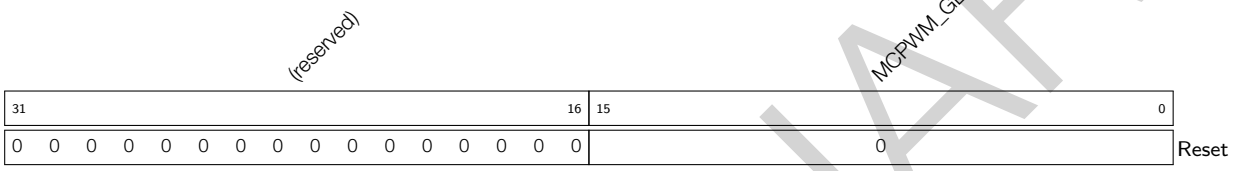
PRELIMINARY

Register 32.46. MCPWM_GEN2_STMP_A_REG (0x00B0)



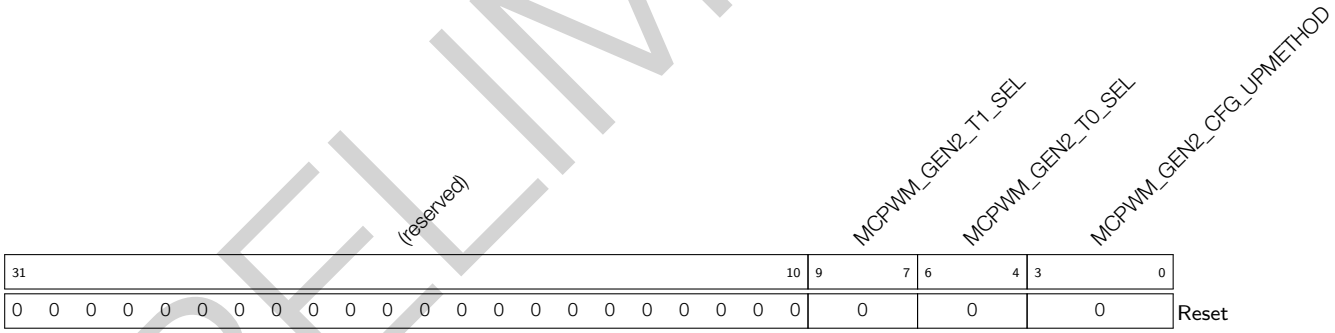
MCPWM_GEN2_A PWM generator 2 time stamp A's shadow register. (R/W)

Register 32.47. MCPWM_GEN2_STMP_B_REG (0x00B4)



MCPWM_GEN2_B PWM generator 2 time stamp B's shadow register. (R/W)

Register 32.48. MCPWM_GEN2_CFG0_REG (0x00B8)



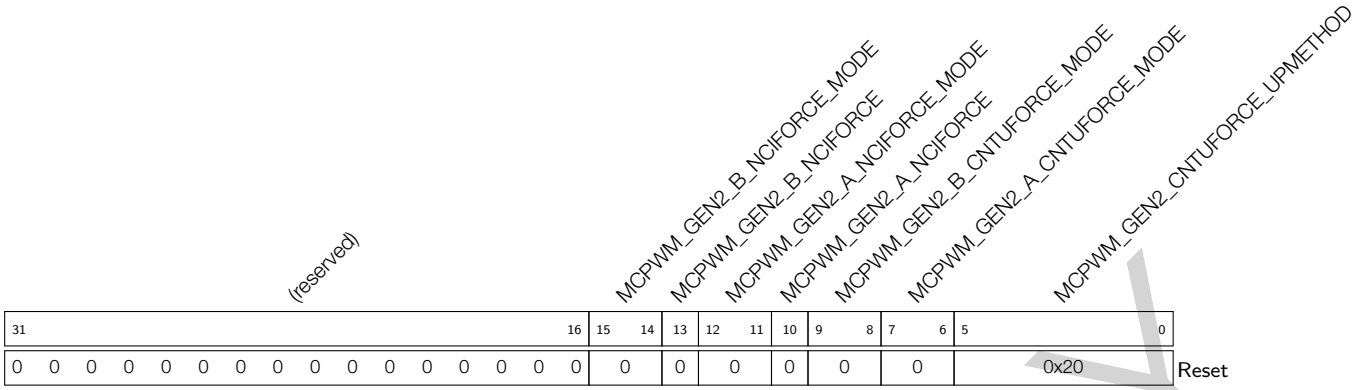
MCPWM_GEN2_CFG_UPMETHOD Update method for PWM generator 2's active register of configuration. 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_GEN2_T0_SEL Source selection for PWM generator 2 event_t0, take effect immediately, 0: fault_event0, 1: fault_event1, 2: fault_event2, 3: sync_taken, 4: none. (R/W)

MCPWM_GEN2_T1_SEL Source selection for PWM generator 2 event_t1, take effect immediately, 0: fault_event0, 1: fault_event1, 2: fault_event2, 3: sync_taken, 4: none. (R/W)

PRELIMINARY

Register 32.49. MCPWM_GEN2_FORCE_REG (0x00BC)



MCPWM_GEN2_CNTUFORCE_UPMETHOD Updating method for continuous software force of PWM generator 2. When all bits are set to 0: immediately; when bit0 is set to 1: TEZ; when bit1 is set to 1: TEP; when bit2 is set to 1: TEA; when bit3 is set to 1: TEB; when bit4 is set to 1: sync; when bit5 is set to 1: disable update. (TEA/B here and below means an event generated when the timer's value equals to that of register A/B.) (R/W)

MCPWM_GEN2_A_CNTUFORCE_MODE Continuous software force mode for PWM2A. 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

MCPWM_GEN2_B_CNTUFORCE_MODE Continuous software force mode for PWM2B. 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

MCPWM_GEN2_A_NCIFORCE Trigger of non-continuous immediate software-force event for PWM2A, a toggle will trigger a force event. (R/W)

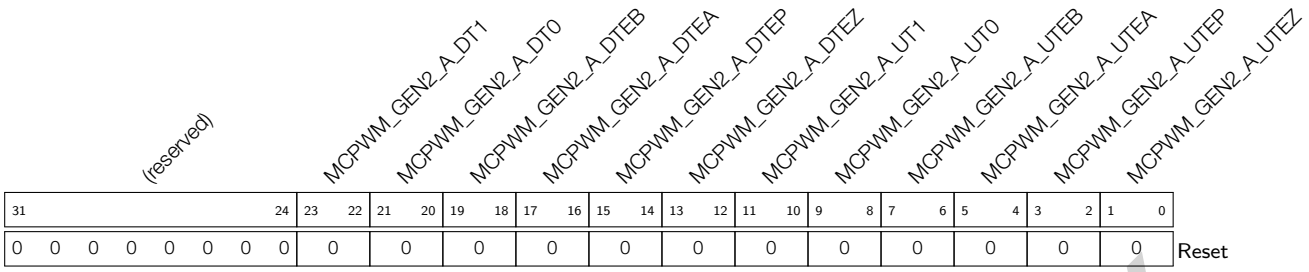
MCPWM_GEN2_A_NCIFORCE_MODE Non-continuous immediate software force mode for PWM2A, 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

MCPWM_GEN2_B_NCIFORCE Trigger of non-continuous immediate software-force event for PWM2B, a toggle will trigger a force event. (R/W)

MCPWM_GEN2_B_NCIFORCE_MODE Non-continuous immediate software force mode for PWM2B. 0: disabled, 1: low, 2: high, 3: disabled. (R/W)

PRELIMINARY

Register 32.50. MCPWM_GEN2_A_REG (0x00C0)



MCPWM_GEN2_A_UTEZ Action on PWM2A triggered by event TEZ when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_A_UTEP Action on PWM2A triggered by event TEP when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_A_UTEA Action on PWM2A triggered by event TEA when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_A_UTEB Action on PWM2A triggered by event TEB when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_A_UT0 Action on PWM2A triggered by event_t0 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_A_UT1 Action on PWM2A triggered by event_t1 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_A_DTEZ Action on PWM2A triggered by event TEZ when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_A_DTEP Action on PWM2A triggered by event TEP when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_A_DTEA Action on PWM2A triggered by event TEA when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

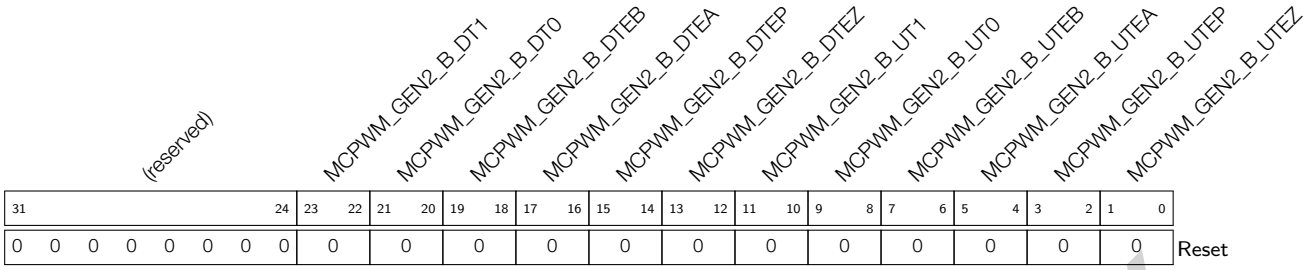
MCPWM_GEN2_A_DTEB Action on PWM2A triggered by event TEB when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_A_DT0 Action on PWM2A triggered by event_t0 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_A_DT1 Action on PWM2A triggered by event_t1 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

PRELIMINARY

Register 32.51. MCPWM_GEN2_B_REG (0x00C4)



MCPWM_GEN2_B_UTEZ Action on PWM2B triggered by event TEZ when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_B_UTEP Action on PWM2B triggered by event TEP when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_B_UTEA Action on PWM2B triggered by event TEA when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_B_UTEB Action on PWM2B triggered by event TEB when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_B_UT0 Action on PWM2B triggered by event_t0 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_B_UT1 Action on PWM2B triggered by event_t1 when timer increasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_B_DTEZ Action on PWM2B triggered by event TEZ when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_B_DTEP Action on PWM2B triggered by event TEP when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_B_DTEA Action on PWM2B triggered by event TEA when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

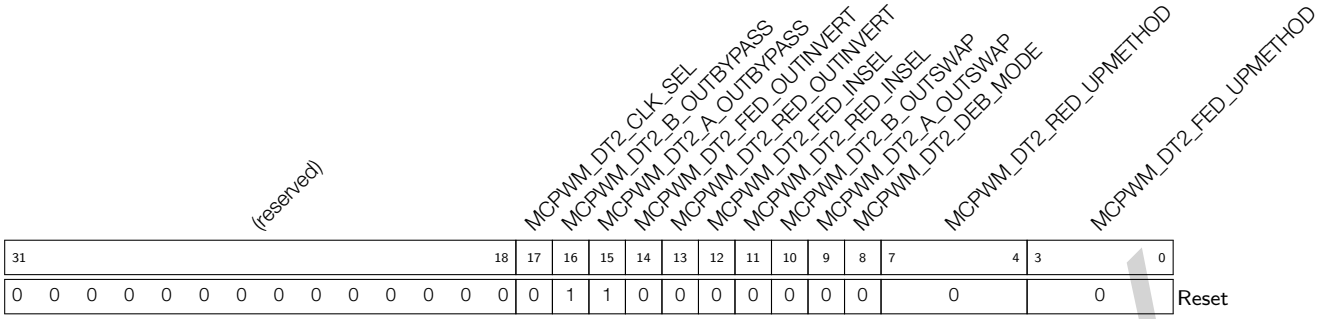
MCPWM_GEN2_B_DTEB Action on PWM2B triggered by event TEB when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_B_DT0 Action on PWM2B triggered by event_t0 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

MCPWM_GEN2_B_DT1 Action on PWM2B triggered by event_t1 when timer decreasing. 0: no change, 1: low, 2: high, 3: toggle. (R/W)

PRELIMINARY

Register 32.52. MCPWM_DT2_CFG_REG (0x00C8)



MCPWM_DT2_FED_UPMETHOD Update method for FED (falling edge delay) active register. 0: immediate; when bit0 is set to 1: tez; when bit1 is set to 1: tep; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_DT2_RED_UPMETHOD Update method for RED (rising edge delay) active register. 0: immediate; when bit0 is set to 1: tez; when bit1 is set to 1: tep; when bit2 is set to 1: sync; when bit3 is set to 1: disable the update. (R/W)

MCPWM_DT2_DEB_MODE S8 in table 32-5, dual-edge B mode. 0: fed/red take effect on different path separately; 1: fed/red take effect on B path, A out is in bypass or dulpB mode. (R/W)

MCPWM_DT2_A_OUTSWAP S6 in table 32-5. (R/W)

MCPWM_DT2_B_OUTSWAP S7 in table 32-5. (R/W)

MCPWM_DT2_RED_INSEL S4 in table 32-5. (R/W)

MCPWM_DT2_FED_INSEL S5 in table 32-5. (R/W)

MCPWM_DT2_RED_OUTINVERT S2 in table 32-5. (R/W)

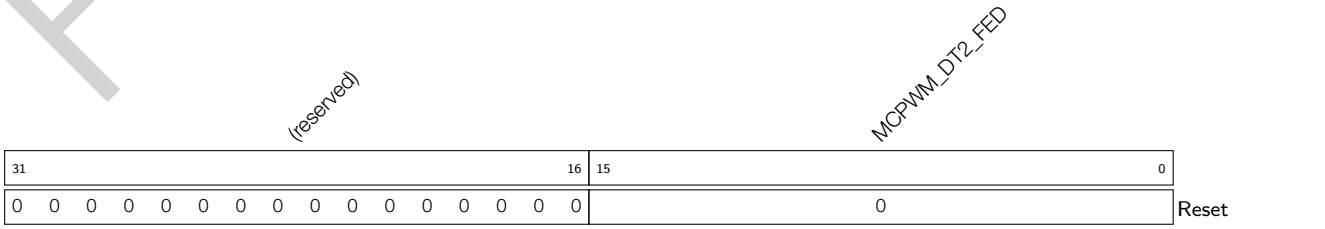
MCPWM_DT2_FED_OUTINVERT S3 in table 32-5. (R/W)

MCPWM_DT2_A_OUTBYPASS S1 in table 32-5. (R/W)

MCPWM_DT2_B_OUTBYPASS S0 in table 32-5. (R/W)

MCPWM_DT2_CLK_SEL Dead time generator 2 clock selection. 0: PWM_clk, 1: PT_clk. (R/W)

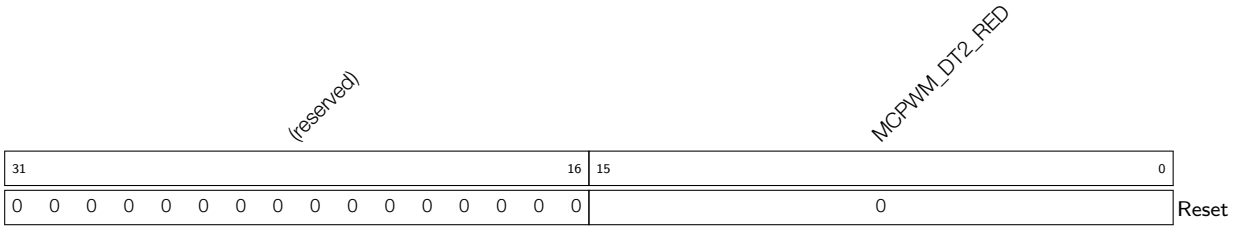
Register 32.53. MCPWM_DT2_FED_CFG_REG (0x00CC)



MCPWM_DT2_FED Shadow register for FED. (R/W)

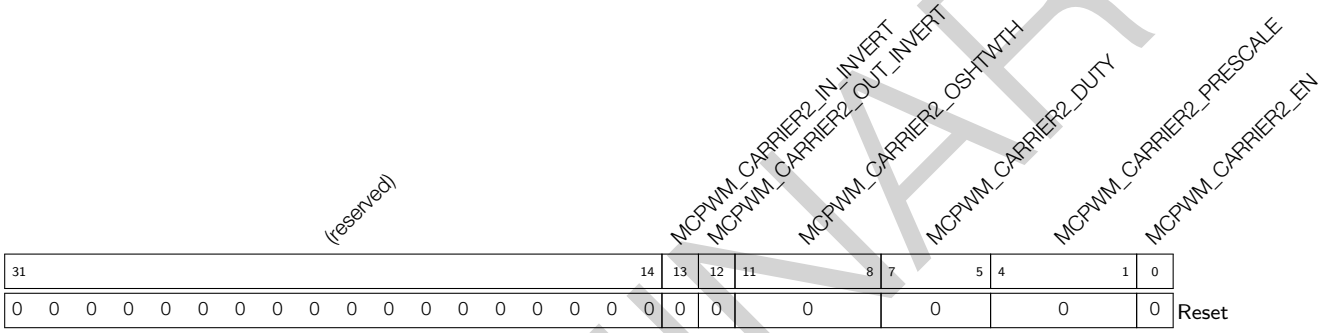
PRELIMINARY

Register 32.54. MCPWM_DT2_RED_CFG_REG (0x00D0)



MCPWM_DT2_RED Shadow register for RED. (R/W)

Register 32.55. MCPWM_CARRIER2_CFG_REG (0x00D4)



MCPWM_CARRIER2_EN When set, carrier2 function is enabled. When cleared, carrier2 is bypassed. (R/W)

MCPWM_CARRIER2_PRESCALE PWM carrier2 clock (PC_clk) prescale value. Period of PC_clk = period of PWM_clk * (PWM_CARRIER0_PRESCALE + 1). (R/W)

MCPWM_CARRIER2_DUTY Carrier duty selection. Duty = PWM_CARRIER0_DUTY / 8. (R/W)

MCPWM_CARRIER2_OSHTWTH Width of the first pulse in number of periods of the carrier. (R/W)

MCPWM_CARRIER2_OUT_INVERT When set, invert the output of PWM2A and PWM2B for this submodule. (R/W)

MCPWM_CARRIER2_IN_INVERT When set, invert the input of PWM2A and PWM2B for this submodule. (R/W)

PRELIMINARY

Register 32.56. MCPWM_FH2_CFG0_REG (0x00D8)



MCPWM_FH2_SW_CBC Enable register for software force cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH2_F2_CBC event_f2 will trigger cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH2_F1_CBC event_f1 will trigger cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH2_F0_CBC event_f0 will trigger cycle-by-cycle mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH2_SW_OST Enable register for software force one-shot mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH2_F2_OST event_f2 will trigger one-shot mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH2_F1_OST event_f1 will trigger one-shot mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH2_F0_OST event_f0 will trigger one-shot mode action. 0: disable, 1: enable. (R/W)

MCPWM_FH2_A_CBC_D Cycle-by-cycle mode action on PWM2A when fault event occurs and timer is decreasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH2_A_CBC_U Cycle-by-cycle mode action on PWM2A when fault event occurs and timer is increasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH2_A_OST_D One-shot mode action on PWM2A when fault event occurs and timer is decreasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH2_A_OST_U One-shot mode action on PWM2A when fault event occurs and timer is increasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH2_B_CBC_D Cycle-by-cycle mode action on PWM2B when fault event occurs and timer is decreasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

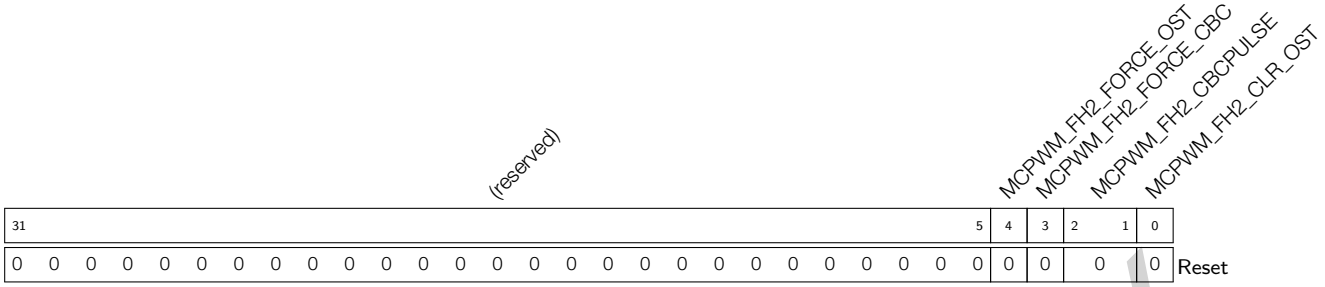
MCPWM_FH2_B_CBC_U Cycle-by-cycle mode action on PWM2B when fault event occurs and timer is increasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH2_B_OST_D One-shot mode action on PWM2B when fault event occurs and timer is decreasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

MCPWM_FH2_B_OST_U One-shot mode action on PWM2B when fault event occurs and timer is increasing. 0: do nothing, 1: force low, 2: force high, 3: toggle. (R/W)

PRELIMINARY

Register 32.57. MCPWM_FH2_CFG1_REG (0x00DC)



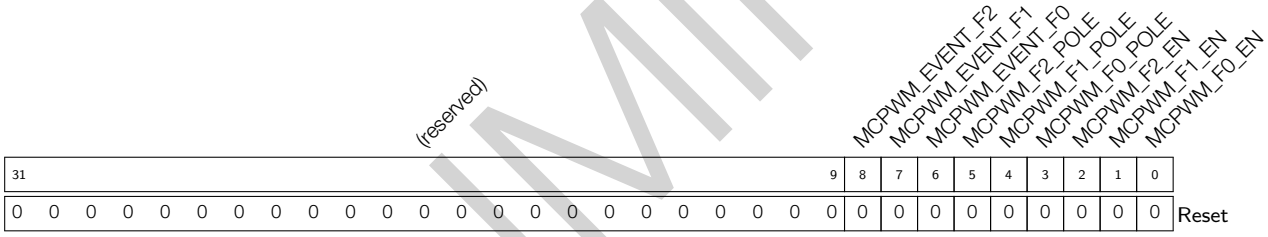
MCPWM_FH2_CLR_OST A rising edge will clear on going one-shot mode action. (R/W)

MCPWM_FH2_CBCPULSE Cycle-by-cycle mode action refresh moment selection. When bit0 is set to 1: TEZ; when bit1 is set to 1: TEP. (R/W)

MCPWM_FH2_FORCE_CBC A toggle triggers a cycle-by-cycle mode action. (R/W)

MCPWM_FH2_FORCE_OST A toggle (software negate its value) triggers a one-shot mode action. (R/W)

Register 32.58. MCPWM_FAULT_DETECT_REG (0x00E4)



MCPWM_F0_EN When set, event_f0 generation is enabled. (R/W)

MCPWM_F1_EN When set, event_f1 generation is enabled. (R/W)

MCPWM_F2_EN When set, event_f2 generation is enabled. (R/W)

MCPWM_F0_POLE Set event_f0 trigger polarity on FAULT0 source from GPIO matrix. 0: level low, 1: level high. (R/W)

MCPWM_F1_POLE Set event_f1 trigger polarity on FAULT1 source from GPIO matrix. 0: level low, 1: level high. (R/W)

MCPWM_F2_POLE Set event_f2 trigger polarity on FAULT2 source from GPIO matrix. 0: level low, 1: level high. (R/W)

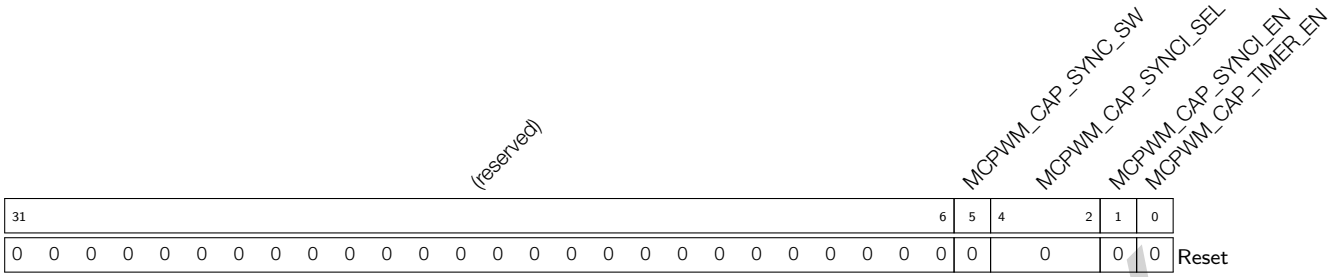
MCPWM_EVENT_F0 Set and reset by hardware. If set, event_f0 is on going. (RO)

MCPWM_EVENT_F1 Set and reset by hardware. If set, event_f1 is on going. (RO)

MCPWM_EVENT_F2 Set and reset by hardware. If set, event_f2 is on going. (RO)

PRELIMINARY

Register 32.59. MCPWM_CAP_TIMER_CFG_REG (0x00E8)



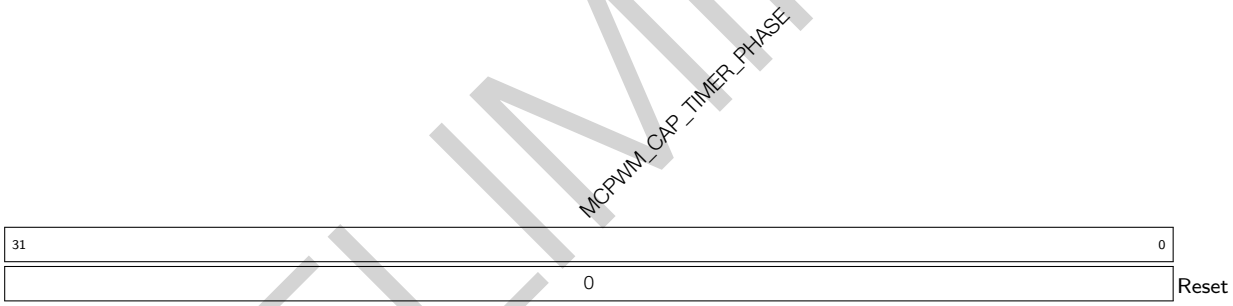
MCPWM_CAP_TIMER_EN When set, capture timer incrementing under APB_clk is enabled. (R/W)

MCPWM_CAP_SYNCI_EN When set, capture timer sync is enabled. (R/W)

MCPWM_CAP_SYNCI_SEL Capture module sync input selection. 0: none, 1: timer0 sync_out, 2: timer1 sync_out, 3: timer2 sync_out, 4: SYNC0 from GPIO matrix, 5: SYNC1 from GPIO matrix, 6: SYNC2 from GPIO matrix. (R/W)

MCPWM_CAP_SYNC_SW When reg_cap_synci_en is 1, write 1 will trigger a capture timer sync, capture timer is loaded with value in phase register. (WT)

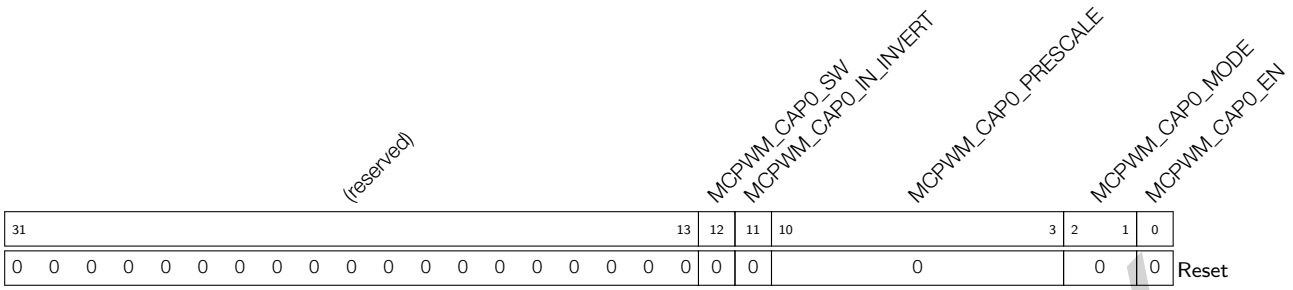
Register 32.60. MCPWM_CAP_TIMER_PHASE_REG (0x00EC)



MCPWM_CAP_TIMER_PHASE Phase value for capture timer sync operation. (R/W)

PRELIMINARY

Register 32.61. MCPWM_CAP_CH0_CFG_REG (0x00F0)



MCPWM_CAP0_EN When set, capture on channel 0 is enabled. (R/W)

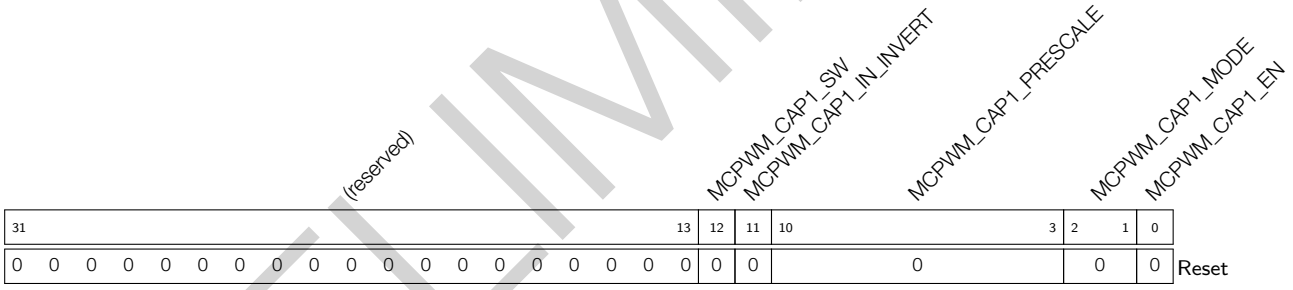
MCPWM_CAP0_MODE Edge of capture on channel 0 after prescaling. When bit0 is set to 1: enable capture on the falling edge, When bit1 is set to 1: enable capture on the rising edge. (R/W)

MCPWM_CAP0_PRESCALE Value of prescaling on rising edge of CAP0. Prescale value = PWM_CAP0_PRESCALE + 1. (R/W)

MCPWM_CAP0_IN_INVERT When set, CAP0 form GPIO matrix is inverted before prescale. (R/W)

MCPWM_CAP0_SW Write 1 will trigger a software forced capture on channel 0. (WT)

Register 32.62. MCPWM_CAP_CH1_CFG_REG (0x00F4)



MCPWM_CAP1_EN When set, capture on channel 1 is enabled. (R/W)

MCPWM_CAP1_MODE Edge of capture on channel 1 after prescaling. When bit0 is set to 1: enable capture on the falling edge, When bit1 is set to 1: enable capture on the rising edge. (R/W)

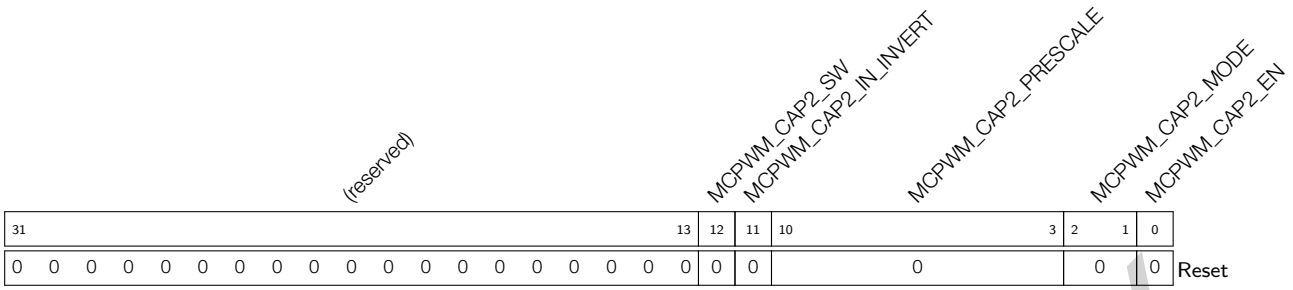
MCPWM_CAP1_PRESCALE Value of prescaling on rising edge of CAP1. Prescale value = PWM_CAP1_PRESCALE + 1. (R/W)

MCPWM_CAP1_IN_INVERT When set, CAP1 form GPIO matrix is inverted before prescale. (R/W)

MCPWM_CAP1_SW Write 1 will trigger a software forced capture on channel 1. (WT)

PRELIMINARY

Register 32.63. MCPWM_CAP_CH2_CFG_REG (0x00F8)



MCPWM_CAP2_EN When set, capture on channel 2 is enabled. (R/W)

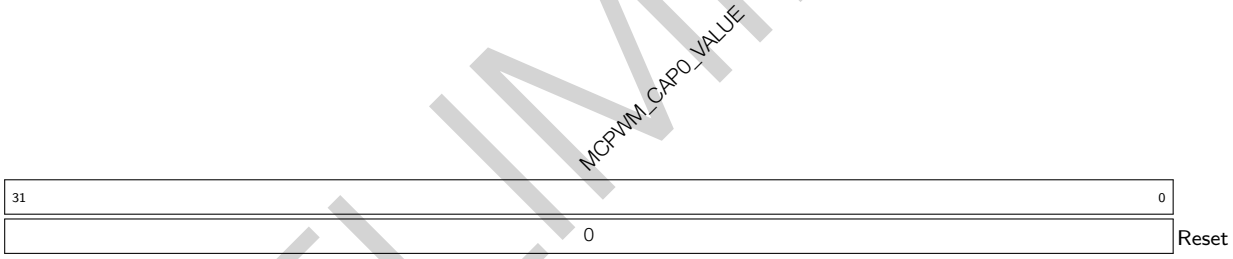
MCPWM_CAP2_MODE Edge of capture on channel 2 after prescaling. When bit0 is set to 1: enable capture on the falling edge, When bit1 is set to 1: enable capture on the rising edge. (R/W)

MCPWM_CAP2_PRESCALE Value of prescaling on rising edge of CAP2. Prescale value = PWM_CAP2_PRESCALE + 1. (R/W)

MCPWM_CAP2_IN_INVERT When set, CAP2 form GPIO matrix is inverted before prescale. (R/W)

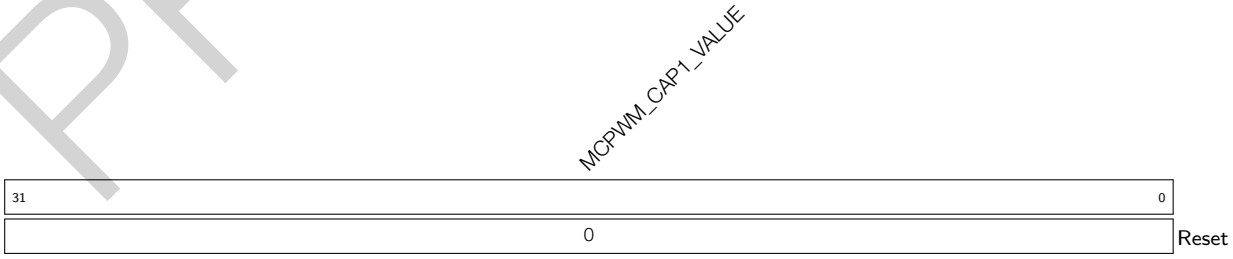
MCPWM_CAP2_SW Write 1 will trigger a software forced capture on channel 2. (WT)

Register 32.64. MCPWM_CAP_CH0_REG (0x00FC)



MCPWM_CAP0_VALUE Value of last capture on channel 0. (RO)

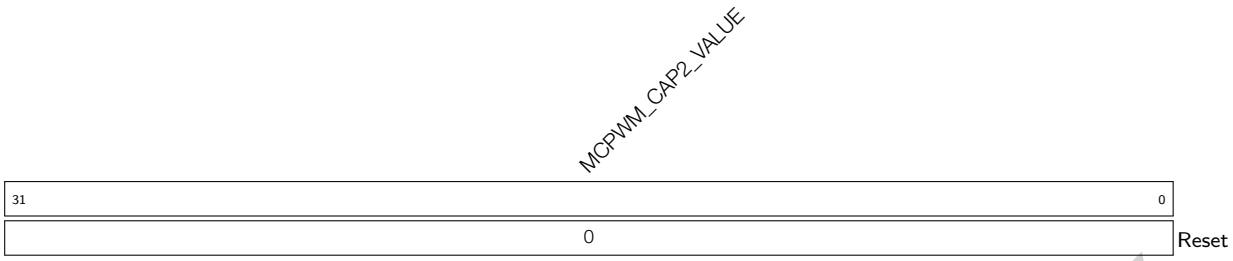
Register 32.65. MCPWM_CAP_CH1_REG (0x0100)



MCPWM_CAP1_VALUE Value of last capture on channel 1. (RO)

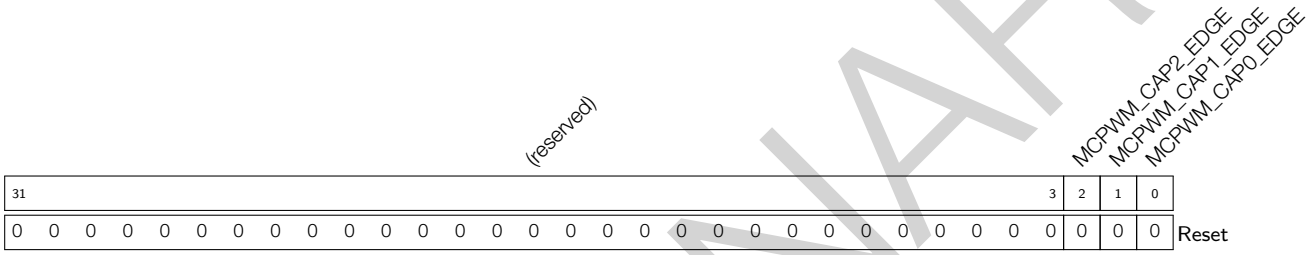
PRELIMINARY

Register 32.66. MCPWM_CAP_CH2_REG (0x0104)



MCPWM_CAP2_VALUE Value of last capture on channel 2. (RO)

Register 32.67. MCPWM_CAP_STATUS_REG (0x0108)



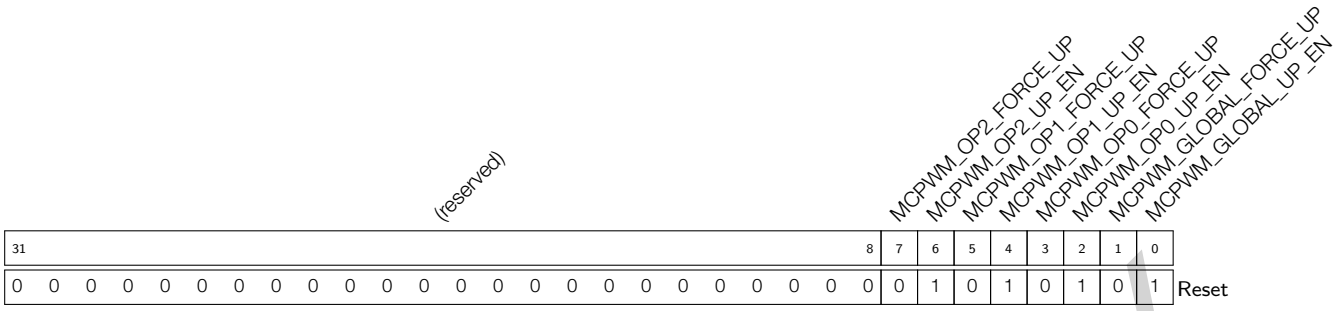
MCPWM_CAP0_EDGE Edge of last capture trigger on channel 0, 0: rising edge, 1: falling edge. (RO)

MCPWM_CAP1_EDGE Edge of last capture trigger on channel 1, 0: rising edge, 1: falling edge. (RO)

MCPWM_CAP2_EDGE Edge of last capture trigger on channel 2, 0: rising edge, 1: falling edge. (RO)

PRELIMINARY

Register 32.68. MCPWM_UPDATE_CFG_REG (0x010C)



MCPWM_GLOBAL_UP_EN The global enable of update of all active registers in MCPWM module. (R/W)

MCPWM_GLOBAL_FORCE_UP A toggle (software invert its value) will trigger a forced update of all active registers in MCPWM module. (R/W)

MCPWM_OP0_UP_EN When set and PWM_GLOBAL_UP_EN is set, update of active registers in PWM operator 0 are enabled. (R/W)

MCPWM_OP0_FORCE_UP A toggle (software invert its value) will trigger a forced update of active registers in PWM operator 0. (R/W)

MCPWM_OP1_UP_EN When set and PWM_GLOBAL_UP_EN is set, update of active registers in PWM operator 1 are enabled. (R/W)

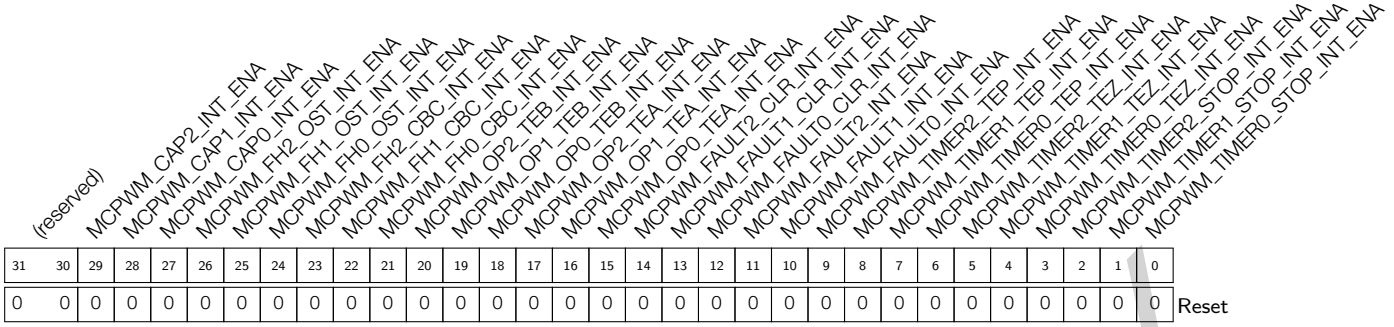
MCPWM_OP1_FORCE_UP A toggle (software invert its value) will trigger a forced update of active registers in PWM operator 1. (R/W)

MCPWM_OP2_UP_EN When set and PWM_GLOBAL_UP_EN is set, update of active registers in PWM operator 2 are enabled. (R/W)

MCPWM_OP2_FORCE_UP A toggle (software invert its value) will trigger a forced update of active registers in PWM operator 2. (R/W)

PRELIMINARY

Register 32.69. MCPWM_INT_ENA_REG (0x0110)



MCPWM_TIMER0_STOP_INT_ENA The enable bit for the interrupt triggered when the timer 0 stops. (R/W)

MCPWM_TIMER1_STOP_INT_ENA The enable bit for the interrupt triggered when the timer 1 stops. (R/W)

MCPWM_TIMER2_STOP_INT_ENA The enable bit for the interrupt triggered when the timer 2 stops. (R/W)

MCPWM_TIMER0_TEZ_INT_ENA The enable bit for the interrupt triggered by a PWM timer 0 TEZ event. (R/W)

MCPWM_TIMER1_TEZ_INT_ENA The enable bit for the interrupt triggered by a PWM timer 1 TEZ event. (R/W)

MCPWM_TIMER2_TEZ_INT_ENA The enable bit for the interrupt triggered by a PWM timer 2 TEZ event. (R/W)

MCPWM_TIMER0_TEP_INT_ENA The enable bit for the interrupt triggered by a PWM timer 0 TEP event. (R/W)

MCPWM_TIMER1_TEP_INT_ENA The enable bit for the interrupt triggered by a PWM timer 1 TEP event. (R/W)

MCPWM_TIMER2_TEP_INT_ENA The enable bit for the interrupt triggered by a PWM timer 2 TEP event. (R/W)

MCPWM_FAULT0_INT_ENA The enable bit for the interrupt triggered when event_f0 starts. (R/W)

MCPWM_FAULT1_INT_ENA The enable bit for the interrupt triggered when event_f1 starts. (R/W)

MCPWM_FAULT2_INT_ENA The enable bit for the interrupt triggered when event_f2 starts. (R/W)

MCPWM_FAULT0_CLR_INT_ENA The enable bit for the interrupt triggered when event_f0 ends. (R/W)

Continued on the next page...

PRELIMINARY

Register 32.69. MCPWM_INT_ENA_REG (0x0110)

Continued from the previous page...

MCPWM_FAULT1_CLR_INT_ENA The enable bit for the interrupt triggered when event_f1 ends. (R/W)

MCPWM_FAULT2_CLR_INT_ENA The enable bit for the interrupt triggered when event_f2 ends. (R/W)

MCPWM_OP0_TEA_INT_ENA The enable bit for the interrupt triggered by a PWM operator 0 TEA event (R/W)

MCPWM_OP1_TEA_INT_ENA The enable bit for the interrupt triggered by a PWM operator 1 TEA event (R/W)

MCPWM_OP2_TEA_INT_ENA The enable bit for the interrupt triggered by a PWM operator 2 TEA event (R/W)

MCPWM_OP0_TEB_INT_ENA The enable bit for the interrupt triggered by a PWM operator 0 TEB event (R/W)

MCPWM_OP1_TEB_INT_ENA The enable bit for the interrupt triggered by a PWM operator 1 TEB event (R/W)

MCPWM_OP2_TEB_INT_ENA The enable bit for the interrupt triggered by a PWM operator 2 TEB event (R/W)

MCPWM_FH0_CBC_INT_ENA The enable bit for the interrupt triggered by a cycle-by-cycle mode action on PWM0. (R/W)

MCPWM_FH1_CBC_INT_ENA The enable bit for the interrupt triggered by a cycle-by-cycle mode action on PWM1. (R/W)

MCPWM_FH2_CBC_INT_ENA The enable bit for the interrupt triggered by a cycle-by-cycle mode action on PWM2. (R/W)

MCPWM_FH0_OST_INT_ENA The enable bit for the interrupt triggered by a one-shot mode action on PWM0. (R/W)

MCPWM_FH1_OST_INT_ENA The enable bit for the interrupt triggered by a one-shot mode action on PWM1. (R/W)

MCPWM_FH2_OST_INT_ENA The enable bit for the interrupt triggered by a one-shot mode action on PWM2. (R/W)

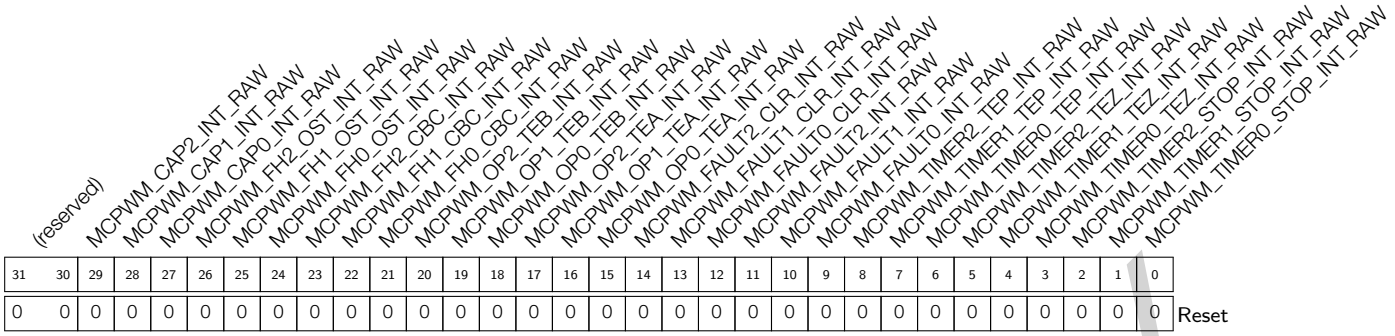
MCPWM_CAP0_INT_ENA The enable bit for the interrupt triggered by capture on channel 0. (R/W)

MCPWM_CAP1_INT_ENA The enable bit for the interrupt triggered by capture on channel 1. (R/W)

MCPWM_CAP2_INT_ENA The enable bit for the interrupt triggered by capture on channel 2. (R/W)

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Register 32.70. MCPWM_INT_RAW_REG (0x0114)



MCPWM_TIMER0_STOP_INT_RAW The raw status bit for the interrupt triggered when the timer 0 stops. (R/WTC/SS)

MCPWM_TIMER1_STOP_INT_RAW The raw status bit for the interrupt triggered when the timer 1 stops. (R/WTC/SS)

MCPWM_TIMER2_STOP_INT_RAW The raw status bit for the interrupt triggered when the timer 2 stops. (R/WTC/SS)

MCPWM_TIMER0_TEZ_INT_RAW The raw status bit for the interrupt triggered by a PWM timer 0 TEZ event. (R/WTC/SS)

MCPWM_TIMER1_TEZ_INT_RAW The raw status bit for the interrupt triggered by a PWM timer 1 TEZ event. (R/WTC/SS)

MCPWM_TIMER2_TEZ_INT_RAW The raw status bit for the interrupt triggered by a PWM timer 2 TEZ event. (R/WTC/SS)

MCPWM_TIMER0_TEP_INT_RAW The raw status bit for the interrupt triggered by a PWM timer 0 TEP event. (R/WTC/SS)

MCPWM_TIMER1_TEP_INT_RAW The raw status bit for the interrupt triggered by a PWM timer 1 TEP event. (R/WTC/SS)

MCPWM_TIMER2_TEP_INT_RAW The raw status bit for the interrupt triggered by a PWM timer 2 TEP event. (R/WTC/SS)

MCPWM_FAULT0_INT_RAW The raw status bit for the interrupt triggered when event_f0 starts. (R/WTC/SS)

MCPWM_FAULT1_INT_RAW The raw status bit for the interrupt triggered when event_f1 starts. (R/WTC/SS)

MCPWM_FAULT2_INT_RAW The raw status bit for the interrupt triggered when event_f2 starts. (R/WTC/SS)

MCPWM_FAULT0_CLR_INT_RAW The raw status bit for the interrupt triggered when event_f0 ends. (R/WTC/SS)

Continued on the next page...

PRELIMINARY

Register 32.70. MCPWM_INT_RAW_REG (0x0114)

Continued from the previous page...

MCPWM_FAULT1_CLR_INT_RAW The raw status bit for the interrupt triggered when event_f1 ends. (R/WTC/SS)

MCPWM_FAULT2_CLR_INT_RAW The raw status bit for the interrupt triggered when event_f2 ends. (R/WTC/SS)

MCPWM_OP0_TEA_INT_RAW The raw status bit for the interrupt triggered by a PWM operator 0 TEA event (R/WTC/SS)

MCPWM_OP1_TEA_INT_RAW The raw status bit for the interrupt triggered by a PWM operator 1 TEA event (R/WTC/SS)

MCPWM_OP2_TEA_INT_RAW The raw status bit for the interrupt triggered by a PWM operator 2 TEA event (R/WTC/SS)

MCPWM_OP0_TEB_INT_RAW The raw status bit for the interrupt triggered by a PWM operator 0 TEB event (R/WTC/SS)

MCPWM_OP1_TEB_INT_RAW The raw status bit for the interrupt triggered by a PWM operator 1 TEB event (R/WTC/SS)

MCPWM_OP2_TEB_INT_RAW The raw status bit for the interrupt triggered by a PWM operator 2 TEB event (R/WTC/SS)

MCPWM_FH0_CBC_INT_RAW The raw status bit for the interrupt triggered by a cycle-by-cycle mode action on PWM0. (R/WTC/SS)

MCPWM_FH1_CBC_INT_RAW The raw status bit for the interrupt triggered by a cycle-by-cycle mode action on PWM1. (R/WTC/SS)

MCPWM_FH2_CBC_INT_RAW The raw status bit for the interrupt triggered by a cycle-by-cycle mode action on PWM2. (R/WTC/SS)

MCPWM_FH0_OST_INT_RAW The raw status bit for the interrupt triggered by a one-shot mode action on PWM0. (R/WTC/SS)

MCPWM_FH1_OST_INT_RAW The raw status bit for the interrupt triggered by a one-shot mode action on PWM1. (R/WTC/SS)

MCPWM_FH2_OST_INT_RAW The raw status bit for the interrupt triggered by a one-shot mode action on PWM2. (R/WTC/SS)

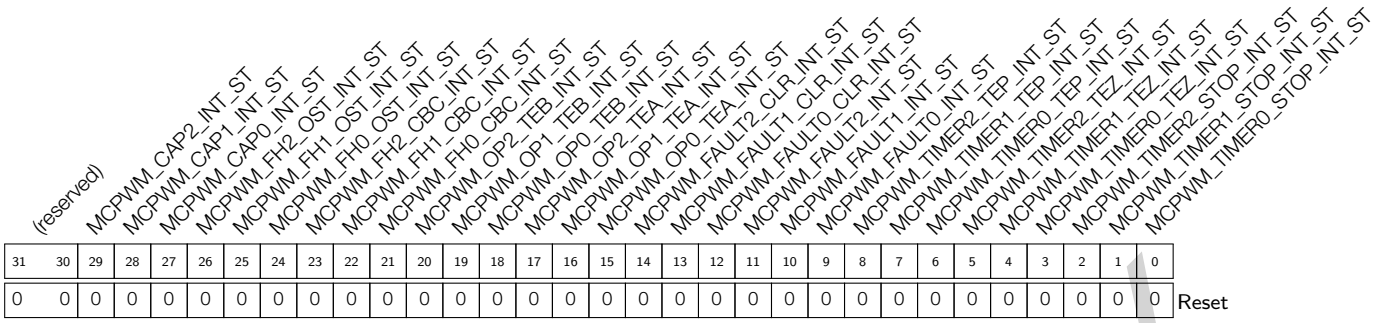
MCPWM_CAP0_INT_RAW The raw status bit for the interrupt triggered by capture on channel 0. (R/WTC/SS)

MCPWM_CAP1_INT_RAW The raw status bit for the interrupt triggered by capture on channel 1. (R/WTC/SS)

MCPWM_CAP2_INT_RAW The raw status bit for the interrupt triggered by capture on channel 2. (R/WTC/SS)

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Register 32.71. MCPWM_INT_ST_REG (0x0118)



MCPWM_TIMER0_STOP_INT_ST The masked status bit for the interrupt triggered when the timer 0 stops. (RO)

MCPWM_TIMER1_STOP_INT_ST The masked status bit for the interrupt triggered when the timer 1 stops. (RO)

MCPWM_TIMER2_STOP_INT_ST The masked status bit for the interrupt triggered when the timer 2 stops. (RO)

MCPWM_TIMER0_TEZ_INT_ST The masked status bit for the interrupt triggered by a PWM timer 0 TEZ event. (RO)

MCPWM_TIMER1_TEZ_INT_ST The masked status bit for the interrupt triggered by a PWM timer 1 TEZ event. (RO)

MCPWM_TIMER2_TEZ_INT_ST The masked status bit for the interrupt triggered by a PWM timer 2 TEZ event. (RO)

MCPWM_TIMER0_TEP_INT_ST The masked status bit for the interrupt triggered by a PWM timer 0 TEP event. (RO)

MCPWM_TIMER1_TEP_INT_ST The masked status bit for the interrupt triggered by a PWM timer 1 TEP event. (RO)

MCPWM_TIMER2_TEP_INT_ST The masked status bit for the interrupt triggered by a PWM timer 2 TEP event. (RO)

MCPWM_FAULT0_INT_ST The masked status bit for the interrupt triggered when event_f0 starts. (RO)

MCPWM_FAULT1_INT_ST The masked status bit for the interrupt triggered when event_f1 starts. (RO)

MCPWM_FAULT2_INT_ST The masked status bit for the interrupt triggered when event_f2 starts. (RO)

MCPWM_FAULT0_CLR_INT_ST The masked status bit for the interrupt triggered when event_f0 ends. (RO)

Continued on the next page...

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Register 32.71. MCPWM_INT_ST_REG (0x0118)

Continued from the previous page...

MCPWM_FAULT1_CLR_INT_ST The masked status bit for the interrupt triggered when event_f1 ends. (RO)

MCPWM_FAULT2_CLR_INT_ST The masked status bit for the interrupt triggered when event_f2 ends. (RO)

MCPWM_OP0_TEA_INT_ST The masked status bit for the interrupt triggered by a PWM operator 0 TEA event (RO)

MCPWM_OP1_TEA_INT_ST The masked status bit for the interrupt triggered by a PWM operator 1 TEA event (RO)

MCPWM_OP2_TEA_INT_ST The masked status bit for the interrupt triggered by a PWM operator 2 TEA event (RO)

MCPWM_OP0_TEB_INT_ST The masked status bit for the interrupt triggered by a PWM operator 0 TEB event (RO)

MCPWM_OP1_TEB_INT_ST The masked status bit for the interrupt triggered by a PWM operator 1 TEB event (RO)

MCPWM_OP2_TEB_INT_ST The masked status bit for the interrupt triggered by a PWM operator 2 TEB event (RO)

MCPWM_FH0_CBC_INT_ST The masked status bit for the interrupt triggered by a cycle-by-cycle mode action on PWM0. (RO)

MCPWM_FH1_CBC_INT_ST The masked status bit for the interrupt triggered by a cycle-by-cycle mode action on PWM1. (RO)

MCPWM_FH2_CBC_INT_ST The masked status bit for the interrupt triggered by a cycle-by-cycle mode action on PWM2. (RO)

MCPWM_FH0_OST_INT_ST The masked status bit for the interrupt triggered by a one-shot mode action on PWM0. (RO)

MCPWM_FH1_OST_INT_ST The masked status bit for the interrupt triggered by a one-shot mode action on PWM1. (RO)

MCPWM_FH2_OST_INT_ST The masked status bit for the interrupt triggered by a one-shot mode action on PWM2. (RO)

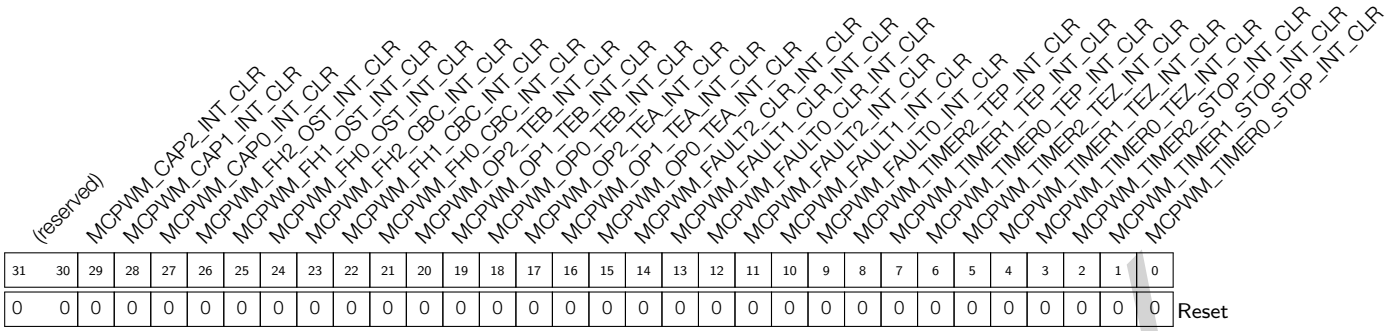
MCPWM_CAP0_INT_ST The masked status bit for the interrupt triggered by capture on channel 0. (RO)

MCPWM_CAP1_INT_ST The masked status bit for the interrupt triggered by capture on channel 1. (RO)

MCPWM_CAP2_INT_ST The masked status bit for the interrupt triggered by capture on channel 2. (RO)

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Register 32.72. MCPWM_INT_CLR_REG (0x011C)



MCPWM_TIMER0_STOP_INT_CLR Set this bit to clear the interrupt triggered when the timer 0 stops. (WT)

MCPWM_TIMER1_STOP_INT_CLR Set this bit to clear the interrupt triggered when the timer 1 stops. (WT)

MCPWM_TIMER2_STOP_INT_CLR Set this bit to clear the interrupt triggered when the timer 2 stops. (WT)

MCPWM_TIMER0_TEZ_INT_CLR Set this bit to clear the interrupt triggered by a PWM timer 0 TEZ event. (WT)

MCPWM_TIMER1_TEZ_INT_CLR Set this bit to clear the interrupt triggered by a PWM timer 1 TEZ event. (WT)

MCPWM_TIMER2_TEZ_INT_CLR Set this bit to clear the interrupt triggered by a PWM timer 2 TEZ event. (WT)

MCPWM_TIMER0_TEP_INT_CLR Set this bit to clear the interrupt triggered by a PWM timer 0 TEP event. (WT)

MCPWM_TIMER1_TEP_INT_CLR Set this bit to clear the interrupt triggered by a PWM timer 1 TEP event. (WT)

MCPWM_TIMER2_TEP_INT_CLR Set this bit to clear the interrupt triggered by a PWM timer 2 TEP event. (WT)

MCPWM_FAULT0_INT_CLR Set this bit to clear the interrupt triggered when event_f0 starts. (WT)

MCPWM_FAULT1_INT_CLR Set this bit to clear the interrupt triggered when event_f1 starts. (WT)

MCPWM_FAULT2_INT_CLR Set this bit to clear the interrupt triggered when event_f2 starts. (WT)

Continued on the next page...

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Register 32.72. MCPWM_INT_CLR_REG (0x011C)

Continued from the previous page...

MCPWM_FAULT0_CLR_INT_CLR Set this bit to clear the interrupt triggered when event_f0 ends. (WT)

MCPWM_FAULT1_CLR_INT_CLR Set this bit to clear the interrupt triggered when event_f1 ends. (WT)

MCPWM_FAULT2_CLR_INT_CLR Set this bit to clear the interrupt triggered when event_f2 ends. (WT)

MCPWM_OP0_TEA_INT_CLR Set this bit to clear the interrupt triggered by a PWM operator 0 TEA event (WT)

MCPWM_OP1_TEA_INT_CLR Set this bit to clear the interrupt triggered by a PWM operator 1 TEA event (WT)

MCPWM_OP2_TEA_INT_CLR Set this bit to clear the interrupt triggered by a PWM operator 2 TEA event (WT)

MCPWM_OP0_TEB_INT_CLR Set this bit to clear the interrupt triggered by a PWM operator 0 TEB event (WT)

MCPWM_OP1_TEB_INT_CLR Set this bit to clear the interrupt triggered by a PWM operator 1 TEB event (WT)

MCPWM_OP2_TEB_INT_CLR Set this bit to clear the interrupt triggered by a PWM operator 2 TEB event (WT)

MCPWM_FH0_CBC_INT_CLR Set this bit to clear the interrupt triggered by a cycle-by-cycle mode action on PWM0. (WT)

MCPWM_FH1_CBC_INT_CLR Set this bit to clear the interrupt triggered by a cycle-by-cycle mode action on PWM1. (WT)

MCPWM_FH2_CBC_INT_CLR Set this bit to clear the interrupt triggered by a cycle-by-cycle mode action on PWM2. (WT)

MCPWM_FH0_OST_INT_CLR Set this bit to clear the interrupt triggered by a one-shot mode action on PWM0. (WT)

MCPWM_FH1_OST_INT_CLR Set this bit to clear the interrupt triggered by a one-shot mode action on PWM1. (WT)

MCPWM_FH2_OST_INT_CLR Set this bit to clear the interrupt triggered by a one-shot mode action on PWM2. (WT)

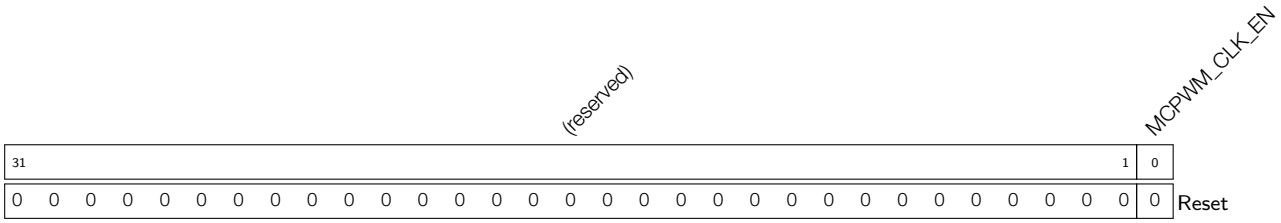
MCPWM_CAP0_INT_CLR Set this bit to clear the interrupt triggered by capture on channel 0. (WT)

MCPWM_CAP1_INT_CLR Set this bit to clear the interrupt triggered by capture on channel 1. (WT)

MCPWM_CAP2_INT_CLR Set this bit to clear the interrupt triggered by capture on channel 2. (WT)

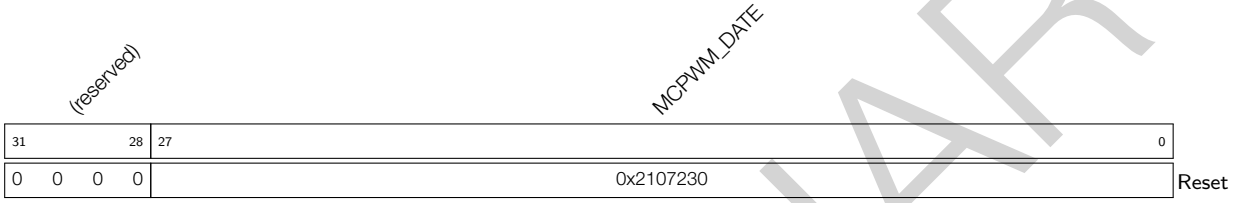
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Register 32.73. MCPWM_CLK_REG (0x0120)



MCPWM_CLK_EN Force clock on for this register file. (R/W)

Register 32.74. MCPWM_VERSION_REG (0x0124)



MCPWM_DATE Version of this register file. (R/W)

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33 Remote Control Peripheral (RMT)

33.1 Overview

The RMT module is designed to send and receive infrared remote control signals. A variety of remote control protocols can be encoded/decoded via software based on the RMT module. The RMT module converts pulse codes stored in the module's built-in RAM into output signals, or converts input signals into pulse codes and stores them in RAM. In addition, the RMT module optionally modulates its output signals with a carrier wave, or optionally demodulates and filters its input signals.

The RMT module has eight channels, numbered from zero to seven. Each channel is able to independently transmit or receive signals.

- Channel 0 ~ 3 (TX channel) are dedicated to sending signals.
- Channel 4 ~ 7 (RX channel) are dedicated to receiving signals.

Each TX/RX channel is controlled by a dedicated set of registers with the same functionality. Channel 3 and channel 7 support DMA access, so the two channels also have a set of DMA-related control and status registers. Registers for each TX channel are indicated by *n* which is used as a placeholder for the channel number, and *m* for each RX channel.

33.2 Features

- Four TX channels
- Four RX channels
- Support multiple channels (programmable) transmitting data simultaneously
- Eight channels share a 384 x 32-bit RAM
- Support modulation on TX pulses
- Support filtering and demodulation on RX pulses
- Wrap TX mode
- Wrap RX mode
- Continuous TX mode
- DMA access for TX mode on channel 3
- DMA access for RX mode on channel 7

33.3 Functional Description

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33.3.1 Architecture

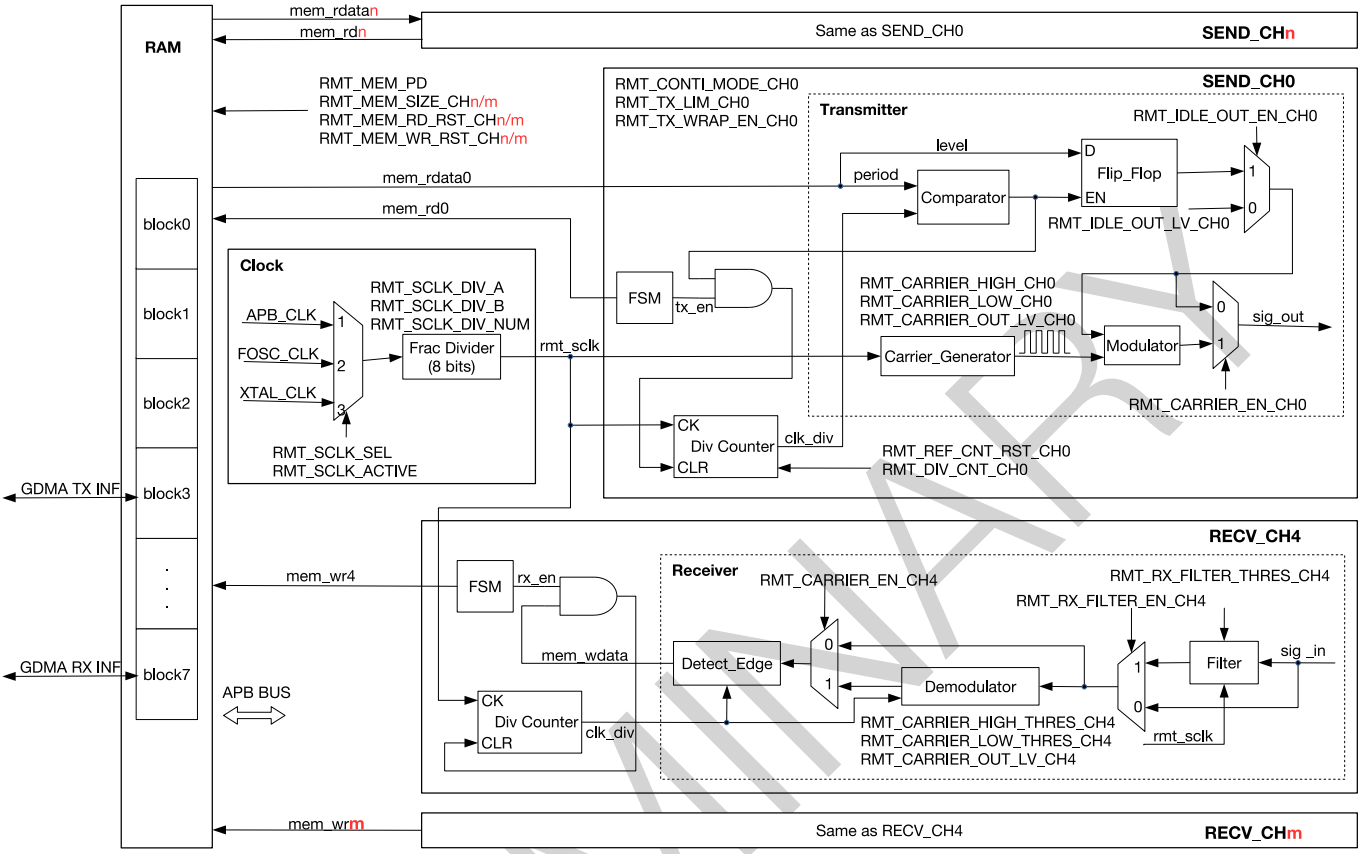


Figure 33-1. RMT Architecture

As shown in Figure 33-1, each TX channel (SEND_CH*n*) has:

- 1 x clock divider counter (Div Counter)
- 1 x state machine (FSM)
- 1 x transmitter

Each RX channel (RECV_CH*m*) has:

- 1 x clock divider counter (Div Counter)
- 1 x state machine (FSM)
- 1 x receiver

The eight channels share a 384 x 32-bit RAM.

33.3.2 RAM

33.3.2.1 RAM Architecture

Figure 33-2 shows the format of pulse code in RAM. Each pulse code contains a 16-bit entry with two fields: “level” and “period”. “level” (0 or 1) indicates a low-/high-level value was received or is going to be sent, while “period” points out the number of clock cycles (see Figure 33-1 clk_div) that the level lasts for.

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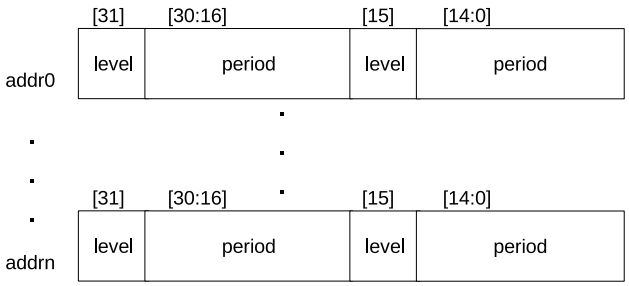


Figure 33-2. Format of Pulse Code in RAM

The minimum value for the period is zero (0) and is interpreted as a transmission end-marker. For a non-zero period (i.e., not an end-marker), its value is limited by APB clock and RMT clock according to the equation below:

$$3 \times T_{apb\_clk} + 5 \times T_{rmt\_sclk} < period \times T_{clk\_div} \qquad (1)$$

Note:

According to the equation above and the frequency of rmt_sclk, the pulse width (i.e. $period \times T_{clk\_div}$) able to be captured by RMT is limited as follows:

- the minimum value of pulse width should be larger than $(3 \times T_{apb\_clk} + 5 \times T_{rmt\_sclk})$.
- the maximum value of pulse width should be smaller than or equal to (the maximum period $\times$ the maximum T_{clk_div}), i.e., $((2^{15} - 1) \times$ the maximum $T_{rmt\_sclk} \times 256$).

For more information about rmt_sclk frequency, or APB_CLK frequency, see Section 33.3.3, or Chapter 6 *Reset and Clock*.

33.3.2.2 Use of RAM

The RAM is divided into eight 48 x 32-bit blocks. By default, each channel uses one block (block 0 for channel 0, block 1 for channel 1, and so on).

If the data size of one single transfer is larger than one block size of TX channel *n* or RX channel *m*, users can configure the channel:

- to enable wrap mode by setting RMT_MEM_TX/RX_WRAP_EN_CH*n*/*m*.
- or to use more blocks by configuring RMT_MEM_SIZE_CH*n*/*m*.

Setting RMT_MEM_SIZE_CH*n*/*m* > 1 allows channel *n*/*m* to use the memory of subsequent channels, block (*n*/*m*) ~ block (*n*/*m* + RMT_MEM_SIZE_CH*n*/*m* -1). If so, the subsequent channels *n*/*m* + 1 ~ *n*/*m* + RMT_MEM_SIZE_CH*n*/*m* - 1 can not be used once their RAM blocks are occupied. For example, if channel 0 is configured to use block 0 and block 1, then channel 1 can not be used due to its block being occupied. But channel 2 and channel 3 are not affected, and can be used normally.

Note that the RAM used by each channel is mapped from low address to high address. Under such mapping, channel 0 is able to use the RAM blocks for channels 1, 2 ... and 7 by setting RMT_MEM_SIZE_CH0, but channel 7 can not use the blocks for channels 0, 1, ... or 6. Therefore, the maximum value of RMT_MEM_SIZE_CH*n* should not exceed (8 - *n*) and the maximum of RMT_MEM_SIZE_CH*m* should not exceed (8 - *m*).

The RMT RAM can be accessed via the APB bus, read by a transmitting channel, and written to by a receiving channel. To avoid any possible access conflict between the receiver writing RAM and the APB bus reading RAM, RMT can be configured to designate the block's owner, be it the receiver or APB bus, by configuring RMT_MEM_OWNER_CH*m*. If this ownership is violated, a flag signal RMT_MEM_OWNER_ERR_CH*m* will be generated.

When the RMT module is inactive, the RAM can be put into low-power mode by setting RMT_MEM_FORCE_PD.

33.3.2.3 RAM Access

APB bus is able to access RAM in FIFO mode and in NONFIFO (Direct Address) mode, depending on the configuration of RMT_APB_FIFO_MASK:

- 1: use NONFIFO mode;
- 0: use FIFO mode.

Channels 3 and 7 also support DMA access.

FIFO Mode

In FIFO mode, the APB reads data from or writes data to RAM via a fixed address stored in RMT_CH*n*/*m*DATA_REG.

NONFIFO Mode

In NONFIFO mode, the APB writes data to or reads data from a continuous address range.

- The write-starting address of TX channel *n* is: RMT base address + 0x800 + (*n* - 1) x 48. The access address for the second data and the following data are RMT base address + 0x800 + (*n* - 1) x 48 + 0x4, and so on, incremented by 0x4.
- The read-starting address of RX channel *m* is: RMT base address + 0x8c0 + (*m* - 1) x 48. The access address for the second data and the following data are RMT base address + 0x8c0 + (*m* - 1) x 48 + 0x4, and so on, incremented by 0x4.

DMA Mode

Channel 3 also supports DMA access. If RMT_DMA_ACCESS_EN_CH3 is set, RAM of channel 3 only allows DMA access. FIFO access or NOFIFO access to channel 3 by the APB bus are forbidden, otherwise **unpredictable consequences may occur.**

To ensure correct data transmission,

1. DMA should be started first.
2. RMT can only start sending data after DMA channel gets data ready, otherwise, unexpected data may be sent.

In normal TX mode, when the RAM of channel 3 is fully written by DMA, an RMT_APB_MEM_WR_ERR_CH3 interrupt is triggered. Setting RMT_MEM_TX_WRAP_EN_CH3 allows channel 3 to transmit more data than one block can fit, with no software operation needed.

Channel 7 also supports DMA access. If RMT_DMA_ACCESS_EN_CH7 is set, the RAM of channel 7 is allowed to send data to DMA. Note in this mode, channel 7's RAM can also be accessed by APB via NONFIFO mode.

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In normal RX mode, when the size of data read by DMA from channel 7 is equal to its RAM size, an RMT_APB_MEM_RD_ERR_CH7 is triggered and the subsequent data is discarded. If RMT_MEM_RX_WRAP_EN_CH7 is set, data of more than one block size can be received with no software wrap operation needed. If channel 7's RAM is full but the DMA still does not start receiving data from the channel, the newly received data by this channel will replace the previous data.

Note:
When channel 7 receives an end-maker, a DMA in_suc_eof interrupt is generated. Two bytes are written to DMA if the period[14:0] is 0, and four bytes to DMA if the period[30:16] is 0.

33.3.3 Clock

The clock source of RMT can be APB_CLK, FOSC_CLK, or XTAL_CLK, depending on the configuration of RMT_SCLK_SEL. RMT clock can be enabled by setting RMT_SCLK_ACTIVE. RMT working clock is obtained by dividing the selected clock source with a fractional divider, see Figure 33-1. The divider is:

$$RMT\_SCLK\_DIV\_NUM + 1 + RMT\_SCLK\_DIV\_A / RMT\_SCLK\_DIV\_B$$

For more information, see Chapter 6 *Reset and Clock*. RMT_DIV_CNT_CH*n*/*m* is used to configure the divider coefficient of internal clock divider for RMT channels. The coefficient is normally equal to the value of RMT_DIV_CNT_CH*n*/*m*, except value 0 that represents divider 256. The clock divider can be reset by setting RMT_REF_CNT_RST_CH*n*/*m*. The clock generated from the divider can be used by the counter (see Figure 33-1).

33.3.4 Transmitter

Note:
Updating the configuration described in this and subsequent sections requires to set RMT_CONF_UPDATE_CH*n* first, see Section 33.3.6.

33.3.4.1 Normal TX Mode

When RMT_TX_START_CH*n* is set, the transmitter of channel *n* starts reading and sending pulse codes from the starting address of its RAM block. The codes are sent starting from low-address entry. When an end-marker (a zero period) is encountered, the transmitter stops the transmission, returns to idle state and generates an RMT_CH*n*_TX_END_INT interrupt. Setting RMT_TX_STOP_CH*n* to 1 also stops the transmission and immediately sets the transmitter back to idle. The output level of a transmitter in idle state is determined by the "level" field of the end-marker or by the content of RMT_IDLE_OUT_LV_CH*n*, depending on the configuration of RMT_IDLE_OUT_EN_CH*n*:

- 0: the level in idle state is determined by the "level" field of the end-marker.
- 1: the level is determined by RMT_IDLE_OUT_LV_CH*n*.

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33.3.4.2 Wrap TX Mode

To transmit more pulse codes than can be fitted in the channel's RAM, users can enable wrap mode by setting RMT_MEM_TX_WRAP_EN_CH*n*. In wrap mode, the transmitter sends the data from RAM in loops till an end-marker is encountered. For example, if RMT_MEM_SIZE_CH*n* = 1, the transmitter starts sending data from the address 48 * *n*, and then the data from higher RAM address. Once the transmitter finishes sending the data from (48 * (*n* + 1) - 1), it continues sending data from 48 * *n* again till encounters an end-marker. Wrap mode is also applicable for RMT_MEM_SIZE_CH*n* > 1.

When the size of transmitted pulse codes is larger than or equal to the value set by RMT_TX_LIM_CH*n*, an RMT_CH*n*_TX_THR_EVENT_INT interrupt is generated. In wrap mode, RMT_TX_LIM_CH*n* can be set to a half or a fraction of the size of the channel's RAM block. When an RMT_CH*n*_TX_THR_EVENT_INT interrupt is detected by software, the already used RAM region can be updated by new pulse codes. In such way, the transmitter can seamlessly send unlimited pulse codes in wrap mode.

Note:
If RAM is accessed by DMA mode, more pulse codes than one block size can be transmitted with no additional operation needed. If accessed by APB bus, wrap mode has to be enabled via software to send more data than one block size.

33.3.4.3 TX Modulation

Transmitter output can be modulated with a carrier wave by setting RMT_CARRIER_EN_CH*n*. The carrier waveform is configurable. In a carrier cycle, the high level lasts for (RMT_CARRIER_HIGH_CH*n* + 1) rmt_sclk cycles, while the low level lasts for (RMT_CARRIER_LOW_CH*n* + 1) rmt_sclk cycles. When RMT_CARRIER_OUT_LV_CH*n* is set, carrier wave is added on the high-level of output signals; while RMT_CARRIER_OUT_LV_CH*n* is cleared, carrier wave is added on the low-level of output signals. Carrier wave can be added on all output signals during modulation, or just added on valid pulse codes (the data stored in RAM), which can be set by configuring RMT_CARRIER_EFF_EN_CH*n*:

- 0: add carrier wave on all output signals.
- 1: add carrier wave only on valid signals.

33.3.4.4 Continuous TX Mode

The continuous TX mode can be enabled by setting RMT_TX_CONTI_MODE_CH*n*. In this mode, the transmitter sends the pulse codes from RAM in loops:

- If an end-marker is encountered, the transmitter starts transmitting from the first data of the channel's RAM again.
- If no end-marker is encountered, the transmitter starts transmitting from the first data again after the last data is transmitted.

If RMT_TX_LOOP_CNT_EN_CH*n* is set, the loop counting is incremented by 1 each time an end-marker is encountered. If the counting reaches the value set by RMT_TX_LOOP_NUM_CH*n*, an RMT_CH*n*_TX_LOOP_INT interrupt is generated. If RMT_LOOP_STOP_EN_CH*n* is set, the transmission stops immediately once an RMT_CH*n*_TX_LOOP_INT interrupt is generated, otherwise, the transmission will continue. In an end-maker, if its period[14:0] is 0, then the period of the previous data must satisfy:

$$6 \times T_{apb\_clk} + 12 \times T_{rmt\_sclk} < period \times T_{clk\_div} \qquad (2)$$

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The period of the other data only need to satisfy relation (1).

33.3.4.5 Simultaneous TX Mode

RMT module supports multiple channels transmitting data simultaneously. To use this function, follow the steps below:

1. Configure RMT_TX_SIM_CH*n* to choose which multiple channels are used to transmit data simultaneously.
2. Set RMT_TX_SIM_EN to enable this transmission mode.
3. Set RMT_TX_START_CH*n* for each selected channel, to start data transmitting.

The transmission starts once the final channel is configured. RMT module also supports simultaneous transmission of channels 0 ~ 2's RAM accessed by APB bus and channel 3's RAM accessed by DMA.

33.3.5 Receiver

33.3.5.1 Normal RX Mode

The receiver of channel *m* is controlled by RMT_RX_EN_CH*m*:

- 1: the receiver starts working.
- 0: the receiver stops receiving data.

When the receiver becomes active, it starts counting from the first edge of the signal, detecting signal levels and counting clock cycles the level lasts for. Each cycle count (period) is then written back to RAM together with the level information (level). When the receiver detects no change in a signal level for a number of clock cycles more than the value set by RMT_IDLE_THRES_CH*m*, the receiver will stop receiving data, return to idle state, and generate an RMT_CH*m*_RX_END_INT interrupt. Please note that RMT_IDLE_THRES_CH*m* should be configured to a maximum value according to your application, otherwise a valid received level may be mistaken as a level in idle state. If the RAM space of this RX channel is used up by the received data, the receiver stops receiving data, and an RMT_CH*n*_ERR_INT interrupt is triggered by RAM FULL event.

33.3.5.2 Wrap RX Mode

To receive more pulse codes than can be fitted in the channel's RAM, users can enable wrap mode for channel *m* by configuring RMT_MEM_RX_WRAP_EN_CH*m*. But if RAM is accessed by DMA mode, more pulse codes than one block size can be received with no additional operation needed. If accessed by APB bus, wrap mode has to be enabled to send more data than one block size. In wrap mode, the receiver stores the received data to RAM space of this channel in loops. Receiving ends, when the receiver detects no change in a signal level for a number of clock cycles more than the value set by RMT_IDLE_THRES_CH*m*. The receiver returns to idle state and generates an RMT_CH*m*_RX_END_INT interrupt. For example, if RMT_MEM_SIZE_CH*m* is set to 1, the receiver starts receiving data and stores the data to address 48 * *m*, and then to higher RAM address. When the receiver finishes storing the received data to (48 * (*m* + 1) - 1), the receiver continues receiving data and storing data to the address 48 * *m* again, no change is detected on a signal level for more than RMT_IDLE_THRES_CH*m* clock cycles. Wrap mode is also applicable for RMT_MEM_SIZE_CH*m* > 1.

An RMT_CH*m*_RX_THR_EVENT_INT interrupt is generated when the size of received pulse codes is larger than or equal to the value set by RMT_CH*m*_RX_LIM_REG. In wrap mode, RMT_CH*m*_RX_LIM_REG can be set to a

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half or a fraction of the size of the channel's RAM block. When an RMT_CH*m*_RX_THR_EVENT_INT interrupt is detected, the already used RAM region can be updated by subsequent data.

33.3.5.3 RX Filtering

Users can enable the receiver to filter input signals by setting RMT_RX_FILTER_EN_CH*m* for channel *m*. The filter samples input signals continuously, and detects the signals which remain unchanged for a continuous RMT_RX_FIL
TER_THRES_CH*m* rmt_sclk cycles as valid, otherwise, the signals will be detected as invalid. Only the valid signals can pass through this filter. The filter removes pulses with a length of less than RMT_RX_FILTER_THRES_CH*m* rmt_sclk cycles.

33.3.5.4 RX Demodulation

Users can enable RX demodulation on input signals or on filtered signals by setting RMT_CARRIER_EN_CH*m*. RX demodulation can be applied to high-level carrier wave or low-level carrier wave, depending on the configuration of RMT_CARRIER_OUT_LV_CH*m*:

- 1: demodulate high-level carrier wave
- 0: demodulate low-level carrier wave

Users can configure RMT_CARRIER_HIGH_THRES_CH*m* and RMT_CARRIER_LOW_THRES_CH*m* to set the thresholds to demodulate high-level carrier or low-level carrier. If the high-level of a signal lasts for less than RMT_CARRIER_HIGH_THRES_CH*m* clk_div cycles, or the low-level lasts for less than RMT_CARRIER_LOW_THRES_CH*m* clk_div cycles, such level is detected as a carrier and then is filtered out.

33.3.6 Configuration Update

To update RMT registers configuration, please set RMT_CONF_UPDATE_CH*n*/*m* for each channel first. All the bits/fields listed in the second column of Table 33-1 should follow this rule.

Table 33-1. Configuration Update

Register	Bit/Field Configuration Update
TX Channel	
RMT_CH*n*CONF0_REG	RMT_CARRIER_OUT_LV_CH*n*
	RMT_CARRIER_EN_CH*n*
	RMT_CARRIER_EFF_EN_CH*n*
	RMT_DIV_CNT_CH*n*
	RMT_TX_STOP_CH*n*
	RMT_IDLE_OUT_EN_CH*n*
	RMT_IDLE_OUT_LV_CH*n*
	RMT_TX_CONTI_MODE_CH*n*
RMT_CH*n*CARRIER_DUTY_REG	RMT_CARRIER_HIGH_CH*n*
	RMT_CARRIER_LOW_CH*n*
RMT_CH*n*_TX_LIM_REG	RMT_TX_LOOP_CNT_EN_CH*n*
	RMT_TX_LOOP_NUM_CH*n*
	RMT_TX_LIM_CH*n*

Cont'd on next page

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Table 33-1 – cont'd from previous page

Register	Bit/Field Configuration Update
RMT_TX_SIM_REG	RMT_TX_SIM_EN
RX Channel	
RMT_CH*m*CONF0_REG	RMT_CARRIER_OUT_LV_CH*m*
	RMT_CARRIER_EN_CH*m*
	RMT_IDLE_THRES_CH*m*
	RMT_DIV_CNT_CH*m*
RMT_CH*m*CONF1_REG	RMT_RX_FILTER_THRES_CH*m*
	RMT_RX_EN_CH*m*
RMT_CH*m*_RX_CARRIER_RM_REG	RMT_CARRIER_HIGH_THRES_CH*m*
	RMT_CARRIER_LOW_THRES_CH*m*
RMT_CH*m*_RX_LIM_REG	RMT_RX_LIM_CH*m*
RMT_REF_CNT_RST_REG	RMT_REF_CNT_RST_CH*m*

33.4 Interrupts

- RMT_CH*n*/*m*_ERR_INT: triggered when channel *n*/*m* does not read or write data correctly. For example, the receiver still tries to write data into RAM when the RAM is full. Or the transmitter still tries to read data from RAM when the RAM is empty.
- RMT_CH*n*_TX_THR_EVENT_INT: triggered when the amount of data the transmitter has sent matches the value of RMT_CH*n*_TX_LIM_REG.
- RMT_CH*m*_RX_THR_EVENT_INT: triggered each time when the amount of data received by the receiver reaches the value set in RMT_CH*m*_RX_LIM_REG.
- RMT_CH*n*_TX_END_INT: triggered when the transmitter has finished transmitting signals.
- RMT_CH*m*_RX_END_INT: triggered when the receiver has finished receiving signals.
- RMT_CH*n*_TX_LOOP_INT: triggered when the loop counting reaches the value set by RMT_TX_LOOP_NUM _CH*n* in continuous TX mode.
- RMT_CH3_DMA_ACCESS_FAIL_INT: triggered when the result of (the entries written to channel 3's RAM - the entries transmitted by channel 3) is larger than channel 3's RAM size, but DAM keeps writing data to this channel.
- RMT_CH7_DMA_ACCESS_FAIL_INT: triggered when the result of (the entries received by channel 7's RAM - the entries read by DMA) is larger than channel 7's RAM size, but channel 7 keeps receiving data.

33.5 Register Summary

The addresses in this section are relative to RMT base address provided in Table 3-3 in Chapter 3 *System and Memory* .

Name	Description	Address	Access
FIFO R/W Register			

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Name	Description	Address	Access
RMT_CH0DATA_REG	The read and write data register for channel 0 by APB FIFO access	0x0000	RO
RMT_CH1DATA_REG	The read and write data register for channel 1 by APB FIFO access	0x0004	RO
RMT_CH2DATA_REG	The read and write data register for channel 2 by APB FIFO access	0x0008	RO
RMT_CH3DATA_REG	The read and write data register for channel 3 by APB FIFO access	0x000C	RO
RMT_CH4DATA_REG	The read and write data register for channel 4 by APB FIFO access	0x0010	RO
RMT_CH5DATA_REG	The read and write data register for channel 5 by APB FIFO access	0x0014	RO
RMT_CH6DATA_REG	The read and write data register for channel 6 by APB FIFO access	0x0018	RO
RMT_CH7DATA_REG	The read and write data register for channel 7 by APB FIFO access	0x001C	RO
Configuration Registers			
RMT_CH0CONF0_REG	Configuration register 0 for channel 0	0x0020	varies
RMT_CH1CONF0_REG	Configuration register 0 for channel 1	0x0024	varies
RMT_CH2CONF0_REG	Configuration register 0 for channel 2	0x0028	varies
RMT_CH3CONF0_REG	Configuration register 0 for channel 3	0x002C	varies
RMT_CH4CONF0_REG	Configuration register 0 for channel 4	0x0030	R/W
RMT_CH4CONF1_REG	Configuration register 1 for channel 4	0x0034	varies
RMT_CH5CONF0_REG	Configuration register 0 for channel 5	0x0038	R/W
RMT_CH5CONF1_REG	Configuration register 1 for channel 5	0x003C	varies
RMT_CH6CONF0_REG	Configuration register 0 for channel 6	0x0040	R/W
RMT_CH6CONF1_REG	Configuration register 1 for channel 6	0x0044	varies
RMT_CH7CONF0_REG	Configuration register 0 for channel 7	0x0048	R/W
RMT_CH7CONF1_REG	Configuration register 1 for channel 7	0x004C	varies
RMT_CH4_RX_CARRIER_RM_REG	Demodulation register for channel 4	0x0090	R/W
RMT_CH5_RX_CARRIER_RM_REG	Demodulation register for channel 5	0x0094	R/W
RMT_CH6_RX_CARRIER_RM_REG	Demodulation register for channel 6	0x0098	R/W
RMT_CH7_RX_CARRIER_RM_REG	Demodulation register for channel 7	0x009C	R/W
RMT_SYS_CONF_REG	Configuration register for RMT APB	0x00C0	R/W
RMT_REF_CNT_RST_REG	Reset register for RMT clock divider	0x00C8	WT
Status Registers			
RMT_CH0STATUS_REG	Channel 0 status register	0x0050	RO
RMT_CH1STATUS_REG	Channel 1 status register	0x0054	RO
RMT_CH2STATUS_REG	Channel 2 status register	0x0058	RO
RMT_CH3STATUS_REG	Channel 3 status register	0x005C	RO
RMT_CH4STATUS_REG	Channel 4 status register	0x0060	RO
RMT_CH5STATUS_REG	Channel 5 status register	0x0064	RO
RMT_CH6STATUS_REG	Channel 6 status register	0x0068	RO

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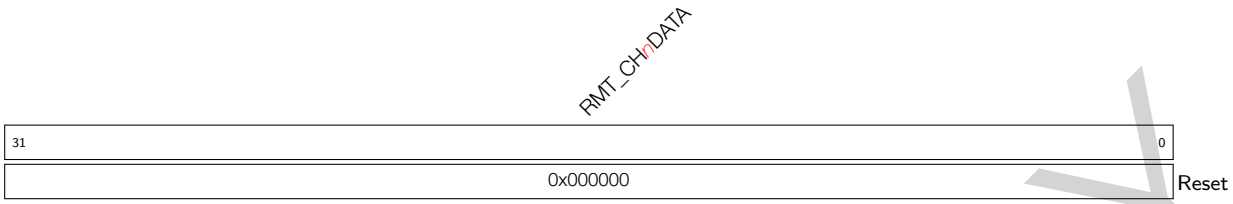
Name	Description	Address	Access
RMT_CH7STATUS_REG	Channel 7 status register	0x006C	RO
Interrupt Registers			
RMT_INT_RAW_REG	Raw interrupt status register	0x0070	R/WTC/SS
RMT_INT_ST_REG	Masked interrupt status register	0x0074	RO
RMT_INT_ENA_REG	Interrupt enable register	0x0078	R/W
RMT_INT_CLR_REG	Interrupt clear register	0x007C	WT
Carrier Wave Duty Cycle Registers			
RMT_CH0CARRIER_DUTY_REG	Duty duty configuration register for channel 0	0x0080	R/W
RMT_CH1CARRIER_DUTY_REG	Duty duty configuration register for channel 1	0x0084	R/W
RMT_CH2CARRIER_DUTY_REG	Duty duty configuration register for channel 2	0x0088	R/W
RMT_CH3CARRIER_DUTY_REG	Duty duty configuration register for channel 3	0x008C	R/W
TX Event Configuration Registers			
RMT_CH0_TX_LIM_REG	Configuration register for channel 0 TX event	0x00A0	varies
RMT_CH1_TX_LIM_REG	Configuration register for channel 1 TX event	0x00A4	varies
RMT_CH2_TX_LIM_REG	Configuration register for channel 2 TX event	0x00A8	varies
RMT_CH3_TX_LIM_REG	Configuration register for channel 3 TX event	0x00AC	varies
RMT_TX_SIM_REG	RMT simultaneous TX register	0x00C4	R/W
RX Event Configuration Registers			
RMT_CH4_RX_LIM_REG	Configuration register for channel 4 RX event	0x00B0	R/W
RMT_CH5_RX_LIM_REG	Configuration register for channel 5 RX event	0x00B4	R/W
RMT_CH6_RX_LIM_REG	Configuration register for channel 6 RX event	0x00B8	R/W
RMT_CH7_RX_LIM_REG	Configuration register for channel 7 RX event	0x00BC	R/W
Version Register			
RMT_DATE_REG	Version control register	0x00CC	R/W

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33.6 Registers

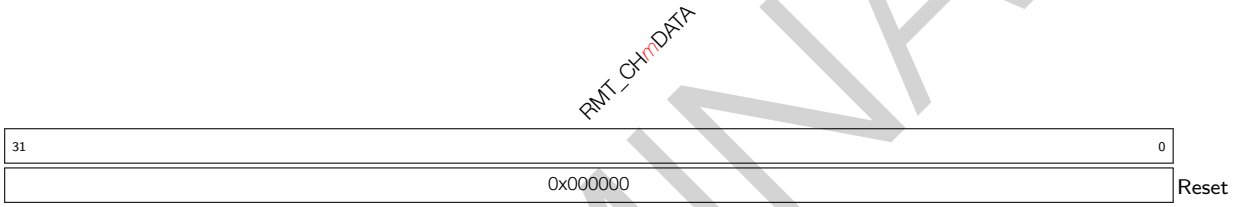
The addresses in this section are relative to RMT base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 33.1. RMT_CH*n*DATA_REG (*n*: 0-3) (0x0000+0x4n*)**



RMT_CH*n*DATA Read and write data for channel *n* via APB FIFO. (RO)

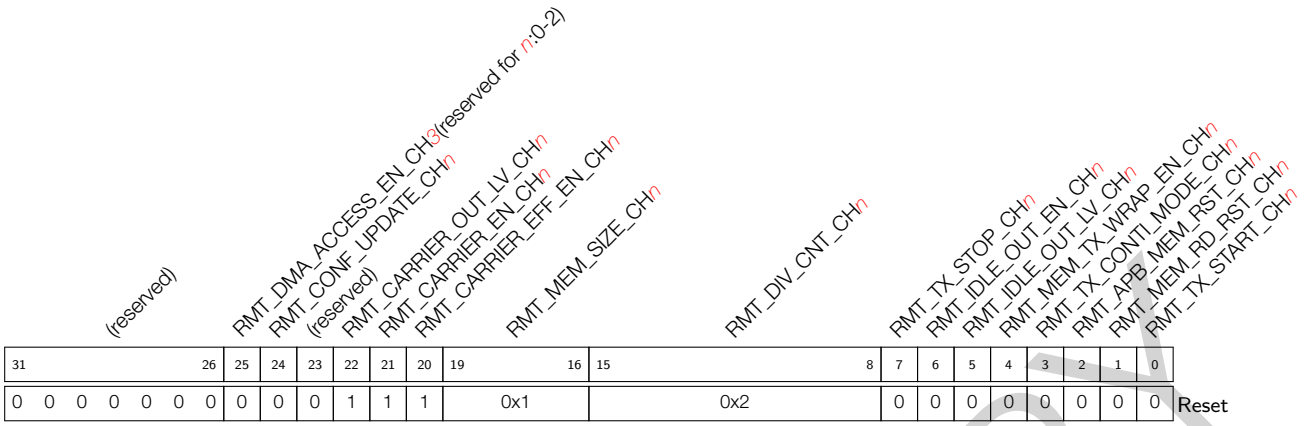
Register 33.2. RMT_CH*m*DATA_REG (*m* = 4, 5, 6, 7) (0x0010, 0x0014, 0x0018, 0x001C)



RMT_CH*m*DATA Read and write data for channel *m* via APB FIFO. (RO)

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Register 33.3. RMT_CH*n*CONF0_REG (*n*: 0-3) (0x0020+0x4n*)**



RMT_TX_START_CH*n* Set this bit to start sending data in channel *n*. (WT)

RMT_MEM_RD_RST_CH*n* Set this bit to reset RAM read address accessed by the transmitter of channel *n*. (WT)

RMT_APB_MEM_RST_CH*n* Set this bit to reset RAM W/R address for channel *n* when accessed by APB FIFO. (WT)

RMT_TX_CONTI_MODE_CH*n* Set this bit to enable continuous TX mode for channel *n*. (R/W)

In this mode, the transmitter starts its transmission from the first data, and in the following transmission:

- if an end-marker is encountered, the transmitter starts transmitting data from the first data again;
- if no end-marker is encountered, the transmitter starts transmitting the first data again when the last data is transmitted.

RMT_MEM_TX_WRAP_EN_CH*n* Set this bit to enable wrap TX mode for channel *n*. In this mode, if the TX data size is larger than the channel's RAM block size, the transmitter continues transmitting the first data again to the last data in loops. (R/W)

RMT_IDLE_OUT_LV_CH*n* This bit configures the level of output signal for channel *n* when the transmitter is in idle state. (R/W)

RMT_IDLE_OUT_EN_CH*n* This is the output enable-bit for channel *n* in idle state. 0: the output level in idle state is determined by the level field of an end-marker. 1: the output level in idle state is determined by RMT_IDLE_OUT_LV_CH*n*. (R/W)

RMT_TX_STOP_CH*n* Set this bit to stop the transmitter of channel *n* sending data out. (R/W/SC)

RMT_DIV_CNT_CH*n* This field is used to configure the divider for clock of channel *n*. (R/W)

RMT_MEM_SIZE_CH*n* This field is used to configure the maximum number of memory blocks allocated to channel *n*. (R/W)

RMT_CARRIER_EFF_EN_CH*n* 1: Add carrier modulation on the output signal only at data-sending state for channel *n*. 0: Add carrier modulation on the output signal at data-sending state and idle state for channel *n*. Only valid when RMT_CARRIER_EN_CH*n* is 1. (R/W)

Continued on the next page...

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Register 33.3. RMT_CH*n*CONF0_REG (*n*: 0-3) (0x0020+0x4n*)**

Continued from the previous page...

RMT_CARRIER_EN_CH*n* This is the carrier modulation enable-bit for channel *n*. 1: Add carrier modulation on the output signal. 0: No carrier modulation is added on output signal. (R/W)

RMT_CARRIER_OUT_LV_CH*n* This bit is used to configure the position of carrier wave for channel *n*. (R/W)

1'h0: add carrier wave on low level.

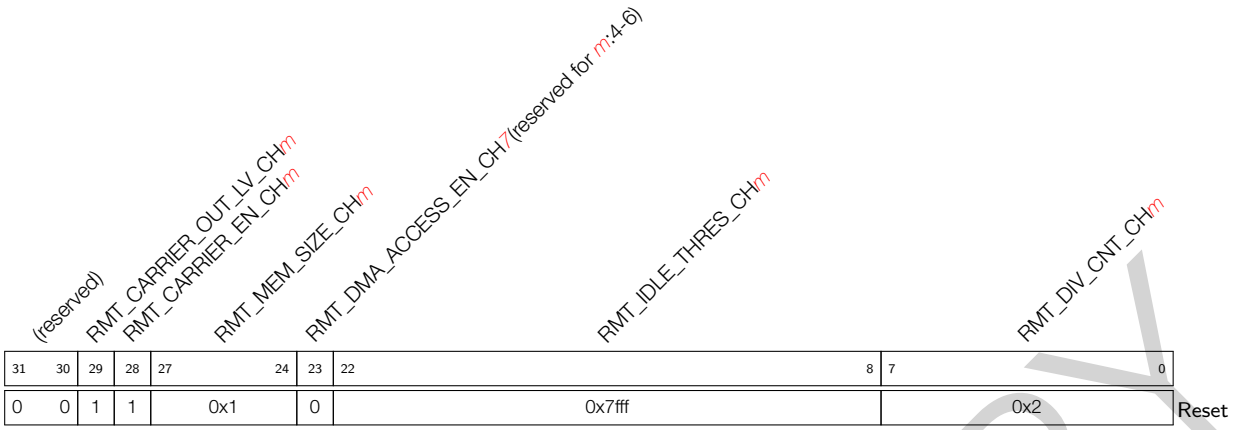
1'h1: add carrier wave on high level.

RMT_CONF_UPDATE_CH*n* Synchronization bit for channel *n* (WT)

RMT_DMA_ACCESS_EN_CH3 (Reserved for channel 0 - 2) DMA access enable bit for channel 3. (R/W)

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Register 33.4. RMT_CH*m*CONF0_REG (*m* = 4, 5, 6, 7) (0x0030, 0x0038, 0x0040, 0x0048)



RMT_DIV_CNT_CH*m* This field is used to configure the clock divider of channel *m*. (R/W)

RMT_IDLE_THRES_CH*m* This field is used to configure RX threshold. When no edge is detected on the input signal for continuous clock cycles longer than this field value, the receiver stops receiving data. (R/W)

RMT_DMA_ACCESS_EN_CH7 (Reserved for channel 4 - 6) DMA access enable bit for channel 7. (R/W)

RMT_MEM_SIZE_CH*m* This field is used to configure the maximum number of memory blocks allocated to channel *m*. (R/W)

RMT_CARRIER_EN_CH*m* This is the carrier demodulation enable-bit for channel *m*. 1: enable carrier demodulation for input signal. 0: disable carrier modulation for input signal. (R/W)

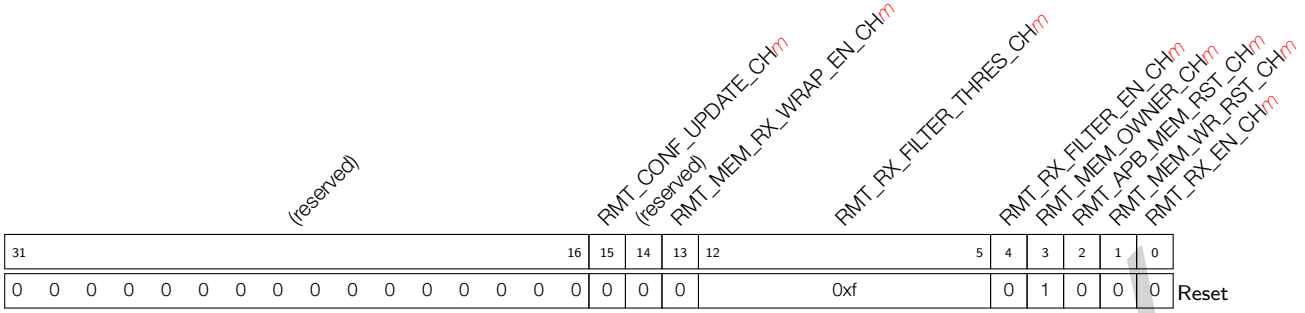
RMT_CARRIER_OUT_LV_CH*m* This bit is used to configure the position of carrier demodulation for channel *m*. (R/W)

1'h0: demodulate low-level carrier wave.

1'h1: demodulate high-level carrier wave.

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Register 33.5. RMT_CH*m*CONF1_REG (*m* = 4, 5, 6, 7) (0x0034, 0x003C, 0x0044, 0x004C)



RMT_RX_EN_CH*m* Set this bit to enable the receiver to start receiving data on channel *m*. (R/W)

RMT_MEM_WR_RST_CH*m* Set this bit to reset RAM write address accessed by the receiver for channel *m*. (WT)

RMT_APB_MEM_RST_CH*m* Set this bit to reset RAM W/R address accessed by APB FIFO for channel *m*. (WT)

RMT_MEM_OWNER_CH*m* This bit marks the ownership of channel *m*'s RAM block. (R/W/SC)

1'h1: Receiver is using the RAM.

1'h0: APB bus is using the RAM.

RMT_RX_FILTER_EN_CH*m* Set this bit to enable the receiver's filter for channel *m*. (R/W)

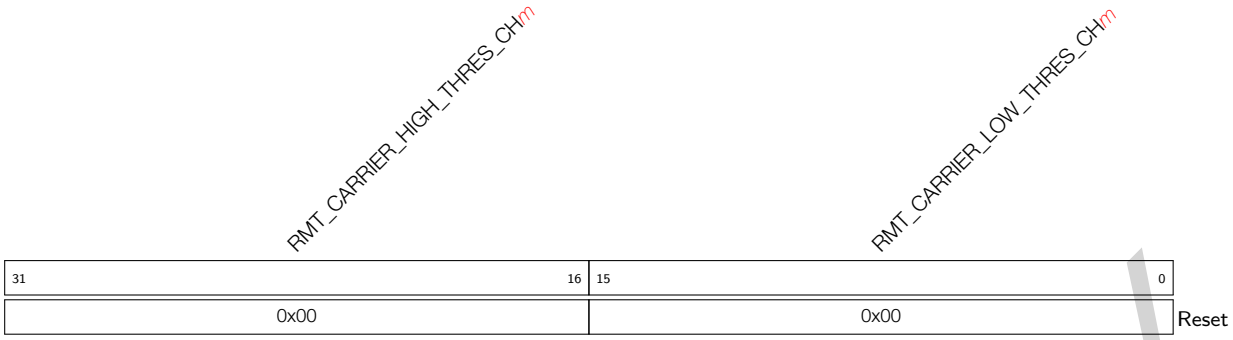
RMT_RX_FILTER_THRES_CH*m* When receiving data, the receiver ignores the input pulse when its width is shorter than this register value in units of rmt_sclk cycles. (R/W)

RMT_MEM_RX_WRAP_EN_CH*m* Set this bit to enable wrap RX mode for channel *m*. In this mode, if the RX data size is larger than channel *m* 's RAM block size, the receiver stores the RX data from the first address to the last address in loops. (R/W)

RMT_CONF_UPDATE_CH*m* Synchronization bit for channel *m*. (WT)

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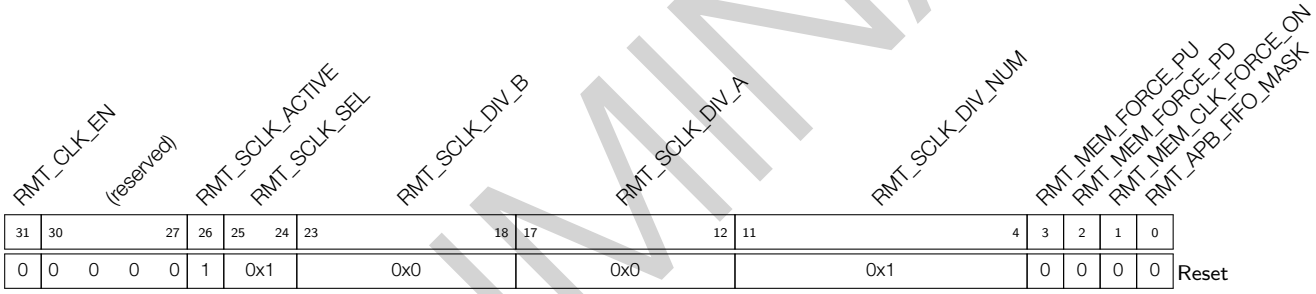
Register 33.6. RMT_CH*m*_RX_CARRIER_RM_REG (*m* = 4, 5, 6, 7) (0x0090, 0x0094, 0x0098, 0x009C)



RMT_CARRIER_LOW_THRES_CH*m* The low level period in a carrier modulation mode is (RMT_CARRIER_LOW_THRES_CH*m* + 1) for channel *m*. (R/W)

RMT_CARRIER_HIGH_THRES_CH*m* The high level period in a carrier modulation mode is (RMT_CARRIER_HIGH_THRES_CH*m* + 1) for channel *m*. (R/W)

Register 33.7. RMT_SYS_CONF_REG (0x00C0)



RMT_APB_FIFO_MASK 1'h1: Access memory directly (NONFIFO mode). 1'h0: Access memory by FIFO (FIFO mode). (R/W)

RMT_MEM_CLK_FORCE_ON Set this bit to enable the clock for RMT memory. (R/W)

RMT_MEM_FORCE_PD Set this bit to power down RMT memory. (R/W)

RMT_MEM_FORCE_PU 1: Disable the power-down function of RMT memory in Light-sleep. 0: Power down RMT memory when RMT is in Light-sleep mode. (R/W)

RMT_SCLK_DIV_NUM The integral part of the fractional divider. (R/W)

RMT_SCLK_DIV_A The numerator of the fractional part of the fractional divider. (R/W)

RMT_SCLK_DIV_B The denominator of the fractional part of the fractional divider. (R/W)

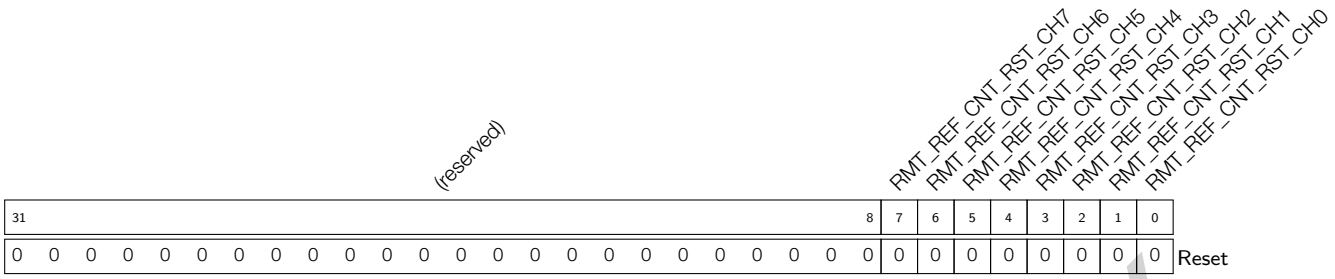
RMT_SCLK_SEL Choose the clock source of rmt_sclk. 1: APB_CLK; 2: FOSC_CLK; 3: XTAL_CLK. (R/W)

RMT_SCLK_ACTIVE rmt_sclk switch. (R/W)

RMT_CLK_EN The enable signal of RMT register clock gate. 1: Power up the drive clock of registers. 0: Power down the drive clock of registers. (R/W)

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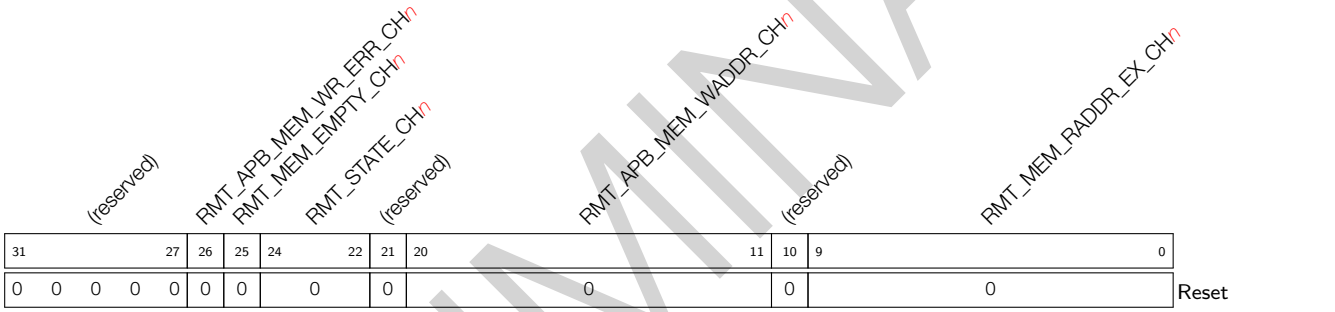
Register 33.8. RMT_REF_CNT_RST_REG (0x00C8)



RMT_REF_CNT_RST_CH*n*(*n* = 0, 1, 2, 3) This bit is used to reset the clock divider of channel *n*. (WT)

RMT_REF_CNT_RST_CH*m* (*m* = 4, 5, 6, 7) This bit is used to reset the clock divider of channel *m*. (WT)

Register 33.9. RMT_CH*n*STATUS_REG (*n*: 0-3) (0x0050+0x4n*)**



RMT_MEM_RADDR_EX_CH*n* This field records the memory address offset when transmitter of channel *n* is using the RAM. (RO)

RMT_APB_MEM_WADDR_CH*n* This field records the memory address offset when writes RAM over APB bus. (RO)

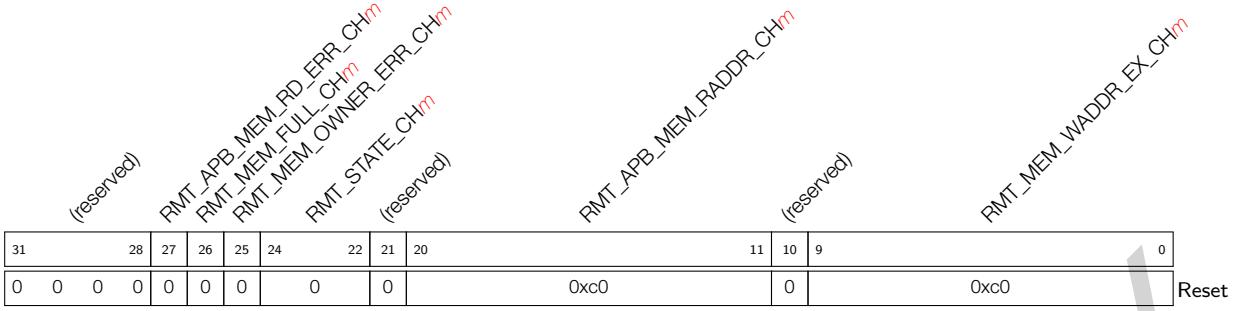
RMT_STATE_CH*n* This field records the FSM status of channel *n*. (RO)

RMT_MEM_EMPTY_CH*n* This status bit will be set when the TX data size is larger than the memory size and the wrap TX mode is disabled. (RO)

RMT_APB_MEM_WR_ERR_CH*n* This status bit will be set if the offset address is out of memory size (overflows) when writes via APB bus. (RO)

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Register 33.10. RMT_CH*m*STATUS_REG (*m* = 4, 5, 6, 7) (0x0060, 0x0064, 0x0068, 0x006C)



RMT_MEM_WADDR_EX_CH*m* This field records the memory address offset when receiver of channel *m* is using the RAM. (RO)

RMT_APB_MEM_RADDR_CH*m* This field records the memory address offset when reads RAM over APB bus. (RO)

RMT_STATE_CH*m* This field records the FSM status of channel *m*. (RO)

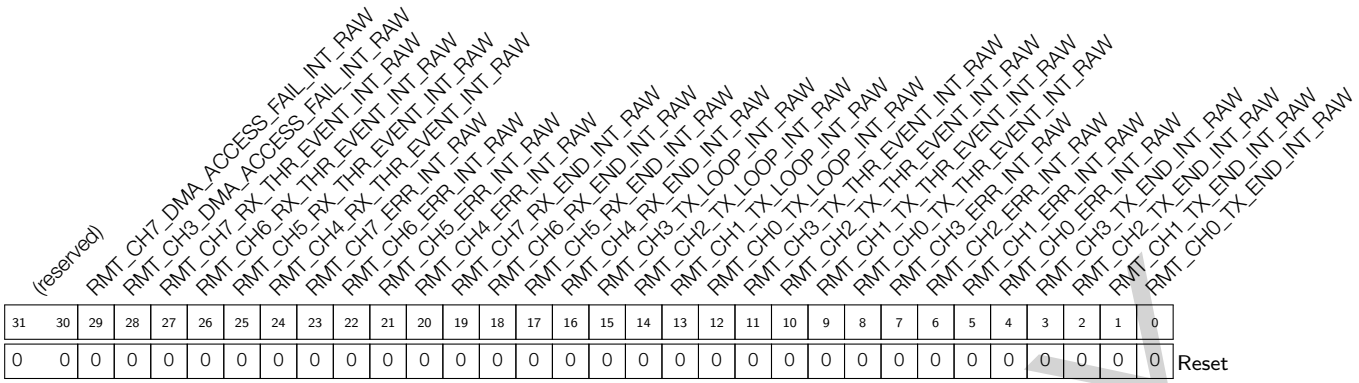
RMT_MEM_OWNER_ERR_CH*m* This status bit will be set when the ownership of memory block is wrong. (RO)

RMT_MEM_FULL_CH*m* This status bit will be set if the receiver receives more data than the memory can fit. (RO)

RMT_APB_MEM_RD_ERR_CH*m* This status bit will be set if the offset address is out of memory size (overflows) when reads RAM via APB bus. (RO)

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Register 33.11. RMT_INT_RAW_REG (0x0070)



RMT_CH*n*_TX_END_INT_RAW (*n* = 0-3) The interrupt raw bit of RMT_CH*n*_TX_END_INT. (R/WTC/SS)

RMT_CH*n*_ERR_INT_RAW (*n* = 0-3) The interrupt raw bit of RMT_CH*n*_ERR_INT. (R/WTC/SS)

RMT_CH*n*_TX_THR_EVENT_INT_RAW (*n* = 0-3) The interrupt raw bit of RMT_CH*n*_TX_THR_EVENT_INT (R/WTC/SS)

RMT_CH*n*_TX_LOOP_INT_RAW (*n* = 0-3) The interrupt raw bit of RMT_CH*n*_TX_LOOP_INT. (R/WTC/SS)

RMT_CH*m*_RX_END_INT_RAW(*m* = 4-7) The interrupt raw bit of RMT_CH*m*_RX_END_INT. (R/WTC/SS)

RMT_CH*m*_ERR_INT_RAW (*m* = 4-7) The interrupt raw bit of RMT_CH*m*_ERR_INT. (R/WTC/SS)

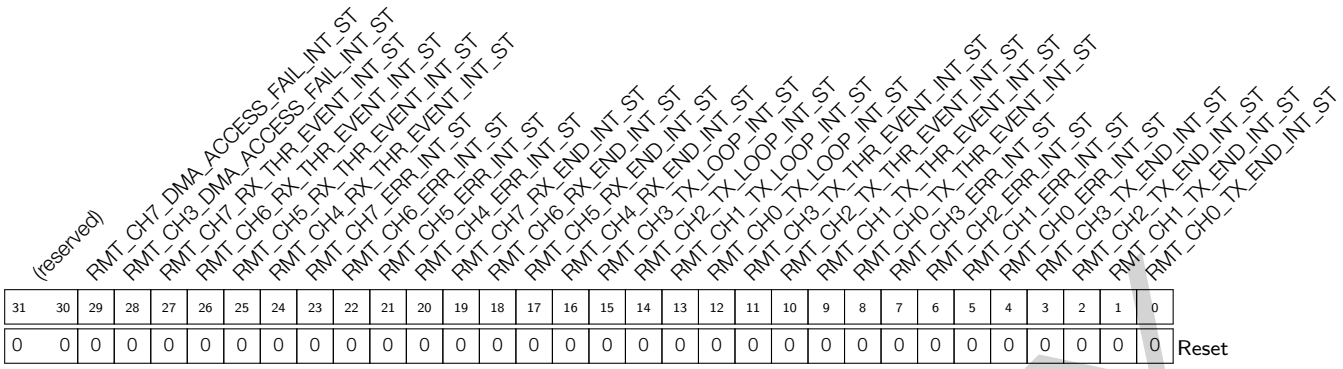
RMT_CH*m*_RX_THR_EVENT_INT_RAW(*m* = 4-7) The interrupt raw bit of RMT_CH*m*_RX_THR_EVENT_INT. (R/WTC/SS)

RMT_CH3_DMA_ACCESS_FAIL_INT_RAW The interrupt raw bit of RMT_CH3_DMA_ACCESS_FAIL_INT. (R/WTC/SS)

RMT_CH7_DMA_ACCESS_FAIL_INT_RAW The interrupt raw bit of RMT_CH7_DMA_ACCESS_FAIL_INT. (R/WTC/SS)

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Register 33.12. RMT_INT_ST_REG (0x0074)



RMT_CH*n*_TX_END_INT_ST (*n* = 0-3) The masked interrupt status bit of RMT_CH*n*_TX_END_INT. (RO)

RMT_CH*n*_ERR_INT_ST (*n* = 0-3) The masked interrupt status bit of RMT_CH*n*_ERR_INT. (RO)

RMT_CH*n*_TX_THR_EVENT_INT_ST (*n* = 0-3) The masked interrupt status bit of RMT_CH*n*_TX_THR_EVENT_INT. (RO)

RMT_CH*n*_TX_LOOP_INT_ST (*n* = 0-3) The masked interrupt status bit of RMT_CH*n*_TX_LOOP_INT. (RO)

RMT_CH*m*_RX_END_INT_ST (*m* = 4-7) The masked interrupt status bit of RMT_CH*m*_RX_END_INT. (RO)

RMT_CH*m*_ERR_INT_ST (*m* = 4-7) The masked interrupt status bit of RMT_CH*m*_ERR_INT. (RO)

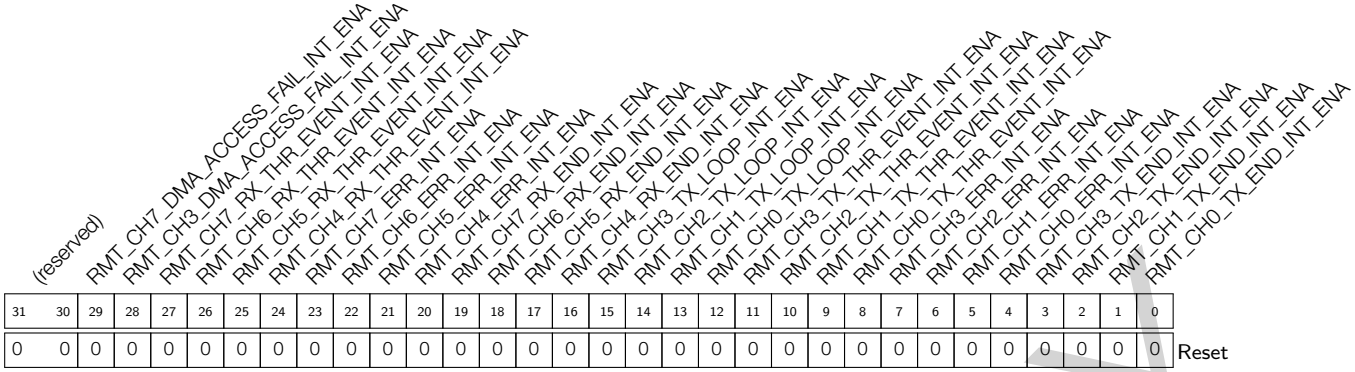
RMT_CH*m*_RX_THR_EVENT_INT_ST (*m* = 4-7) The masked interrupt status bit of RMT_CH*m*_RX_THR_EVENT_INT. (RO)

RMT_CH3_DMA_ACCESS_FAIL_INT_ST The masked interrupt status bit of RMT_CH3_DMA_ACCESS_FAIL_INT. (RO)

RMT_CH7_DMA_ACCESS_FAIL_INT_ST The masked interrupt status bit of RMT_CH7_DMA_ACCESS_FAIL_INT. (RO)

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Register 33.13. RMT_INT_ENA_REG (0x0078)



RMT_CH*n*_TX_END_INT_ENA (*n* = 0-3) The interrupt enable bit of RMT_CH*n*_TX_END_INT. (R/W)

RMT_CH*n*_ERR_INT_ENA (*n* = 0-3) The interrupt enable bit of RMT_CH*n*_ERR_INT. (R/W)

RMT_CH*n*_TX_THR_EVENT_INT_ENA (*n* = 0-3) The interrupt enable bit of RMT_CH*n*_TX_THR_EVENT_INT. (R/W)

RMT_CH*n*_TX_LOOP_INT_ENA (*n* = 0-3) The interrupt enable bit of RMT_CH*n*_TX_LOOP_INT. (R/W)

RMT_CH*m*_RX_END_INT_ENA (*m* = 4-7) The interrupt enable bit of RMT_CH*m*_RX_END_INT. (R/W)

RMT_CH*m*_ERR_INT_ENA (*m* = 4-7) The interrupt enable bit of RMT_CH*m*_ERR_INT. (R/W)

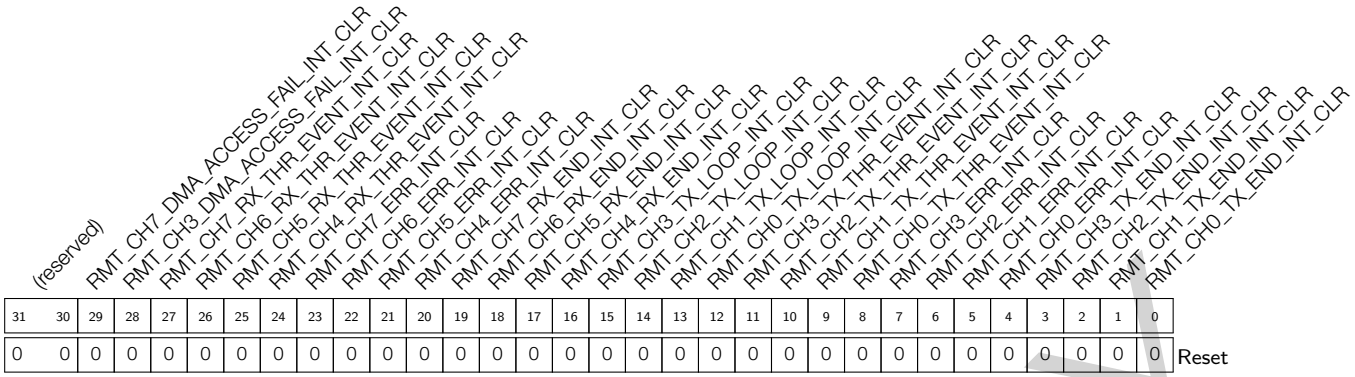
RMT_CH*m*_RX_THR_EVENT_INT_ENA (*m* = 4-7) The interrupt enable bit of RMT_CH*m*_RX_THR_EVENT_INT. (R/W)

RMT_CH3_DMA_ACCESS_FAIL_INT_ENA The interrupt enable bit of RMT_CH3_DMA_ACCESS_FAIL_INT. (R/W)

RMT_CH7_DMA_ACCESS_FAIL_INT_ENA The interrupt enable bit of RMT_CH7_DMA_ACCESS_FAIL_INT. (R/W)

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Register 33.14. RMT_INT_CLR_REG (0x007C)



RMT_CH*n*_TX_END_INT_CLR (*n* = 0-3) Set this bit to clear RMT_CH*n*_TX_END_INT interrupt. (WT)

RMT_CH*n*_ERR_INT_CLR (*n* = 0-3) Set this bit to clear RMT_CH*n*_ERR_INT interrupt. (WT)

RMT_CH*n*_TX_THR_EVENT_INT_CLR (*n* = 0-3) Set this bit to clear RMT_CH*n*_TX_THR_EVENT_INT interrupt. (WT)

RMT_CH*n*_TX_LOOP_INT_CLR (*n* = 0-3) Set this bit to clear RMT_CH*n*_TX_LOOP_INT interrupt. (WT)

RMT_CH*m*_RX_END_INT_CLR (*m* = 4-7) Set this bit to clear RMT_CH*m*_RX_END_INT interrupt. (WT)

RMT_CH*m*_ERR_INT_CLR (*m* = 4-7) Set this bit to clear RMT_CH*m*_ERR_INT interrupt. (WT)

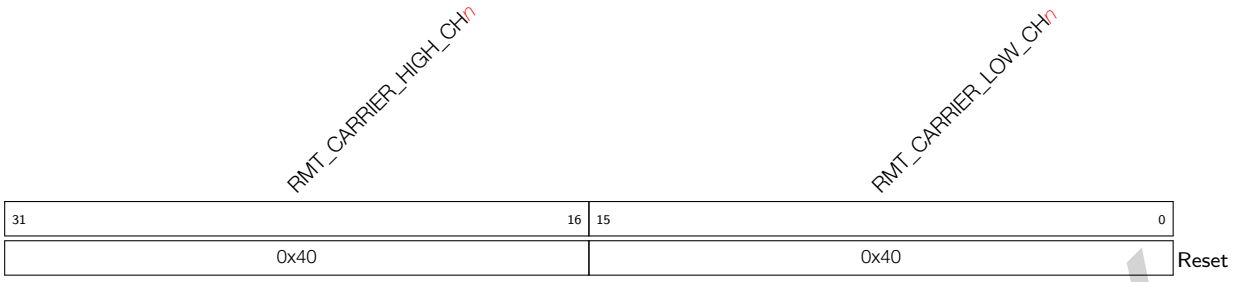
RMT_CH*m*_RX_THR_EVENT_INT_CLR (*m* = 4-7) Set this bit to clear RMT_CH*m*_RX_THR_EVENT_INT interrupt. (WT)

RMT_CH3_DMA_ACCESS_FAIL_INT_CLR Set this bit to clear RMT_CH3_DMA_ACCESS_FAIL_INT interrupt. (WT)

RMT_CH7_DMA_ACCESS_FAIL_INT_CLR Set this bit to clear RMT_CH7_DMA_ACCESS_FAIL_INT interrupt. (WT)

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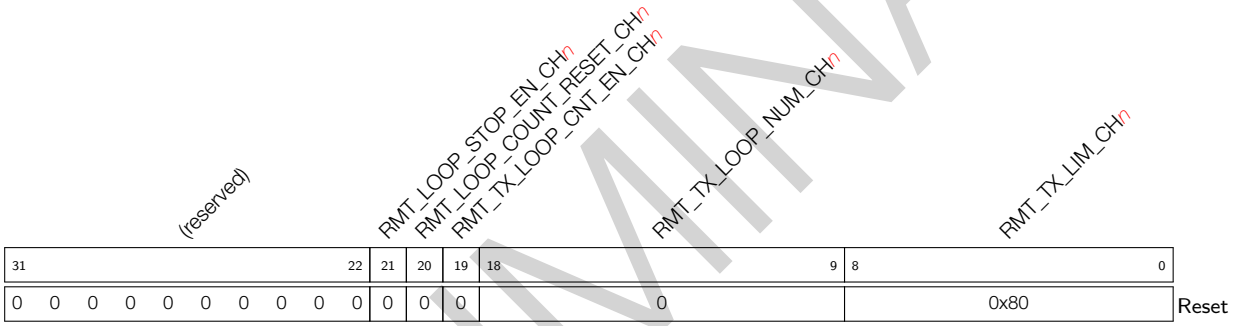
Register 33.15. RMT_CH*n*CARRIER_DUTY_REG (*n*: 0-3) (0x0080+0x4n*)**



RMT_CARRIER_LOW_CH*n* This field is used to configure carrier wave's low level clock period for channel *n*. (R/W)

RMT_CARRIER_HIGH_CH*n* This field is used to configure carrier wave's high level clock period for channel *n*. (R/W)

Register 33.16. RMT_CH*n*_TX_LIM_REG (*n*: 0-3) (0x00A0+0x4n*)**



RMT_TX_LIM_CH*n* This field is used to configure the maximum entries that channel *n* can send out. (R/W)

RMT_TX_LOOP_NUM_CH*n* This field is used to configure the maximum loop count when continuous TX mode is enabled. (R/W)

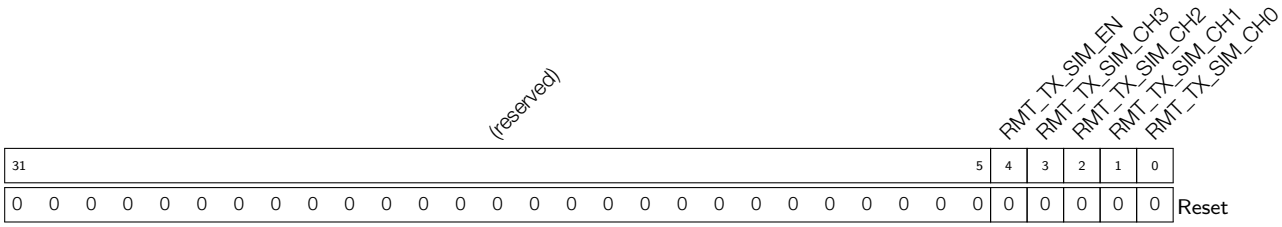
RMT_TX_LOOP_CNT_EN_CH*n* This bit is the enable bit for loop counting. (R/W)

RMT_LOOP_COUNT_RESET_CH*n* This bit is used to reset the loop count when continuous TX mode is enabled. (WT)

RMT_LOOP_STOP_EN_CH*n* Set this bit, if the loop counting reaches the value set in RMT_TX_LOOP_CNT_EN_CH*n*, continuous TX mode will be stopped. (R/W)

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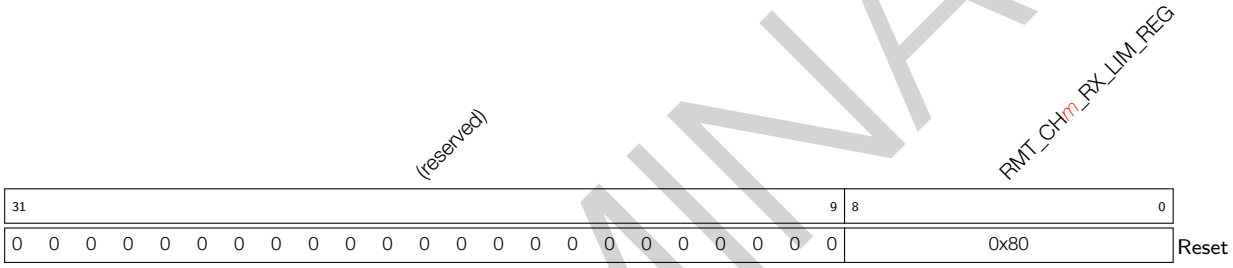
Register 33.17. RMT_TX_SIM_REG (0x00C4)



RMT_TX_SIM_CH*n* (*n* = 0-3) Set this bit to enable channel *n* to start sending data simultaneously with other enabled channels. (R/W)

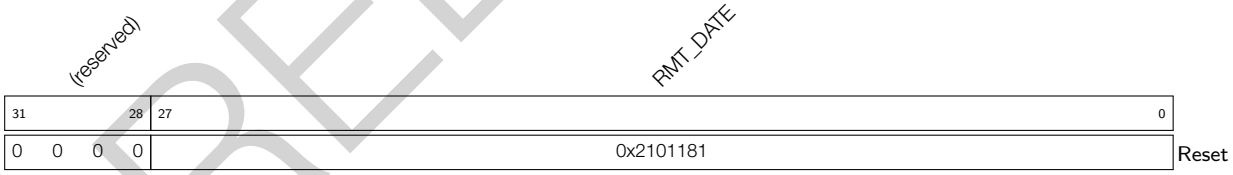
RMT_TX_SIM_EN This bit is used to enable multiple channels to start sending data simultaneously. (R/W)

Register 33.18. RMT_CH*m*_RX_LIM_REG (*m* = 4, 5, 6, 7) (0x00B0, 0x00B4, 0x00B8, 0x00BC)



RMT_CH*m*_RX_LIM_REG This field is used to configure the maximum entries that channel *m* can receive. (R/W)

Register 33.19. RMT_DATE_REG (0x00CC)



RMT_DATE Version control register. (R/W)

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34 Pulse Count Controller (PCNT)

The pulse count controller (PCNT) is designed to count input pulses. It can increment or decrement a pulse counter value by keeping track of rising (positive) or falling (negative) edges of the input pulse signal. The PCNT has four independent pulse counters called units, which have their groups of registers. There is only one clock in PCNT, which is APB_CLK. In this chapter, *n* denotes the number of a unit from 0 ~ 3.

Each unit includes two channels (ch0 and ch1) which can independently increment or decrement its pulse counter value. The remainder of the chapter will mostly focus on channel 0 (ch0) as the functionality of the two channels is identical.

As shown in Figure 34-1, each channel has two input signals:

1. One input pulse signal (e.g. sig_ch0_u*n*, the input pulse signal for ch0 of unit *n* ch0)
2. One control signal (e.g. ctrl_ch0_u*n*, the control signal for ch0 of unit *n* ch0)

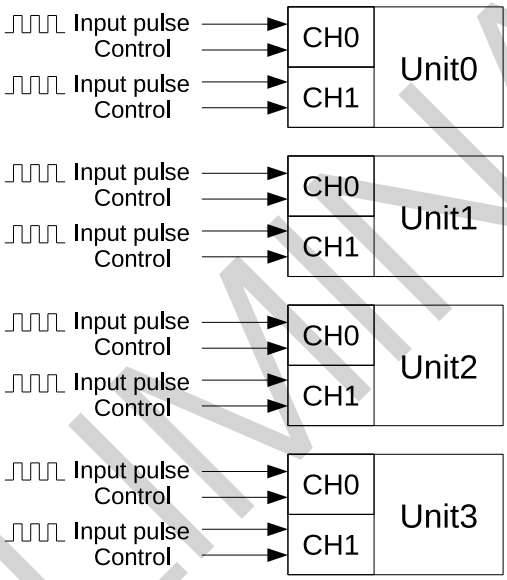


Figure 34-1. PCNT Block Diagram

34.1 Features

A PCNT has the following features:

- Four independent pulse counters (units) that count from 1 to 65535
- Each unit consists of two independent channels sharing one pulse counter
- All channels have input pulse signals (e.g. sig_ch0_u*n*) with their corresponding control signals (e.g. ctrl_ch0_u*n*)
- Independently filter glitches of input pulse signals (sig_ch0_u*n* and sig_ch1_u*n*) and control signals (ctrl_ch0_u*n* and ctrl_ch1_u*n*) on each unit
- Each channel has the following parameters:
    1. Selection between counting on positive or negative edges of the input pulse signal

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2. Configuration to Increment, Decrement, or Disable counter mode for control signal's high and low states

- Maximum frequency of pulses: 40 MHz

34.2 Functional Description

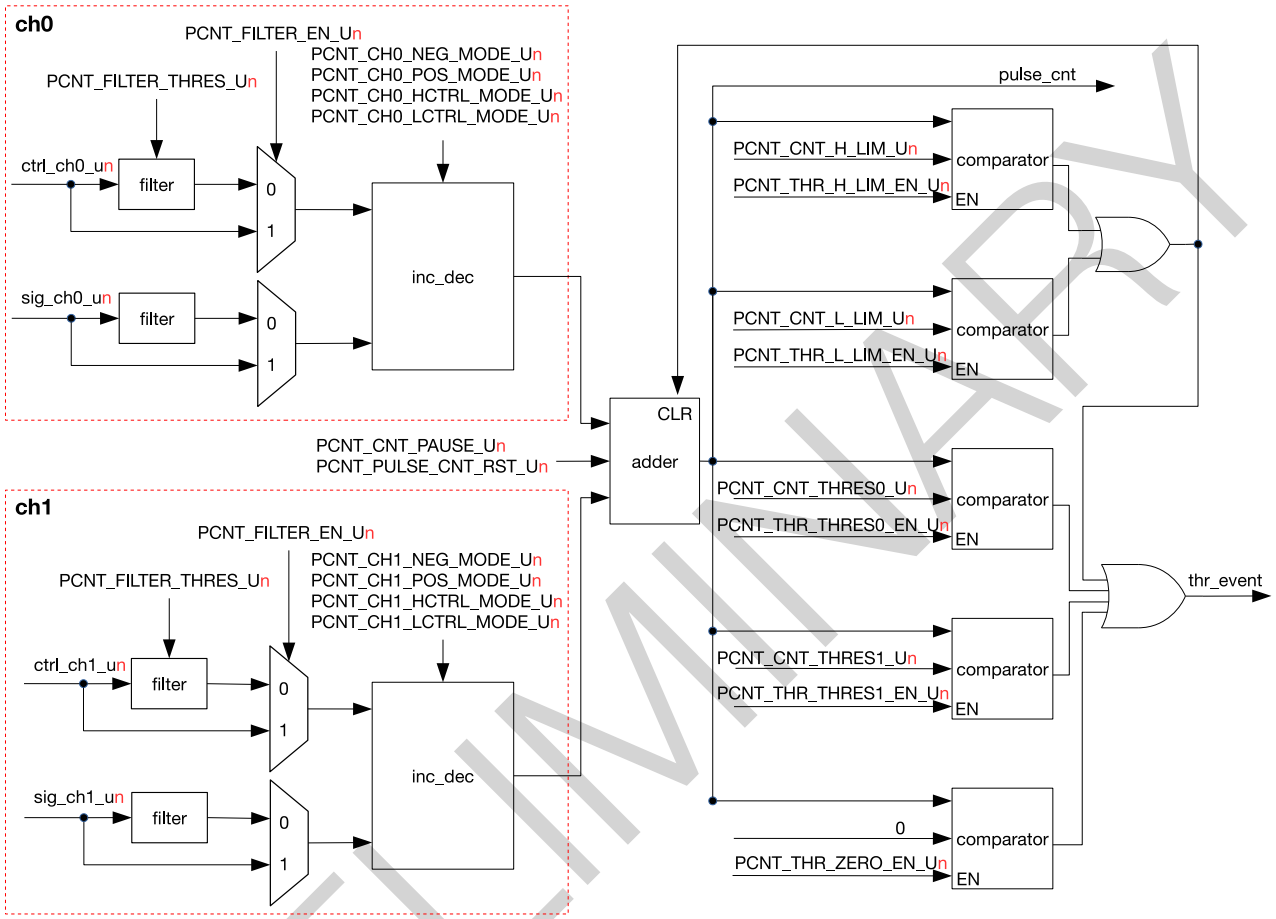


Figure 34-2. PCNT Unit Architecture

Figure 34-2 shows PCNT's architecture. As stated above, ctrl_ch0_u*n* is the control signal for ch0 of unit *n*. Its high and low states can be assigned different counter modes and used for pulse counting of the channel's input pulse signal sig_ch0_u*n* on negative or positive edges. The available counter modes are as follows:

- Increment mode: When a channel detects an active edge of sig_ch0_u*n* (can be configured by software), the counter value pulse_cnt increases by 1. Upon reaching PCNT_CNT_H_LIM_U*n*, pulse_cnt is cleared. If the channel's counter mode is changed or if PCNT_CNT_PAUSE_U*n* is set before pulse_cnt reaches PCNT_CNT_H_LIM_U*n*, then pulse_cnt freezes and its counter mode changes.
- Decrement mode: When a channel detects an active edge of sig_ch0_u*n* (can be configured by software), the counter value pulse_cnt decreases by 1. Upon reaching PCNT_CNT_L_LIM_U*n*, pulse_cnt is cleared. If the channel's counter mode is changed or if PCNT_CNT_PAUSE_U*n* is set before pulse_cnt reaches PCNT_CNT_H_LIM_U*n*, then pulse_cnt freezes and its counter mode changes.
- Disable mode: Counting is disabled, and the counter value pulse_cnt freezes.

Table 34-1 to Table 34-4 provide information on how to configure the counter mode for channel 0.

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Table 34-1. Counter Mode. Positive Edge of Input Pulse Signal. Control Signal in Low State

PCNT_CH0_POS_MODE_U*n*	PCNT_CH0_LCTRL_MODE_U*n*	Counter Mode
1	0	Increment
	1	Decrement
	Others	Disable
2	0	Decrement
	1	Increment
	Others	Disable
Others	N/A	Disable

Table 34-2. Counter Mode. Positive Edge of Input Pulse Signal. Control Signal in High State

PCNT_CH0_POS_MODE_U*n*	PCNT_CH0_HCTRL_MODE_U*n*	Counter Mode
1	0	Increment
	1	Decrement
	Others	Disable
2	0	Decrement
	1	Increment
	Others	Disable
Others	N/A	Disable

Table 34-3. Counter Mode. Negative Edge of Input Pulse Signal. Control Signal in Low State

PCNT_CH0_NEG_MODE_U*n*	PCNT_CH0_LCTRL_MODE_U*n*	Counter Mode
1	0	Increment
	1	Decrement
	Others	Disable
2	0	Decrement
	1	Increment
	Others	Disable
Others	N/A	Disable

Table 34-4. Counter Mode. Negative Edge of Input Pulse Signal. Control Signal in High State

PCNT_CH0_NEG_MODE_U*n*	PCNT_CH0_HCTRL_MODE_U*n*	Counter Mode
1	0	Increment
	1	Decrement
	Others	Disable
2	0	Decrement
	1	Increment
	Others	Disable
Others	N/A	Disable

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Each unit has one filter for all its control and input pulse signals. A filter can be enabled with the bit PCNT_FILTER_EN_U*n*. The filter monitors the signals and ignores all the noise, i.e. the glitches with pulse widths shorter than PCNT_FILTER_THRES_U*n* APB clock cycles in length.

As previously mentioned, each unit has two channels which process different input pulse signals and increase or decrease values via their respective inc_dec modules, then the two channels send these values to the adder module which has a 16-bit wide signed register. This adder can be suspended by setting PCNT_CNT_PAUSE_U*n*, and cleared by setting PCNT_PULSE_CNT_RST_U*n*.

The PCNT has five watchpoints that share one interrupt. The interrupt can be enabled or disabled by interrupt enable signals of each individual watchpoint.

- Maximum count value: When pulse_cnt reaches PCNT_CNT_H_LIM_U*n*, a high limit interrupt is triggered and PCNT_CNT_THR_H_LIM_LAT_U*n* is high.
- Minimum count value: When pulse_cnt reaches PCNT_CNT_L_LIM_U*n*, a low limit interrupt is triggered and PCNT_CNT_THR_L_LIM_LAT_U*n* is high.
- Two threshold values: When pulse_cnt equals either PCNT_CNT_THRES0_U*n* or PCNT_CNT_THRES1_U*n*, an interrupt is triggered and either PCNT_CNT_THR_THRES0_LAT_U*n* or PCNT_CNT_THR_THRES1_LAT_U*n* is high respectively.
- Zero: When pulse_cnt is 0, an interrupt is triggered and PCNT_CNT_THR_ZERO_LAT_U*n* is valid.

34.3 Applications

In each unit, channel 0 and channel 1 can be configured to work independently or together. The three subsections below provide details of channel 0 incrementing independently, channel 0 decrementing independently, and channel 0 and channel 1 incrementing together. For other working modes not elaborated in this section (e.g. channel 1 incrementing/decremeting independently, or one channel incrementing while the other decrementing), reference can be made to these three subsections.

34.3.1 Channel 0 Incrementing Independently

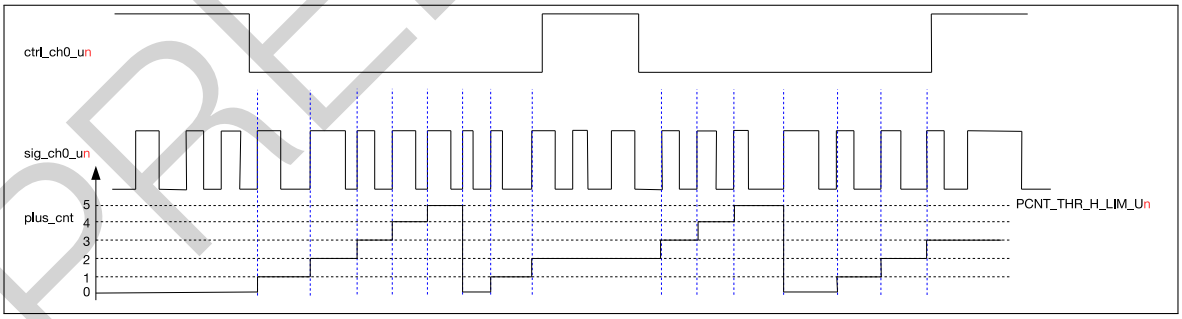


Figure 34-3. Channel 0 Up Counting Diagram

Figure 34-3 illustrates how channel 0 is configured to increment independently on the positive edge of sig_ch0_u*n* while channel 1 is disabled (see subsection 34.2 for how to disable channel 1). The configuration of channel 0 is shown below.

- PCNT_CH0_LCTRL_MODE_U*n*=0: When ctrl_ch0_u*n* is low, the counter mode specified for the low state turns on, in this case it is Increment mode.

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- PCNT_CH0_HCTRL_MODE_U*n*=2: When ctrl_ch0_u*n* is high, the counter mode specified for the low state turns on, in this case it is Disable mode.
- PCNT_CH0_POS_MODE_U*n*=1: The counter increments on the positive edge of sig_ch0_u*n*.
- PCNT_CH0_NEG_MODE_U*n*=0: The counter idles on the negative edge of sig_ch0_u*n*.
- PCNT_CNT_H_LIM_U*n*=5: When pulse_cnt counts up to PCNT_CNT_H_LIM_U*n*, it is cleared.

34.3.2 Channel 0 Decrementing Independently

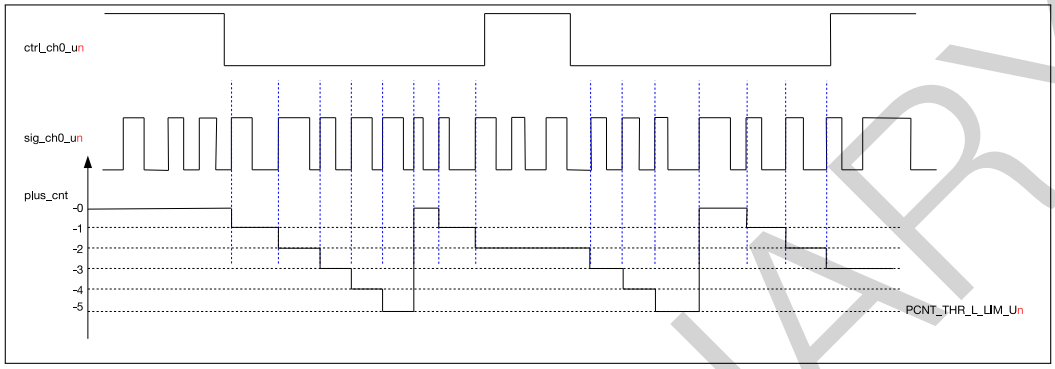


Figure 34-4. Channel 0 Down Counting Diagram

Figure 34-4 illustrates how channel 0 is configured to decrement independently on the positive edge of sig_ch0_u*n* while channel 1 is disabled. The configuration of channel 0 in this case differs from that in Figure 34-3 in the following aspects:

- PCNT_CH0_POS_MODE_U*n*=2: the counter decrements on the positive edge of sig_ch0_u*n*.
- PCNT_CNT_L_LIM_U*n*=-5: when pulse_cnt counts down to PCNT_CNT_L_LIM_U*n*, it is cleared.

34.3.3 Channel 0 and Channel 1 Incrementing Together

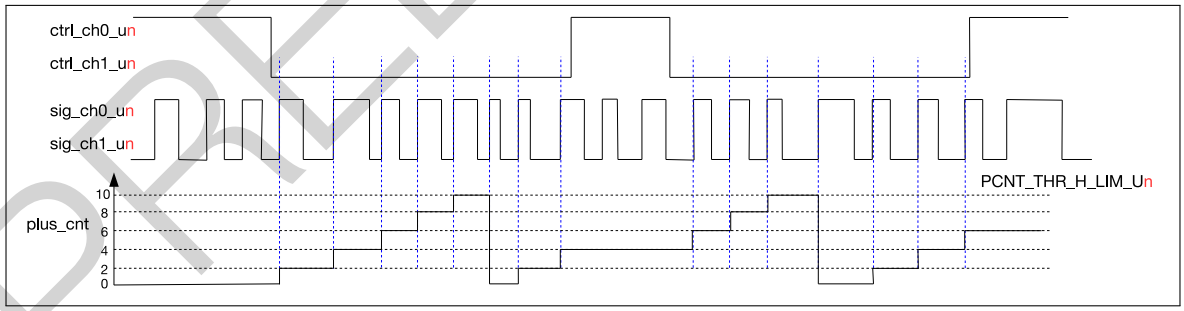


Figure 34-5. Two Channels Up Counting Diagram

Figure 34-5 illustrates how channel 0 and channel 1 are configured to increment on the positive edge of sig_ch0_u*n* and sig_ch1_u*n* respectively at the same time. It can be seen in Figure 34-5 that control signal ctrl_ch0_u*n* and ctrl_ch1_u*n* have the same waveform, so as input pulse signal sig_ch0_u*n* and sig_ch1_u*n*. The configuration procedure is shown below.

- For channel 0:

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  - PCNT_CH0_LCTRL_MODE_U*n*=0: When ctrl_ch0_u*n* is low, the counter mode specified for the low state turns on, in this case it is Increment mode.
  - PCNT_CH0_HCTRL_MODE_U*n*=2: When ctrl_ch0_u*n* is high, the counter mode specified for the low state turns on, in this case it is Disable mode.
  - PCNT_CH0_POS_MODE_U*n*=1: The counter increments on the positive edge of sig_ch0_u*n*.
  - PCNT_CH0_NEG_MODE_U*n*=0: The counter idles on the negative edge of sig_ch0_u*n*.
- For channel 1:
  - PCNT_CH1_LCTRL_MODE_U*n*=0: When ctrl_ch1_u*n* is low, the counter mode specified for the low state turns on, in this case it is Increment mode.
  - PCNT_CH1_HCTRL_MODE_U*n*=2: When ctrl_ch1_u*n* is high, the counter mode specified for the low state turns on, in this case it is Disable mode.
  - PCNT_CH1_POS_MODE_U*n*=1: The counter increments on the positive edge of sig_ch1_u*n*.
  - PCNT_CH1_NEG_MODE_U*n*=0: The counter idles on the negative edge of sig_ch1_u*n*.
- PCNT_CNT_H_LIM_U*n*=10: When pulse_cnt counts up to PCNT_CNT_H_LIM_U*n*, it is cleared.

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34.4 Register Summary

The addresses in this section are relative to Pulse Count Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

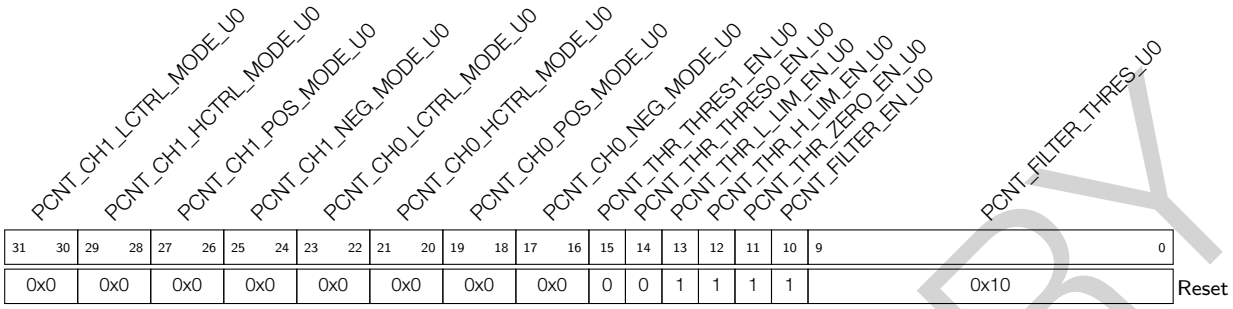
Name	Description	Address	Access
Configuration Register			
PCNT_U0_CONF0_REG	Configuration register 0 for unit 0	0x0000	R/W
PCNT_U0_CONF1_REG	Configuration register 1 for unit 0	0x0004	R/W
PCNT_U0_CONF2_REG	Configuration register 2 for unit 0	0x0008	R/W
PCNT_U1_CONF0_REG	Configuration register 0 for unit 1	0x000C	R/W
PCNT_U1_CONF1_REG	Configuration register 1 for unit 1	0x0010	R/W
PCNT_U1_CONF2_REG	Configuration register 2 for unit 1	0x0014	R/W
PCNT_U2_CONF0_REG	Configuration register 0 for unit 2	0x0018	R/W
PCNT_U2_CONF1_REG	Configuration register 1 for unit 2	0x001C	R/W
PCNT_U2_CONF2_REG	Configuration register 2 for unit 2	0x0020	R/W
PCNT_U3_CONF0_REG	Configuration register 0 for unit 3	0x0024	R/W
PCNT_U3_CONF1_REG	Configuration register 1 for unit 3	0x0028	R/W
PCNT_U3_CONF2_REG	Configuration register 2 for unit 3	0x002C	R/W
PCNT_CTRL_REG	Control register for all counters	0x0060	R/W
Status Register			
PCNT_U0_CNT_REG	Counter value for unit 0	0x0030	RO
PCNT_U1_CNT_REG	Counter value for unit 1	0x0034	RO
PCNT_U2_CNT_REG	Counter value for unit 2	0x0038	RO
PCNT_U3_CNT_REG	Counter value for unit 3	0x003C	RO
PCNT_U0_STATUS_REG	PNCT UNIT0 status register	0x0050	RO
PCNT_U1_STATUS_REG	PNCT UNIT1 status register	0x0054	RO
PCNT_U2_STATUS_REG	PNCT UNIT2 status register	0x0058	RO
PCNT_U3_STATUS_REG	PNCT UNIT3 status register	0x005C	RO
Interrupt Register			
PCNT_INT_RAW_REG	Interrupt raw status register	0x0040	RO
PCNT_INT_ST_REG	Interrupt status register	0x0044	RO
PCNT_INT_ENA_REG	Interrupt enable register	0x0048	R/W
PCNT_INT_CLR_REG	Interrupt clear register	0x004C	WO
Version Register			
PCNT_DATE_REG	PCNT version control register	0x00FC	R/W

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34.5 Registers

The addresses in this section are relative to Pulse Count Controller base address provided in Table 3-3 in Chapter 3 *System and Memory*.

Register 34.1. PCNT_U*n*_CONF0_REG (*n*: 0-3) (0x0000+0xCn*)**



PCNT_FILTER_THRES_U*n* This sets the maximum threshold, in APB_CLK cycles, for the filter.

Any pulses with width less than this will be ignored when the filter is enabled. (R/W)

PCNT_FILTER_EN_U*n* This is the enable bit for unit *n*'s input filter. (R/W)

PCNT_THR_ZERO_EN_U*n* This is the enable bit for unit *n*'s zero comparator. (R/W)

PCNT_THR_H_LIM_EN_U*n* This is the enable bit for unit *n*'s thr_h_lim comparator. (R/W)

PCNT_THR_L_LIM_EN_U*n* This is the enable bit for unit *n*'s thr_l_lim comparator. (R/W)

PCNT_THR_THRES0_EN_U*n* This is the enable bit for unit *n*'s thres0 comparator. (R/W)

PCNT_THR_THRES1_EN_U*n* This is the enable bit for unit *n*'s thres1 comparator. (R/W)

PCNT_CH0_NEG_MODE_U*n* This register sets the behavior when the signal input of channel 0 detects a negative edge.

1: Increase the counter; 2: Decrease the counter; 0, 3: No effect on counter (R/W)

PCNT_CH0_POS_MODE_U*n* This register sets the behavior when the signal input of channel 0 detects a positive edge.

1: Increase the counter; 2: Decrease the counter; 0, 3: No effect on counter (R/W)

PCNT_CH0_HCTRL_MODE_U*n* This register configures how the CH*n*_POS_MODE/CH*n*_NEG_MODE settings will be modified when the control signal is high.

0: No modification; 1: Invert behavior (increase -> decrease, decrease -> increase); 2, 3: Inhibit counter modification (R/W)

Continued on the next page...

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Register 34.1. PCNT_U*n*_CONF0_REG (*n*: 0-3) (0x0000+0xCn*)**

Continued from the previous page...

PCNT_CH0_LCTRL_MODE_U*n* This register configures how the CH*n*_POS_MODE/CH*n*_NEG_MODE settings will be modified when the control signal is low.

0: No modification; 1: Invert behavior (increase -> decrease, decrease -> increase); 2, 3: Inhibit counter modification (R/W)

PCNT_CH1_NEG_MODE_U*n* This register sets the behavior when the signal input of channel 1 detects a negative edge.

1: Increment the counter; 2: Decrement the counter; 0, 3: No effect on counter (R/W)

PCNT_CH1_POS_MODE_U*n* This register sets the behavior when the signal input of channel 1 detects a positive edge.

1: Increment the counter; 2: Decrement the counter; 0, 3: No effect on counter (R/W)

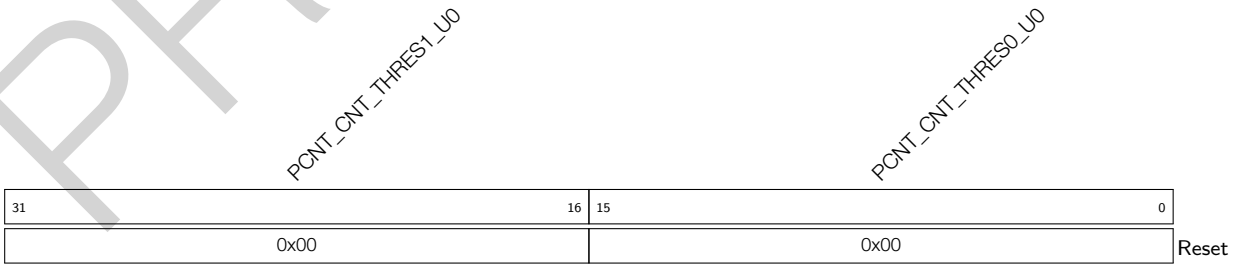
PCNT_CH1_HCTRL_MODE_U*n* This register configures how the CH*n*_POS_MODE/CH*n*_NEG_MODE settings will be modified when the control signal is high.

0: No modification; 1: Invert behavior (increase -> decrease, decrease -> increase); 2, 3: Inhibit counter modification (R/W)

PCNT_CH1_LCTRL_MODE_U*n* This register configures how the CH*n*_POS_MODE/CH*n*_NEG_MODE settings will be modified when the control signal is low.

0: No modification; 1: Invert behavior (increase -> decrease, decrease -> increase); 2, 3: Inhibit counter modification (R/W)

Register 34.2. PCNT_U*n*_CONF1_REG (*n*: 0-3) (0x0004+0xCn*)**

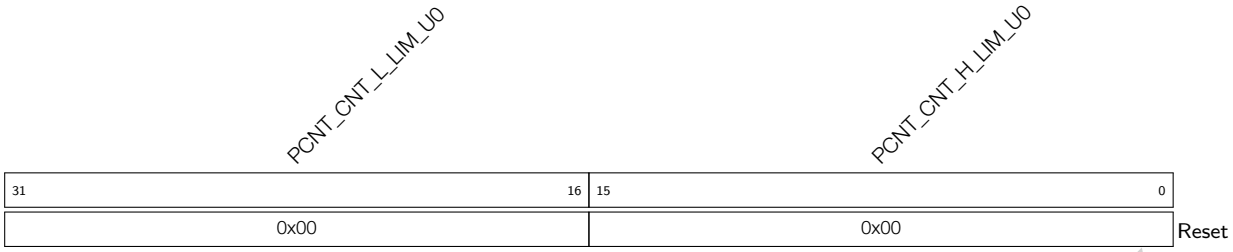


PCNT_CNT_THRES0_U*n* This register is used to configure the thres0 value for unit *n*. (R/W)

PCNT_CNT_THRES1_U*n* This register is used to configure the thres1 value for unit *n*. (R/W)

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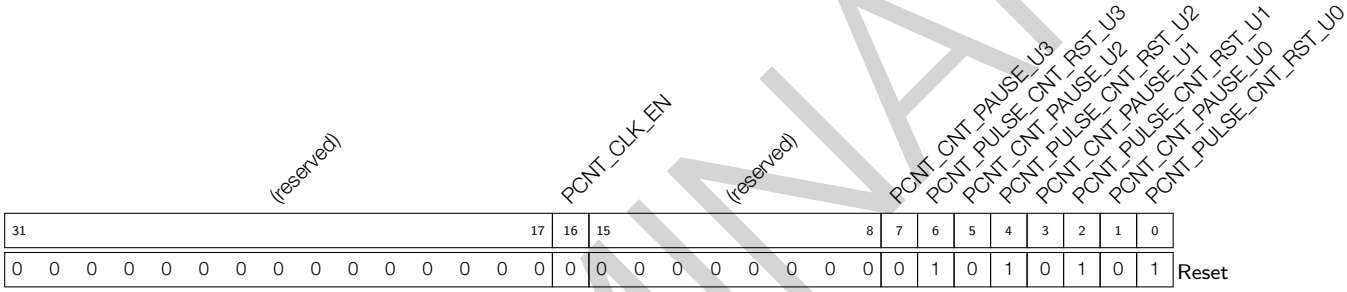
Register 34.3. PCNT_U*n*_CONF2_REG (*n*: 0-3) (0x0008+0xCn*)**



PCNT_CNT_H_LIM_U*n* This register is used to configure the thr_h_lim value for unit *n*. (R/W)

PCNT_CNT_L_LIM_U*n* This register is used to configure the thr_l_lim value for unit *n*. (R/W)

Register 34.4. PCNT_CTRL_REG (0x0060)

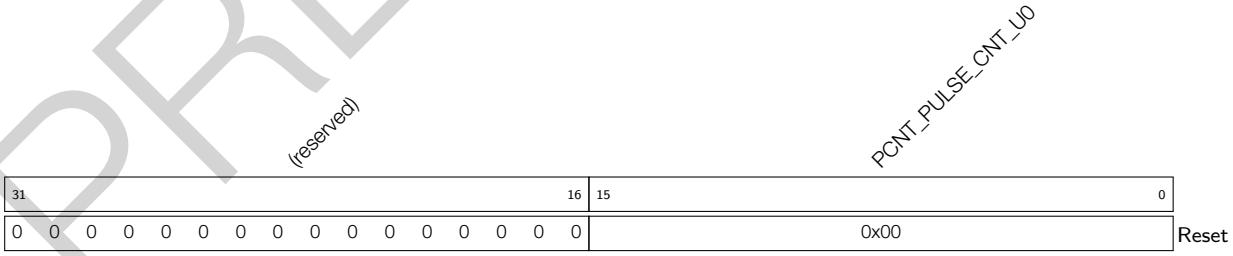


PCNT_PULSE_CNT_RST_U*n* Set this bit to clear unit *n*'s counter. (R/W)

PCNT_CNT_PAUSE_U*n* Set this bit to freeze unit *n*'s counter. (R/W)

PCNT_CLK_EN The registers clock gate enable signal of PCNT module. 1: the registers can be read and written by application. 0: the registers can not be read or written by application (R/W)

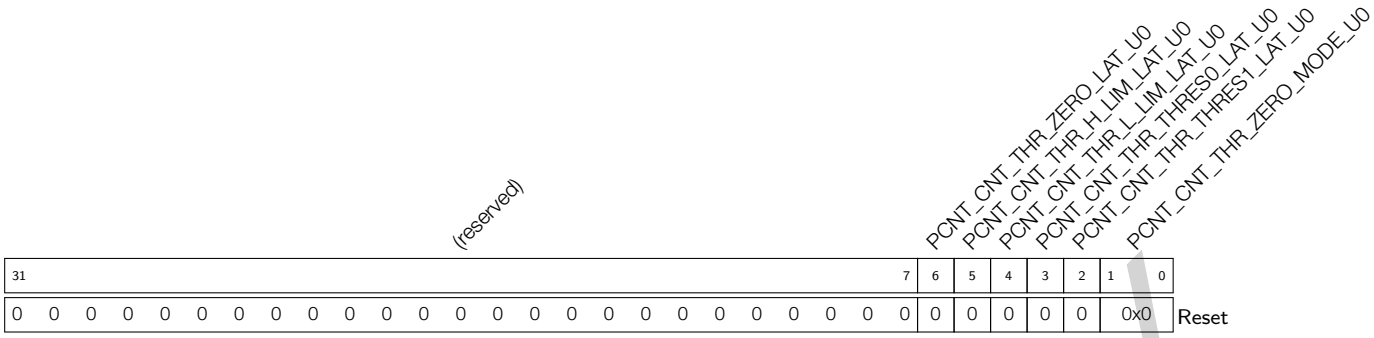
Register 34.5. PCNT_U*n*_CNT_REG (*n*: 0-3) (0x0030+0x4n*)**



PCNT_PULSE_CNT_U*n* This register stores the current pulse count value for unit *n*. (RO)

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Register 34.6. PCNT_U*n*_STATUS_REG (*n*: 0-3) (0x0050+0x4n*)**



PCNT_CNT_THR_ZERO_MODE_U*n* The pulse counter status of PCNT_U*n* corresponding to 0. 0: pulse counter decreases from positive to 0. 1: pulse counter increases from negative to 0. 2: pulse counter is negative. 3: pulse counter is positive. (RO)

PCNT_CNT_THR_THRES1_LAT_U*n* The latched value of thres1 event of PCNT_U*n* when threshold event interrupt is valid. 1: the current pulse counter equals to thres1 and thres1 event is valid. 0: others (RO)

PCNT_CNT_THR_THRES0_LAT_U*n* The latched value of thres0 event of PCNT_U*n* when threshold event interrupt is valid. 1: the current pulse counter equals to thres0 and thres0 event is valid. 0: others (RO)

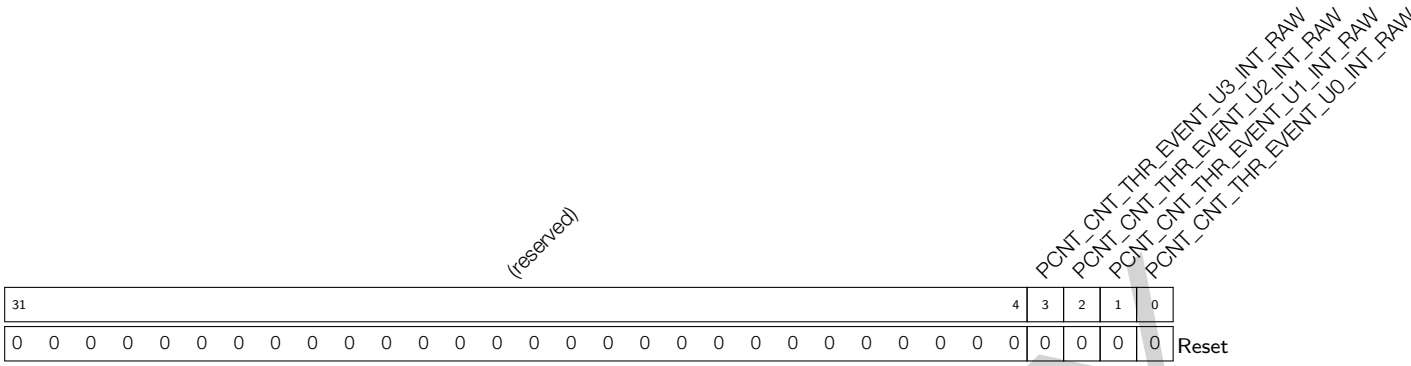
PCNT_CNT_THR_L_LIM_LAT_U*n* The latched value of low limit event of PCNT_U*n* when threshold event interrupt is valid. 1: the current pulse counter equals to thr_l_lim and low limit event is valid. 0: others (RO)

PCNT_CNT_THR_H_LIM_LAT_U*n* The latched value of high limit event of PCNT_U*n* when threshold event interrupt is valid. 1: the current pulse counter equals to thr_h_lim and high limit event is valid. 0: others (RO)

PCNT_CNT_THR_ZERO_LAT_U*n* The latched value of zero threshold event of PCNT_U*n* when threshold event interrupt is valid. 1: the current pulse counter equals to 0 and zero threshold event is valid. 0: others (RO)

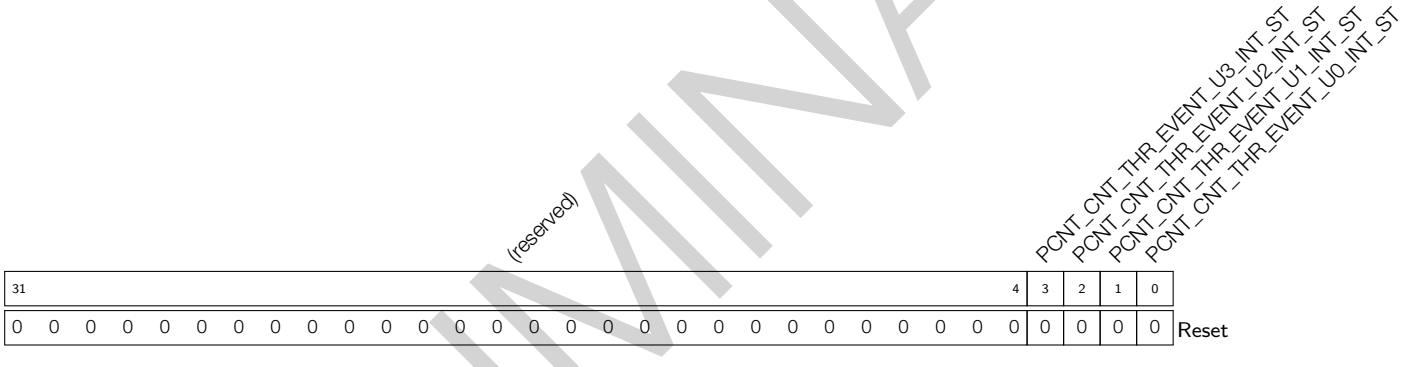
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Register 34.7. PCNT_INT_RAW_REG (0x0040)



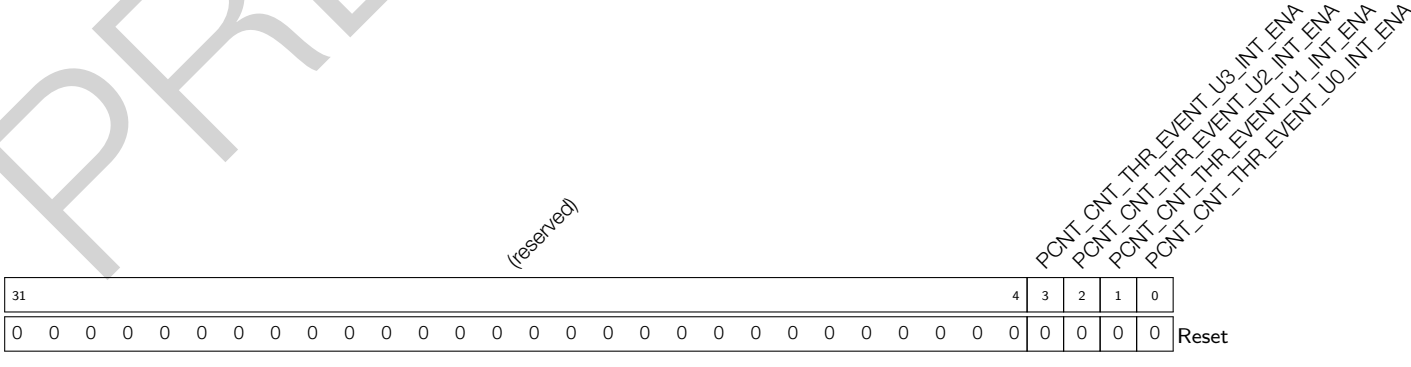
PCNT_CNT_THR_EVENT_U*n*_INT_RAW The raw interrupt status bit for the PCNT_CNT_THR_EVENT_U*n*_INT interrupt. (RO)

Register 34.8. PCNT_INT_ST_REG (0x0044)



PCNT_CNT_THR_EVENT_U*n*_INT_ST The masked interrupt status bit for the PCNT_CNT_THR_EVENT_U*n*_INT interrupt. (RO)

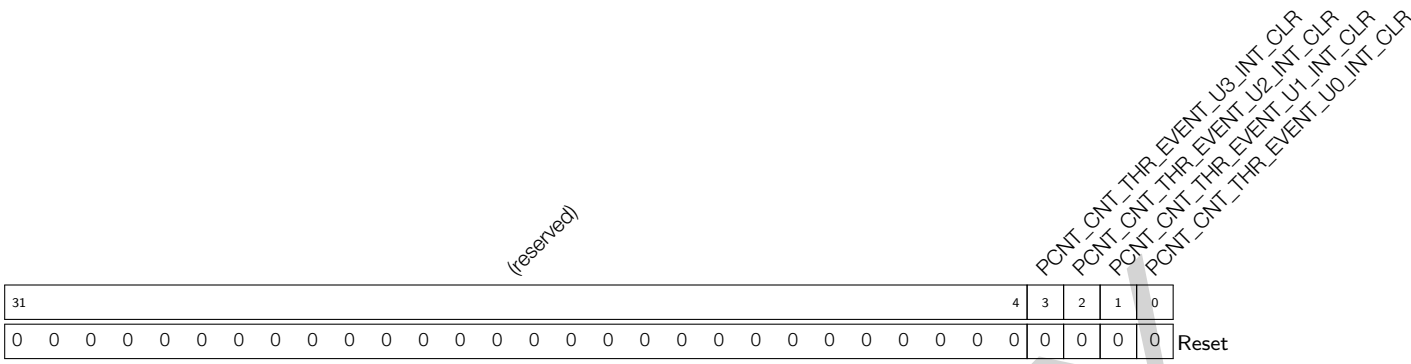
Register 34.9. PCNT_INT_ENA_REG (0x0048)



PCNT_CNT_THR_EVENT_U*n*_INT_ENA The interrupt enable bit for the PCNT_CNT_THR_EVENT_U*n*_INT interrupt. (R/W)

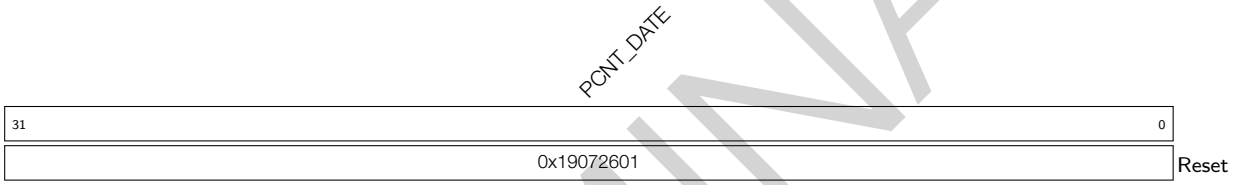
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Register 34.10. PCNT_INT_CLR_REG (0x004C)



PCNT_CNT_THR_EVENT_U*n*_INT_CLR Set this bit to clear the PCNT_CNT_THR_EVENT_U*n*_INT interrupt. (WO)

Register 34.11. PCNT_DATE_REG (0x00FC)



PCNT_DATE This is the PCNT version control register. (R/W)

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35 Related Documentation and Resources

Related Documentation

- ESP32-S3 Series Datasheet – Specifications of the ESP32-S3 hardware.
- ESP32-S3 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-S3 into your hardware product.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-S3 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-S3 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S3 Series SoCs* – Browse through all ESP32-S3 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-S3
- *ESP32-S3 Series Modules* – Browse through all ESP32-S3-based modules.
  https://espressif.com/en/products/modules?id=ESP32-S3
- *ESP32-S3 Series DevKits* – Browse through all ESP32-S3-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-S3
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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Glossary

Abbreviations for Peripherals

AES	AES (Advanced Encryption Standard) Accelerator
BOOTCTRL	Chip Boot Control
DS	Digital Signature
DMA	DMA (Direct Memory Access) Controller
eFuse	eFuse Controller
HMAC	HMAC (Hash-based Message Authentication Code) Accelerator
I2C	I2C (Inter-Integrated Circuit) Controller
I2S	I2S (Inter-IC Sound) Controller
LEDC	LED Control PWM (Pulse Width Modulation)
MCPWM	Motor Control PWM (Pulse Width Modulation)
PCNT	Pulse Count Controller
RMT	Remote Control Peripheral
RNG	Random Number Generator
RSA	RSA (Rivest Shamir Adleman) Accelerator
SDHOST	SD/MMC Host Controller
SHA	SHA (Secure Hash Algorithm) Accelerator
SPI	SPI (Serial Peripheral Interface) Controller
SYSTIMER	System Timer
TIMG	Timer Group
TWAI	Two-wire Automotive Interface
UART	UART (Universal Asynchronous Receiver-Transmitter) Controller
ULP Coprocessor	Ultra-low-power Coprocessor
USB OTG	USB On-The-Go
WDT	Watchdog Timers

Abbreviations for Registers

ISO	Isolation. When a module is power down, its output pins will be stuck in unknown state (some middle voltage). "ISO" registers will control to isolate its output pins to be a determined value, so it will not affect the status of other working modules which are not power down.
NMI	Non-maskable interrupt.
REG	Register.
R/W	Read/write. Software can read and write to these bits.
RO	Read-only. Software can only read these bits.
SYSREG	System Registers
WO	Write-only. Software can only write to these bits.

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Revision History

Date	Version	Release notes
2022-06-01	v0.6	Updated the following chapters: • Chapter 2 *GDMA Controller (GDMA)* • Chapter 4 *eFuse Controller* • Chapter 7 *Chip Boot Control*
2022-04-06	v0.5	Added the following chapters: • Chapter 13 *Permission Control (PMS)* • Chapter 14 *World Controller* Updated the following chapter: • Chapter 3 *System and Memory*
2022-02-24	v0.4	Added Chapter 26 *LCD and Camera Controller (LCD_CAM)* Updated the following chapters: • Chapter 1 *ULP Coprocessor (ULP-FSM, ULP-RISC-V)* • Chapter 4 *eFuse Controller* • Chapter 5 *IO MUX and GPIO Matrix (GPIO, IO MUX)* • Chapter 6 *Reset and Clock* • Chapter 7 *Chip Boot Control* • Chapter 28 *USB On-The-Go (USB)*
2021-12-16	v0.3	Added the following chapters: • Chapter 1 *ULP Coprocessor (ULP-FSM, ULP-RISC-V)* • Chapter 2 *GDMA Controller (GDMA)* • Chapter 9 *System Timer (SYSTIMER)* • Chapter 22 *Clock Glitch Detection* • Chapter 25 *I2C Controller (I2C)* • Chapter 32 *Motor Control PWM (MCPWM)* • Chapter 33 *Remote Control Peripheral (RMT)* Updated the following chapters: • Chapter 4 *eFuse Controller* • Chapter 18 *RSA Accelerator (RSA)* • Chapter 19 *HMAC Accelerator (HMAC)* • Chapter 20 *Digital Signature (DS)*

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Date	Version	Release notes
2021-09-30	v0.2	Added the following chapters: • Chapter 15 *System Registers* • Chapter 19 *HMAC Accelerator (HMAC)* • Chapter 21 *External Memory Encryption and Decryption (XTS_AES)* • Chapter 24 *UART Controller (UART)* • Chapter 29 *USB Serial/JTAG Controller (USB_SERIAL_JTAG)* Updated the following Chapters: • Chapter 4 *eFuse Controller* • Chapter 27 *Two-wire Automotive Interface (TWAI®)*
2021-07-09	v0.1	Preliminary release

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